

Approval Sheet

| | |
|------------------------------|--------------------------------------|
| Customer | |
| Product Number | M5DZ-AGS2PC0Q-P |
| Data Rate | 5600 MT/s |
| Pin | 262 pin |
| CI-tRCD-tRP | 46-45-45 |
| Operating temperature | Tc=0 to 95°C |
| Date | 11th December 2023 |

**The Total Solution For
Industrial Flash Storage**

Rev 1.0

1. Features

- JEDEC Standard 262-pin Small Outline Dual In-Line Memory Module
- VDD=VDDQ= 1.1V (1.067V ~ 1.166V)
- VPP=1.8V (1.746V ~ 1.908V)
- VDDSPD= 1.8V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42,46,50
- tREFI 3.9us for 0°C ≤Tcase < 85°C, tREFI 1.95us for 85°C < Tcase ≤ 95°C
- On-Die ECC
- PMIC on DIMM, nominal supply 5V/2A, VIN_Bulk input supply range: 4.25 V to 5.5 V
- Fly-by topology
- I3C/I2C support
- Terminated control and C/A bus
- SPD EEPROM Hub and Integrated Thermal Sensor
- Halogen-free

Specification

| Density | Data Rate | IC Configuration | DIMM Organization | Number of IC | Number of rank | Side | ECC |
|---------|-----------|------------------|-------------------|--------------|----------------|------|-----|
| 16GB | 5600 MT/s | 2Gx8 (16Gb) | 2Gx72 | 10 | 1 | 1 | Y |

Key timing parameters

| tCK (ns) | tRCD (ns) | tRP (ns) | tRAS (ns) | tRC (ns) |
|-------------|--------------|-------------|--------------|-------------|
| 0.357 | 16.00 | 16.00 | 32 | 48.00 |

tRFC parameter by IC Configuration

| Parameter | IC Configuration | | | | Unit |
|------------|------------------|------|------|------|------|
| | 8Gb | 16Gb | 24Gb | 32Gb | |
| tRFC1,min | 195 | 295 | TBD | TBD | ns |
| tRFC2,min | 130 | 160 | TBD | TBD | ns |
| tRFCsb,min | 115 | 130 | TBD | TBD | ns |

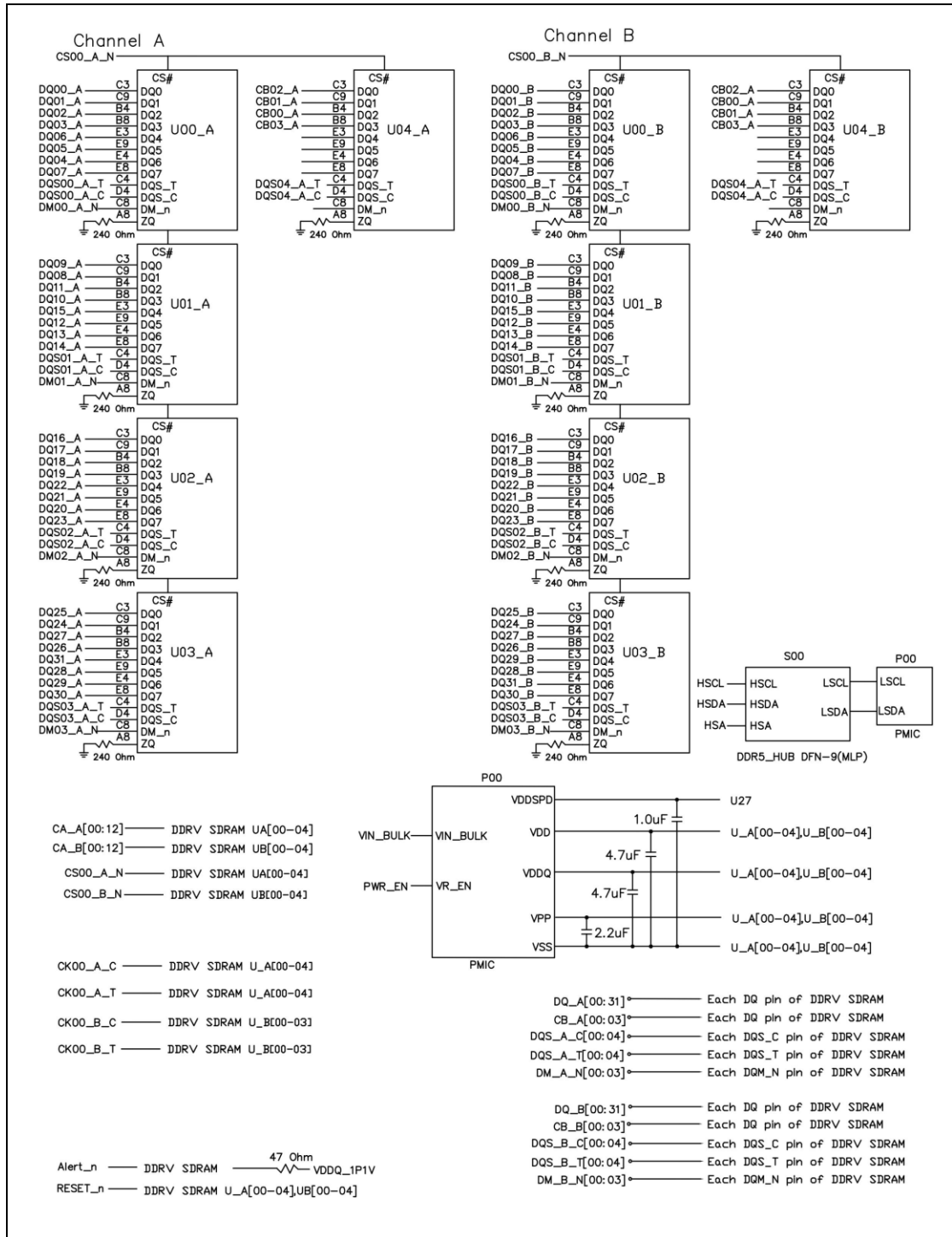
2. Pin Assignments

| 262-Pin DDR5 SODIMM Front | | | | | | | | 262-Pin DDR5 SODIMM Back | | | | | | | |
|---------------------------|----------|-----|----------|-----|----------|-----|----------|--------------------------|----------|-----|----------|-----|----------|-----|----------|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | VIN_BULK | 67 | Vss | 133 | CK0_A_c | 199 | DQ8_B | 2 | HAS | 68 | DQ21_A | 134 | CK1_A_c | 200 | Vss |
| 3 | VIN_BULK | 69 | DQ22_A | 135 | Vss | 201 | Vss | 4 | HSCL | 70 | Vss | 136 | Vss | 202 | DQ9_B |
| 5 | RFU | 71 | Vss | 137 | CK0_B_t | 203 | DQ10_B | 6 | HSDA | 72 | DQ23_A | 138 | CK1_B_t | 204 | Vss |
| 7 | PWR_GOOD | 73 | DQ24_A | 139 | CK0_B_c | 205 | Vss | 8 | PWR_EN | 74 | Vss | 140 | CK1_B_c | 206 | DQ11_B |
| 9 | Vss | 75 | Vss | 141 | Vss | 207 | DQS1_B_c | 10 | Vss | 76 | DQ25_A | 142 | Vss | 208 | Vss |
| 11 | DQ0_A | 77 | DQ26_A | 143 | RFU | 209 | DQS1_B_t | 12 | DQ1_A | 78 | Vss | 144 | CA12_B | 210 | DM1_B_n |
| 13 | Vss | 79 | Vss | 145 | CA11_B | 211 | Vss | 14 | Vss | 80 | DQ27_A | 146 | CA10_B | 212 | Vss |
| 15 | DQ2_A | 81 | DQS3_A_c | 147 | Vss | 213 | DQ12_B | 16 | DQ3_A | 82 | Vss | 148 | Vss | 214 | DQ13_B |
| 17 | Vss | 83 | DQS3_A_t | 149 | CA9_B | 215 | Vss | 18 | Vss | 84 | DM3_A_n | 150 | CA8_B | 216 | Vss |
| 19 | DM0_A_n | 85 | Vss | 151 | CA7_B | 217 | DQ14_B | 20 | DQS0_A_c | 86 | Vss | 152 | CA6_B | 218 | DQ15_B |
| 21 | Vss | 87 | DQ28_A | 153 | Vss | 219 | Vss | 22 | DQS0_A_t | 88 | DQ29_A | 154 | Vss | 220 | Vss |
| 23 | DQ4_A | 89 | Vss | 155 | CA5_B | 221 | DQ16_B | 24 | Vss | 90 | Vss | 156 | CA4_B | 222 | DQ17_B |
| 25 | Vss | 91 | DQ30_A | 157 | CA3_B | 223 | Vss | 26 | DQ5_A | 92 | DQ31_A | 158 | CA2_B | 224 | Vss |
| 27 | DQ6_A | 93 | Vss | 159 | Vss | 225 | DQ18_B | 28 | Vss | 94 | Vss | 160 | Vss | 226 | DQ19_B |
| 29 | Vss | 95 | CB0_A | 161 | CS0_B_n | 227 | Vss | 30 | DQ7_A | 96 | CB1_A | 162 | CA1_B | 228 | Vss |
| 31 | DQ8_A | 97 | Vss | 163 | RESET_n | 229 | DM2_B_n | 32 | Vss | 98 | Vss | 164 | CA0_B | 230 | DQS2_B_c |
| 33 | Vss | 99 | CB2_A | 165 | CS1_B_n | 231 | Vss | 34 | DQ9_A | 100 | DQS4_A_c | 166 | Vss | 232 | DQS2_B_t |
| 35 | DQ10_A | 101 | Vss | 167 | Vss | 233 | DQ20_B | 36 | Vss | 102 | DQS4_A_t | 168 | CB0_B | 234 | Vss |
| 37 | Vss | 103 | CB3_A | 169 | DQS4_B_c | 235 | Vss | 38 | DQ11_A | 104 | Vss | 170 | Vss | 236 | DQ21_B |
| 39 | DQS1_A_c | 105 | Vss | 171 | DQS4_B_t | 237 | DQ22_B | 40 | Vss | 106 | CS0_A_n | 172 | CB1_B | 238 | Vss |
| 41 | DQS1_A_t | 107 | CA0_A | 173 | Vss | 239 | Vss | 42 | DM1_A_n | 108 | ALERT_n | 174 | Vss | 240 | DQ23_B |
| 43 | Vss | 109 | CA1_A | 175 | CB3_B | 241 | DQ24_B | 44 | Vss | 110 | CS1_A_n | 176 | CB2_B | 242 | Vss |
| 45 | DQ12_A | 111 | Vss | 177 | Vss | 243 | Vss | 46 | DQ13_A | 112 | Vss | 178 | Vss | 244 | DQ25_B |
| 47 | Vss | 113 | CA2_A | 179 | DQ0_B | 245 | DQ26_B | 48 | Vss | 114 | CA3_A | 180 | DQ1_B | 246 | Vss |
| 49 | DQ14_A | 115 | CA4_A | 181 | Vss | 247 | Vss | 50 | DQ_15_A | 116 | CA5_A | 182 | Vss | 248 | DQ27_B |
| 51 | Vss | 117 | Vss | 183 | DQ2_B | 249 | DQS3_B_c | 52 | Vss | 118 | Vss | 184 | DQ3_B | 250 | Vss |
| 53 | DQ16_A | 119 | CA6_A | 185 | Vss | 251 | DQS3_B_t | 54 | DQ17_A | 120 | CA7_A | 186 | Vss | 252 | DM3_B_n |
| 55 | Vss | 121 | CA8_A | 187 | DM0_B_n | 253 | Vss | 56 | Vss | 122 | CA9_A | 188 | DQS0_B_c | 254 | Vss |
| 57 | DQ18_A | 123 | Vss | 189 | Vss | 255 | DQ28_B | 58 | DQ19_A | 124 | Vss | 190 | DQS0_B_t | 256 | DQ29_B |
| 59 | Vss | 125 | CA10_A | 191 | DQ4_B | 257 | Vss | 60 | Vss | 126 | CA11_A | 192 | Vss | 258 | Vss |
| 61 | DM2_A_n | 127 | CA12_A | 193 | Vss | 259 | DQ30_B | 62 | DQS2_A_c | 128 | RFU | 194 | DQ5_B | 260 | DQ31_B |
| 63 | Vss | 129 | Vss | 195 | DQ6_B | 261 | Vss | 64 | DQS2_A_t | 130 | Vss | 196 | Vss | 262 | Vss |
| 65 | DQ20_A | 131 | CK0_A_t | 197 | Vss | | | 66 | Vss | 132 | CK1_A_t | 198 | DQ7_B | | |

3. Pin Descriptions

| Symbol | Type | I/O Level | Description | Symbol | Type | I/O Level | Description |
|--------------------------|------------------|-----------|-------------------------------|------------------------------|------------------|-----------|-----------------------------|
| CK_t, CK_c | Input | VDDQ | Clock | DQ[31:0]_A DQ[31:0]_B | Input/ Output | VDDQ | Data Input/Output |
| CA[12:0]_A CA[12:0]_B | Input | VDDQ | Command/Address Inputs | CB[3:0]_A CB[3:0]_B | Input/ Output | VDDQ | ECC Check Bits Input/Output |
| CS[1:0]_A CS[1:0]_B | Input | VDDQ | Chip Select | DQS[4:0]_A_t DQS[4:0]_B_t | Input/ Output | VDDQ | Data Strobe |
| ALERT_n | Output | VDDQ | Alert | DQS[4:0]_A_c DQS[4:0]_B_c | Input/ Output | VDDQ | Data Strobe |
| RESET_n | CMOS Input | VDDQ | Active Low Asynchronous Reset | DM[3:0]_A_n DM[3:0]_B_n | Input | VDDQ | Input Data Mask |
| PWR_GOOD | Input/ Output | VDDQ | Power Good Indicator | VIN_BULK | Supply | | External Power Supply |
| HSCL | Input | VOUT | Host Sideband Bus Clock | PWR_EN | Input | | PMIC Enable |
| HSDA | Input/ Output | VOUT | Host Sideband Bus Data | VSS | Supply | | Ground |
| HSA | Input | GND | Host Sideband Bus Device ID | RFU | | | Reserved for future use |

4. Function Block Diagram



5. Thermal Characteristics

| Symbol | Parameter | | Rating | Units | Note |
|------------------------|-----------------------|------------------------|------------|-------|---------|
| T_c | Operation Temperature | Normal Operating Temp. | 0 to 85 | °C | 1,2,3 |
| | | Extended Temp. | 85 to 95 | °C | 1,2,3,4 |
| T_{stg} | Storage Temperature | | -55 to 100 | °C | 5 |

Note:

1. Maximum operating case temperature; T_c is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_c during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_c during operation.
4. If T_c exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95μs interval refresh rate.
5. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

6. IDD, IDDQ and IPP Specifications

| Symbol | Description | Value | | Units |
|--------|--|----------|----------|-------|
| | | IDD Max. | IPP Max. | |
| IDD0 | Operating One Bank Active-Precharge Current | 460 | 180 | mA |
| IDD0F | Operating Four Bank Active-Precharge Current | 840 | 280 | mA |
| IDD2N | Precharge Standby Current | 280 | 140 | mA |
| IDD2P | Precharge Power-Down Current | 660 | 140 | mA |
| IDD3N | Active Standby Current | 570 | 160 | mA |
| IDD3P | Active Power-Down Current | 330 | 160 | mA |
| IDD4R | Operating Burst Read Current | 1940 | 210 | mA |
| IDD4W | Operating Burst Write Current | 2200 | 180 | mA |
| IDD5B | Burst Refresh Current (Normal Refresh Mode) | 2570 | 810 | mA |
| IDD5C | Burst Refresh Current (Same Bank Refresh Mode) | 990 | 360 | mA |
| IDD6N | Self Refresh Current: Normal Temperature Range | 640 | 270 | mA |
| IDD6E | Self Refresh Current: Extended Temperature Range | 940 | 350 | mA |
| IDD7 | Operating Bank Interleave Read Current | 3140 | 730 | mA |
| IDD8 | Maximum Power Saving Deep Power Down Current | 200 | 140 | mA |

7. Timing Parameters

| Parameter | Symbol | 5600 | | 6000 | | 6400 | | Unit |
|---|------------|-------------------------|-----|-------------------------|-----|-------------------------|-----|------|
| | | Min | Max | Min | Max | Min | Max | |
| Clock Timing | | | | | | | | |
| Average clock period | tCK,AVG | 0.357 | | 0.333 | | 0.312 | | ns |
| Command and Address Timing | | | | | | | | |
| Read to Read command delay for same bank group | tCCD_L | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | nCK |
| WRITE to WRITE command delay for same bank group | tCCD_L_WR | 32nCK, 20ns (MAX) | | 32nCK, 20ns (MAX) | | 32nCK, 20ns (MAX) | | nCK |
| WRITE to WRITE command delay for same bank group, second WRITE not RMW | tCCD_L_WR2 | 16nCK, 10ns (MAX) | | 16nCK, 10ns (MAX) | | 16nCK, 10ns (MAX) | | nCK |
| Read to Read or Write to Write command delay for different bank group for BL16, BC8 OTF | tCCD_S | 8 | | 8 | | 8 | | nCK |
| ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size | tRRD_S,2K | 8 | | 8 | | 8 | | nCK |
| ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size | tRRD_S,1K | 8 | | 8 | | 8 | | nCK |
| ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size | tRRD_L,2K | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | nCK |
| ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size | tRRD_L,1K | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | nCK |
| Four activate window for | tFAW,2K | 40nCK, | | 40nCK, | | 40nCK, | | ns |

| | | | | | | | | |
|---|---------|-----------------------------|--|-----------------------------|--|-----------------------------|--|-----|
| 2KB page size | | 14.280ns (MAX) | | 13.333ns (MAX) | | 12.500ns (MAX) | | |
| Four activate window for 1KB page size | tFAW,1K | 32nCK, 11.428ns (MAX) | | 32nCK, 10.666ns (MAX) | | 32nCK, 10.000ns (MAX) | | ns |
| Delay from start of internal WRITE transaction to internal READ command for different bank group | tWTR_S | 2.5 | | 2.5 | | 2.5 | | ns |
| Delay from start of internal WRITE transaction to internal READ command for same bank group | tWTR_L | 10 | | 10 | | 10 | | ns |
| Delay from start of internal WRITE transaction to internal READ with AUTO PRECHARGE command for same bank | tWTRA | tWR-tRTP | | tWR-tRTP | | tWR-tRTP | | ns |
| Internal READ command to PRECHARGE command delay | tRTP | 7.5 | | 7.5 | | 7.5 | | ns |
| PRECHARGE to PRECHARGE delay | tPPD | 2 | | 2 | | 2 | | nCK |
| WRITE recovery time | tWR | 30 | | 30 | | 30 | | ns |

9. RoHS Declaration

| | | |
|--|------------------------------------|----------|
| innodisk | 宜鼎國際股份有限公司 Innodisk Corporation | Page 1/2 |
| Tel:(02)7703-3000 Internet: https://www.innodisk.com/ | | |
| RoHS 自我宣告書 (RoHS Declaration of Conformity) | | |
| Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products | | |
| <p>一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及 (EU) 2015/863 關於 RoHS 之規範要求。 Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.</p> <p>二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。 Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.</p> <p>三、 本公司聲明我們的產品符合 RoHS 指令的附件中 7(a)、7(c)-I、6(c) 允許豁免。 We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.</p> <p>※ 7(a) Lead in high melting temperature type solders (i. e. lead-based alloys containing 85% by weight or more lead).</p> <p>※ 7(c)-I Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.</p> <p>※ 6(c) Copper alloy containing up to 4% lead by weight. (This exemption applies to products that use antennas)</p> | | |
| Name of hazardous substance | Limited of RoHS ppm (mg/kg) | |
| 鉛 (Pb) | < 1000 ppm | |
| 汞 (Hg) | < 1000 ppm | |
| 鎘 (Cd) | < 100 ppm | |
| 六價鉻 (Cr 6+) | < 1000 ppm | |
| 多溴聯苯 (PBBs) | < 1000 ppm | |
| 多溴二苯醚 (PBDEs) | < 1000 ppm | |
| 鄰苯二甲酸二(2-乙基己基)酯 (DEHP) | < 1000 ppm | |
| 鄰苯二甲酸丁酯苯甲酯 (BBP) | < 1000 ppm | |
| 鄰苯二甲酸二丁酯 (DBP) | < 1000 ppm | |

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宜鼎國際股份有限公司
Innodisk Corporation

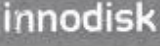


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| | |
|------------------|------------|
| 鄰苯二甲酸二異丁酯 (DIBP) | < 1000 ppm |
|------------------|------------|

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司Company Representative 公司代表人： Randy Chien 簡川勝Company Representative Title 公司代表人職稱： Chairman 董事長Date 日期： 2021 / 06 / 09

10. REACH Declaration

| | |
|--|--|
|  | <p style="text-align: center;">宜鼎國際股份有限公司 Innodisk Corporation REACH Declaration</p> |
| <p style="text-align: right;">Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: https://www.innodisk.com/</p> | |
| <p>Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006). We hereby confirm that the product(s),</p> | |
| <p>Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.</p> | |
| <ul style="list-style-type: none"> ■ The standard products of not listed in the <u>Appendix2</u> meet the requirements of REACH SVHC regulations(SVHCs < 0.1% in Article), as described in the candidate list table currently including 224 substances and shown on the ECHA website. (http://echa.europa.eu/de/candidate-list-table). ■ The standard products listed in the <u>Appendix2</u> contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table. Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs > 0.1% in Article). ■ Comply with REACH Annex XVII. | |
| <p style="text-align: center;">Guarantor</p> | |
| <p>Company name 公司名稱： <u>Innodisk Corporation 宜鼎國際股份有限公司</u></p> | |
| <p>Company Representative 公司代表人： <u> 陳怡全</u></p> | |
| <p>Company Representative Title 公司代表人職稱： <u>QA Manager 品保經理</u></p> | |
| <p>Date 日期： <u>2022 / 06 / 14</u></p> | |
|  | |

Revision Log

| Rev | Date | Modification |
|-----|--------------------------------|---------------------|
| 0.1 | 11 th December 2023 | Preliminary Edition |
| 1.0 | 11 th December 2023 | Official released |