

CorePower – Emergency Backup Power Supply White Paper

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1. Introduction

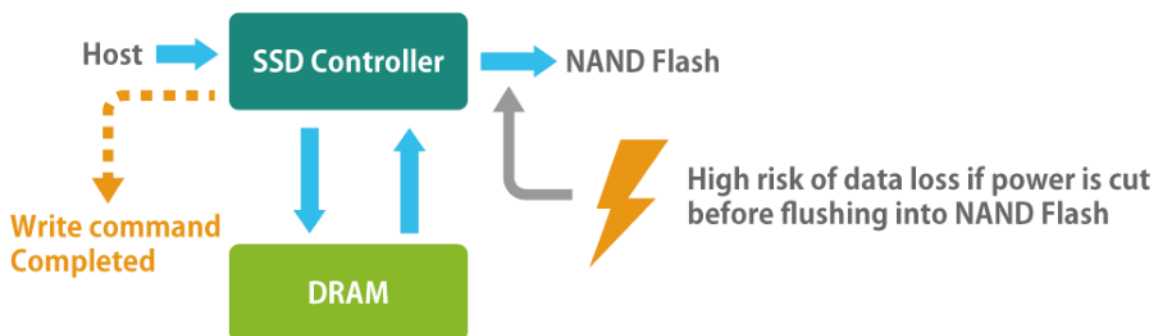
Since SSDs are often deployed in demanding environments, power disruptions may occur unexpectedly and potentially cause catastrophic damages to the data in the drive. Especially for SSDs with built-in volatile DRAM buffer, data can be lost if a power outage occurs before the cached data is moved into the non-volatile NAND Flash.

2. Potential Data Risks by Power Failure

Power instabilities can harm SSDs' productivity and efficiency, and eventually lead to higher maintenance cost. Frequently observed damages caused by power instability include data loss, Link Table damage and page corruption as explained in the following sections.

2.1 Data Loss Risk

If the power supply is insufficient, SSDs are unable to complete programming to the NAND blocks. In other words, data in the transferring progress between the host system and the SSD could be at risk of being lost, if the power supply is unstable. This risk may be more apparent for SSDs designed with a DRAM as write cache for random performance improvement. For SSDs with DRAM cache, the controller will temporarily store data from host write in the DRAM cache first, and the host will be informed that the write operation is completed. Then the data will be moved from DRAM to NAND flash. If a sudden power outage occurs during this process, there would be data loss.



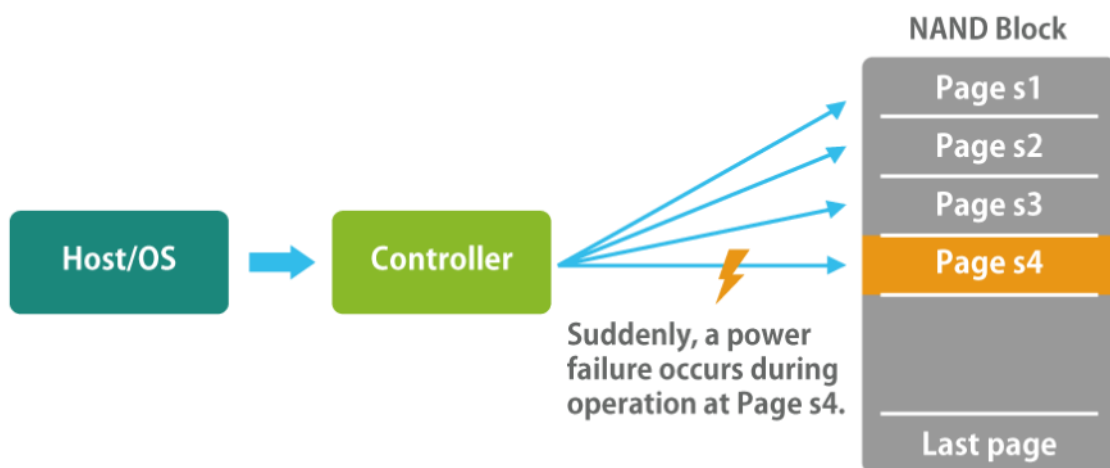
2.2 Link Table Damage

In an unexpected power-down, the mapping information processed by Link Table is at great risk. The reason is that mapping information of Link Table, like DRAM write cache, is temporarily cached in the controller stage and it becomes "solid" or "hardened" information once it is moved into flash memory. In other words, mapping information can be lost if a power failure occurs before it is flushed into the

physical blocks. If mapping information is lost and the Link Table is damaged, the device may show corrupted data at the next power up and the host might not be able to retrieve valid data from the device.

2.3 Corrupted Page

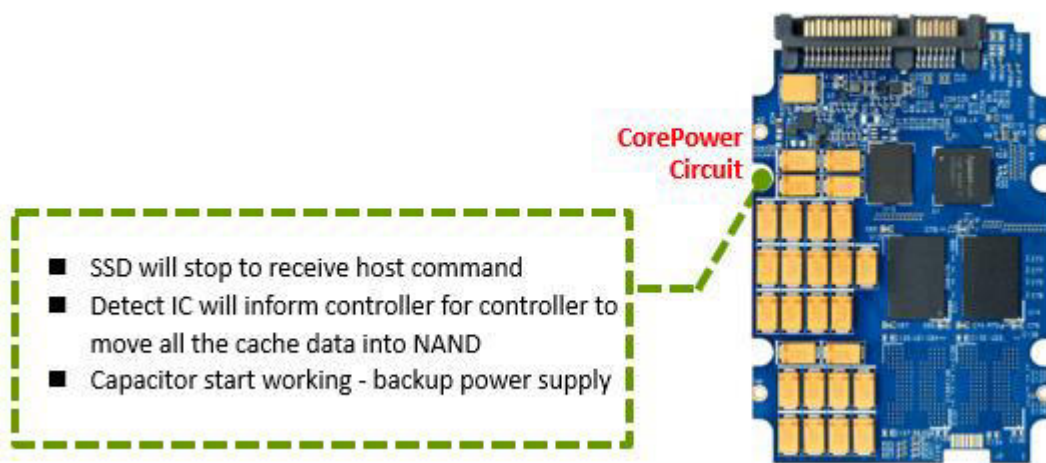
NAND flash programming is usually divided into multiple write operations and each is written to a page of a block. As illustrated below, the write operation is carried out one page at a time in most NAND flash devices. If a sudden power failure occurs during the programming, the page with programming-in-progress data will be found invalid and with error. For instance, in the following illustration, the host is performing write operations to a NAND block. Suddenly, power goes off while page s4 is being programmed. Data written by the previous program operations on page s1, s2, and s3 can be retained because the data has already been written into the flash chips during programming operation. However, data in page s4 is invalid with error when the power resumes. The ECC in firmware will detect and correct the error in page s4 to ensure data integrity of the entire block.



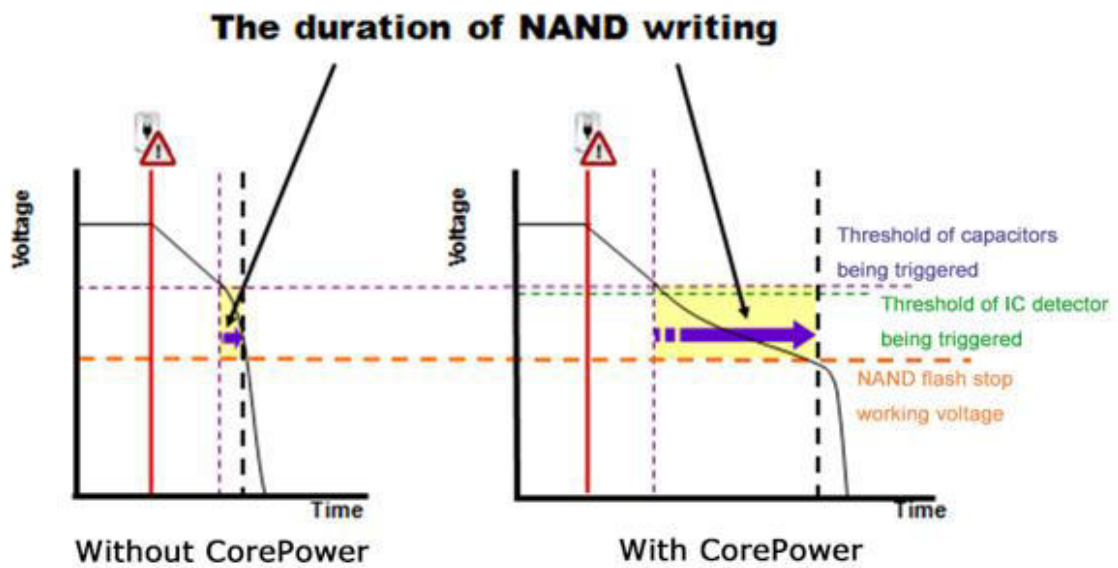
3. CorePower

To protect SSD data integrity from the disastrous scenarios above, Apacer has developed the hardware-based technology named CorePower. The CorePower technological implementation equips Apacer SSDs with comprehensive power solution that provides multiple reliability measures. The following will discuss some scenarios to explain how this technology protects SSDs from power disruptions.

If the voltage supply is cut, for instance, by accidental power off or sudden blackout, the data would be shortly lost. To prevent this situation from happening, the CorePower equips SSDs with powerful tantalum capacitors that can deliver sufficient urgent power current so that the flash controller can take this extended moment to flush cached and essential data into NAND Flash blocks.

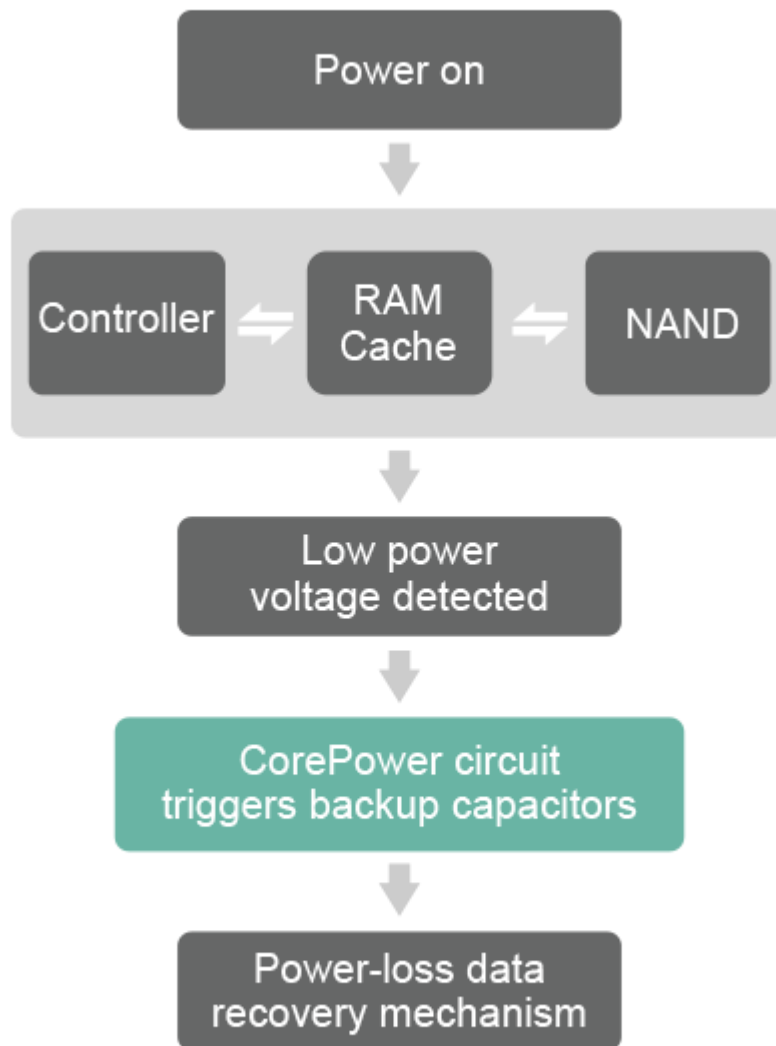


To ensure proper operations, CorePower equips SSDs with reliable and enduring tantalum capacitors that not only allow the controller to gain the needed extended moment from urgent backup power current, but also the ability to operate in a wide range of ambient temperatures. Moreover, CorePower is an ideal power solution for applications where reliability and performance are concerned.



4. Conclusion

It's hard to predict when power supply may be lost. In order to minimize the negative effects that disruption of power supply can have on SSDs, Apacer developed the CorePower protection mechanism. It's the best way to reduce permanent damage due to power interruption while also preserving data integrity. Ask your Apacer Representative to learn more about this cutting-edge technology.



Firmware Solution + CorePower

Revision History

Revision	Description	Date
1.0	Official release	6/20/2016
1.1	Updated the template to the latest format	12/29/2020
1.2	Updated chart graphics	3/18/2021
1.3	Updated capacitor information	5/31/2023

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