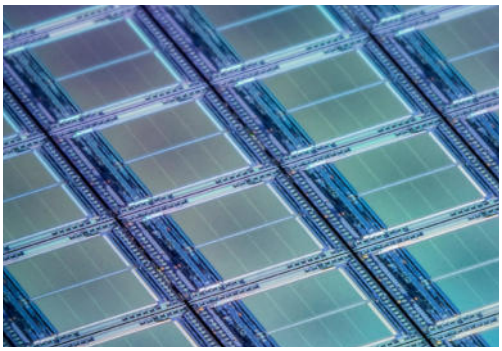
White Paper

iSLC – Claiming the Middle Ground of the High-end Industrial SSD Market



Summary

iSLC is a NAND flash technology designed to optimize the balance between cost and performance. This firmware technology is based on the framework of 3D triple-level cell (TLC) NAND Flash, where each cell of 3D TLC NAND Flash is made to hold only 1 bit per cell instead of 3 bits, thereby enabling the effective emulation of single-level cell (SLC) NAND Flash.

iSLC is a hybrid of 3D TLC and SLC technology with a performance closer to SLC and durability much superior to 3D TLC. The price of iSLC is roughly between the prices of 3D TLC and SLC.

In the market, the program/erase cycles (P/E cycles) of 3D TLC can reach up to 3,000 times, while SLC boasts 60,000 times. Innodisk's exclusive technology elevates iSLC to achieve 30,000 P/E cycles. Furthermare, with the latest Ultra iSLC advanced technology, the P/E cycles can reach up to 100,000 times. The burn-in test result indicates that the P/E cycles of the iSLC solid-state drive (SSD) greatly surpass the stated P/E cycle limitations, and no data loss or read failure was found.

In terms of the operating life test, iSLC outperforms 3D TLC devices under the same operating conditions. As for the writing test, results show that iSLC is comparable with SLC in performance.

Introduction

Choosing the optimal storage solution for system integrators can be very challenging. Although 3D TLC has sufficient storage capacity, it cannot provide the demanded performance and durability. Meanwhile, the cost of SLC may outweigh its disadvantages. Therefore, iSLC technology was developed for the demands between high-end/critical SLC and the low-end 3D TLC markets.

iSLC technology is a flash memory solution for improving the performance, reliability, and durability of 3D TLC NAND flash. Through screening and programming the SSD firmware, the capability of the cells can be enhanced, allowing 3D TLC NAND flash to emulate SLC NAND.

The primary purpose of this white paper is to explain the differences among the NAND mentioned above Flash technologies and how iSLC has become a solution with broader applications for embedded and advanced products markets.

Background

Manufacturers developed ways to store more bits and data in each NAND Flash cell as technology evolves. Devices based on TLC technology have been manufactured, holding 3 bits in each cell. Manufacturers are also conducting research and development on the quad-level cells (QLC) technology, which will enable storing 4 bits in each cell. Such a trend will further reduce costs and increase storage capacity.

As each TLC cell can hold 3 bits, there are 8 possible states for each cell; similarly, QLC cells have 16 possible states. As the number of bits that a cell can hold increases, the states of these cells become even more intertwined, causing the fault tolerance rate of each state to decrease. Therefore, the disadvantage of such capacity-enhancing technology is that the number of P/E cycles allowed by each unit will be greatly reduced, reducing the storage unit service life.

The increase in the bits a cell can store causes a decrease in state fault tolerance. Why?

SLC has 2 possible states, while TLC has 8 possible states. Within the same voltage range of the cell, being divided into two is enough to represent the 2 states of SLC. But it takes 8 divisions to represent the 8 states of TLC. That is, as soon as the state of TLC is slightly shifted by interference, it may repeat its adjacent state. As for SLC, its original state is not easily influenced by such factors. Even though the error bits caused by such interferences can be fixed with the error correction code (ECC), they will still impact the performance. A lower error bit rate of an SSD unit thus indicates better performance.

The increase in the bits that a cell can store causes the number of P/E cycles allowed per cell to decrease. Why?

There is an inherent problem in SSD: cell degradation. When a cell is programmed or erased, a relatively powerful electric shock is generated, and such a process will slightly damage the cell substrate each time. The integrity of the substrate directly affects the ability of the cell to maintain its state. The more P/E cycles there are, the more damage is done to the substrate, resulting in the cell having less ability to maintain its state. However, as SLC has better state fault tolerance, greater state drift is allowed without data misjudgment, making SLC more tolerant of substrate damages from P/E cycles. On the contrary, TLC is less tolerant of substrate damage from P/E cycles. When the cell allows more P/E cycles, the lifespan of the unit will be longer.

However, for ordinary consumers, the development of 3D TLC or other technologies allowing more bits per cell is still exciting news because it makes SSDs more affordable, and durability is still sufficient for daily use. As for enterprise and industrial applications, they demand higher P/E cycles and stricter performance requirements. Thus, 3D TLC (or other technologies allowing more bits per cell) is inappropriate for such applications.

SLC vs 3D TLC

The major difference between SLC and 3D TLC is the number of bits that each NAND cell holds. SLC stores 1 bit of data per cell, while 3D TLC stores 3 bits of data per NAND cell, which makes SLC more fault-tolerant than 3D TLC while supporting more PE Cycles per cell. SLC can provide better durability and is a perfect choice for advanced applications. Other differences between SLC and 3D TLC include the time for reading, writing, and erasing, the P/E cycle, and how error bits are handled (as shown in Table 1).

Table 1: Comparing SLC and 3D TLC

	Program Page	Erase Block	P/E Cycle	Bits corrected by ECC
SLC (24nm)	400μs	4ms	60K	24 bit/ 1024Bytes
3D TLC	2300μs	10ms	3K	120 bit/ 1024Bytes

As the table shows, on top of the faster speed, the raw bit error rate (RBER) of SLC, which is the number of written bit errors, is also lower. For example, If the sequence 01 01 01 01 is written as 01 11 11 01, two error bits have occurred. In the case of RBER, there are 2 error bits out of 8, resulting in an error rate of 0.25 or 25%.

SLC NAND is more reliable and durable than 3D TLC, making it the ideal choice for industrial and enterprise applications. However, compared to the costly SLC NAND, 3D TLC NAND's affordability is still rather advantageous, even if some performance and durability will be sacrificed. The popularity of 3D TLC NAND is mainly driven by its low price, which has led 3D TLC NAND manufacturers to produce units of higher capacity to be more cost-effective. However, such a tradeoff will result in reduced reliability and durability, as shown in Figure 1. As NAND Flash technology has been upgraded from 32 layers to 112 layers, manufacturers need higher ECC capabilities to compensate for the reduction in reliability and durability.

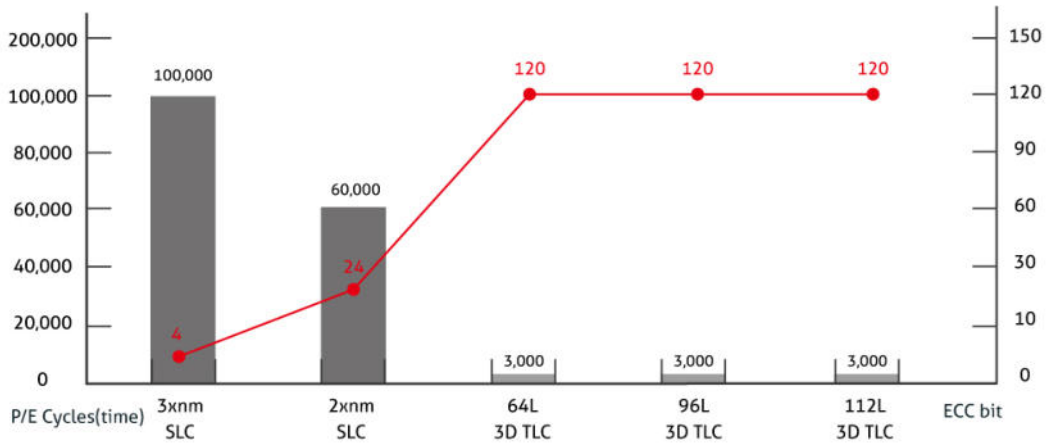


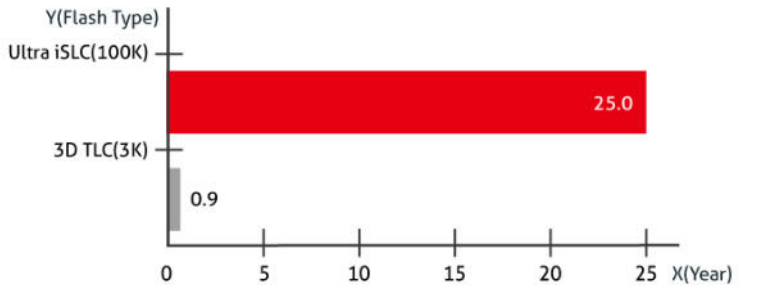
Figure 1 : NAND Flash Trend

Many applications lie between these two flash memory types. 3D TLC is excluded due to performance and durability requirements. Therefore, system integrators have no choice but to use the more costly SLC options.

Cost-performance Optimization with iSLC

Ideally, iSLC should have a performance on par with SLC flash, while its cost is close to choosing a 3D TLC flash.

Figure 2 shows an example of increased durability. Using a 2TB SSD, while the Drive Writes Per Day (DWPD) is 10, the lifespan of an Ultra iSLC unit can still last for 25 years, while a 3D TLC unit can last less than 1 year before failing. The lifespan of an Ultra iSLC unit is about 30 times longer than a 3D TLC unit.



Note: The above diagram is based on a test environment for a 100% sequential write.

Figure 2: Ultra iSLC and 3D TLC endurance comparison

iSLC uses in-house designed firmware that forces 3D TLC flash to emulate SLC cells. Each SLC cell can only store 1 bit (1 or 0), while 3D TLC can hold 3 bits (000, 001, 010, 011, 100, 101, 110, 111). iSLC can emulate SLC by having only 1 bit in each NAND cell (see Figure 3). Such firmware configuration allows the flash to work like SLC flash, which also improves the durability and data retention levels of 3D TLC NAND flash.

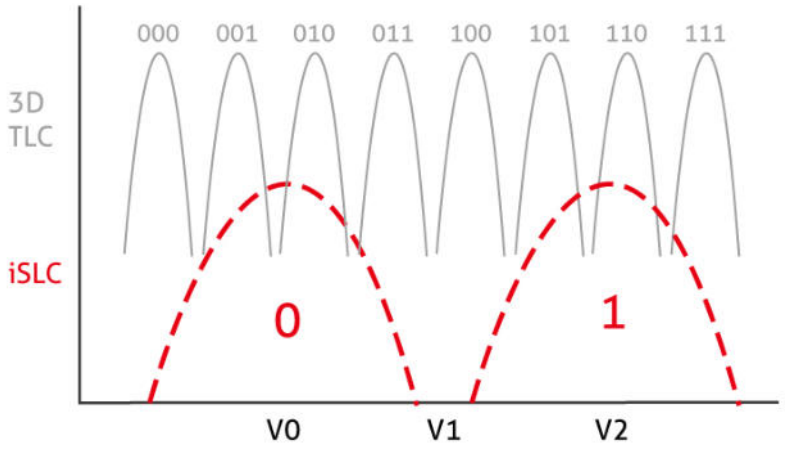


Figure 3: iSLC firmware technology

Test Data

The average durability of Ultra iSLC exceeds 100,000 P/E cycles, which significantly prolongs the service life of the drive when compared to a 3D TLC flash.

Our tests indicate that the error bits of Ultra iSLC are lower than 3D TLC. When comparing the technology nodes of Ultra iSLC and 3D TLC, as the 112L Ultra iSLC P/E cycle reaches 100,000 times, the number of error bits is about 2. When the P/E cycle of 3D TLC goes 3,200 times, the number of error bits is about 16. Table 2 shows the comparison of the number of error bits between Ultra iSLC and 3D TLC .

Table 2: Error bits Comparison between Ultra iSLC and 3D TLC

Flash Type	Average Erase Count	Error bit
Ultra iSLC	100,000	2 bits
3D TLC	3,200	16 bits

Note.

1. The number of error bits that 3D TLC series controllers can fix all reaches 120bits/1K, which means that when the P/E cycle reaches the guaranteed number of times, the occurrence of error bits is still substantially within the range of the controller's fixing ability
2. The above values are for reference only. The occurrence of error bit will vary according to the actual usage

Conclusion

The advantages of iSLC and Ultra iSLC can be summarized as:
- Extended lifetime and improved reliability compared to 3D TLC
- Performance similar to SLC
- About half the price of SLC

Ultra iSLC technology achieves a fine balance between cost-effectiveness and performance. Increasing the number of P/E cycles extends the product lifespan, reaching up to 10 times that of similar 3D TLC devices while matching the performance of SLC flash memory. These attributes make Ultra iSLC an ideal storage solution, particularly well-suited for the high-end industrial and embedded products markets, where cost-efficient alternatives are in demand.

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