MB970

Intel ® Ivy Bridge / PCH
ATX Motherboard

USER'S MANUAL

Version 1.0A

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Table of Contents

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Introduction

Product Description

The MB970 ATX motherboard is based on the latest Intel$^@$ Q77 chipset. The platform supports 3rd generation Intel$^@$ Core processor family with LGA1155 packing and features an integrated dual-channel DDR3 memory controller as well as a graphics core.

The latest Intel$^@$ processors provide advanced performance in both computing and graphics quality. This meets the requirement of customers in the gaming, POS, digital signage and server market segment.

The Q77 platform is made with 22 nanometer technology that supports Intel's first processor architecture to unite the CPU and the graphics core on the transistor level. The MB970 ATX board utilizes the dramatic increase in performance provided this Intel's latest cutting-edge technology. Measuring 305mm x 244mm, the MB970 offers fast 6Gbps SATA support (2 ports), USB3.0 (2 ports) and interfaces for DVI-D, DVI-I and DP displays. MB970VF features Intel Active Management Technology 8.0.

MB970 FEATURES:

- Supports Intel$^@$ 3rd Generation Core i7/i5/i3 QC/DC desktop processors
- Four DDR3 DIMM, 1066/1333/1600MHz, Max. 32GB memory
- Dual Intel$^@$ PCI-Express Gigabit LAN
- Integrated Graphics for DVI-I, DVI-D/HDMI displays
- 4x SATA 2.0, 2x SATA 3.0, 10x USB 2.0, USB 3.0 (4 ports), 4x COM, Watchdog timer
- 1x PCI-E (x16), 3x PCI-E (x1), 3x PCI
- Optional AMT (MB970VF only)

Checklist

Your MB970 package should include the items listed below.

- The MB970 ATX motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Serial ATA cable

MB970 Specifications

Product Name	**MB97VF/MB970F**
Form Factor	ATX
CPU Type	- Intel® Ivy Bridge 22nm QC/DC DT processor - LGA package 37.5 mm x 37.5mm(TDP: QC= 95W/65W/45W ; DC=65W/45W) **Ivy-DT CPU socket compatible with Sandy Bridge
CPU Speed	Up to 3.8GHz
Cache	Up to 8MB
CPU Socket	**LGA1155 (Socket H2)**
Chipset	Intel® Q77[MB970VF] / B75[MB970F] PCH 27 x 27 mm package size
BIOS	AMI BIOS, support ACPI Function
Memory	Intel® Ivy-Bridge DT processors integrated memory controller DDRIII 1067/1333/1600 MHz - DIMM x 4 (w/o ECC), Max.32GB

VGA	- Intel® Ivy-Bridge DT processor integrated Gfx
	- Supports 3 independent displays
	- Improvement in 3D graphic performance (DX 11.1, OpenGL 3.1, Open CL1.1)
	- One analog port (VGA) and 3 digital ports (DisplayPort, DVI/HDMI & SDVO)
	   DVI-I X 1 (thru Level shifter ASM1442)
	   DVI-D X 1 (thru DP to DVI converter PS161)
	   DisplayPort X 1

LAN	1. Intel® Lewisville 82579LM GbE PHY[MI970VF only] or 82579**V** GbE PHY [MI970F only] 2. Intel® 82583V as 2nd GbE
USB	USB **2.0** host controller, supports **8** or **10** ports w/ two EHCI, 7 UHCI controllers - 4 ports in the rear panel - Others reserved for onboard pin header - 6 ports for MB970VF ; **4** ports for MB970F USB **3.0** host controller, supports **4** ports
Serial ATA	Intel® Q77 / B75 PCH built-in SATA controller, supports total 6 ports **2** x SATA (3.0) 6Gbps/+ 4 x SATA (2.0) 3Gbps ports [MB970VF] **1**x SATA (3.0) 6Gbps/+ 4 x SATA (2.0) 3Gbps ports [MB970F]
Storage Device	CFast [SATA CF] connector x1
Audio	Intel® Q77 PCH built-in High Definition Audio controller+ ALC892 w/ 7.1 CH
LPC I/O	Fintek **F81866AD-I** (Ver. C) COM1 (RS232/422/485), COM2~COM4 (RS232) Hardware Monitor (2 thermal inputs, 4 voltage monitor inputs & **3** x fan headers) COM1/2 with pin-9 with power for 2 ports (500mA for each port)
Digital IO	4 in & 4 out
IAMT(8.0)	Intel® Q77 PCH built-in (**MB970VF only)** - Intel® Active Management Technology Version 8.0
TPM 1.2	Winbond WPCT210A (**MB970VF only)**
PCI to ISA	ITE IT8888G x1 for high ISA bus
Expansion Slots	- PCI-Express (16x) x1 [PEG]; PCI-Express 1x) x3; PCI x3; ISA x1
Edge Connectors	DVI-D + DVI-I stack connector; Dual DB9 stack connector for COM #1, #2 Dual USB (3.0) dual stack connector; DP stack connector Gigabit LAN RJ-45 + dual USB (2.0) stack connector x2 RCA Jack 3 x 1 for HD Audio
Onboard Header/ Connector	2 ports x SATA **III** [Blue color]; 4 ports x SATA II 2x5 pin-header x3 for 6 ports USB; 2x5 pin-header for front panel audio 2x10 box-header for COM3 (RS232) & COM4 (RS232) 2x5 pin-header for Digital IO
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
System Voltage	**ATX**
Others	LAN Wakeup, vProTM [MB970VF only], EuP feature (F81866AD-I integrated)

| Board Size	305mm x 244mm

Board Dimensions
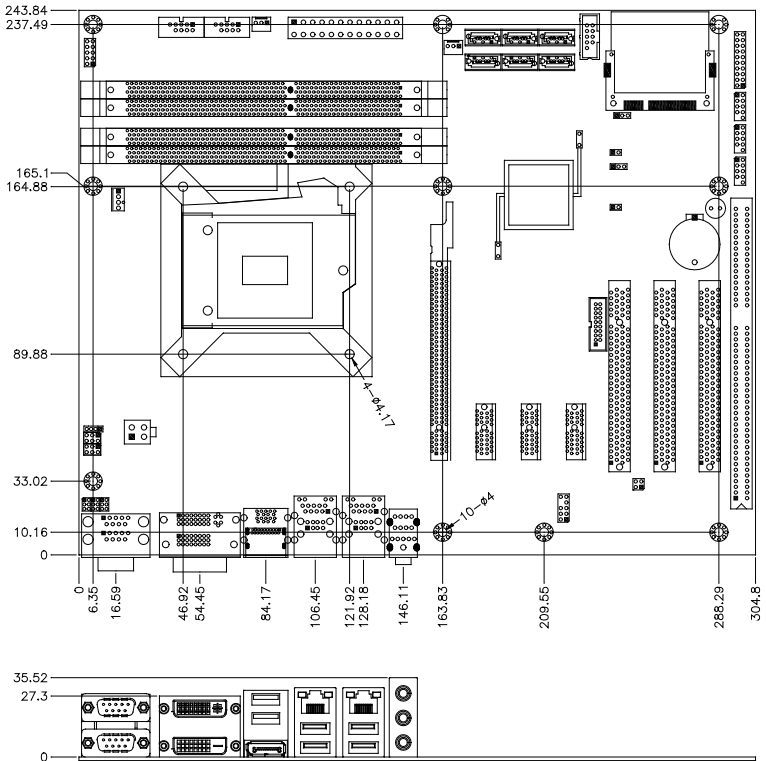
Installations

This section provides information on how to use the jumpers and connectors on the MB970 in order to set up a workable system. The topics covered are:

Installing the CPU

The MB970 board supports an LGA1155 Socket (shown below) for Intel Sandy Bridge processors.

To install the CPU, unlock first the socket by pressing the lever sideways, then lift it up to a 90-degree. Then, position the CPU above the socket such that the CPU corner aligns with the gold triangle matching the socket corner with a small triangle. Carefully insert the CPU into the socket and push down the lever to secure the CPU. Then, install the heat sink and fan.
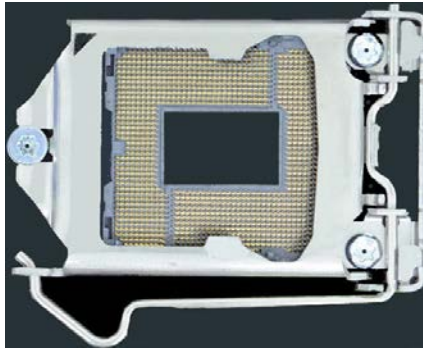
NOTE: *Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

Installing the Memory

The MB970 board supports four DDR3 memory socket for a maximum total memory of 32GB in DDR3 DIMM memory type.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.

2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.

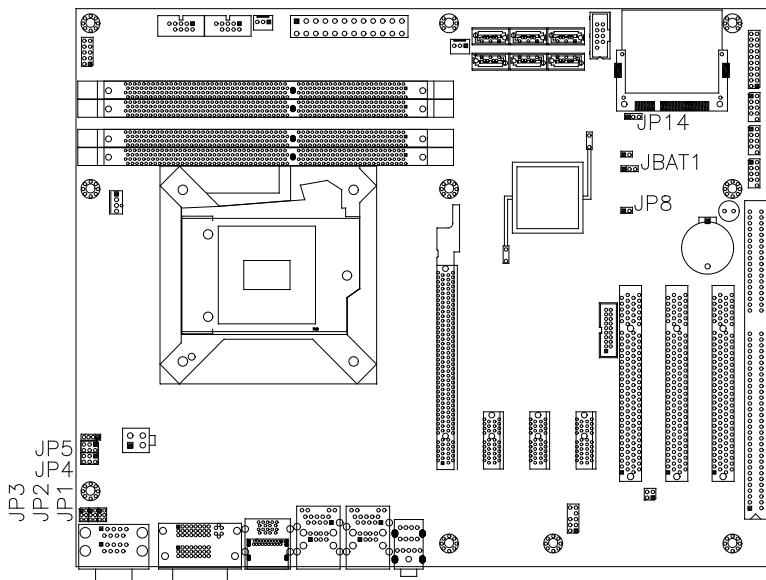3. To remove the DDR3 module, press the clips with both hands.
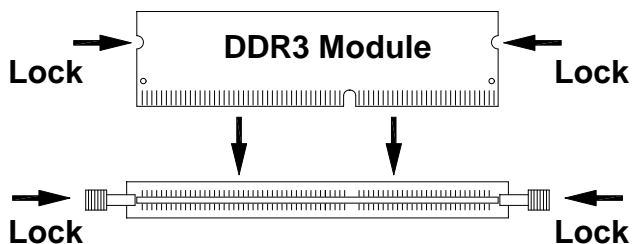
Setting the Jumpers

Jumpers are used on MB970 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on MB970 and their respective functions.

Jumper Locations on MB970

JBAT1: Clear CMOS Contents
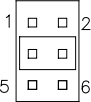
JBAT1	Setting	Function
□ □ □ 1 2 3	Pin 1-2 Short/Closed	Normal
□ □ □ 1 2 3	Pin 2-3 Short/Closed	Clear CMOS

JP1, JP2, JP3: RS232/RS422/RS485 (COM1) Selection
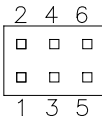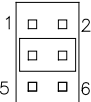
COM1 Function	RS-232	RS-422	RS-485
Jumper Setting (pin closed)	JP1: 3-5&4-6	JP1: 1-3&2-4	JP1: 1-3&2-4
	JP3: 1-2	JP3: 3-4	JP3: 5-6
	JP2: 3-5 & 4-6	JP2: 1-3 & 2-4	JP2: 1-3 & 2-4

2 4 6
□ □ □
□ □ □
1 3 5

JP4: COM1 RS232 RI/+5V/+12V Power Setting

JP4	Setting	Function
1 □ □ 2 □ □ 5 □ □ 6	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 5-6 Short/Closed	+5V

JP5: COM2 RS232 RI/+5V/+12V Power Setting

JP5	Setting	Function
1 □ □ 2 □ □ 5 □ □ 6	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 5-6 Short/Closed	+5V

JP8: Flash Descriptor Security Override (Factory use only)

JP8	Flash Descriptor Security Override
Open	Disabled (Default)
Close	Enabled

JP14: SATA (CN12) / CFAST (CN16) Selection

JBAT1	Setting	Function
`□ □ | □` 1 2 3	Pin 1-2 Short/Closed	CFAST
`□ | □ □` 1 2 3	Pin 2-3 Short/Closed	SATA

Connectors on MB970

Connector Locations on MB970

CN2: COM1 and COM2 Serial Ports
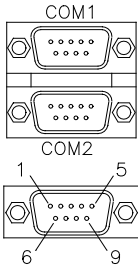
Pin #	Signal Name		
	RS-232	**R2-422**	**RS-485**
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC
10	NC	NC	NC

CN3: DVI-D and DVI-I Connector
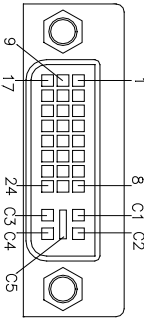
Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	HOT POWER
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
VSYNC	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	Red
SHIELD 1/3	11	C2	Green
DATA 3-	12	C3	Blue
DATA 3+	13	C4	HSYNC
DDC POWER	14	C5	A GROUND2
A GROUND 1	15	C6	A GROUND3
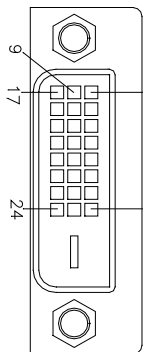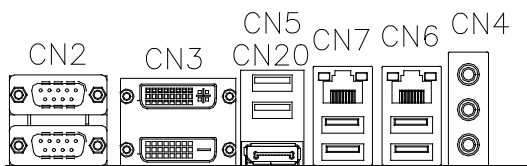
Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	HOT POWER
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
N.C	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	N.C.
SHIELD 1/3	11	C2	N.C.
DATA 3-	12	C3	N.C.
DATA 3+	13	C4	N.C.
DDC POWER	14	C5	N.C.
A GROUND 1	15	C6	N.C.

CN20: USB3.0 Connector

J19, J20: COM3, COM4 RS232 Serial Ports

Signal Name	Pin #	Pin #	Signal Name
DCD#	1	6	DSR#
SIN#	2	7	RTS#
SOUT	3	8	CTS#
DTR#	4	9	RI#
GND	5	X	KEY

CN7: Gigabit LAN (Intel 82579LM) + USB 2/3

CN6: Gigabit LAN (Intel 82583V) + USB 0/1
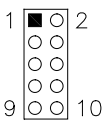
CN4: HD Audio Connector

CN5: Display Port Connector

CN9, CN10, CN11, CN12, CN13, CN14: SATA Connectors
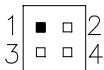
CN8: Compact Flash Connector

J1: Audio Pin Header for Chassis Front Panel

Signal Name	Pin	Pin	Signal Name
MIC IN_L	1	2	Ground
MIC IN_R	3	4	DET
LINE_R	5	6	Ground
Sense	7	8	KEY
LINE_L	9	10	Ground
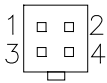
J2: SPDIF I/O

Pin #	Signal Name
1	SPDIF IN
2	Ground
3	SPDIF OUT
4	Ground

J3: ATX 12V Power Connector
This connector supplies the CPU operating voltage.

Pin #	Signal Name
1	Ground
2	Ground
3	+12V
4	+12V

J4: ISA Slot (shared with PCI1)

J19, J20: COM3, COM4 RS232 Serial Ports

Signal Name	Pin #	Pin #	Signal Name
DCD#	1	6	DSR#
SIN#	2	7	RTS#
SOUT	3	8	CTS#
DTR#	4	9	RI#
GND	5	X	KEY

J7, J12, J14: USB Connectors
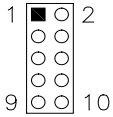
Signal Name	Pin	Pin	Signal Name
VCC	1	2	VCC
D0-	3	4	D1-
D0+	5	6	D1+
GND	7	8	GND
KEY	9	10	NC

J15: Front Panel Function Connector
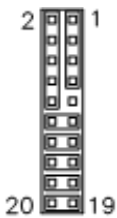
Signal Name	Pin #	Pin #	Signal Name
SPK +	1	2	PWR LED +
NC	3	4	NC
SPK – (GND)	5	6	PWR LED- (GND)
SPK – (GND)	7	8	NC
NC	9	10	NC
NC	11	12	NC
PWR_SW	13	14	PWR_SW
NC	15	16	NC
RST	17	18	GND
HDD LED -	19	20	HDD LED +
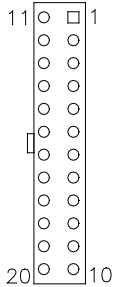
J16: Digital I/O
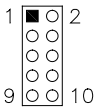
Signal Name	Pin	Pin	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0
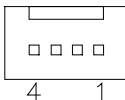
J17: SPI Flash Connector (Factory use only)

J18: ATX Power Supply Connector
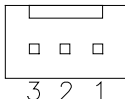
Signal Name	Pin #	Pin #	Signal Name
3.3V	11	1	3.3V
-12V	12	2	3.3V
Ground	13	3	Ground
PS-ON	14	4	+5V
Ground	15	5	Ground
Ground	16	6	+5V
Ground	17	7	Ground
-5V	18	8	Power good
+5V	19	9	5VSB
+5V	20	10	+12V

CPU_FAN1: CPU Fan Power Connector
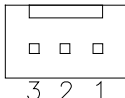
Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Control

SYS_FAN1: System Fan1 Power Connector

Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

SYS_FAN2: System Fan2 Power Connector

Pin #	Signal Name
1	Ground
2	+12V
3	NC

PCIE2: PCI-E X16 Slot

PCIE3, PCIE4, PCIE5: PCI-E X1 Slot

PCI1-PCI3: PCI 32-bit Slot

BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

```
Press  <DEL>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

Main Settings

Aptio Setup Utility – Copyright © 2011 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit	
BIOS Information					Choose the system default language	
System Language		[English]			→ ←Select Screen	
System Date		[Tue 01/20/2009]			↑↓ Select Item	
Access Level		Administrator			Enter: Select	
					+- Change Field	
					F1: General Help	
					F2: Previous Values	
					F3: Optimized Default	
					F4: Save ESC: Exit	

System Language
Choose the system default language.

System Date
Set the Date. Use Tab to switch between Data elements.

System Time
Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

► PCI Subsystem Settings
► ACPI Settings
► Wake up event setting
► Trusted Computing
► CPU Configuration
► SATA Configuration
► Shutdown Temperature Configuration
► iSmart Controller
► AMT Configuration
► Acoustic Management Configuration
► USB Configuration
► F81866 Super IO Configuration
► F81866 H/W Monitor
► CPU PPM Configuration

```
→ ←Select Screen
↑↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

PCI Subsystem Settings

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

PCI Bus Driver Version	V 2.0502
PCI 64bit Resources Handing	
Above 4G Decoding	Disabled
PCI Common Settings	
PCI Latency Timer	32 PCI Bus Clocks
VGA Palette Snoop	Disabled
PERR# Generation	Disabled
SERR# Generation	Disabled
► PCI Express Settings	

```
→ ←Select Screen
↑↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

Above 4G Decoding

Enables or Disables 64bit capable devices to be decoded in above 4G address space (only if system supports 64 bit PCI decoding).

PCI Latency Timer
Value to be programmed into PCI Latency Timer Register.

VGA Palette Snoop
Enables or disables VGA Palette Registers Snooping.

PERR# Generation
Enables or disables PCI device to generate PERR#.

SERR# Generation
Enables or disables PCI device to generate SERR#.

PCI Express Settings
Change PCI Express devices settings.

PCI Express Settings

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
PCI Express Device Register Settings					
Relaxed Ordering			Disabled		
Extended Tag			Disabled		
No Snoop			Enabled		
Maximum Payload			Auto		→ ←Select Screen
Maximum Read Request			Auto		↑↓ Select Item
					Enter: Select
PCI Express Link Register Settings					+- Change Field
ASPM Support			Disabled		F1: General Help
WARNING: Enabling ASPM may cause			Disabled		F2: Previous Values
some PCI-E devices to fail					F3: Optimized Default
Extended Synch			Disabled		F4: Save ESC: Exit
Link Training Retry			5		
Link Training Timeout (uS)			100		
Unpopulated Links			Keep Link ON		

Relaxed Ordering
Enables or disables PCI Express Device Relaxed Ordering.

Extended Tag
If ENABLED allows device to use 8-bit Tag field as a requester.

No Snoop
Enables or disables PCI Express Device No Snoop option.

Maximum Payload
Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Maximum Read Request
Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support
Set the ASPM Level: Force L0s – Force all links to L0s State:
AUTO – BIOS auto configure :   DISABLE – Disables ASPM.

Extended Synch
If ENABLED allows generation of Extended Synchronization patterns.

Link Training Retry
Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Link Training Timeout (uS)
Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

Unpopulated Links
In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

ACPI Settings

Main	Advanced	Chipset	Boot	Security	Save & Exit

ACPI Settings

Enable Hibernation	Enabled
ACPI Sleep State	S3 (Suspend to R…)
Lock Legacy Resources	Disabled
S3 Video Repost	Disabled

→ ←Select Screen
↑↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

Enable Hibernation
Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State
Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

Lock Legacy Resources
Enabled or Disabled Lock of Legacy Resources.

S3 Video Repost
Enable or disable S3 Video Repost.

Wake up event settings

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
Wake system with Fixed Time			Disabled		
Wake up hour			0		
Wake up minute			0		
Wake up second			0		
					→ ←Select Screen
Wake on Ring			Disabled		↑ ↓ Select Item
Wake on PCI PME			Disabled		Enter: Select
Wake on PCIE Wake Event			Disabled		+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

Wake system with Fixed Time
Enables or Disables System wake on alarm event. When enabled, System will wake on the hr::min:: sec specified.

Wake on PCIE PME Wake Event
The options are Disabled and Enabled.

Trusted Computing

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
TPM Configuration					
TPM SUPPORT			Disabled		→ ←Select Screen
					↑ ↓ Select Item
Current TPM Status Information					Enter: Select
TPM SUPPORT OFF					+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

TPM Support
This configuration is supported only with MB970VF. Enables or Disables TPM support. O.S. will not show TPM. Reset of platform is required.

Security Device Support
Enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

CPU Configuration

This section shows the CPU configuration parameters.

<div align="center">Aptio Setup Utility</div>

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
CPU Configuration					
Intel® Core ™ i7-3770 CPU @ 3.40GHz					
Processor Stepping		306a8			
Microcode Revision		c			
Max CPU Speed		3400 MHz			
Min CPU Speed		1600 MHz			
CPU Speed		3400 MHz			
Processor Cores		4			
Intel HT Technology		Supported			
Intel VT-x Technology		Supported			
Intel SMX Technology		Supported			
64-bit		Supported			
Hyper-threading		Enabled			→ ←Select Screen
Active Processor Cores		All			↑↓ Select Item
Limit CPUID Maximum		Disabled			Enter: Select
Execute Disable Bit		Enabled			+- Change Field
Intel Virtualization Technology		Disabled			F1: General Help
Hardware Prefetcher		Disabled			F2: Previous Values
Adjacent Cache Line Prefetch		Enabled			F3: Optimized Default
					F4: Save ESC: Exit

Hyper-threading
Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

Active Processor Cores
Number of cores to enable in each processor package.

Limit CPUID Maximum
Disabled for Windows XP.

Execute Disable Bit
XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, Re33dHat Enterprise 3 Update 3.)

Intel Virtualization Technology
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Hardware Prefetcher
To turn on/off the Mid level Cache (L2) streamer Prefetcher.

Adjacent Cache Line Prefetch
To turn on/off prefetching of adjacent cache lines.

SATA Configuration
SATA Devices Configuration.

Aptio Setup Utility					
Main	**Advanced**	Chipset	Boot	Security	Save & Exit
SATA Controller(s)		Enabled			
SATA Mode Selection		RAID			
Aggressive LPM Support		Enabled			
SATA Controller Speed		Gen3			
SATA Port0		Empty			→ ←Select Screen
Software Preserve		Unknown			↑ ↓ Select Item
SATA Port1		Empty			Enter: Select
Software Preserve		Unknown			+- Change Field
SATA Port2		Empty			F1: General Help
Software Preserve		Unknown			F2: Previous Values
SATA Port3		Empty			F3: Optimized Default
Software Preserve		Unknown			F4: Save ESC: Exit
SATA Port4		Empty			
Software Preserve		Unknown			
SATA Port5		Empty			
Software Preserve		Unknown			

SATA Controller(s)
Enable / Disable Serial ATA Controller.

SATA Mode Selection
(1) IDE Mode.
(2) AHCI Mode.
(3) RAID Mode.

Shutdown Temperature Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

APCI Shutdown Temperature	Disabled

→ ←Select Screen
↑↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

ACPI Shutdown Temperature
The default setting is Disabled.

iSmart Controller

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

iSmart Controller

Power-On after Power failure	Disable

| Schedule Slot 1 | None |
| Schedule Slot 2 | None |

→ ←Select Screen
↑↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

ISmart Controller
Setup the power on time for the system.

Schedule Slot 1 / 2
Setup the hour/minute for system power on.

AMT Configuration

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

Intel AMT	Enabled
BIOS Hotkey Pressed	Disabled
MEBx Selection Screen	Disabled
Hide Un-Configure ME Confirmation	Disabled
Un-Configure ME	Disabled
Amt Wait Timer	0
Activate Remote Assistance Process	Disabled
USB Configure	Enabled
PET Progress	Enabled
AMT CIRA Timeout	0
Watchdog	Disabled
OS Timer	0
BIOS Timer	0

```
→ ←Select Screen
↑↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

AMT Configuration
This configuration is supported only with MB970VF (with iAMT function). Options are Enabled and Disabled.
Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

Unconfigure ME
This configuration is supported only with MB970VF (with iAMT function). Perform AMT/ME unconfigure without password operation.

Amt Wait Timer
Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

Activate Remote Assistance Process
Trigger CIRA boot.

PET Progress
User can Enable/Disable PET Events progress to receive PET events or not.

Watchdog Timer
This configuration is supported only with MB970VF (with iAMT function). Enable/Disable Watchdog Timer.

Acoustic Management Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit

Acoustic Management Configuration

Acoustic Management   Disabled

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

USB Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

USB Configuration

USB Devices:
    2 Hubs

Legacy USB Support	Enabled
USB3.0 Support	Enabled
XHCI Hand-off	Enabled
EHCI Hand-off	Enabled
Port 60/64 Emulation	Enabled
USB hardware delays and time-outs:	
USB Transfer time-out	20 sec
Device reset tine-out	20 sec
Device power-up delay	Auto

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected.
DISABLE option will keep USB devices available only for EFI
applications.

USB3.0 Support

Enable/Disable USB3.0 (XHCI) Controller support.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The
XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off
Enabled/Disabled. This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

Port 64/60 Emulation
Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

USB Transfer time-out
The time-out value for Control, Bulk, and Interrupt transfers.

Device reset tine-out
USB mass Storage device start Unit command time-out.

Device power-up delay
Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

F81866 Super IO Configuration

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit
Super IO Configuration					
					→ ←Select Screen
F81866 Super IO Chip		F81866			↑↓ Select Item
► Serial Port 0 Configuration					Enter: Select
► Serial Port 1 Configuration					+- Change Field
► Serial Port 2 Configuration					F1: General Help
► Serial Port 3 Configuration					F2: Previous Values
					F3: Optimized Default
F81866 ERP Support		All Enable			F4: Save ESC: Exit
USB3.0 Port0/1 POWER Management		Enabled			
USB3.0 Port2/3 POWER Management		Enabled			

Serial Port Configuration
Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

F81866 H/W Monitor

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

PC Health Status

CPU_Fan1 smart fan control	Disabled
SYS_Fan1 smart fan control	Disabled
SYS_Fan2 smart fan control	Disabled
CPU temperature	+41 C
SYS temperature	+35 C
CPU_FAN1 Speed	2115 RPM
SYS_ FAN1 Speed	N/A
SYS_ FAN2 Speed	N/A
Vcore	+1.000 V
+5V	+5.213 V
+12V	+12.408 V
1.5V	+1.544 V
+3.3V	+3.424 V

→ ←Select Screen
↑↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

Fan1/Fan2 Smart Fan Control

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

CPU PPM Configuration

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

CPU PPM Configuration

EIST   Enabled
Turbo Mode   Enabled

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

EIST
Enable/Disable Intel SpeedStep.

Chipset Settings
This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

► PCH-IO Configuration
► System Agent (SA) Configuration

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

PCH-IO Configuration

This section allows you to configure the North Bridge Chipset.

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

Intel PCH RC Version	1.1.0.0	
Intel PCH SKU Name	Q77	
Intel PCH Rev ID	O4/C1	
► PCI Express Configuration		
► USB Configuration		
► PCH Azalia Configuration		
PCH LAN Controller	Enabled	
Wake on LAN	Enabled	
High Precision Event Timer Configuration		
High Precision Timer	Enabled	→ ← Select Screen
		↑↓ Select Item
SLP_S4 Assertion Width	4-5 Seconds	Enter: Select
Restore AC Power Loss	Power On	+- Change Field
		F1: General Help
		F2: Previous Values
		F3: Optimized Default
		F4: Save ESC: Exit

PCH LAN Controller
Enable or disable onboard NIC.

Wake on LAN
Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

SLP_S4 Assertion Width
Select a minimum assertion width of the SLP_S4# signal.

Restore AC Power Loss
Select AC power state when power is re-applied after a power failure.

PCI Express Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit

PCI Express Configuration

PCI Express Clock Gating	Enabled
DMI Link ASPM Control	Enabled
DMI Link Extended Synch Control	Disabled
PCIe-USB Glitch W/A	Disabled
Subtractive Decode	Disabled

► PCI Express Root Port 1
► PCI Express Root Port 2
► PCI Express Root Port 3
► PCI Express Root Port 4
► PCI Express Root Port 5
   PCI-E Port 6 is assigned to LAN
► PCI Express Root Port 7
► PCI Express Root Port 8

```
→ ←    Select Screen
↑↓ Select Item
Enter: Select
+-   Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

PCI Express Clock Gating
Enable or disable PCI Express Clock Gating for each root port.

DMI Link ASPM Control
The control of Active State Power Management on both NB side and SB side of the DMI link.

PCIe-USB Glitch W/A
PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG port.

USB Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
USB Configuration					
XHCI Pre-Boot Driver		Enabled			
xHCI Mode		Smart Auto			
HS Port #1 Switchable		Enabled			
HS Port #2 Switchable		Enabled			
HS Port #3 Switchable		Enabled			
HS Port #4 Switchable		Enabled			→ ← Select Screen
xHCI Streams		Enabled			↑↓ Select Item
					Enter: Select
EHCI1		Enabled			+- Change Field
					F1: General Help
EHCI2		Enabled			F2: Previous Values
					F3: Optimized Default
USB Ports Per-Port Disable Control		Disabled			F4: Save ESC: Exit

HS Port #1/2/3/4 Switchable
Allows for HS port switching between xHCI and EHCI. If disabled, port is routed to EHCI. If HS port is routed to xHCI, the corresponding SS port is enabled.

xHCI Streams
Enable or disable xHCI Maximum Primary Stream Array Size.

EHCI1/2
Control the USAB EHCI (USB 2.0) functions. One EHCI controller must always be enabled.

USB Ports Per-Port Disable Control
Control each of the USB ports (0~13) disabling.

PCH Azalia Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
PCH Azalia Configuration					→ ← Select Screen
					↑ ↓ Select Item
Azalia			Auto		Enter: Select
					+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

Azalia
Control Detection of the Azalia device.
Disabled = Azalia will unconditionally disabled.
Enabled Azalia will be unconditionally enabled.
Auto = Azalia will enabled if present, disabled otherwise.

System Agent (SA) Configuration
Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
System Agent Bridge Name			IvyBridge		
System Agent RC Version			1.1.0.0		
VT-d Capability			Supported		
VT-d			Enabled		
CHAP Device (B0:D7:F0)			Disabled		
Thermal Device (B0:D4:F0)			Disabled		→ ←Select Screen
Enable NB CRID			Disabled		↑ ↓ Select Item
BDAT ACPI Table Support			Disabled		Enter: Select
C-State Pre-Wake			Enabled		+- Change Field
					F1: General Help
► Graphics Configuration					F2: Previous Values
► Memory Configuration					F3: Optimized Default
					F4: Save ESC: Exit

VT-d
Check to enable VT-d function on MCH.

Enable NB CRID
Enable or disable NB CRID WorkAround.

C-State Pre-Wake
Controls C-State Pre-Wake feature for ARAT, in SSKPD[57].

Graphics Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
Graphics Configuration					
IGFX VBIOS Version			2132		
IGfx Frequency			350 MHz		
Primary Display			Auto		
Internal Graphics			Auto		→ ←Select Screen
GTT Size			2MB		↑↓ Select Item
Aperture Size			256MB		Enter: Select
DVMT Pre-Allocated			64M		+- Change Field
DVMT Total Gfx Mode			Disabled		F1: General Help
► LCD Control					F2: Previous Values
					F3: Optimized Default
					F4: Save ESC: Exit

Primary Display
Select which of IGFX/PEG/PCI graphics device should be primary display or select SG for switchable Gfx.

Internal Graphics
Keep IGD enabled based on the setup options.

DVMT Pre-Allocated
Select DVMT 5.0 Pre-Allocated (Fixed) graphics memory size used by the internal graphics device.

DVMT Total Gfx Mem
Select DVMT 5.0 total graphics memory size used by the internal graphics device.

Gfx Low Power Mode
This option is applicable for SFF only.

Primary IGFX Boot Display (LCD Control)
Select the Video Device that will be activated during POST. This has no effect if external graphics present. Secondary booty display selection will appear based on your selection. VGA modes will be supported only on primary display.

Memory Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

Memory Information

Memory Frequency	1333 MHz
Total Memory	8192 MB (DDR3)
DIMM#0	2048 MB (DDR3)
DIMM#1	2048 MB (DDR3)
DIMM#2	2048 MB (DDR3)
DIMM#3	2048 MB (DDR3)
CAS Latency (tCL)	9
Minimum delay time	
CAS to RAS (tRCDmin)	9
Row Precharge (tRPmin)	9
Active to Precharge (tRASmin)	24

→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

Boot Settings

This section allows you to configure the boot settings.

Aptio Setup Utility

Main	Advanced	Chipset	**Boot**	Security	Save & Exit

Boot Configuration	
Setup Prompt Timeout	1
Bootup NumLock State	On
Quiet Boot	Disabled
Fast Boot	Disabled
CSM16 Module Version	07.69
GateA20 Active	Upon Request
Option ROM Messages	Force BIOS
INT19 Trap Response	Immediate
Boot Option Priorities	
► CSM parameters	

```
→ ←Select Screen
↑↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

Setup Prompt Timeout
Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State
Select the keyboard NumLock state.

Quiet Boot
Enables/Disables Quiet Boot option.

Fast Boot
Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

GateA20 Active
UPON REQUEST – GA20 can be disabled using BIOS services.
ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages
Set display mode for Option ROM. Options are Force BIOS and Keep Current.

INT19 Trap Response
Enable: Allows Option ROMs to trap Int 19.

Boot Option Priorities
Sets the system boot order.

CSM parameters
This section allows you to configure the boot settings.

		Aptio Setup Utility			
Main	Advanced	Chipset	**Boot**	Security	Save & Exit

```
Launch CSM                        Always
Boot option filter                UEFI and Legacy
Launch PXE OpROM policy           Do not launch
Launch Storage OpROM policy       Legacy only
Launch Video OpROM policy         Legacy only
                                                → ←Select Screen
Other PCI device ROM priority     Legacy OpROM   ↑ ↓ Select Item
                                                Enter: Select
                                                +-  Change Field
                                                F1: General Help
                                                F2: Previous Values
                                                F3: Optimized Default
                                                F4: Save  ESC: Exit
```

Boot option filter
This option controls what devices system can boot to.

Launch PXE OpROM policy
Controls the execution of UEFI and Legacy PXE OpROM.

Launch Storatge OpROM policy
Controls the execution of UEFI and Legacy Storage OpROM.

Launch Video OpROM policy
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI device ROM priority
For PCI devices other than Network, Mass storage or Video defines
which OpROM to launch.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit

Password Description

If ONLY the Administrator's password is set, then this only limit access to Setup and is only asked for when entering Setup.
If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights

The password length must be

in the following range:

Minimum length   3

Maximum length   20

Administrator Password
User Password

→ ←**Select Screen**
↑↓ **Select Item**
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings

Main	**Advanced**	Chipset	Boot	Security	Save & Exit

Save Changes and Exit
Discard Changes and Exit
Save Changes and Reset
Discard Changes and Reset

Save Options
Save Changes
Discard Changes

Restore Defaults
Save as User Defaults
Restore User Defaults

```
→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+-  Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save  ESC: Exit
```

Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) 7 Series Chipset Drivers*.

2. Click *Intel(R) Chipset Software Installation Utility.*

3. When the Welcome screen to the Intel® Chipset Device Software appears, click *Next* to continue.
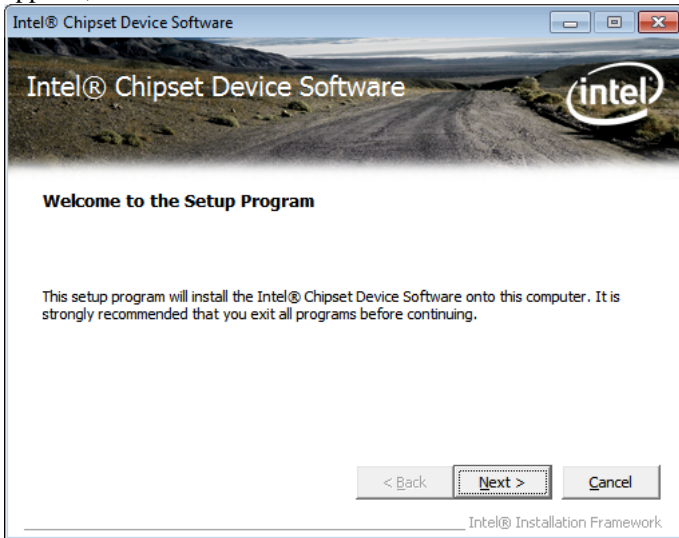
4. Click *Yes* to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click *Next* to continue the installation.
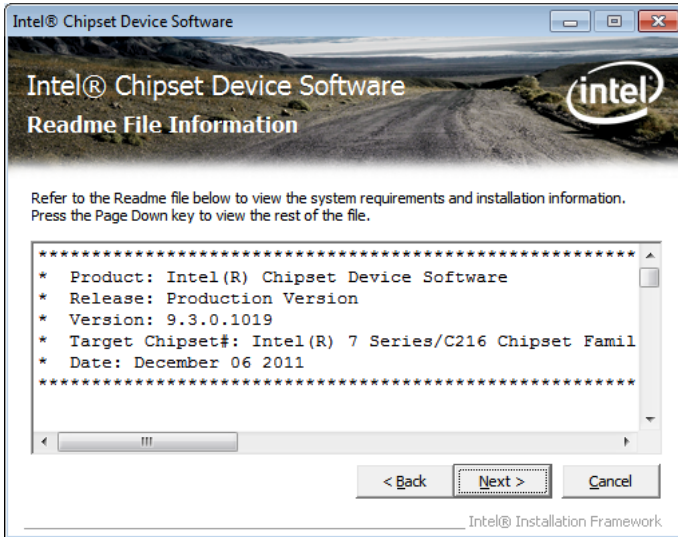
6. The Setup process is now complete. Click *Finish* to restart the computer and for changes to take effect.
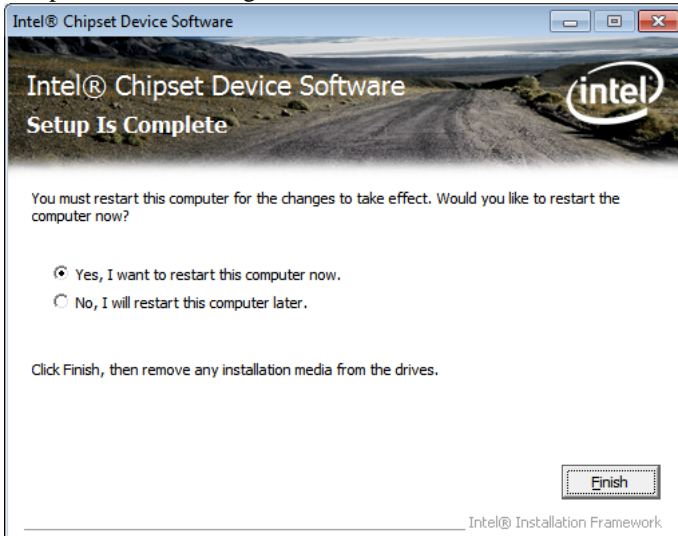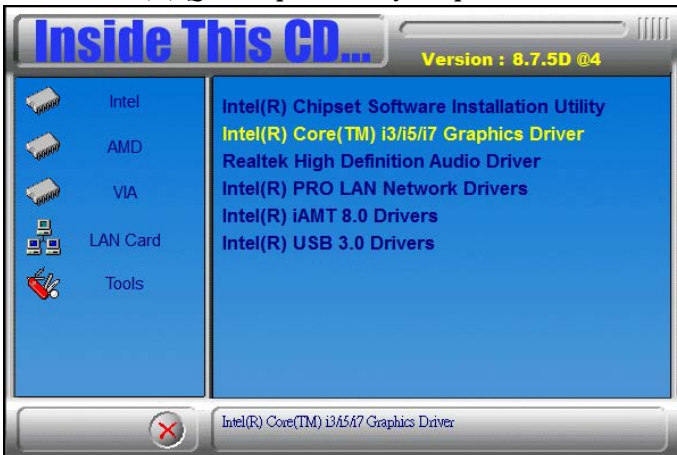
VGA Drivers Installation

NOTE: Before installing the *Intel(R) Q77 Chipset Family Graphics Driver*, the Microsoft .NET Framework 3.5 SPI should be first installed.
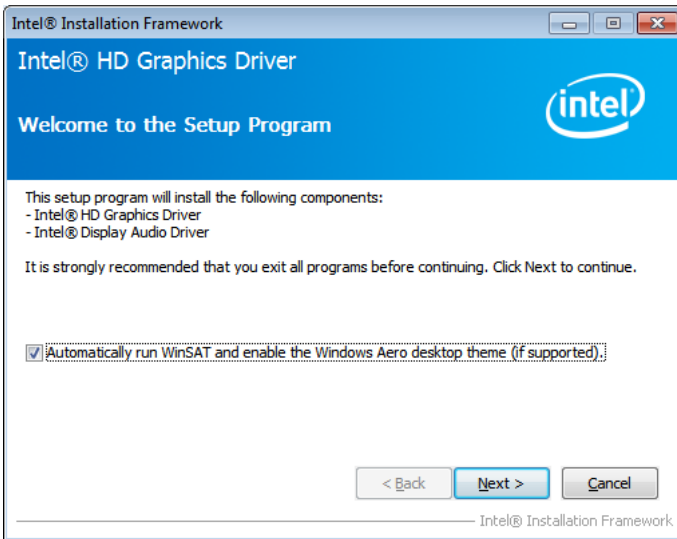
To install the VGA drivers, follow the steps below.

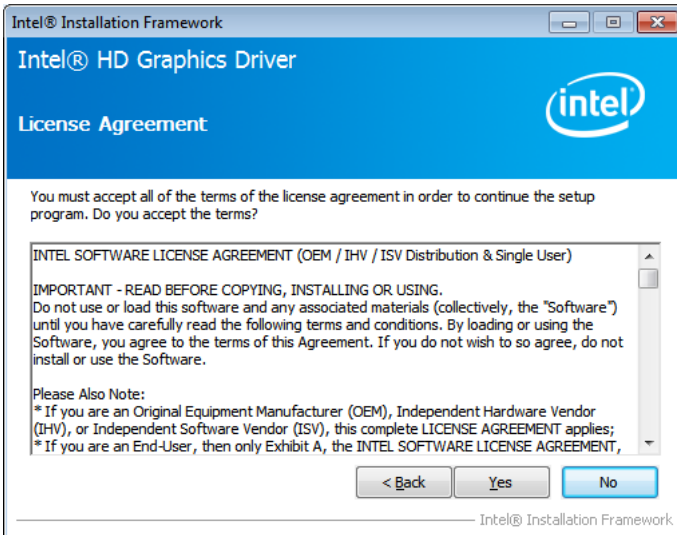1. Insert the CD that comes with the board. Click **Intel** and then **Intel(R) Q7 Series Chipset Drivers**.

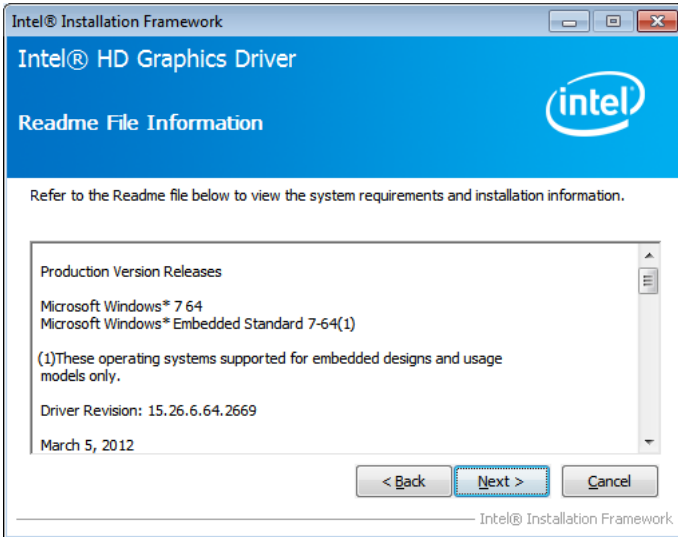2. Click **Intel(R) Q77 Chipset Family Graphics Driver.**

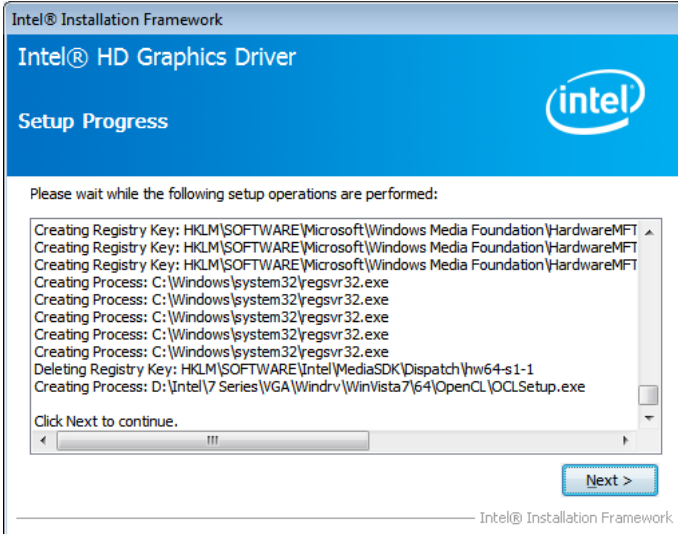3. When the Welcome screen appears, click *Next* to continue.

4. Click *Yes* to to agree with the license agreement and continue the installation.

5. On the Readme File Information screen, click **Next** to continue the installation of the Intel® Graphics Media Accelerator Driver.

6. On Setup Progress screen, click **Next** to continue.

7. Setup complete. Click **Finish** to restart the computer and for changes to take effect.

Realtek HD Audio Driver Installation

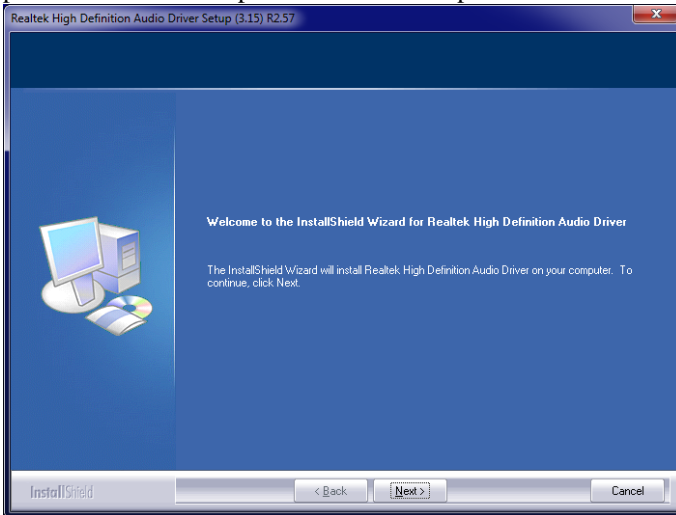Follow the steps below to install the Realtek HD Audio Drivers.
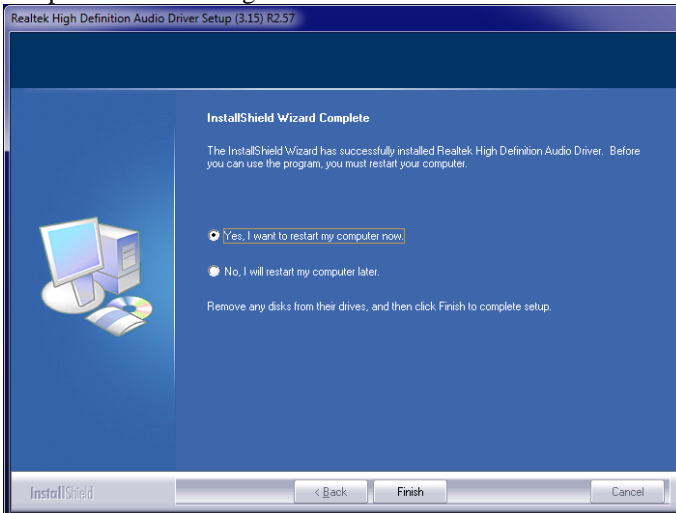1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) Q7 Series Chipset Drivers*.

2. Click *Realtek High Definition Audio Driver.*

3. On the Welcome to the InstallShield Wizard screen, click *Next* to proceed with and complete the installation process.

4. The InstallShield Wizard Complete. Click *Finish* to restart the computer and for changes to take effect.

LAN Drivers Installation

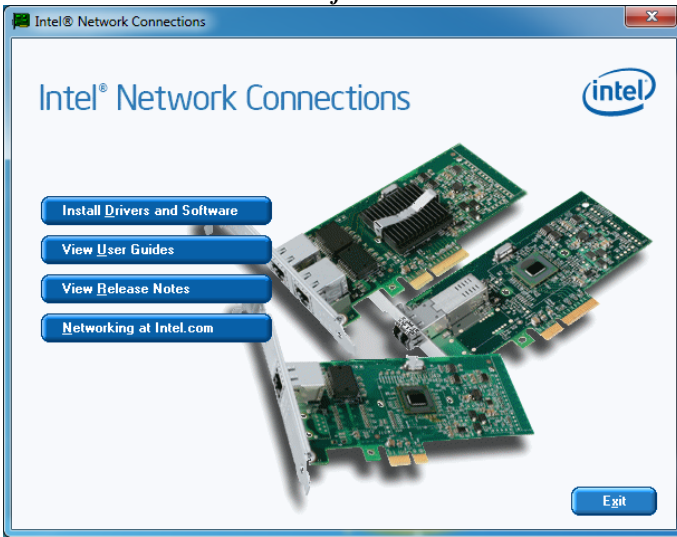1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) Q7 Series Chipset Drivers*.

2. Click *Intel(R) PRO LAN Network Driver.*

3. Click *Install Drivers and Software.*

4. When the Welcome screen appears, click *Next*.
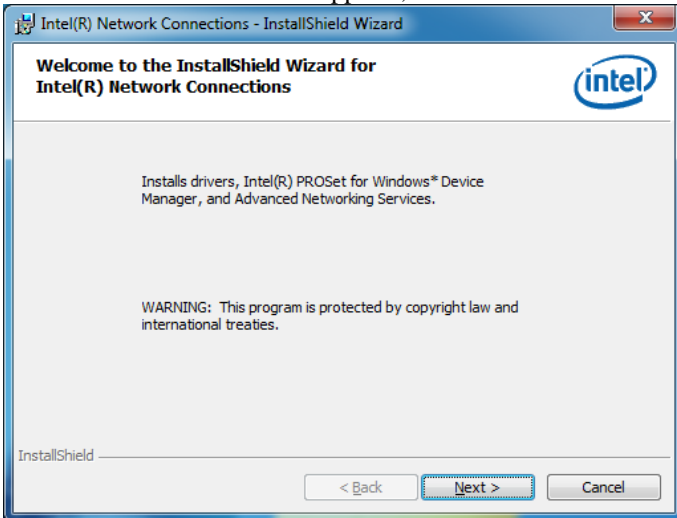
5. Click *Next* to to agree with the license agreement.
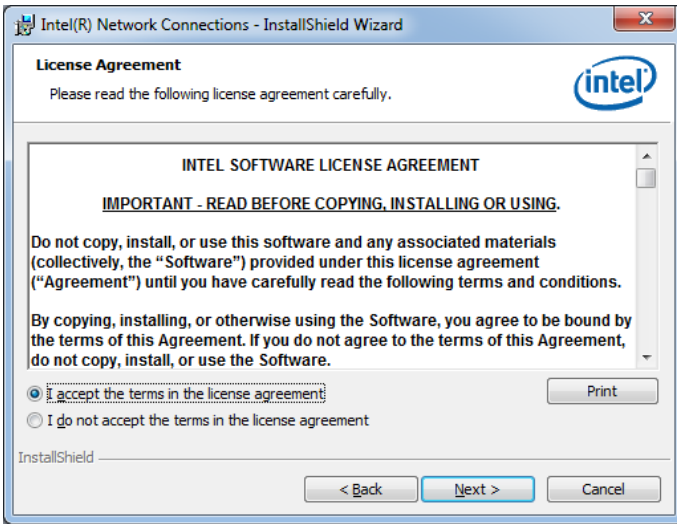
6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.
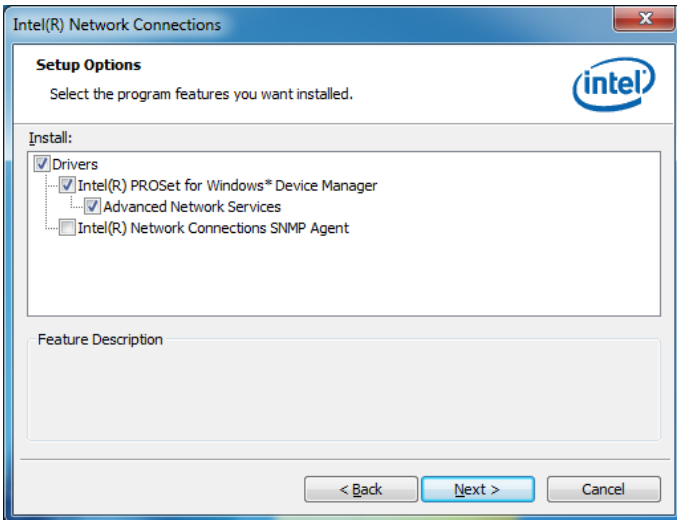
7. The wizard is ready to begin installation. Click **Install** to begin the installation.
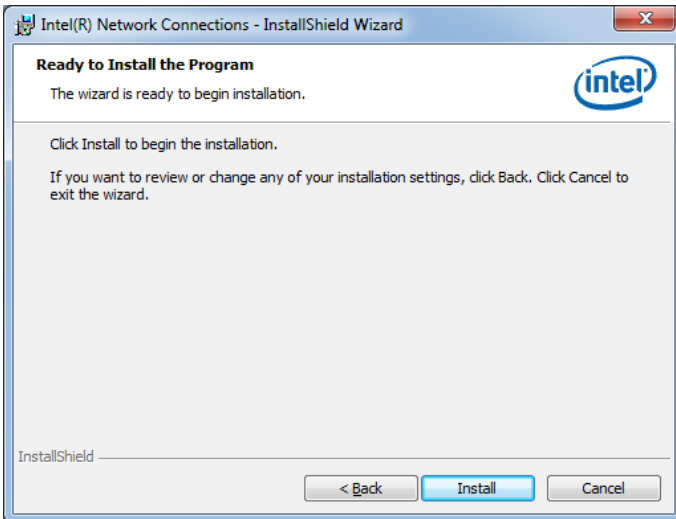
8. When InstallShield Wizard is complete, click **Finish**.
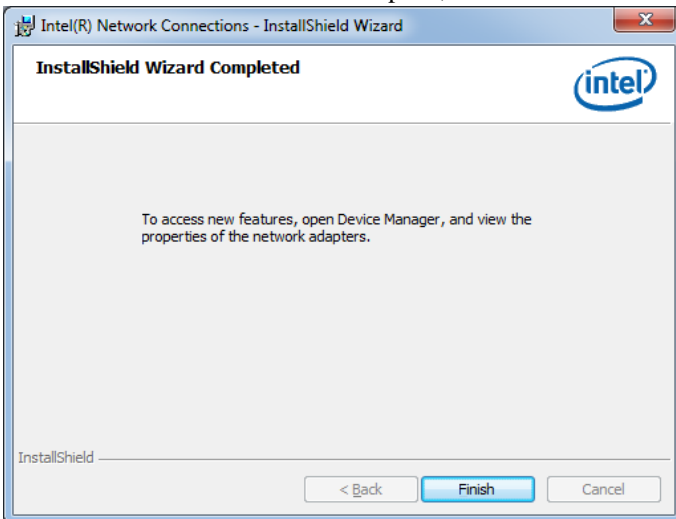
Intel® Management Engine Interface

REMARKS: The Intel iAMT 8.0 Drivers can be installed on MB970VF, not MB970F.

> ⚠ The following application requires Microsoft .NET Framework 3.5 or later: Intel® Management Engine Components. Please install the latest version of Microsoft .NET Framework from Microsoft Download Center to run this application correctly.

Follow the steps below to install the Intel Management Engine.

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) AMT 8.0 Drivers*.

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click *Next*.
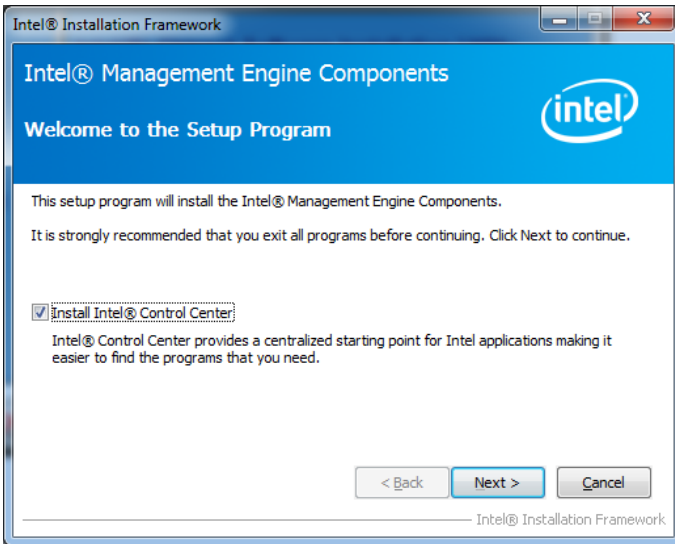
3. Click *Yes* to to agree with the license agreement.
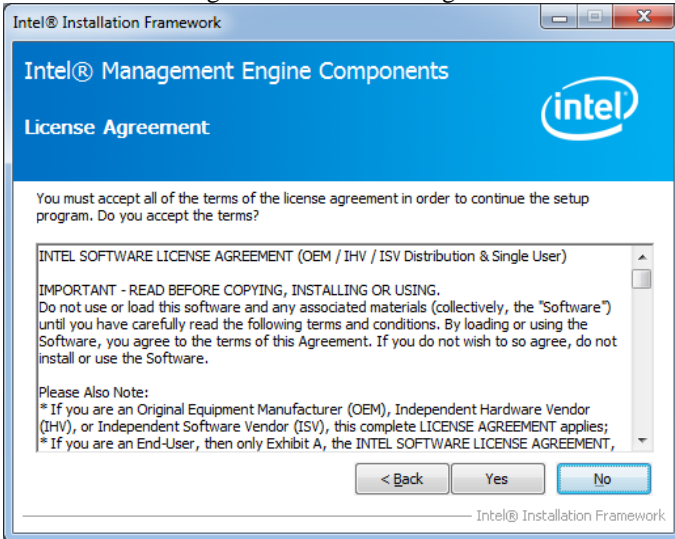
4. When the Setup Progress screen appears, click *Next*. Then, click *Finish* when the setup progress has been successfully installed.
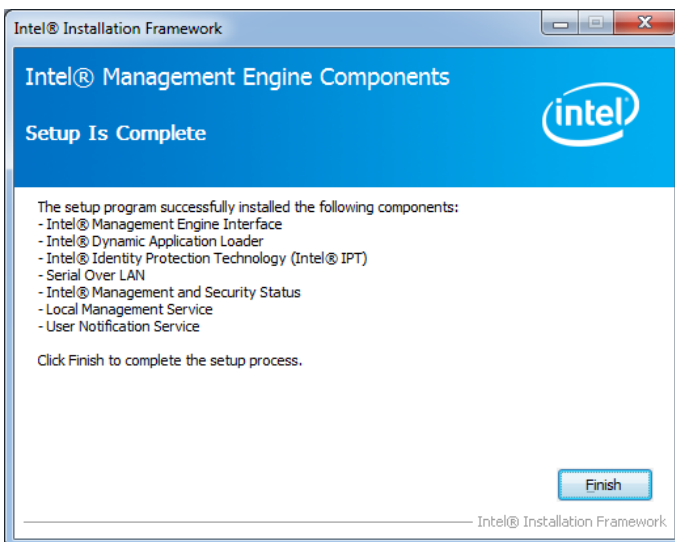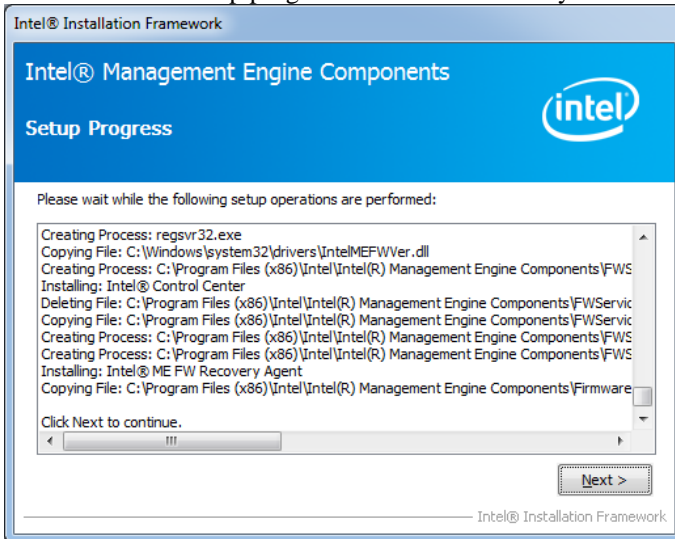
Intel® USB 3.0 Drivers

1. Insert the CD that comes with the board. Click *Intel* and then *Intel(R) Q7 Series Chipset Drivers*.

2. Click *Intel(R) USB 3.0 Drivers.*
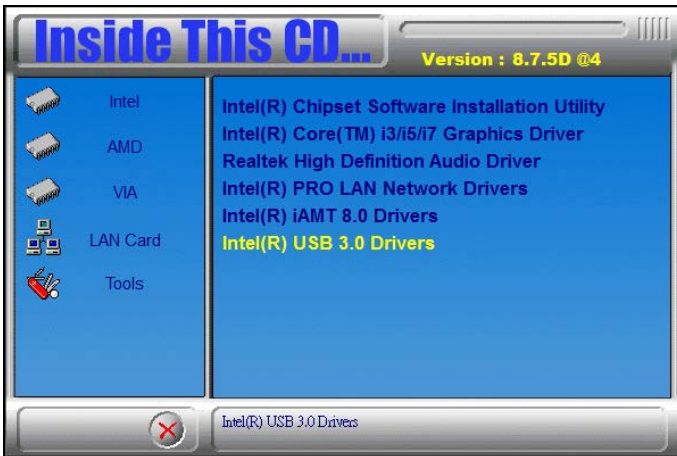
3. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click *Next*.
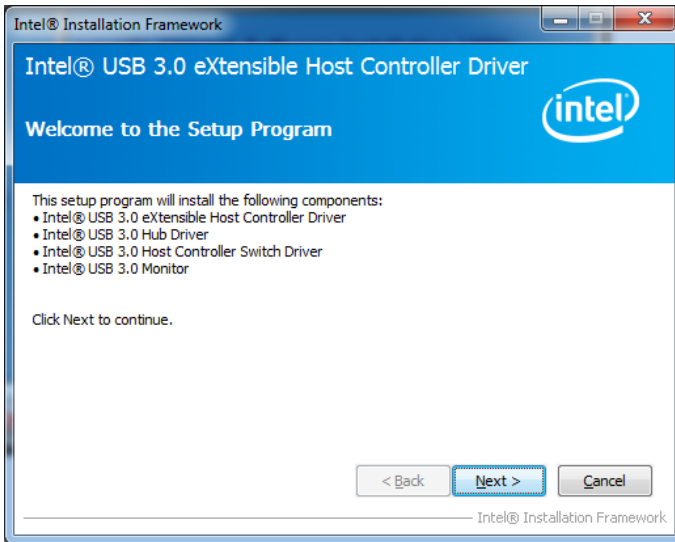
4. Click *Yes* to to agree with the license agreement and continue the installation.

5. On the Readme File Information screen, click *Next* to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

6. Setup complete. Click *Finish* to restart the computer and for changes to take effect.

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Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
2F8h - 2FFh	Serial Port #2(COM2)
2B0h- 2DFh	Graphics adapter Controller
360h - 36Fh	Network Ports
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ8	Real Time Clock
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//-------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//-------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//-------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81866 watch dog program\n");

        SIO = Init_F81866();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81866, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime); }
        else
        {       DisableWDT();       }

        return 0;
```

```
}
//-------------------------------------------------------------------------
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_F81866_Reg(0x2B);
        bBuf &= (~0x20);
        Set_F81866_Reg(0x2B, bBuf);                         //Enable WDTO

        Set_F81866_LD(0x07);                                //switch to logic device 7
        Set_F81866_Reg(0x30, 0x01);                         //enable timer

        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= (~0x0F);
        bBuf |= 0x52;
        Set_F81866_Reg(0xF5, bBuf);                         //count mode is second

        Set_F81866_Reg(0xF6, interval);          //set timer

        bBuf = Get_F81866_Reg(0xFA);
        bBuf |= 0x01;
        Set_F81866_Reg(0xFA, bBuf);                         //enable WDTO output

        bBuf = Get_F81866_Reg(0xF5);
        bBuf |= 0x20;
        Set_F81866_Reg(0xF5, bBuf);                         //start counting
}
//-------------------------------------------------------------------------
void DisableWDT(void)
{
        unsigned char bBuf;

        Set_F81866_LD(0x07);                                //switch to logic device 7

        bBuf = Get_F81866_Reg(0xFA);
        bBuf &= ~0x01;
        Set_F81866_Reg(0xFA, bBuf);                         //disable WDTO output

        bBuf = Get_F81866_Reg(0xF5);
        bBuf &= ~0x20;
        bBuf |= 0x40;
        Set_F81866_Reg(0xF5, bBuf);                         //disable WDT
}
//-------------------------------------------------------------------------
```

```
//-------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-------------------------------------------------------------------------
#include "F81866.H"
#include <dos.h>
//-------------------------------------------------------------------------
unsigned int F81866_BASE;
void Unlock_F81866 (void);
void Lock_F81866 (void);
//-------------------------------------------------------------------------
unsigned int Init_F81866(void)
{
        unsigned int result;
        unsigned char ucDid;

        F81866_BASE = 0x4E;
        result = F81866_BASE;

        ucDid = Get_F81866_Reg(0x20);
        if (ucDid == 0x07)                              //Fintek 81866
        {       goto Init_Finish;       }

        F81866_BASE = 0x2E;
        result = F81866_BASE;

        ucDid = Get_F81866_Reg(0x20);
        if (ucDid == 0x07)                              //Fintek 81866
        {       goto Init_Finish;       }

        F81866_BASE = 0x00;
        result = F81866_BASE;

Init_Finish:
        return (result);
}
//-------------------------------------------------------------------------
void Unlock_F81866 (void)
{
        outportb(F81866_INDEX_PORT, F81866_UNLOCK);
        outportb(F81866_INDEX_PORT, F81866_UNLOCK);
}
//-------------------------------------------------------------------------
void Lock_F81866 (void)
{
        outportb(F81866_INDEX_PORT, F81866_LOCK);
}
//-------------------------------------------------------------------------
void Set_F81866_LD( unsigned char LD)
{
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, F81866_REG_LD);
        outportb(F81866_DATA_PORT, LD);
        Lock_F81866();
}
//-------------------------------------------------------------------------
void Set_F81866_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, REG);
        outportb(F81866_DATA_PORT, DATA);
        Lock_F81866();
}
//-------------------------------------------------------------------------
```

```
unsigned char Get_F81866_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, REG);
        Result = inportb(F81866_DATA_PORT);
        Lock_F81866();
        return Result;
}
//---------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#ifndef __F81866_H
#define __F81866_H                      1
//---------------------------------------------------------------------------
#define      F81866_INDEX_PORT          (F81866_BASE)
#define      F81866_DATA_PORT           (F81866_BASE+1)
//---------------------------------------------------------------------------
#define      F81866_REG_LD              0x07
//---------------------------------------------------------------------------
#define F81866_UNLOCK            0x87
#define      F81866_LOCK                0xAA
//---------------------------------------------------------------------------
unsigned int Init_F81866(void);
void Set_F81866_LD( unsigned char);
void Set_F81866_Reg( unsigned char, unsigned char);
unsigned char Get_F81866_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif //__F81866_H
```