MI970VF/MI970F

Intel® QM77 / HM76
Mini-ITX Motherboard

USER'S MANUAL

Version 1.2

Acknowledgments

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Introduction

Product Description

The MI970VF Mini ITX motherboard is based on the latest Intel® QM77 chipset. The platform supports 3rd generation Intel® Core processor family with rPGA988B packing and feature an integrated dual-channel DDR3 memory controller as well as a graphics core.

The latest Intel® processors provide advanced performance in both computing and graphics quality. This meets the requirement of customers in the gaming, POS, digital signage and server market segment.

The QM77 platform is made with 22-nanometer technology that supports Intel's first processor architecture to unite the CPU and the graphics core on the transistor level. The MI970VF Mini ITX board utilizes the dramatic increase in performance provided this Intel's latest cutting-edge technology. Measuring 170mm x 170mm, the MI970F offers fast 6Gbps SATA support (2 ports), USB3.0 (4 ports) and interfaces for DVI-D, DVI-I, LVDS and DisplayPort displays. MI970VF features Intel Active Management Technology 8.0.

MI970F FEATURES:

- Supports Intel® 3rd Generation Core i7/i5/i3 QC/DC mobile processors
- Two DDR3 SoDIMM, 1066/1333/1600MHz, Max. 16GB memory
- Dual Intel® PCI-Express Gigabit LAN
- Integrated Graphics for DVI-I, DVI-D/DisplayPort/LVDS displays
- 4x SATA 2.0, 2x SATA 3.0, 8x USB 2.0, USB 3.0 (4 ports), 4x COM, Watchdog timer
- 1x PCI-E (x16), 2x Mini PCI-E
- Optional AMT (MI970VF only)

Checklist

Your MI970 package should include the items listed below.

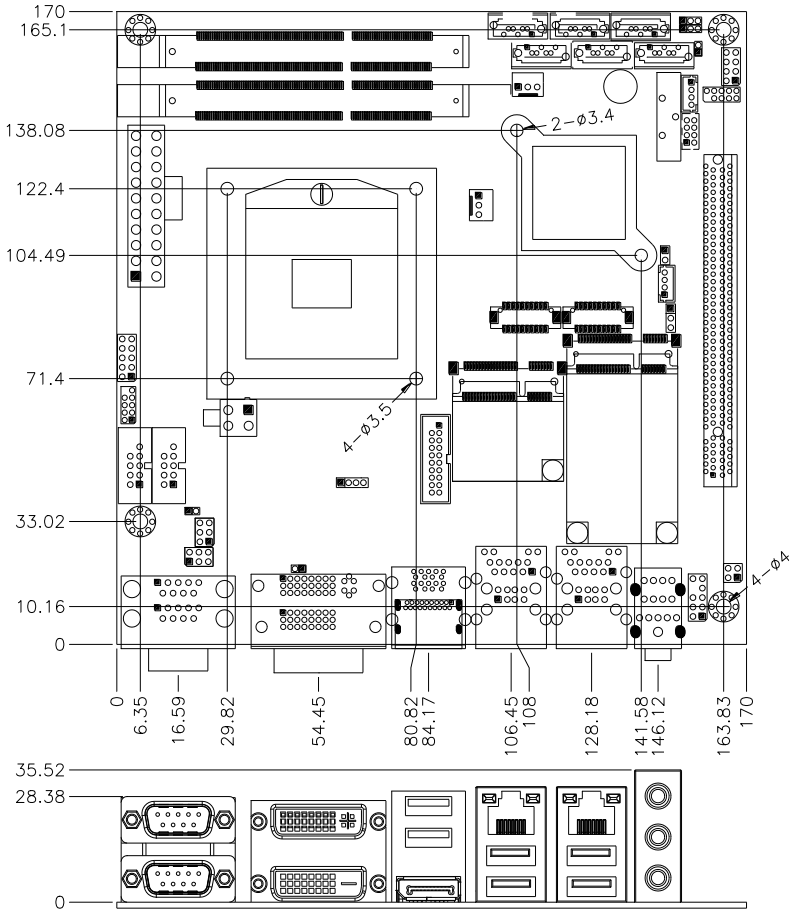
- The MI970 Mini-ITX motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Serial ATA cable

MI970 Specifications

Product Name	**MI970F [Supports ErP]** **MI970VF [Supports iAMT 8.0, TPM & vPro]**
Form Factor	Mini-ITX
CPU Type	- Intel® 3rd Generation Core ™i7/i5/i3 mobile processors - rPGA package, 37.5 mm x 37.5mm - TDP: QC = 45W/ DC = 35W **Ivy Bridge CPU socket is **compatible** with Sandy Bridge CPU**
CPU Speed	Up to 2.7GHz
Cache	Up to 8MB
CPU Socket	rPGA 988B (Socket G2)
Chipset	Intel® QM77Platform Controller Hub (MI970VF) Intel® HM76Platform Controller Hub (MI970F) 25 x 27 mm package size
BIOS	AMI BIOS [16MB SPI ROM]
Memory	Intel® Ivy-Bridge mobile processors integrated memory controller DDRIII 1066/1333/1600 MHz - SO-DIMM [204-pin vertical type]x 2 (Non-ECC), Max. 16GB
VGA	- Intel® Ivy-Bridge mobile processor integrated Gfx, supports 3 independent displays, Direct X 11, OpenGL 3.1, Open CL 1.1 ● DVI-I X 1 (thru Level shifter ASM1442) ● DVI-D X 1 (thru DP to DVI converter **ANX9830C**) ● DisplayPort x 1 ● LVDS : DF13 x 2 for dual channel 24-bit support
LAN	1. Intel® Lewisville 82579LM GbE PHY [MI970VF only] or Intel® Lewisville 82579V GbE PHY [MI970F only] 2. Intel® 82583V as 2nd GbE
USB	USB 2.0 host controller [Panther Point integrated], supports **8** ports - 4 ports in the rear panel - 2 ports via onboard pin header (2.0mm pitch) - 2 ports via MiniPCIe sockets USB 3.0 host controller [Panther Point integrated], support 4 ports - 2 ports in the rear panel - 2 ports via onboard box-header type [Blue color]
Serial ATA	Intel® QM77 PCH built-in SATA controller, supports total 6 ports 2 x SATA (3.0) 6Gbps+ **4** x SATA (2.0) 3Gbps ports
Audio	Intel® QM77 PCH built-in High Definition Audio controller + Realtek ALC892 w/ 7.1 channels
LPC I/O	Fintek **F81866AD-I** (128-pin LQFP [14mm x 14 mm]) COM1 (RS232/422/485) [EXAR SP339EER1 232/422/485 transceiver x 1 for jumper-less] COM2/COM3/COM4 (RS232), Hardware Monitor (2 thermal inputs,4 voltage monitor inputs & 2 Fan headers) [CPU FAN & SYS FAN(DC Fan type, 3-pin connector)] COM1/2 with pin-9 with power for 2 ports (500 mA for each port)
Digital IO	4 in & 4 out
TPM 1.2	Nuvoton WPCT210AA0WX (MI970VF only) **Operation temperature for 0 ~ +60 degree C only**
iAMT	Intel® QM77 PCH built-in (MI970VF only) - Intel® Active Management Technology ver. 8.0
Expansion Slots	- PCI-Express (16x) x1 [Gen 3.0 PEG] - Mini PCI-Express x**1** port [Full-sized] w/mSATA +USB 2.0 support - Mini PCI-Express x**1** port [Half-sized] w/ USB 2.0 support

Edge Connector	Dual DB9 stack connector for COM #1 / #2 DVI-D + DVI-I stack connector x 1 USB(3.0) dual stack + DP connector x1 RJ-45 + dual USB(2.0) stack connector x2 Triplet type Jack 3 x 1 for HD Audio
Onboard Header/Connector	2 ports x SATA **III** [Blue color] , **4** ports x SATA II , mSATA (w/JEDEC MO-300) **[Share with SATA #5]** DF-11 8 pins connector x 1 for 2 ports USB 2.0 DF-13 20 pins connector x 2 for dual –channel LVDS 2x10 pins box-header x 1 for **2** ports USB 3.0 [Blue color] 2x5 pins pin-header x 1 for front panel audio [Support 7.1 Channel] 2x5 pins pin-header x 2 for COM3 & COM4 2x5 pins pin-header x 1 for Digital IO 4 pins box header x 1 for LCD backlight control
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
System Voltage	**ATX standard 20-pin type** **4 pin type (+12V only)[For full system loading usage]**
Others	- vPro [MI970VF only] - ErP feature for MI970F(F81866AD-I integrated ,WOL from 2nd GbE - **iSMART function (TI MSP430G2433)** - **AT24C02C EEPROM [SO8 type] via SMbus (Optional)**
Board Size	170mm x 170mm

Board Dimensions



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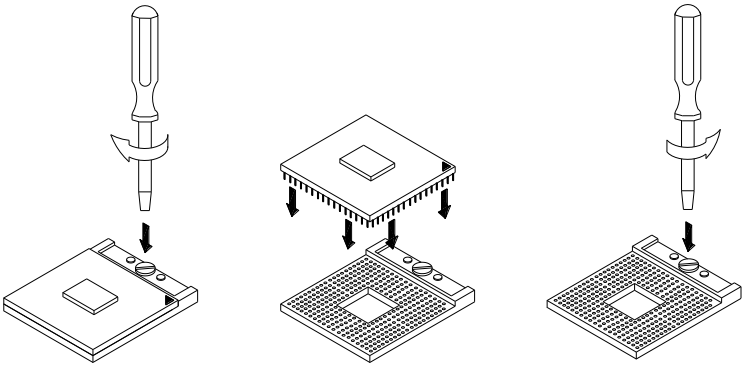
Installations

This section provides information on how to use the jumpers and connectors on the MI970 in order to set up a workable system. The topics covered are:

Installing the CPU

The MI970 board supports rPGA988B socket for Intel® Ivy Bridge Dual Core mobile processors.
The processor socket comes with a screw to secure the processor. As shown in the left picture below, loosen the screw first before inserting the processor. Place the processor into the socket by making sure the notch on the corner of the CPU corresponds with the notch on the inside of the socket. Once the processor has slide into the socket, fasten the screw. Refer to the figures below.



***NOTE**: Ensure that the CPU heat sink and the CPU top surface are in total contact to avoid CPU overheating problem that would cause your system to hang or be unstable.*

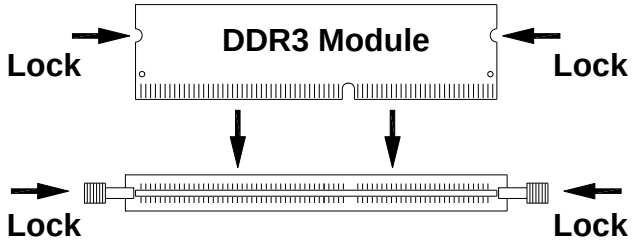
Installing the Memory

The MI970 board supports two DDR3 memory socket for a maximum total memory of 16GB in DDR3 SO-DIMM memory type.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

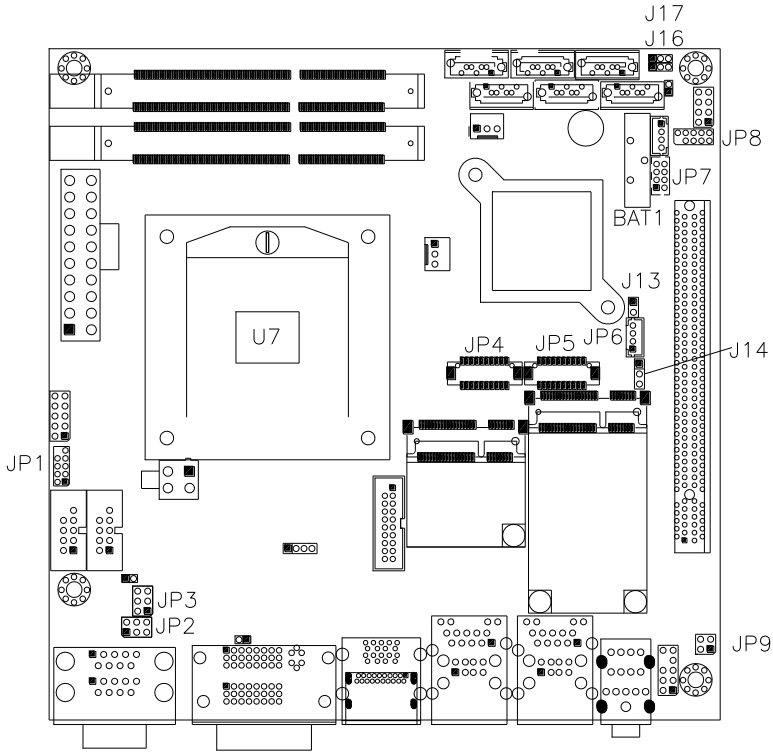
1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.
2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.
3. To remove the DDR3 module, press the clips with both hands.



Setting the Jumpers

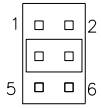
Jumpers are used on MI970 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on MI970 and their respective functions.

Jumper Locations on MI970

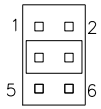


JP1: LPC debug Connector (Factory use only)

JP2: COM1 RS232 RI/+5V/+12V Power Setting

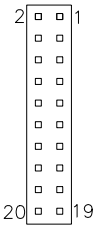
JP2	Setting	Function
	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 5-6 Short/Closed	+5V

JP3: COM2 RS232 RI/+5V/+12V Power Setting

JP3	Setting	Function
	Pin 1-2 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 5-6 Short/Closed	+5V

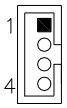
JP4, JP5: LVDS Connectors (1st channel, 2nd channel)

The LVDS connectors on board consist of the first channel (LVDS1) and second channel (LVDS2).



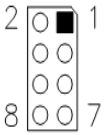
Signal Name	Pin #	Pin #	Signal Name
TX0-	2	1	TX0+
Ground	4	3	Ground
TX1-	6	5	TX1+
5V/3.3V	8	7	Ground
TX3-	10	9	TX3+
TX2-	12	11	TX2+
Ground	14	13	Ground
TXC-	16	15	TXC+
5V/3.3V	18	17	ENABKL
+12V	20	19	+12V

JP6: LCD Backlight Connector



Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Brightness Control
4	Ground

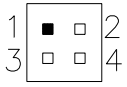
JP7: USB4/USB5 Connector



Signal Name	Pin #	Pin #	Signal Name
Vcc	1	2	Ground
D0-	3	4	D1+
D0+	5	6	D1-
Ground	7	8	Vcc

JP8: SPI Flash connector (Factory use only)

JP9: SPDIF I/O



Pin #	Signal Name
1	SPDIF IN
2	Ground
3	SPDIF OUT
4	Ground

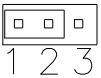
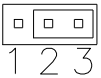
J13: Flash Descriptor Security Override (Factory use only)

J13	Flash Descriptor Security Override
Open	Disabled (Default)
Close	Enabled

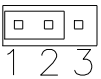
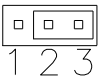
J14: LCD Panel Power Selection

J14	LCD Panel Power
	3.3V
	5V

J16: Clear ME Contents

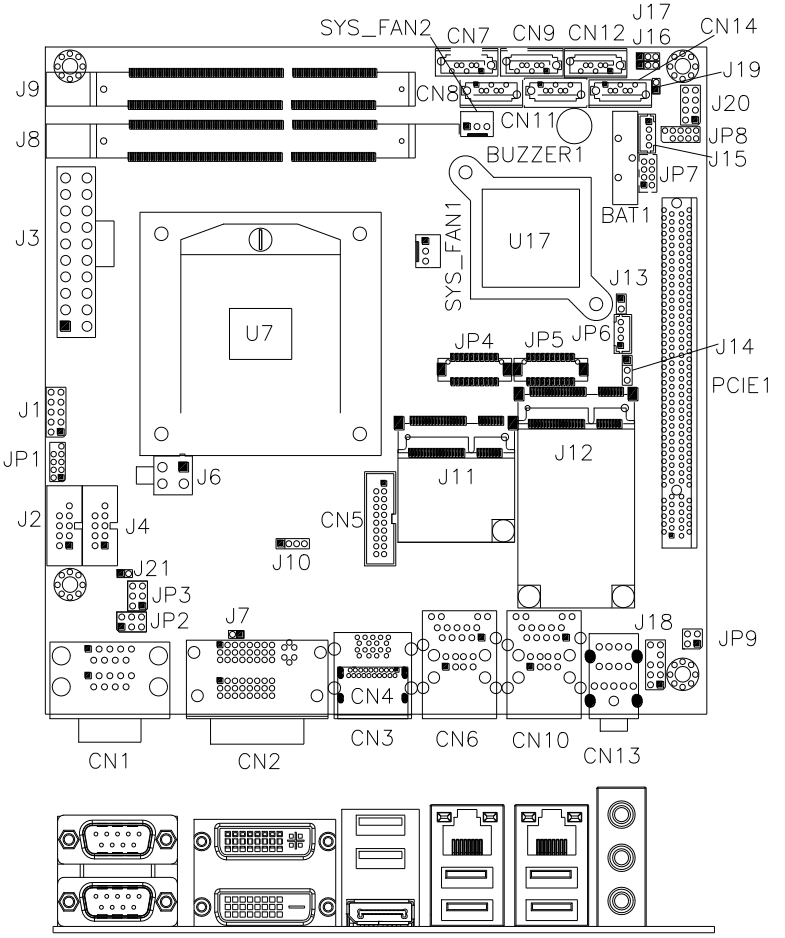
J16	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear

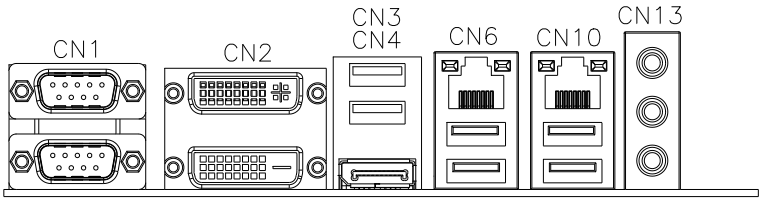
J17: Clear CMOS Contents

J17	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear CMOS

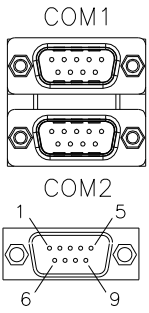
Connectors on MI970

Connector Locations on MI970



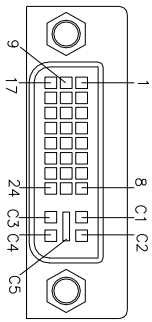


CN1: COM1 and COM2 Serial Ports

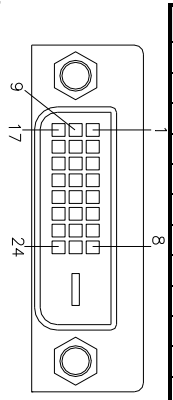


Pin #	Signal Name		
	RS-232	R2-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC
10	NC	NC	NC

CN2: DVI-D and DVI-I Connector

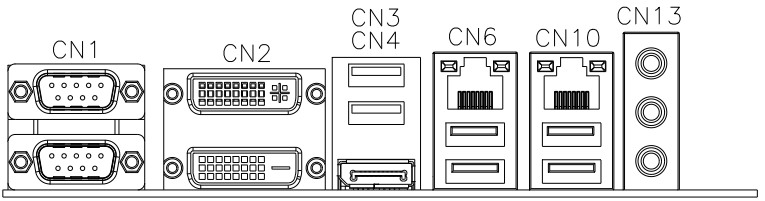


Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	HOT POWER
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
N.C	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	Analog Red
SHIELD 1/3	11	C2	Analog Green
DATA 3-	12	C3	Analog Blue
DATA 3+	13	C4	Analog HYNC
DDC POWER	14	C5	A GROUND2
A GROUND 1	15	C6	A GROUND3



DVI-I

Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	HOT POWER
DATA 2+	2	17	DATA 0-
Shield 2/4	3	18	DATA 0+
DATA 4-	4	19	SHIELD 0/5
DATA 4+	5	20	DATA 5-
DDC CLOCK	6	21	DATA 5+
DDC DATA	7	22	SHIELD CLK
N.C	8	23	CLOCK -
DATA 1-	9	24	CLOCK +
DATA 1+	10	C1	N.C.
SHIELD 1/3	11	C2	N.C.
DATA 3-	12	C3	N.C.
DATA 3+	13	C4	N.C.
DDC POWER	14	C5	N.C.
A GROUND 1	15	C6	N.C.



CN3: USB3

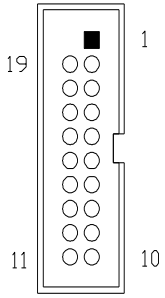
CN4: DisplayPort

CN6: Gigabit LAN (82579LM/V) +USB2 12/13

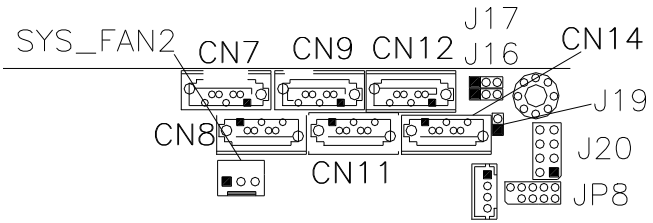
CN10: Gigabit LAN (82583V) + USB2 8/9

CN13: HDA Audio connector

CN5: USB3 Connector



Signal Name	Pin #	Pin #	Signal Name
Vcc	1	X	
P1_SSRX-	2	19	Vcc
P1_SSRX+	3	18	P2_SSRX-
GND	4	17	P2_SSRX+
P1_SSTX-	5	16	GND
P1_SSTX+	6	15	P2_SSTX-
GND	7	14	P2_SSTX+
P1_U2_D-	8	13	GND
P1_U2_D+	9	12	P2_U2_D-
NC	10	11	P2_U2_D+



CN7: SATA3 Connector Port2

CN8: SATA3 Connector Port1

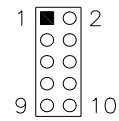
CN9: SATA2 Connector Port4

CN11: SATA2 Connector Port3

CN12: SATA2 Connector Port6 (Share with mSATA)

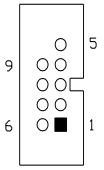
CN14: SATA2 Connector Port5

J1: Digital I/O Connector (4 in, 4 out)



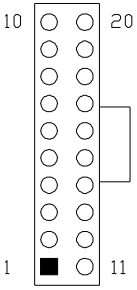
Signal Name	Pin #	Pin #	Signal Name
Ground	1	2	+5V
Out3	3	4	Out1
Out2	5	6	Out0
IN3	7	8	IN1
IN2	9	10	IN0

J4, J2: COM3, COM4 RS232 Serial Ports



Signal Name	Pin #	Pin #	Signal Name
DCD#	1	6	DSR#
SIN#	2	7	RTS#
SOUT	3	8	CTS#
DTR#	4	9	RI#
GND	5	X	KEY

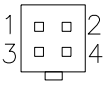
J3: ATX Power Supply Connector



Signal Name	Pin #	Pin #	Signal Name
3.3V	11	1	3.3V
-12V	12	2	3.3V
Ground	13	3	Ground
PS-ON	14	4	+5V
Ground	15	5	Ground
Ground	16	6	+5V
Ground	17	7	Ground
-5V	18	8	Power good
+5V	19	9	5VSB
+5V	20	10	+12V

J6: ATX 12V Power Connector

This connector supplies the CPU operating voltage.



Pin #	Signal Name
1	Ground
2	Ground
3	+12V
4	+12V

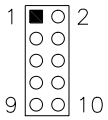
J8: DDR SO-DIMM Channel A

J9: DDR SO-DIMM Channel B

J11: Mini-PCIE Connector

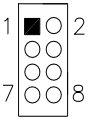
J12: Mini-PCIE Connector and mSATA/share with CN12

J18: Audio Pin Header for Chassis Front Panel



Signal Name	Pin #	Pin #	Signal Name
MIC IN_L	1	2	Ground
MIC IN_R	3	4	DET
LINE_R	5	6	Ground
Sense	7	8	KEY
LINE_L	9	10	Ground

J20: Front Panel

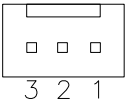


Signal Name	Pin #	Pin #	Signal Name
Power BTN	1	2	Power BTN
HDD LED+	3	4	HDD LED-
Reset BTN	5	6	Reset BTN
Power LED+	7	8	Power LED-

J21: PCIE Configuration (Support from PCB V1.1)

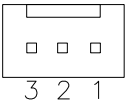
J21	PCIE Configuration
OPEN	PCIE X16 (DEFAULT)
CLOSE	PCIE X8, X8

SYS_FAN1: CPU Fan Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

SYS_FAN2: System Fan Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection

BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

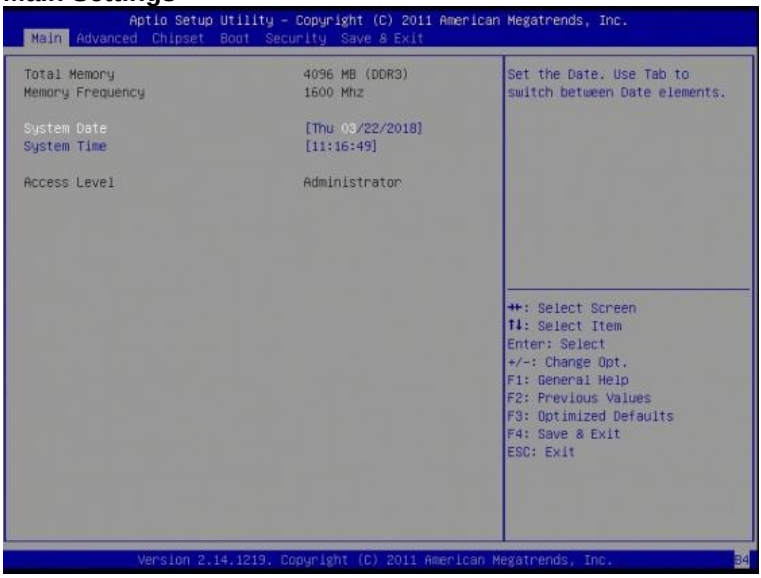
```
Press  <DEL>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

Main Settings

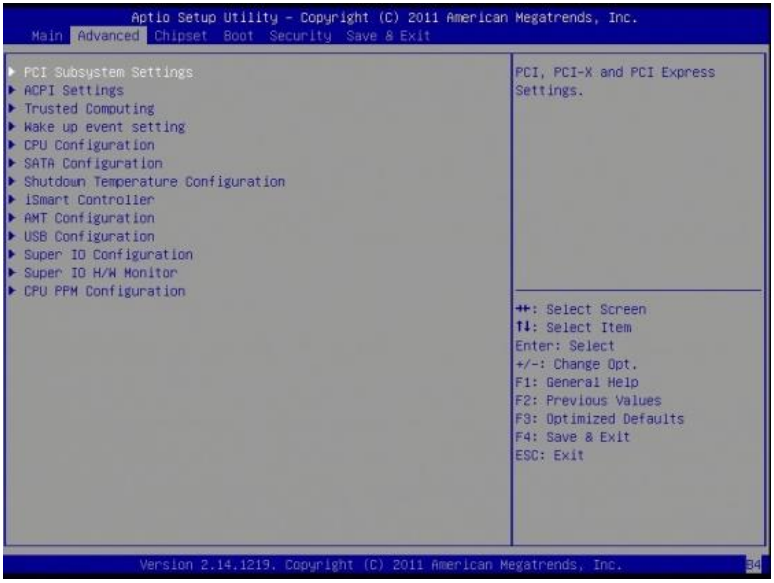


System Date
Set the Date. Use Tab to switch between Data elements.

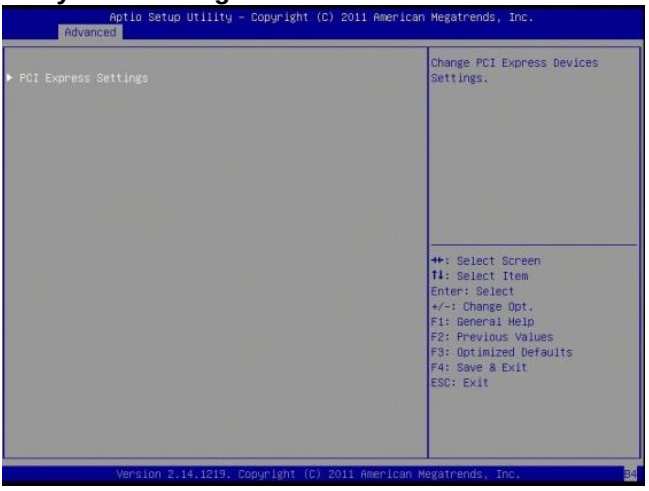
System Time
Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



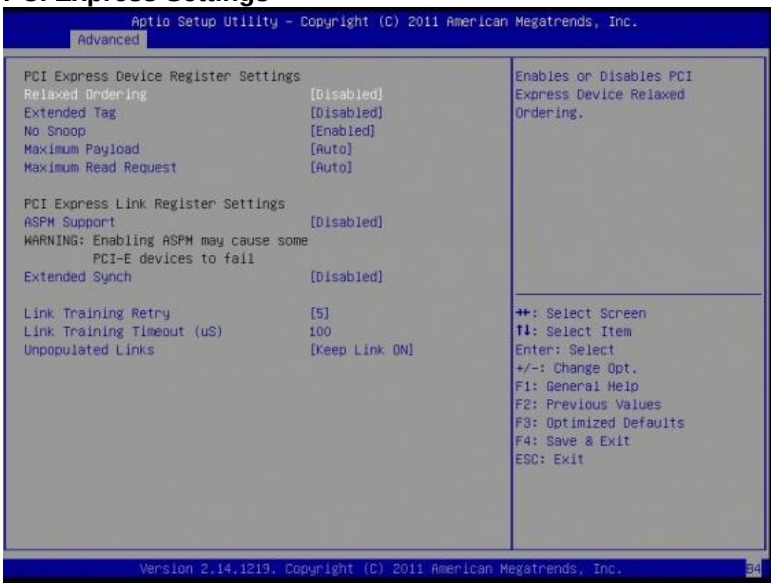
PCI Subsystem Settings



PCI Express Settings

Change PCI Express devices settings.

PCI Express Settings



Relaxed Ordering
Enables or disables PCI Express Device Relaxed Ordering.

Extended Tag
If ENABLED allows device to use 8-bit Tag field as a requester.

No Snoop
Enables or disables PCI Express Device No Snoop option.

Maximum Payload
Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Maximum Read Request
Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support
Set the ASPM Level: Force L0s – Force all links to L0s State:
AUTO – BIOS auto configure ： DISABLE – Disables ASPM.

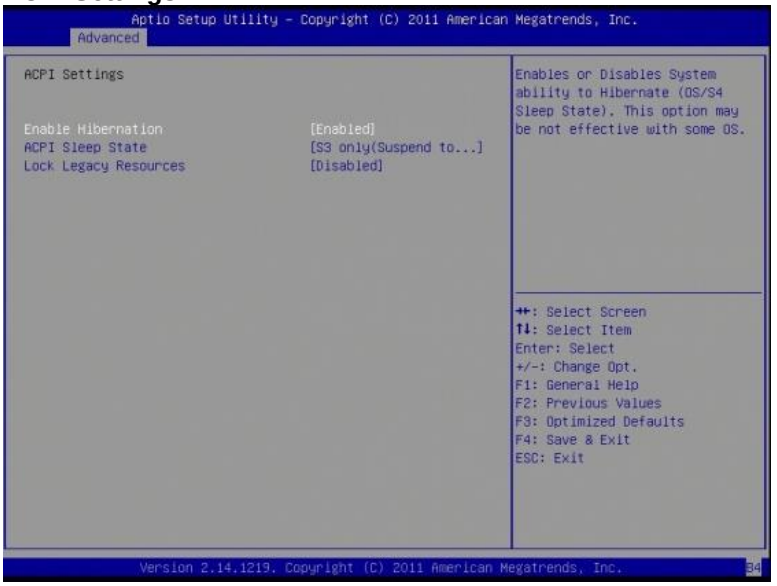
Extended Synch
If ENABLED allows generation of Extended Synchronization patterns.

Link Training Retry
Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Link Training Timeout (uS)
Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

Unpopulated Links
In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

ACPI Settings

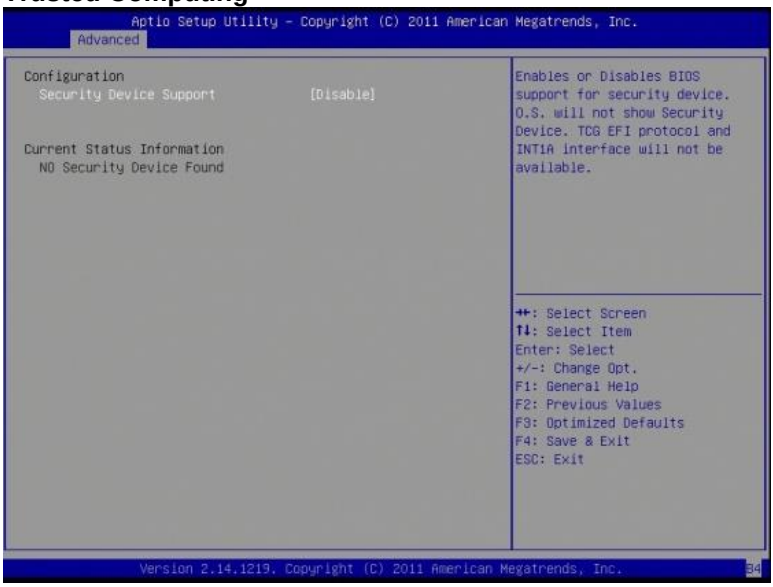


Enable Hibernation
Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State
Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

Lock Legacy Resources
Enabled or Disabled Lock of Legacy Resources.

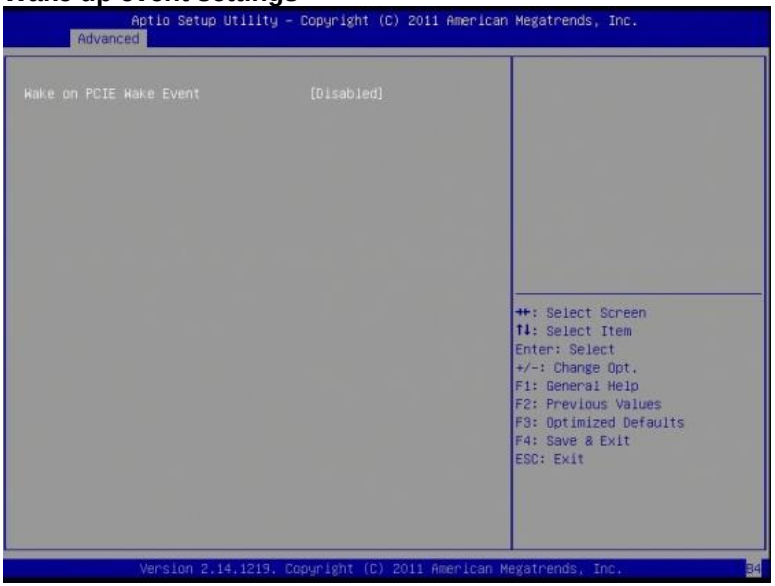
Trusted Computing



Security Device Support

Enables or disables BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

Wake up event settings

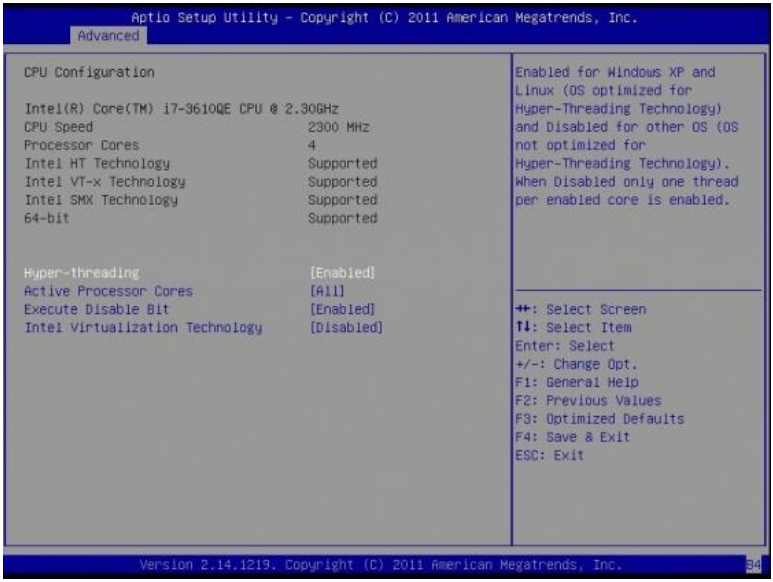


Wake on PCIE PME Wake Event

The options are Disabled and Enabled.

CPU Configuration

This section shows the CPU configuration parameters.



Hyper-threading

Enabled for Windows XP and Linux (OS optimized for Hyper-Threading Technology) and Disabled for other OS (OS not optimized for Hyper-Threading Technology). When Disabled, only one thread per enabled core is enabled.

Active Processor Cores

Number of cores to enable in each processor package.

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS (Windows Server 2003 SP1, Windows XP SP2, SuSE Linux 9.2, RedHat Enterprise 3 Update 3.)

Intel Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

SATA Configuration

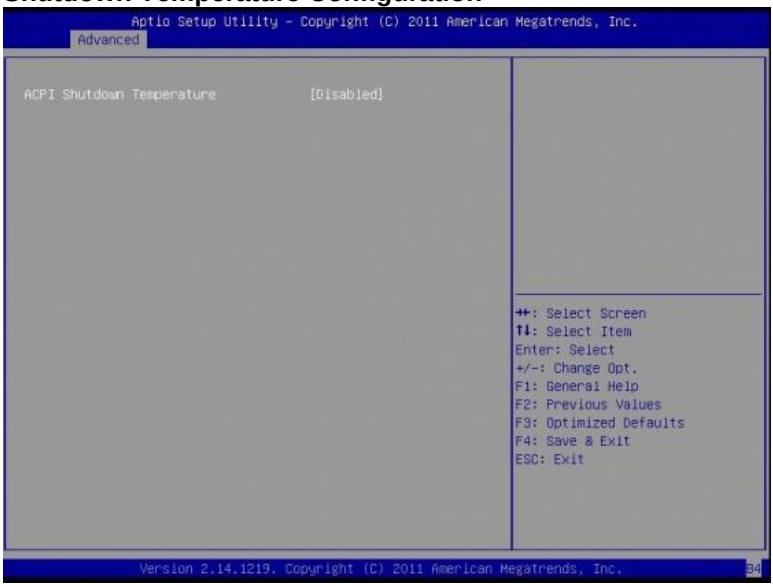
SATA Controller(s)

Enable / Disable Serial ATA Controller.

SATA Mode Selection

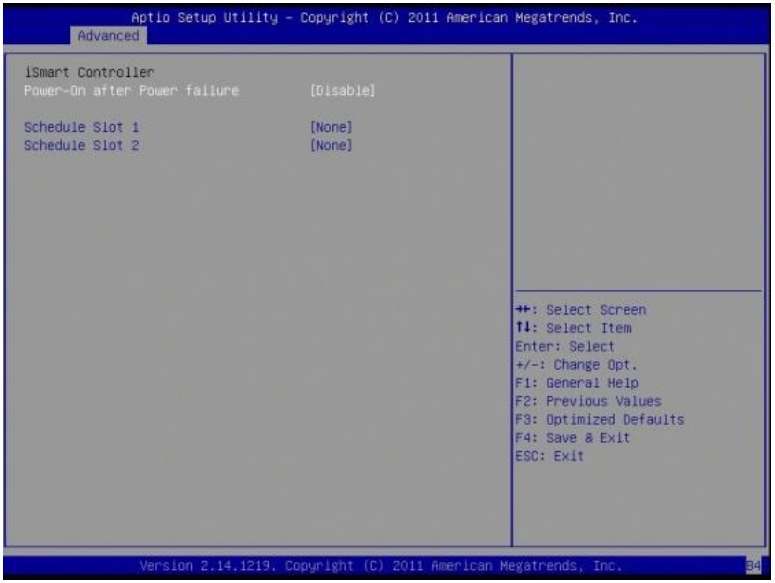
(1) IDE Mode.
(2) AHCI Mode.
(3) RAID Mode.

Shutdown Temperature Configuration



ACPI Shutdown Temperature
The default setting is Disabled.

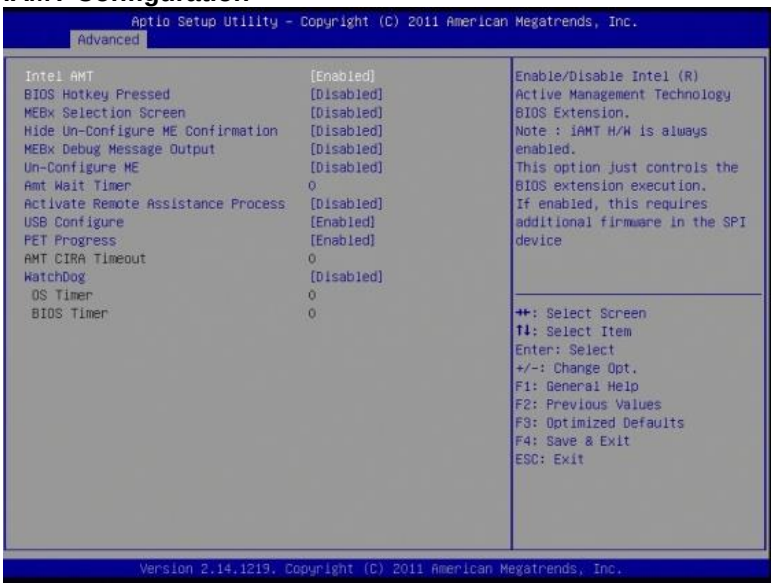
iSmart Controller



ISmart Controller
Setup the power on time for the system.

Schedule Slot 1 / 2
Setup the hour/minute for system power on.

iAMT Configuration



iAMT Configuration

This configuration is supported only with MI970VF (with iAMT function). Options are Enabled and Disabled.
Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

Unconfigure ME

This configuration is supported only with MI970VF (with iAMT function). Perform AMT/ME unconfigure without password operation.

Amt Wait Timer

Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

Activate Remote Assistance Process

Trigger CIRA boot.

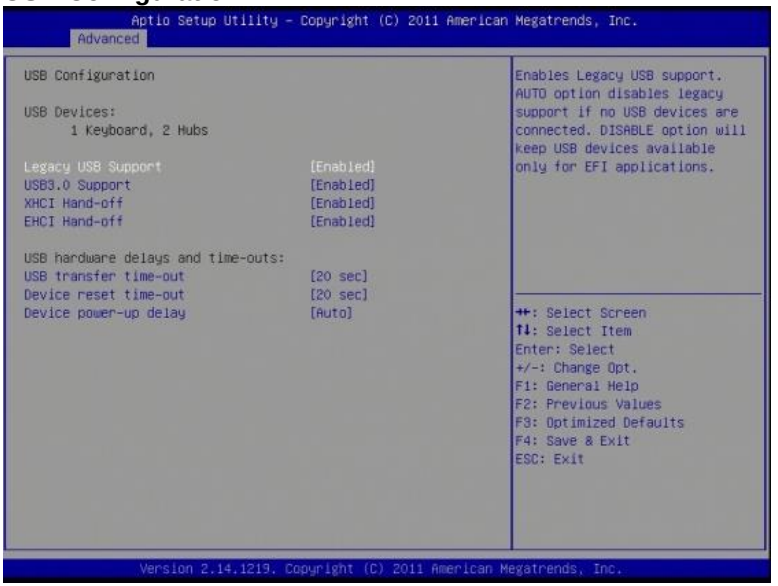
PET Progress

User can Enable/Disable PET Events progress to receive PET events or not.

Watchdog Timer

This configuration is supported only with MI970VF (with iAMT function). Enable/Disable Watchdog Timer.

USB Configuration



Legacy USB Support
Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected.
DISABLE option will keep USB devices available only for EFI applications.

USB3.0 Support
Enable/Disable USB3.0 (XHCI) Controller support.

XHCI Hand-off
This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off
Enabled/Disabled. This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

Port 64/60 Emulation
Enables I/O port 60h/64h emulation support. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.

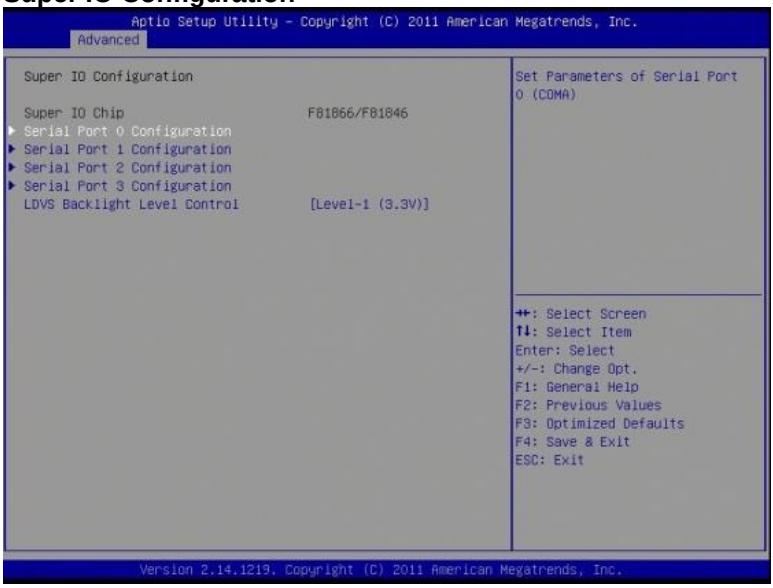
USB Transfer time-out
The time-out value for Control, Bulk, and Interrupt transfers.

Device reset tine-out
USB mass Storage device start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

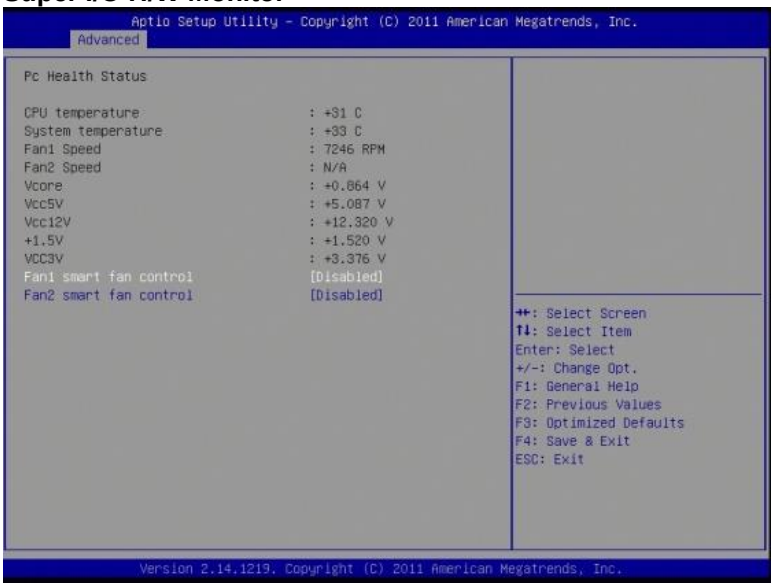
Super IO Configuration



Serial Port Configuration

Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select optimal settings for the Super IO Device.

Super I/O H/W Monitor



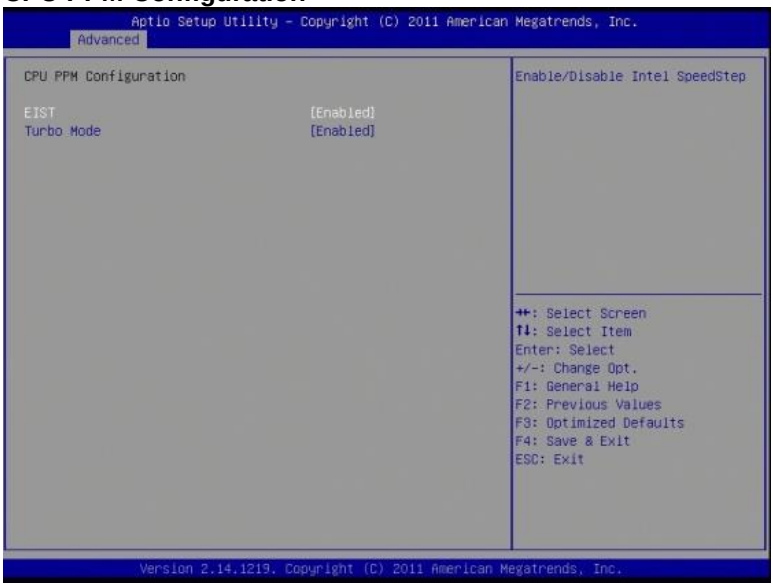
Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

Fan1/Fan2 Smart Fan Control

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

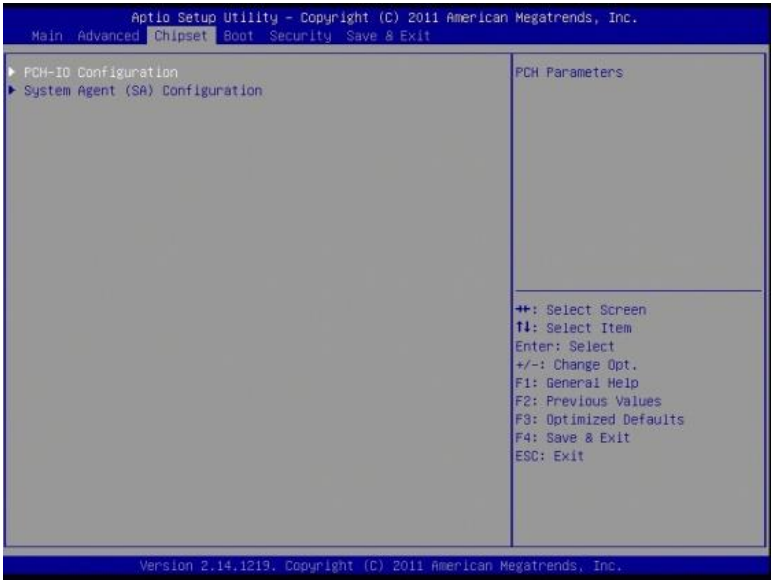
CPU PPM Configuration



EIST

Enable/Disable Intel SpeedStep.

Chipset Settings



PCH-IO Configuration

This section allows you to configure the North Bridge Chipset.

PCH LAN Controller

Enable or disable onboard NIC.

Wake on LAN

Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

SLP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.

PCI Express Configuration

PCI Express Clock Gating

Enable or disable PCI Express Clock Gating for each root port.

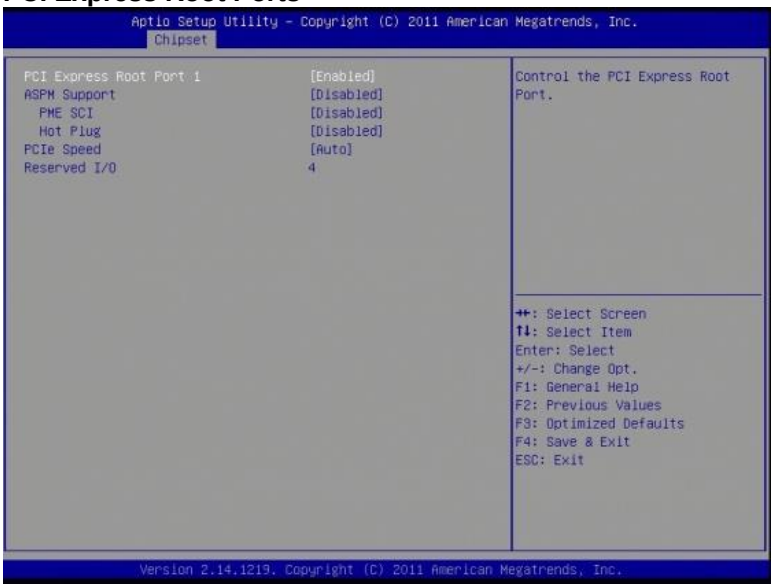
DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI link.

PCIe-USB Glitch W/A

PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG port.

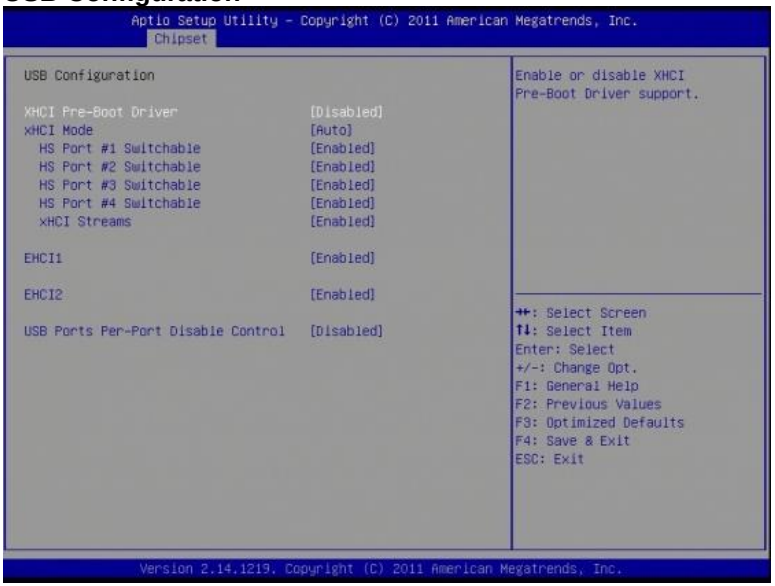
PCI Express Root Ports



PCI Express Root Ports 1~ 8

Controls the PCI Express root ports 1 ~ 8.

USB Configuration



HS Port #1/2/3/4 Switchable

Allows for HS port switching between xHCI and EHCI. If disabled, port is routed to EHCI. If HS port is routed to xHCI, the corresponding SS port is enabled.

xHCI Streams

Enable or disable xHCI Maximum Primary Stream Array Size.

EHCI1/2

Control the USAB EHCI (USB 2.0) functions. One EHCI controller must always be enabled.

USB Ports Per-Port Disable Control

Control each of the USB ports (0~13) disabling.

PCH Azalia Configuration

Azalia

Control Detection of the Azalia device.
Disabled = Azalia will unconditionally disabled.
Enabled Azalia will be unconditionally enabled.
Auto = Azalia will enabled if present, disabled otherwise.

System Agent (SA) Configuration

VT-d

Check to enable VT-d function on MCH.

Graphics Configuration

Primary Display
Select which of IGFX/PEG/PCI graphics device should be primary display or select SG for switchable Gfx.

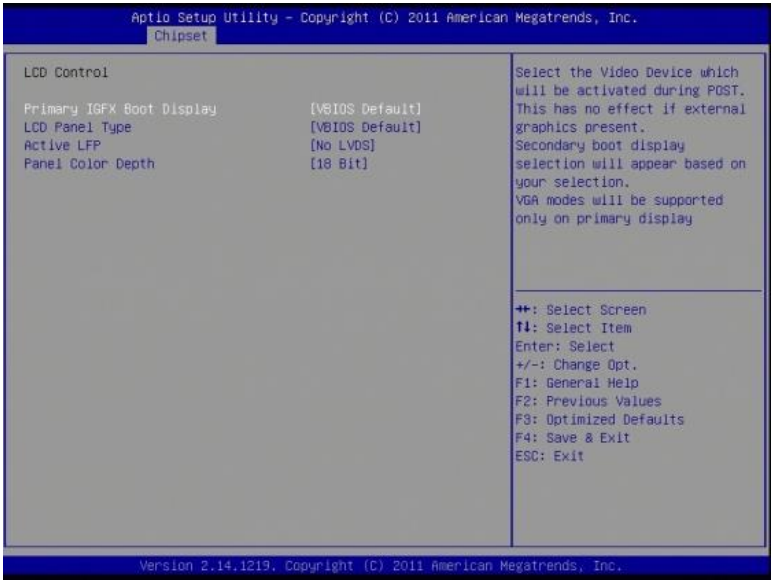
Internal Graphics
Keep IGD enabled based on the setup options.

DVMT Pre-Allocated
Select DVMT 5.0 Pre-Allocated (Fixed) graphics memory size used by the internal graphics device.

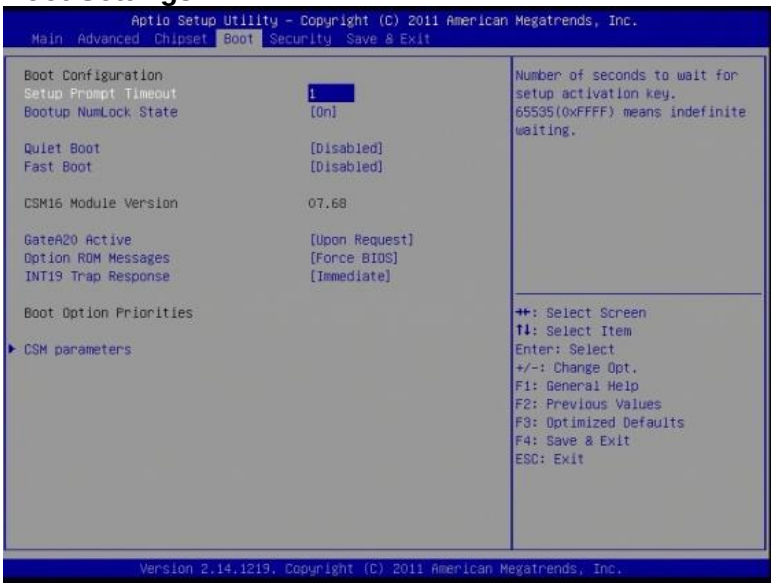
DVMT Total Gfx Memory
Select DVMT 5.0 total graphics memory size used by the internal graphics device.

LCD Control

Select the Video Device that will be activated during POST. This has no effect if external graphics present. Secondary booty display selection will appear based on your selection. VGA modes will be supported only on primary display.



Boot Settings



Setup Prompt Timeout
Number of seconds to wait for setup activation key. 65535(0xFFFF) means indefinite waiting.

Bootup NumLock State
Select the keyboard NumLock state.

Quiet Boot
Enables/Disables Quiet Boot option.

Fast Boot
Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. No effect for BBS boot options.

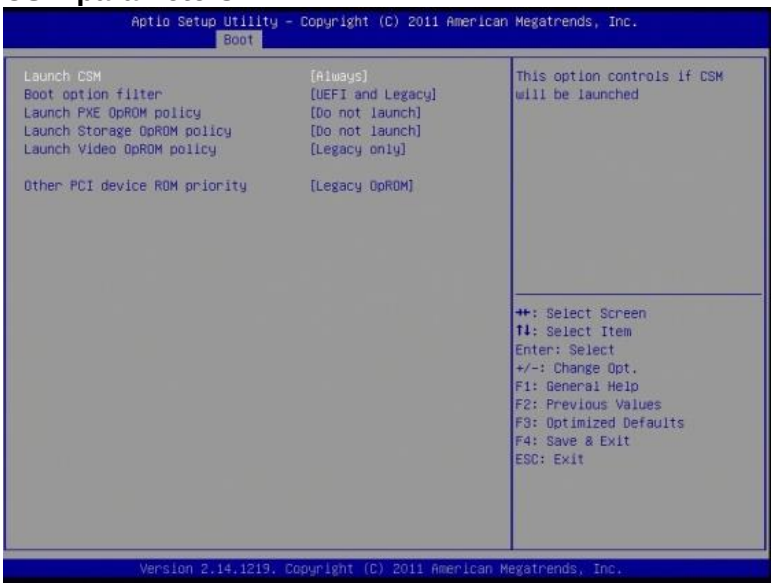
GateA20 Active
UPON REQUEST – GA20 can be disabled using BIOS services.
ALWAYS – do not allow disabling GA20; this option is useful when any RT code is executed above 1MB.

Option ROM Messages
Set display mode for Option ROM. Options are Force BIOS and Keep Current.

INT19 Trap Response
Enable: Allows Option ROMs to trap Int 19.

Boot Option Priorities
Sets the system boot order.

CSM parameters



Boot option filter
This option controls what devices system can boot to.

Launch PXE OpROM policy
Controls the execution of UEFI and Legacy PXE OpROM.

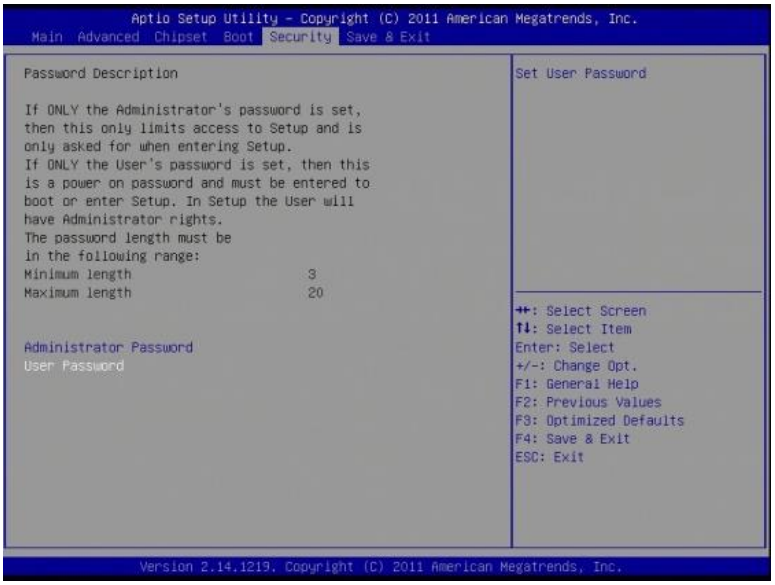
Launch Storatge OpROM policy
Controls the execution of UEFI and Legacy Storage OpROM.

Launch Video OpROM policy
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI device ROM priority
For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings

Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

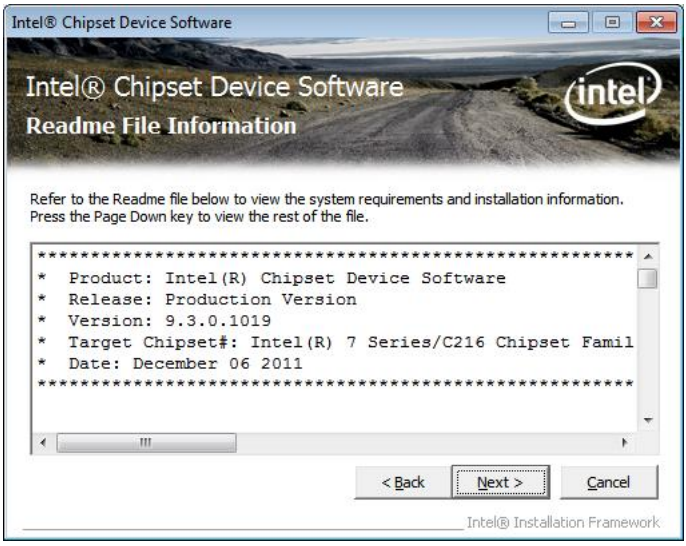
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) 7 Series Chipset Drivers***.

2. Click ***Intel(R) Chipset Software Installation Utility.***

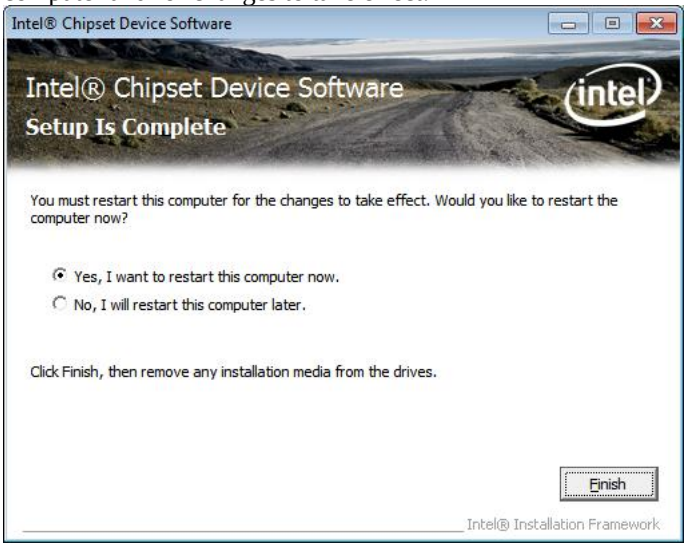
3. When the Welcome screen to the Intel® Chipset Device Software appears, click ***Next*** to continue.

4. Click ***Yes*** to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click ***Next*** to continue the installation.



6. The Setup process is now complete. Click ***Finish*** to restart the computer and for changes to take effect.



VGA Drivers Installation

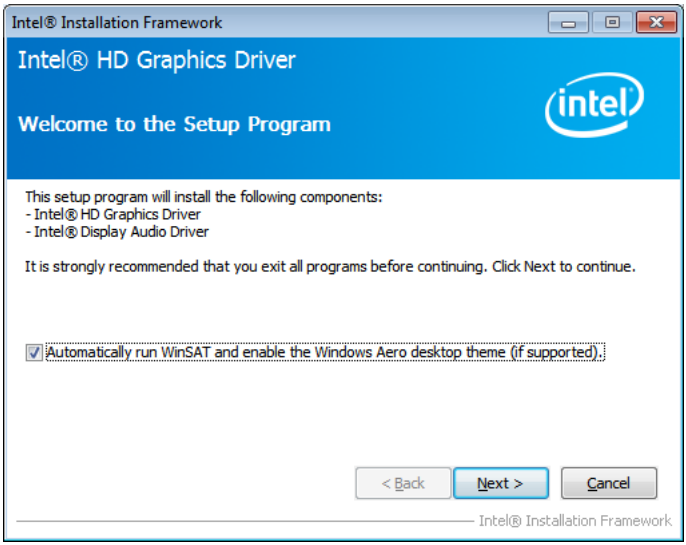
NOTE: Before installing the *Intel(R) Q77 Chipset Family Graphics Driver,* the Microsoft .NET Framework 3.5 SPI should be first installed.

To install the VGA drivers, follow the steps below.

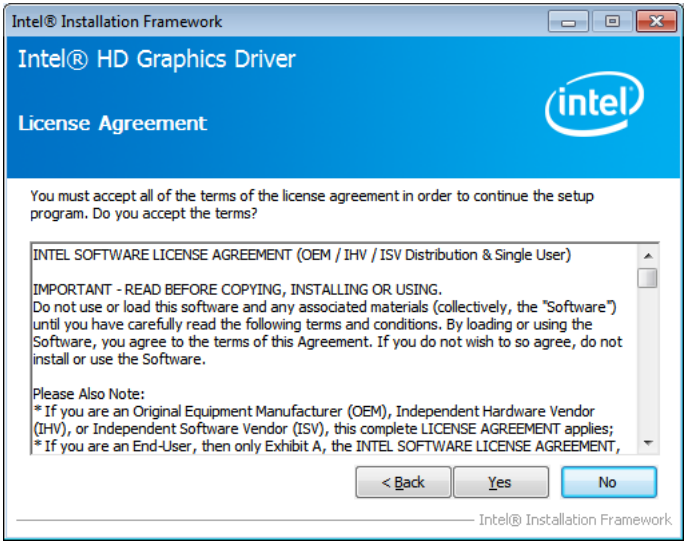
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) Q7 Series Chipset Drivers***.

2. Click ***Intel(R) Q77 Chipset Family Graphics Driver.***

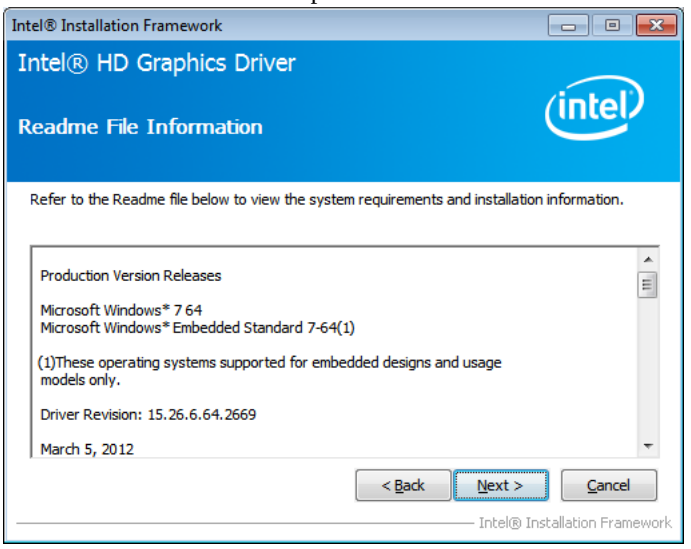
3. When the Welcome screen appears, click ***Next*** to continue.



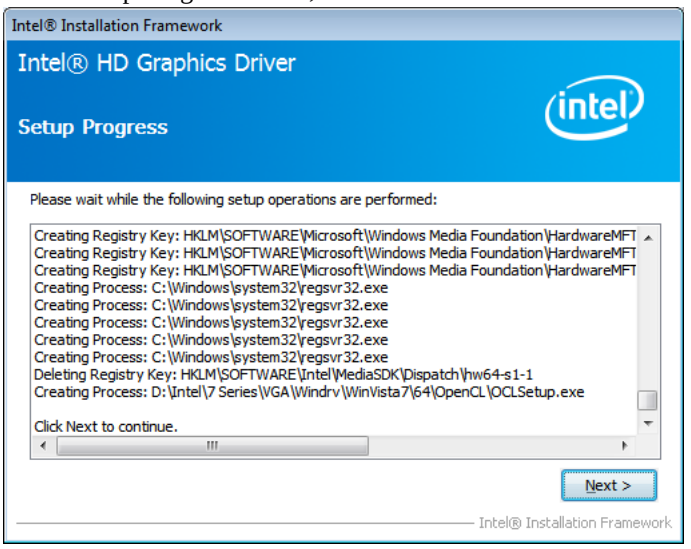
4. Click ***Yes*** to to agree with the license agreement and continue the installation.



5. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® Graphics Media Accelerator Driver.



6. On Setup Progress screen, click ***Next*** to continue.



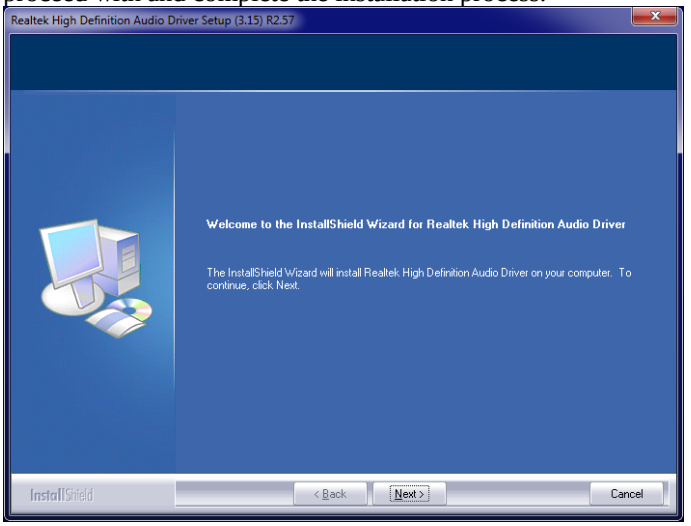
7. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Realtek HD Audio Driver Installation

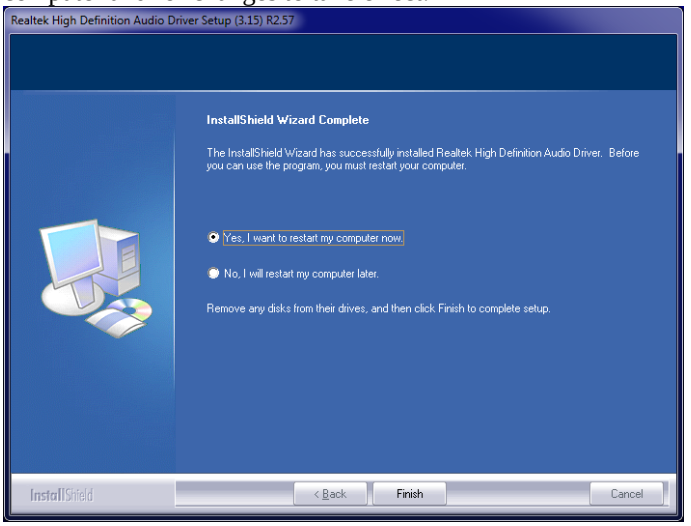
Follow the steps below to install the Realtek HD Audio Drivers.
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) Q7 Series Chipset Drivers***.

2. Click ***Realtek High Definition Audio Driver.***

3. On the Welcome to the InstallShield Wizard screen, click ***Next*** to proceed with and complete the installation process.



4. The InstallShield Wizard Complete. Click ***Finish*** to restart the computer and for changes to take effect.

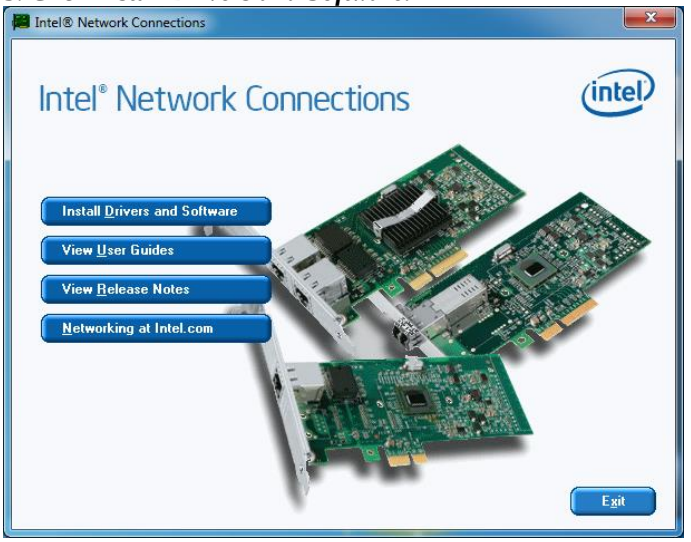


LAN Drivers Installation

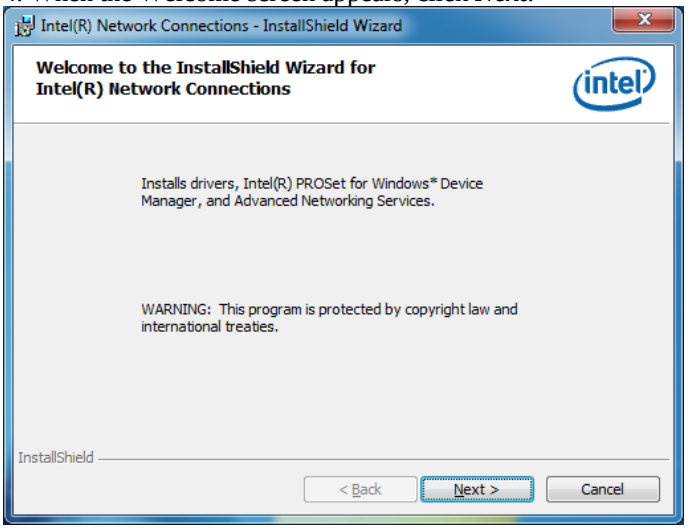
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) Q7 Series Chipset Drivers***.

2. Click ***Intel(R) PRO LAN Network Driver.***

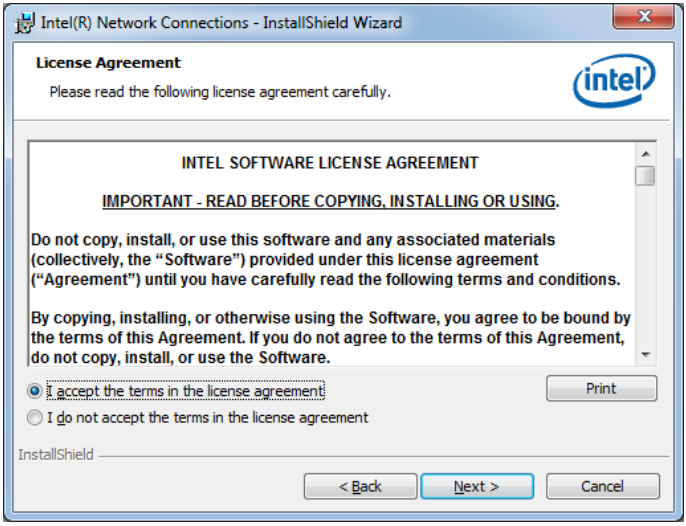
3. Click ***Install Drivers and Software.***



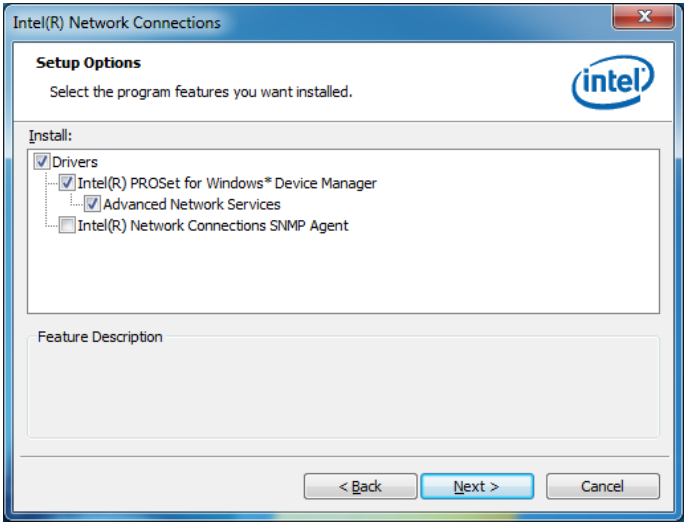
4. When the Welcome screen appears, click ***Next***.



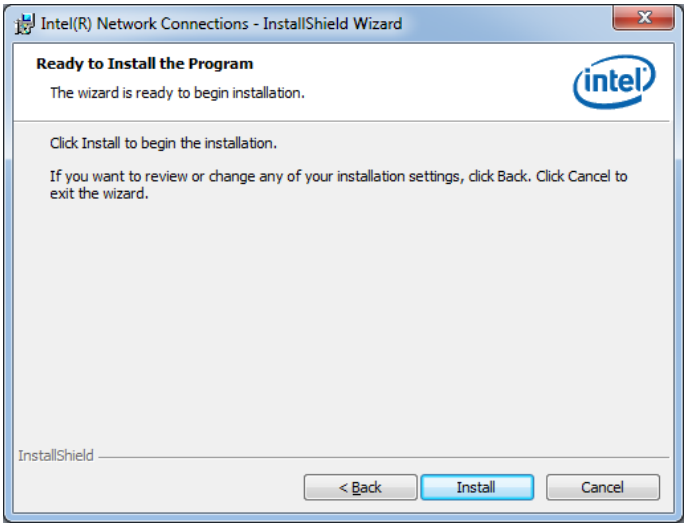
5. Click ***Next*** to to agree with the license agreement.



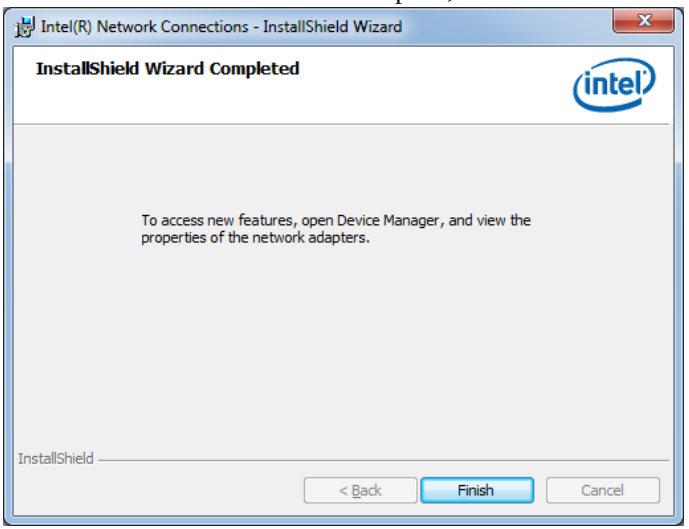
6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.



7. The wizard is ready to begin installation. Click ***Install*** to begin the installation.



8. When InstallShield Wizard is complete, click ***Finish***.



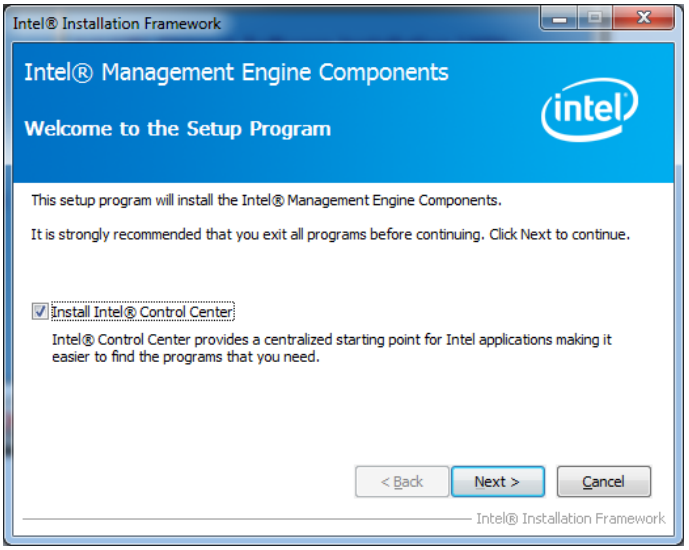
Intel® Management Engine Interface

REMARKS: The Intel iAMT 8.0 Drivers can be installed on MI970VF, not MI970F.

Follow the steps below to install the Intel Management Engine.

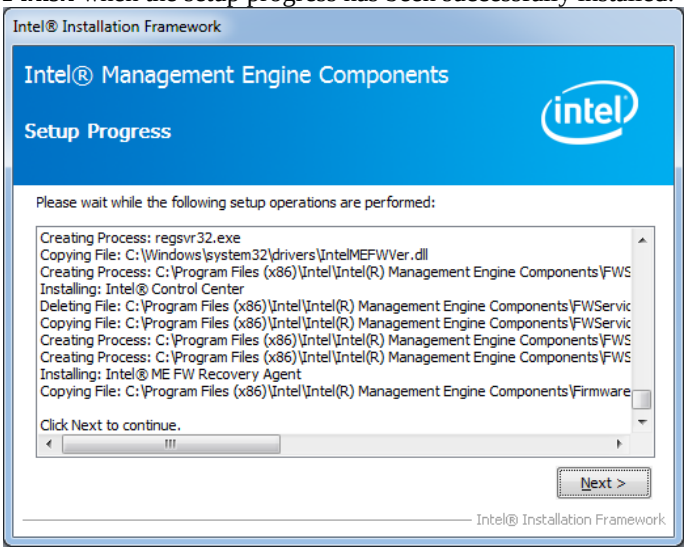
1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) AMT 8.0 Drivers***.

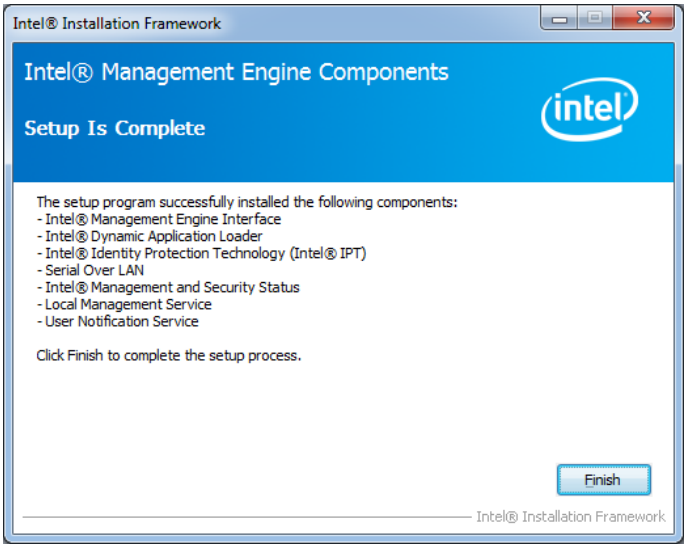
2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click ***Next***.



3. Click ***Yes*** to to agree with the license agreement.

4. When the Setup Progress screen appears, click ***Next***. Then, click ***Finish*** when the setup progress has been successfully installed.



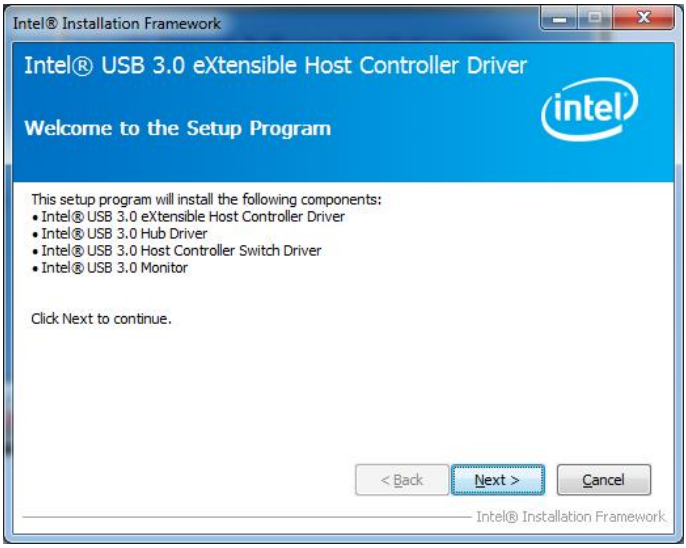


Intel® USB 3.0 Drivers

1. Insert the CD that comes with the board. Click ***Intel*** and then ***Intel(R) Q7 Series Chipset Drivers***.

2. Click ***Intel(R) USB 3.0 Drivers.***

3. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click ***Next***.



4. Click ***Yes*** to to agree with the license agreement and continue the installation.

5. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

6. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 03Fh	Interrupt Controller #1
040h - 05Fh	Timer
060h - 06Fh	Keyboard Controller
070h - 07Fh	Real Time Clock, NMI
080h - 09Fh	DMA Page Register
0A0h - 0BFh	Interrupt Controller #2
0C0h - 0DFh	DMA Controller #2
0F0h	Clear Math Coprocessor Busy Signal
0F1h	Reset Math Coprocessor
1F0h - 1F7h	IDE Interface
278h - 27Fh	Parallel Port #2(LPT2)
2E8h – 2EFh	Serial Port #4(COM4)
2F8h - 2FFh	Serial Port #2(COM2)
2B0h- 2DFh	Graphics adapter Controller
360h - 36Fh	Network Ports
3B0h - 3BFh	Monochrome & Printer adapter
3C0h - 3CFh	EGA adapter
3D0h - 3DFh	CGA adapter
3E8h – 3EFh	Serial Port #3(COM3)
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ2	Interrupt Cascade
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ5	Reserved
IRQ6	Reserved
IRQ7	Reserved
IRQ8	Real Time Clock
IRQ9	Reserved
IRQ10	Serial Port #3
IRQ11	Serial Port #4
IRQ12	PS/2 Mouse
IRQ13	80287
IRQ14	Primary IDE
IRQ15	Secondary IDE

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81865.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81865 watch dog program\n");

        SIO = Init_F81865();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81865, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime);  }
        else
        {       DisableWDT();          }

        return 0;
}
```

```
//-------------------------------------------------------------------------
void EnableWDT(int interval)
{
	unsigned char bBuf;

	bBuf = Get_F81865_Reg(0x2B);
	bBuf &= (~0x20);
	Set_F81865_Reg(0x2B, bBuf);			//Enable WDTO

	Set_F81865_LD(0x07);				//switch to logic device 7
	Set_F81865_Reg(0x30, 0x01);			//enable timer

	bBuf = Get_F81865_Reg(0xF5);
	bBuf &= (~0x0F);
	bBuf |= 0x52;
	Set_F81865_Reg(0xF5, bBuf);			//count mode is second

	Set_F81865_Reg(0xF6, interval);		//set timer

	bBuf = Get_F81865_Reg(0xFA);
	bBuf |= 0x01;
	Set_F81865_Reg(0xFA, bBuf);			//enable WDTO output

	bBuf = Get_F81865_Reg(0xF5);
	bBuf |= 0x20;
	Set_F81865_Reg(0xF5, bBuf);			//start counting
}
//-------------------------------------------------------------------------
void DisableWDT(void)
{
	unsigned char bBuf;

	Set_F81865_LD(0x07);				//switch to logic device 7

	bBuf = Get_F81865_Reg(0xFA);
	bBuf &= ~0x01;
	Set_F81865_Reg(0xFA, bBuf);			//disable WDTO output

	bBuf = Get_F81865_Reg(0xF5);
	bBuf &= ~0x20;
	bBuf |= 0x40;
	Set_F81865_Reg(0xF5, bBuf);			//disable WDT
}
//-------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81865.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81865_BASE;
void Unlock_F81865 (void);
void Lock_F81865 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81865(void)
{
	unsigned int result;
	unsigned char ucDid;

	F81865_BASE = 0x4E;
	result = F81865_BASE;

	ucDid = Get_F81865_Reg(0x20);
	if (ucDid == 0x07)                                  //Fintek 81865
	{	goto Init_Finish;	}

	F81865_BASE = 0x2E;
	result = F81865_BASE;

	ucDid = Get_F81865_Reg(0x20);
	if (ucDid == 0x07)                                  //Fintek 81865
	{	goto Init_Finish;	}

	F81865_BASE = 0x00;
	result = F81865_BASE;

Init_Finish:
	return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81865 (void)
{
	outportb(F81865_INDEX_PORT, F81865_UNLOCK);
	outportb(F81865_INDEX_PORT, F81865_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81865 (void)
{
	outportb(F81865_INDEX_PORT, F81865_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81865_LD( unsigned char LD)
{
	Unlock_F81865();
	outportb(F81865_INDEX_PORT, F81865_REG_LD);
	outportb(F81865_DATA_PORT, LD);
	Lock_F81865();
}
//---------------------------------------------------------------------------
void Set_F81865_Reg( unsigned char REG, unsigned char DATA)
{
	Unlock_F81865();
	outportb(F81865_INDEX_PORT, REG);
	outportb(F81865_DATA_PORT, DATA);
	Lock_F81865();
}
```

```
//---------------------------------------------------------------------------
unsigned char Get_F81865_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81865();
        outportb(F81865_INDEX_PORT, REG);
        Result = inportb(F81865_DATA_PORT);
        Lock_F81865();
        return Result;
}
//---------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#ifndef __F81865_H
#define __F81865_H                     1
//---------------------------------------------------------------------------
#define F81865_INDEX_PORT       (F81865_BASE)
#define F81865_DATA_PORT        (F81865_BASE+1)
//---------------------------------------------------------------------------
#define F81865_REG_LD           0x07
//---------------------------------------------------------------------------
#define F81865_UNLOCK           0x87
#define F81865_LOCK                     0xAA
//---------------------------------------------------------------------------
unsigned int Init_F81865(void);
void Set_F81865_LD( unsigned char);
void Set_F81865_Reg( unsigned char, unsigned char);
unsigned char Get_F81865_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif  //__F81865_H
```