IB908F

Intel® Haswell-ULT

3.5” Disk Size SBC

USER’S MANUAL

Version 1.1

Acknowledgments

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Introduction

Product Description

The IB908F is a 3.5-inch single board computer based on the Intel® Haswell-ULT MCP processors.

The IB908F platform is well-suited for low-power and high-performance designs in a broad range of markets including Industrial Control & Automation, Digital Signage, Thin Client, Electronic Gaming Machines, and SMB storage appliances.

IB908F Features:

- Supports Intel® 4th generation mobile Core™ i MCP processors
- Two DDR3L SO-DIMM, 1333/1600 MHz, Max. 16GB memory
- Integrated graphics for DVI-I, LVDS displays
- 2 x SATA III connector
- 2x COM port connector
- 2 x Mini-PCIe(x1) slot *(w/ USB/MSATA support)*
- 2x GbE (RJ-45) connector
- 1x 9V to 24V DC-IN power connector

Checklist

Your IB908F package should include the items listed below.

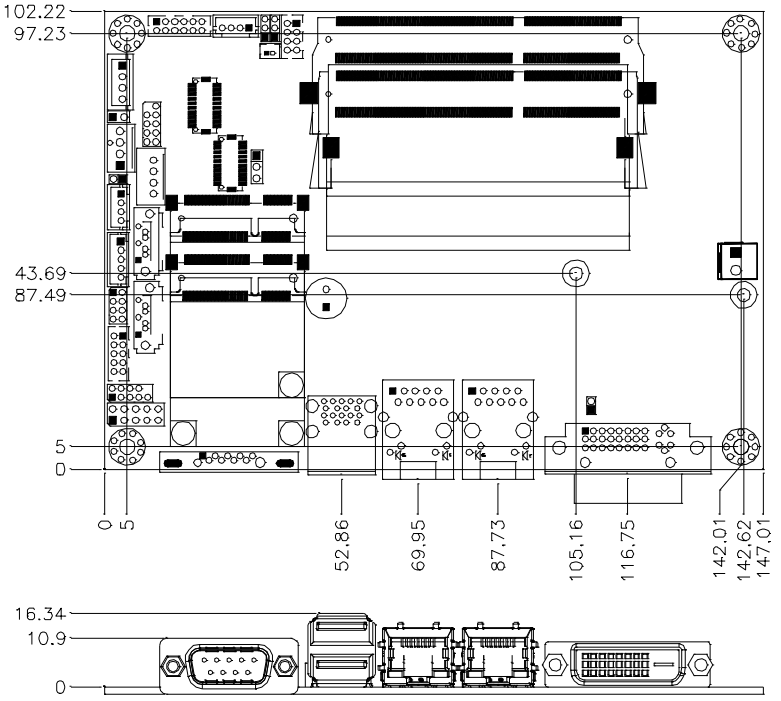
- The IB908F SBC
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility
- Optional cable kit (containing DC in power cable/PW87, COM port cable / PK1H, SATA & HDD power cable/SATA-26 and USB 2.0 cable/USB-29)
- Other options: Audio-18 audio cable, HSIB908-BGA-1 heatsink

IB908F Specifications

Product Name	**IB908F**
Form Factor	3.5" SBC
CPU Type	- Intel® 4th generation mobile Core™ i MCP processors (22nm monolithic) - TDP = 15W (DC) , FCBGA1168 @ solder side
CPU Speed	Intel® Core™ i7-4650U processor (1.7GHz) **[IB908AF-4650]** Intel® Core™ i5-4300U processor (1.9GHz) **[IB908AF-4300]** Intel® Core™ i3-4010U processor (1.7GHz) **[IB908F-4010]** Intel® Celeron® 2980U processor (1.6GHz) **[IB908F-2980]**
Cache	Up to 4MB
Chipset	Integrated in Intel® 4th Generation Core™ i U-series processor
BIOS	AMI BIOS
Memory	Intel® 4th Gen. Core™ i U-series processor integrated memory controller - DDR3L (1.35V) @1600 MHz, SO-DIMM [204-pin vertical] x **2** - Max. 16GB, Non-ECC
Display	Intel® 4th Gen. Core™ i U-series processor integrated Gfx, supports 3 independent displays, Direct X 11.1, OpenGL 3.2, Open CL 1.2 - DVI-I x 1 (Thru DDI#1 w/ Level shifter [ASM1442K] for DVI + DP to VGA [NXP PTN3392])
LVDS	- LVDS(Thru eDP, via NXP PTN3460 bridge IC) 24-bit dual channels LVDS interface w/DF20 socket x2
LAN	Intel® I218LM GbE PHY (IB908AF-4650& IB908AF-4300) or I218V GbE PHY (IB908F-4010 & IB908F-2980) Intel® I211AT as 2nd GbE
USB	- Intel® 4th Gen. Core™ i U-series processor integrated USB 2.0 host controller, supports **4** x USB 2.0: **2**-ports onboard pin header + 2 port thru MiniPCIe - Intel® 4th Gen. Core™ i U-series processor integrated USB 3.0 host controller, supports **2** x USB 3.0 in the rear panel

Serial ATA Ports	Intel® 4th Gen. Core™ i U-series processor built-in SATA controller 2 x SATA 3.0 (6Gbps) and 2 x mSATA via MiniPCIe slots (w/NXP CBTL02043A switching IC)
Audio	Intel® 4th Gen. Core™ i U-series processor built-in High Definition Audio controller + Realtek ALC269Q-VC2-GR Codec [6mm **x** 6mm @ MQFN48] w/ class-D speaker amplifier(2W per channel @ 5V power supply)
LPC I/O	Nuvoton NCT6102D [128-pin LQFP, 14 mm x 14mm x 1.4mm) COM1 (RS232/422/485) [EXAR SP339EER1 232/422/485 transceiver for jumper-less]; COM2 (RS232 only) [SIPEX SP3243EBER, QFN32] [Hardware Monitor] 2 x Thermal inputs 2 x Voltage monitoring 1 x CPU Fan (PWM Fan type, 4-pin connector)
Digital IO	4 in & 4 out
iAMT(9.5)	For IB908AF-4650 / IB908AF-4300
Expansion Slots	1x mSATA/mPCIe(x1) w/ USB signal [Half-sized] 1x mSATA/mPCIe(x1) w/ USB signal [Full-sized]
Edge Connector	DVI-I x 1 RJ45 x2 for LAN#1 & #2 USB 3.0 stack connector x 1 for USB1 / 2 [Blue color] DB9 x 1 for COM #1
Onboard Header/Connector	DF20-20 socket connector x 2 for 24-bit dual channel LVDS 2 ports x SATA III [Blue color] 2x4 pins header x 1 for 2 USB 2.0 ports [DF11] 2x6 pins box header x1 for Audio [DF11] 1x4 pins box header x1 for Speaker out 2x5 pins box header x1 for COM2 2x5 pins headers x 1 for LPC (Debug purposes only) 5 pins box header x1 for smart battery 4 pins box header x1 for backlight/brightness control 4 pins power connector x1 for SATA HDD 2 pins power connector x1 for DC-in [180 degree vertical type]
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
Power Input	+9V ~ +24V DC-in
RoHS	Yes
Board Size	102mm x 147mm
OS supported	Windows 8 / Embedded; Windows 7 / Embedded Linux
Others	Heatsink i-SMART (Auto-scheduler & Power fail resume function) EEPROM 24C02(Reserved for designing, M-SO8 package)

Board Dimensions



Installations

This section provides information on how to use the jumpers and connectors on the IB908F in order to set up a workable system. The topics covered are:

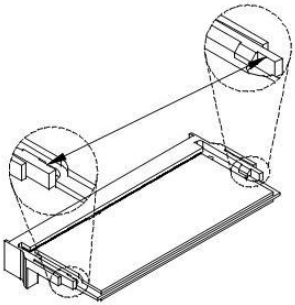
Installing the Memory

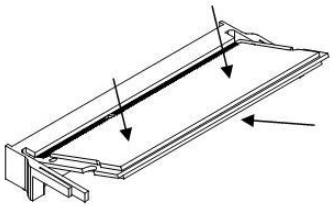
The IB908F board supports TWO DDR3L memory socket for a maximum total memory of 16GB DDR3L memory type.

Installing and Removing Memory Modules

To install the DDR3L modules, locate the memory slot on the board and perform the following steps:

1. Hold the DDR3L module so that the key of the DDR3L module aligned with that on the memory slot.
2. Gently push the DDR3L module in an upright position until the clips of the slot close to hold the DDR3L module in place when the DDR3L module touches the bottom of the slot.
3. To remove the DDR3L module, press the clips with both hands.

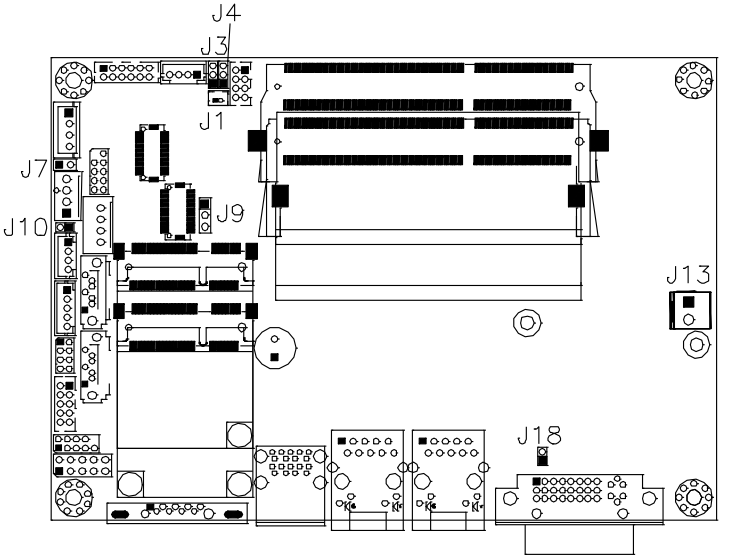




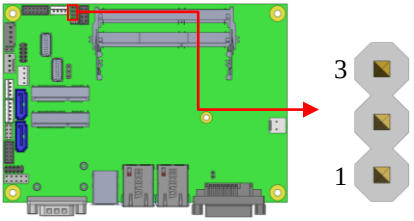
Setting the Jumpers

Jumpers are used on IB908F to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on IB908F and their respective functions.

Jumper Locations on IB908F

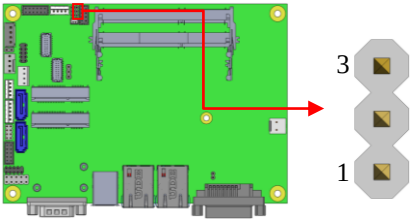


J3: Clear CMOS Contents



J3	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear CMOS

J4: Clear ME Contents

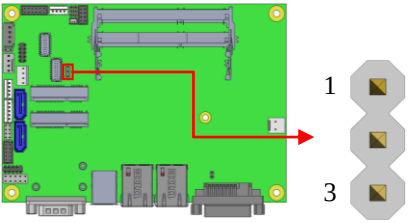


J4	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear ME RTC REGISTER

J7: Flash Descriptor Security Override (Factory use only)

J7	Flash Descriptor Security Override
Open	Disabled (Default)
Close	Enabled

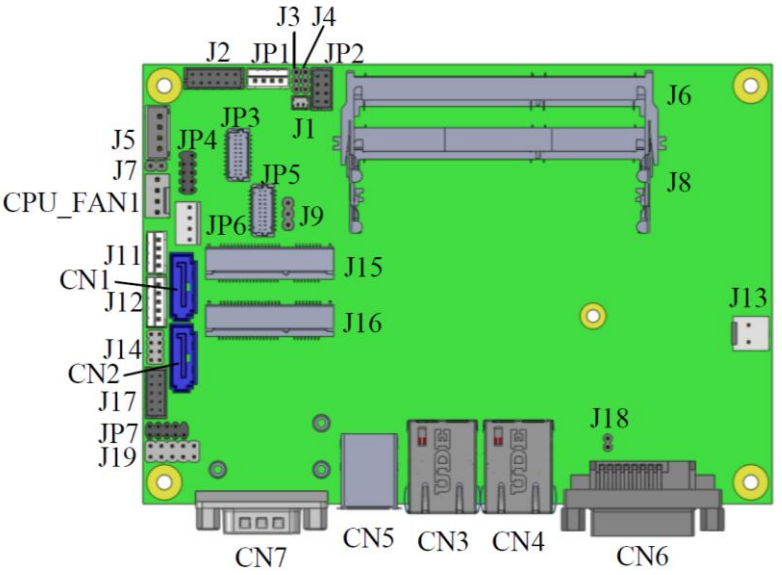
J9: LVDS Panel Power Selection

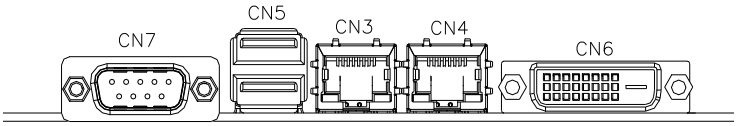


J9	Setting	Panel Voltage
	Pin 1-2 Short/Closed	3.3V (default)
	Pin 2-3 Short/Closed	5V

Connectors on IB908F

Connector Locations on IB908F





CN3, CN4: Gigabit LAN

CN3: Intel® Clarkville I218V/I218LM GbE PHY

CN4: Intel® Pearsonville I211AT as 2nd GbE

CN5: USB 1/2 Connector

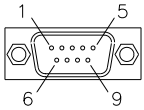
CN6: VGA DVI-I Connector

CN7: DB9 Connector

(COM1) is a DB-9 connector.

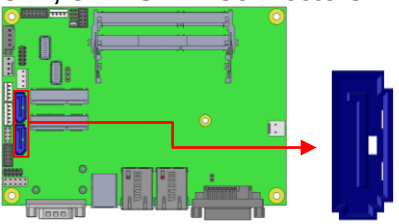
Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	6	DSR, Data set ready
RXD, Receive data	2	7	RTS, Request to send
TXD, Transmit data	3	8	CTS, Clear to send
DTR, Data terminal ready	4	9	RI, Ring indicator
GND, ground	5	10	Not Used

COM1 is jumper-less for RS-232, RS-422 and RS-485 and is to be configured with BIOS Selection.

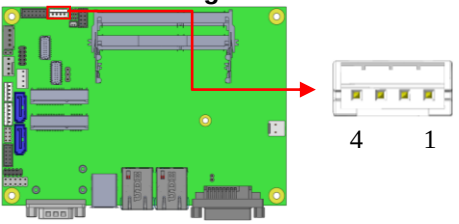


Pin #	Signal Name		
	RS-232	**R2-422**	**RS-485**
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC
10	NC	NC	NC

CN1, CN2: SATA Connectors

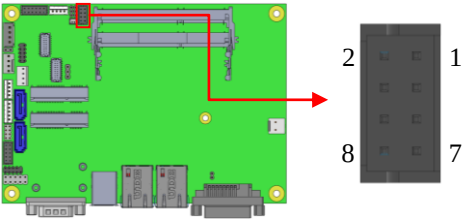


JP1: LCD Backlight Connector



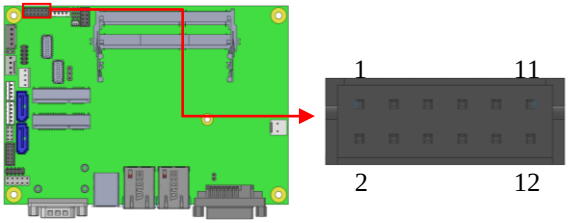
Pin #	Signal Name
1	+12V
2	Backlight Enable
3	Brightness Control
4	Ground

JP2: USB3/4 Connector



Signal Name	Pin #	Pin #	Signal Name
Vcc	1	2	Ground
D0-	3	4	D1+
D0+	5	6	D1-
Ground	7	8	Vcc

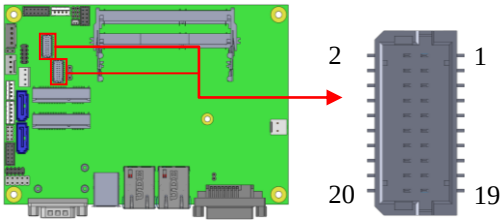
J2: Audio Connector (DF11 Connector)



Signal Name	Pin #	Pin #	Signal Name
LINEOUT_R	2	1	LINEOUT_L
Ground	4	3	JD_FRONT
LINEIN_R	6	5	LINEIN_L
Ground	8	7	JD_LINEIN
MIC-R	10	9	MIC_L
Ground	12	11	JD_MIC1

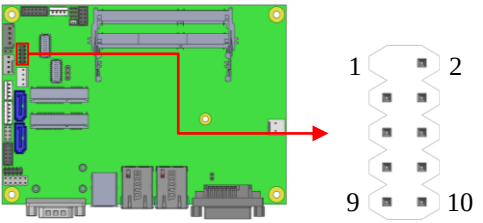
JP3, JP5: LVDS Connectors (LVDS1,LVDS2)

The LVDS connectors (Hirose DF20G-20DP-1V) on board consist of the first channel (LVDS1) and second channel (LVDS2).

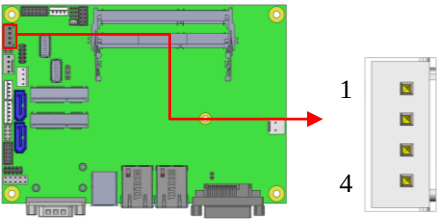


Signal Name	Pin #	Pin #	Signal Name
TX0N	2	1	TX0P
Ground	4	3	Ground
TX1N	6	5	TX1P
Ground	8	7	Ground
TX2N	10	9	TX2P
Ground	12	11	Ground
CLKN	14	13	CLKP
Ground	16	15	Ground
TX3N	18	17	TX3P
Power	20	19	Power

JP4: SPI Flash Connector (factory use only)

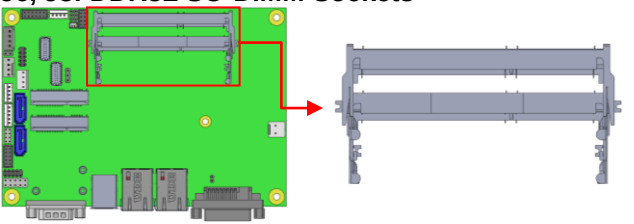


J5: Amplifier Connector

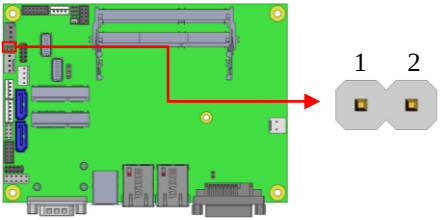


Pin #	Signal Name
1	OUTL+
2	OUTL-
3	OUTR-
4	OUTR+

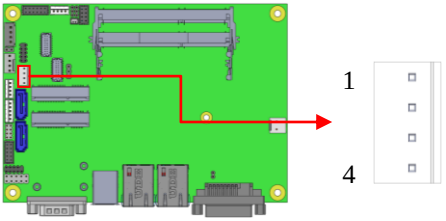
J6, J8: DDR3L SO-DIMM Sockets



J7: Factory use only

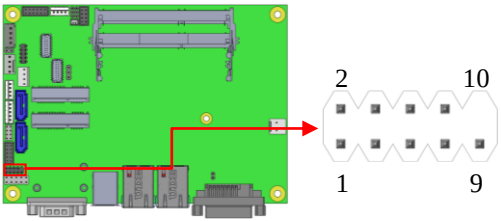


JP6: SATA HDD Power Connectors

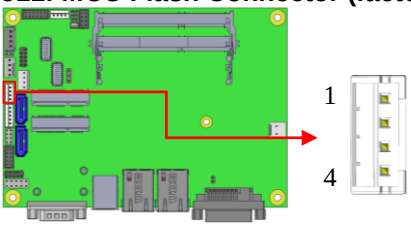


Pin #	Signal Name
1	+5V
2	Ground
3	Ground
4	+12V

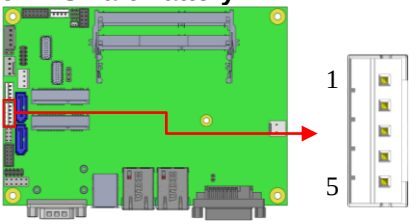
JP7: Debug 80 Port Connector (factory use only)



J11: MCU Flash Connector (factory use only)

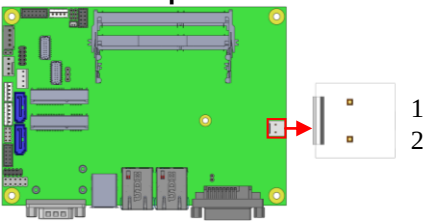


J12: Smart Battery



Pin #	Signal Name
1	RST#
2	ICHSWI#
3	Ground
4	SMB_DATA
5	SMB_CLK

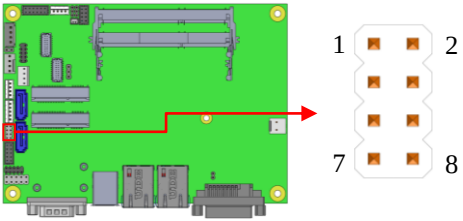
J13: Board Input Power Connector



Pin #	Signal Name
1	**+9V to +24V**
2	GND

J14: Front Panel Connector

The following table shows the pin outs of the 2x4 pin header



Signal Name	Pin #	Pin #	Signal Name
Ground	1	2	PWR_SW
PWR_LED+	3	4	PWR_LED-
HDD_LED+	5	6	HDD_LED-
Ground	7	8	RESET

J14 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status.

J14 is an 8-pin header that provides interfaces for the following functions.

ATX Power ON Switch: Pins 1 and 2

This 2-pin connector is an "ATX Power Supply On/Off Switch" on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.

Power LED: Pins 3 and 4

Pin #	Signal Name
3	LED(+)
4	LED(-)

Hard Disk Drive LED Connector: Pins 5 and 6

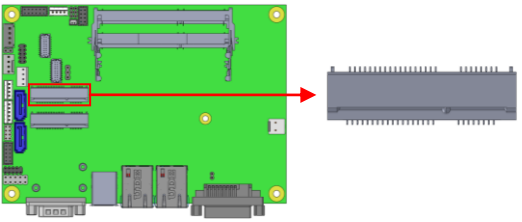
This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.

Pin #	Signal Name
5	LED(+)
6	LED(-)

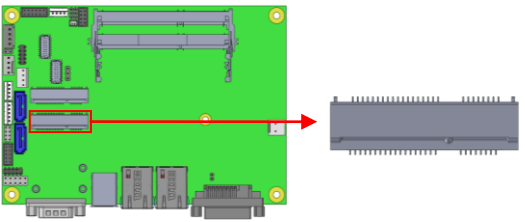
Reset Switch: Pins 7 and 8

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.

J15: Mini PCIE Connector (Supports mSATA)

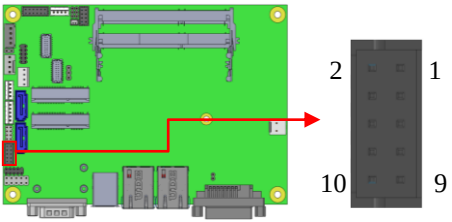


J16: Mini PCIE Connector (Half Size/ Supports mSATA)



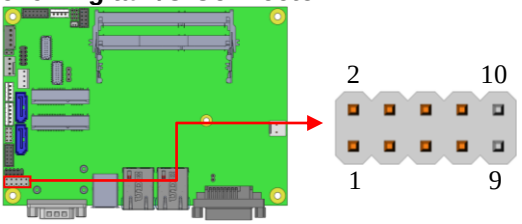
**** The gap of height between J15 & J16 is following PCI Express Mini Card electromechanical spec. ****

J17: COM2/RS232 Serial Port



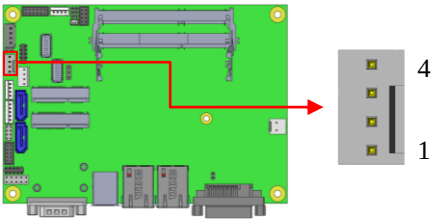
Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	2	RXD, Receive data
TXD, Transmit data	3	4	Data terminal ready
GND, ground	5	6	DSR, Data set ready
RTS, Request to send	7	8	CTS, Clear to send
RI, Ring indicator	9	10	Not Used

J19: Digital I/O Connector



Signal Name	Pin #	Pin #	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

CPU_FAN1: CPU Fan Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Control

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BIOS Setup

This chapter describes the different settings available in the BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also adds virus and password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

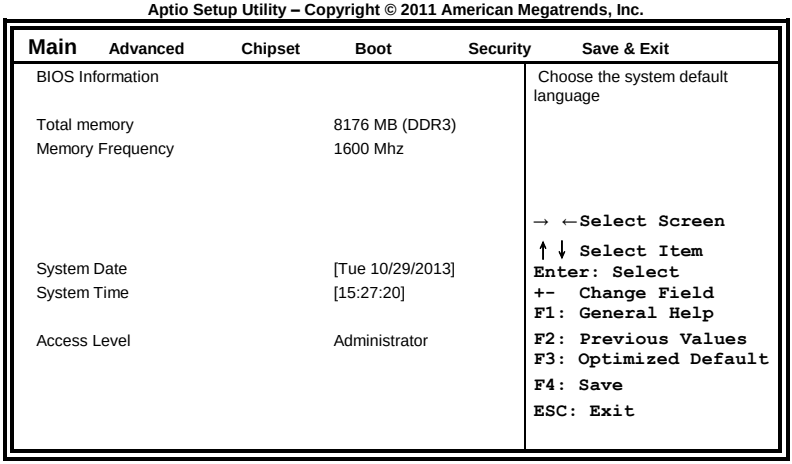
The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

```
Press  <DEL> or <ESC>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Main Settings



System Date

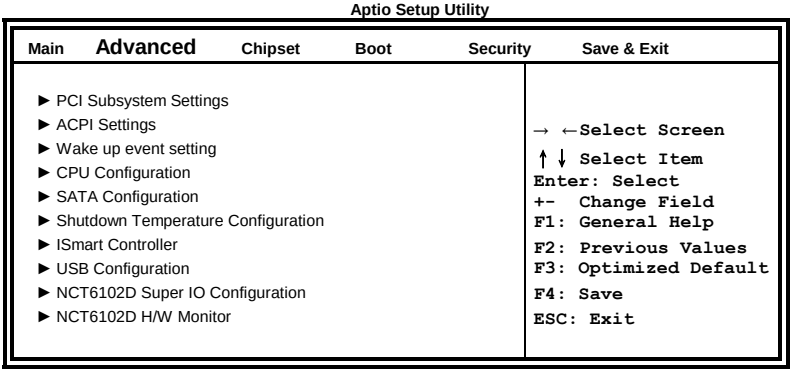
Set the Date. Use Tab to switch between Data elements.

System Time

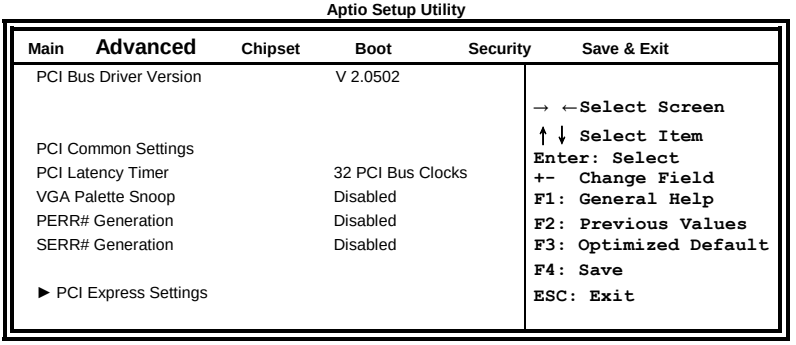
Set the Time. Use Tab to switch between Data elements.

Advanced Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



PCI Subsystem Settings



PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

VGA Palette Snoop

Enables or disables VGA Palette Registers Snooping.

PERR# Generation

Enables or disables PCI device to generate PERR#.

SERR# Generation

Enables or disables PCI device to generate SERR#.

PCI Express Settings

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
PCI Express Device Register Settings					
Relaxed Ordering			Disabled		
Extended Tag			Disabled		
No Snoop			Enabled		
Maximum Payload			Auto		
Maximum Read Request			Auto		
PCI Express Link Register Settings					
ASPM Support			Disabled		
WARNING: Enabling ASPM may cause PCI-E devices to fail					
Extended Synch			Disabled		
Link Training Retry			5		
Link Training Timeout (uS)			100		
Unpopulated Links			Keep Link ON		
Restore PCIE Registers			Disabled		

→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

Relaxed Ordering
Enables or disables PCI Express Device Relaxed Ordering.

Extended Tag
If ENABLED allows device to use 8-bit Tag field as a requester.

No Snoop
Enables or disables PCI Express Device No Snoop option.

Maximum Payload
Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Maximum Read Request
Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support
Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

Extended Synch
If ENABLED allows generation of Extended Synchronization patterns.

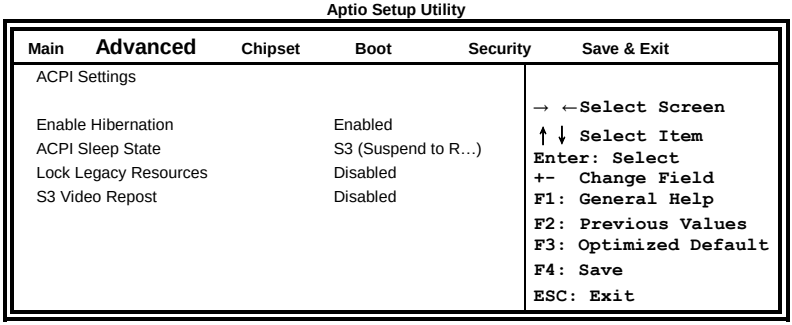
Link Training Retry
Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Link Training Timeout (uS)
Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

Unpopulated Links
In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

Restore PCIE Registers
On non-PCI Express aware OS's (Pre Windows Vista) some devices may not be correctly reinitialized after S3.Enabling this restore PCI Express device configuration on S3 resume
Warning: Enabling this may cause issues with other hardware after S3 resume.1

ACPI Settings



Enable Hibernation

Enables or Disables System ability to hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State

Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

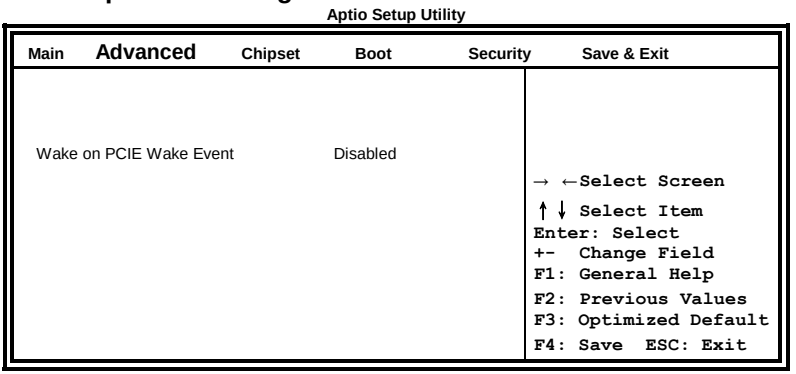
Lock Legacy Resources

Enabled or Disabled Lock of Legacy Resources.

S3 Video Repost

Enable or disable S3 Video Repost.

Wake up event settings

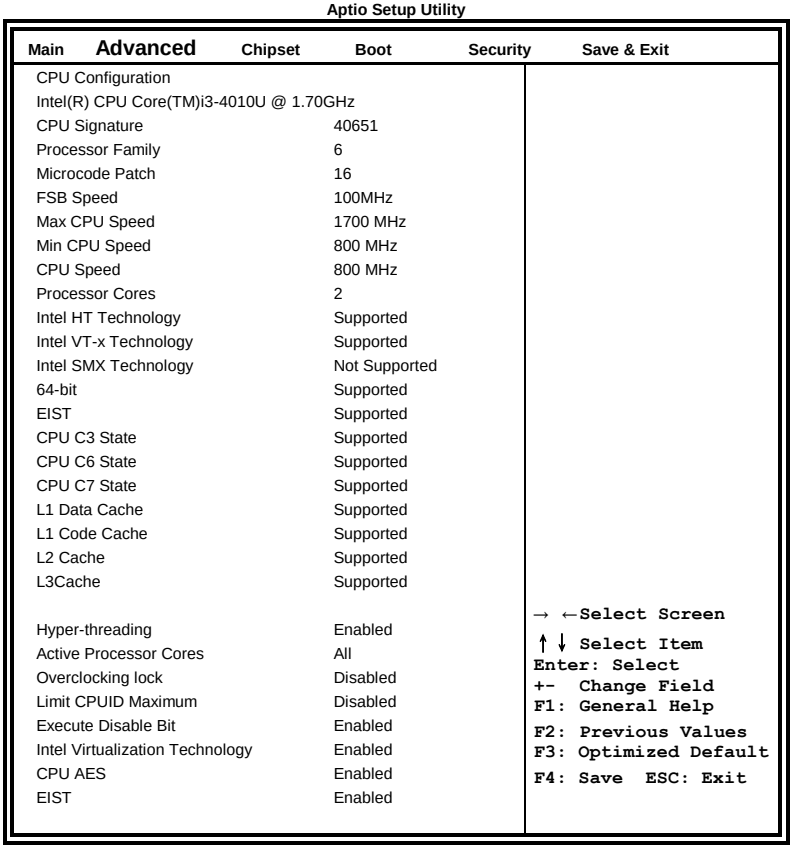


Wake on PCIE PME Wake Event

The options are Disabled and Enabled.

CPU Configuration

This section shows the CPU configuration parameters.



Hyper-threading

Select the performance state that the BIOS will set before OS handoff.

Active Processor Cores

Number of cores to enable in each processor package.

Overclocking lock

Flex_RATIO(194)MSR

Limit CPUID Maximum
Disabled for Windows XP.

Execute Disable Bit
XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS

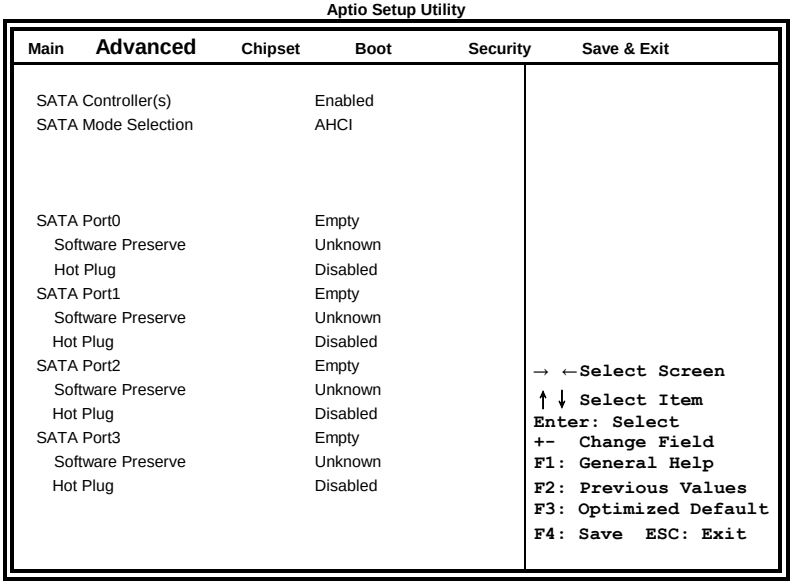
Intel Virtualization Technology
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

CPU AES
Enabled/Disabled CPU Advanced Encryption Standard instructions

EIST
Enabled/Disabled Intel Speedstep.

SATA Configuration

SATA Devices Configuration.



SATA Controller(s)

Enable / Disable Serial ATA Controller.

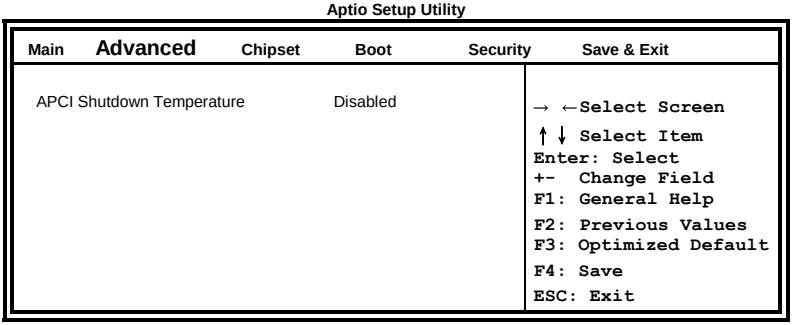
SATA Mode Selection

(1) AHCI Mode.
(2) RAID Mode.

Hot Plug

Designates this port as Hot P;uggable.

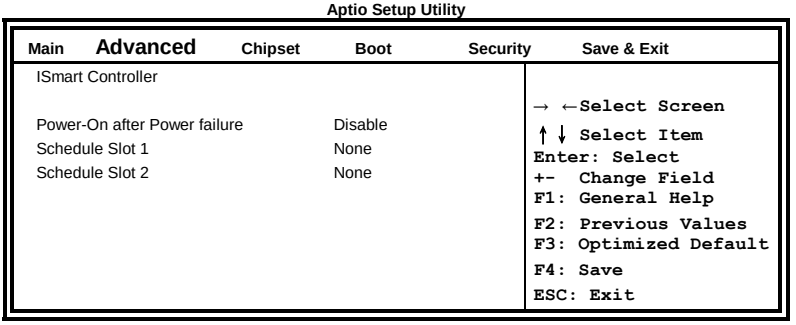
Shutdown Temperature Configuration



ACPI Shutdown Temperature

The default setting is Disabled.

ISmart Controller



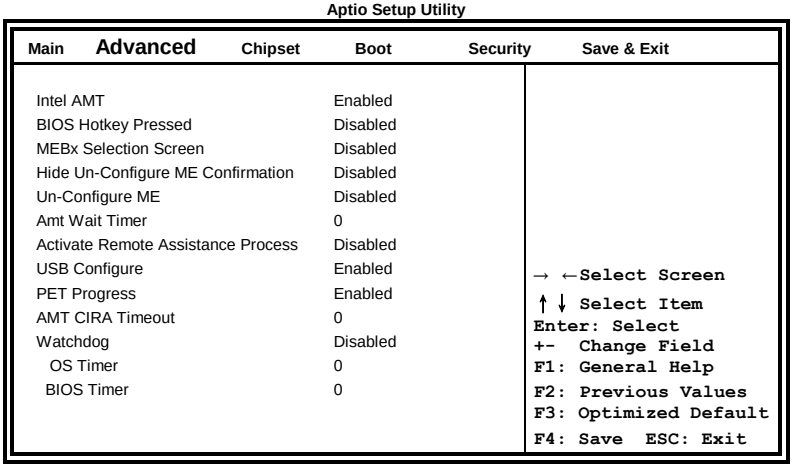
Power-On after Power failure

Enable or Disable.

Schedule Slot 1 / 2

Setup the hour/minute for system power on.

AMT Configuration



AMT Configuration

This configuration is supported iAMT function. Options are Enabled and Disabled.

Note: iAMT H/W is always enabled. This option just controls the BIOS extension execution. If enabled, this requires additional firmware in the SPI device.

Unconfigure ME

Perform AMT/ME unconfigure without password operation.

Amt Wait Timer

Set timer to wait before sending ASF_GET_BOOT_OPTIONS.

Activate Remote Assistance Process

Trigger CIRA boot.

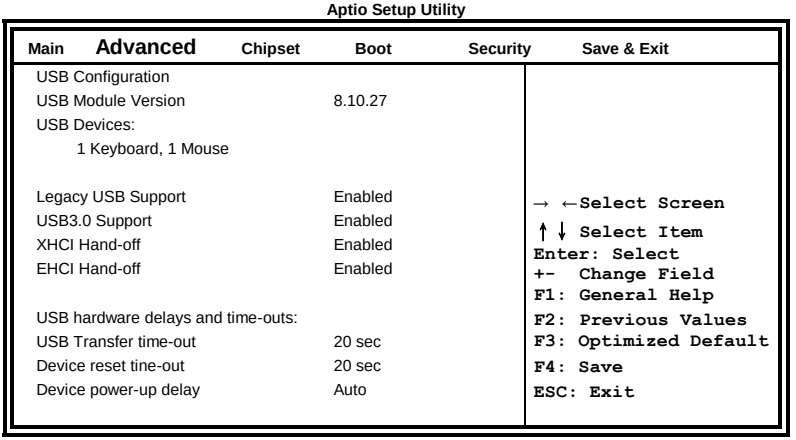
PET Progress

User can Enable/Disable PET Events progress to receive PET events or not.

Watchdog Timer

Enable/Disable Watchdog Timer.

USB Configuration



Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected.
DISABLE option keeps USB devices available only for EFI applications.

USB3.0 Support

Enable/Disable USB3.0 (XHCI) Controller support.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off

Enabled/Disabled. This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB Transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

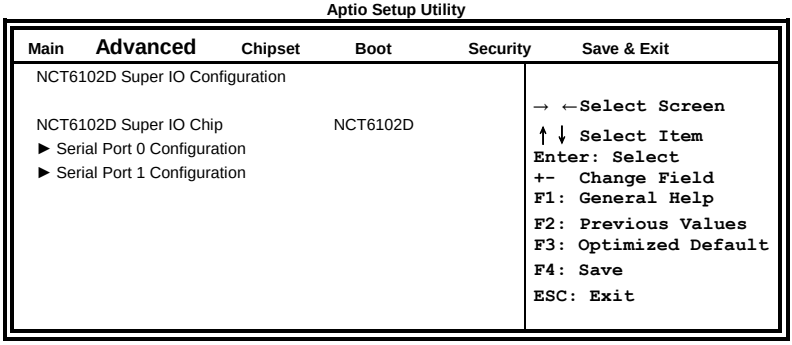
Device reset time-out

USB mass Storage device start Unit command time-out.

Device power-up delay

Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

NCT6102D Super IO Configuration



Serial Port Configuration

Set parameters of serial ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

NCT6102D H/W Monitor

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
PC Health Status					
Smart Fan Function			Disabled		
SYS Temp			+40 C		
CPU Temp			+43 C		
CpuFan Speed			4166		
Vcore			+1.808 V		
+5V			+4.918 V		
+12V			+12.000 V		
1.35V			+1.376 V		

→ ←Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save
ESC: Exit

Smart Fan Function

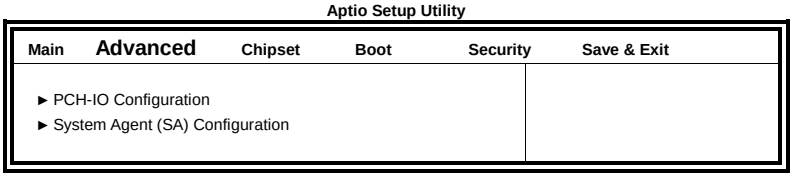
This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the board. The values are read-only values as monitored by the system and show the PC health status.

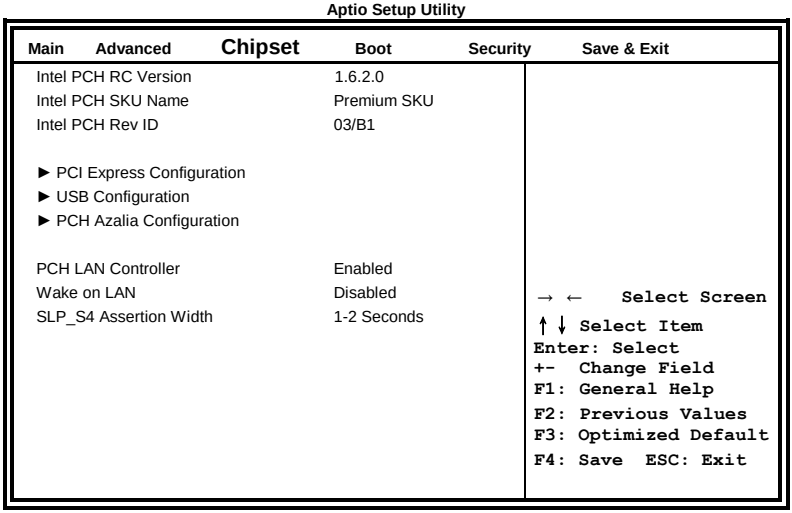
Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



PCH-IO Configuration

This section allows you to configure the North Bridge Chipset.



PCH LAN Controller

Enable or disable onboard NIC.

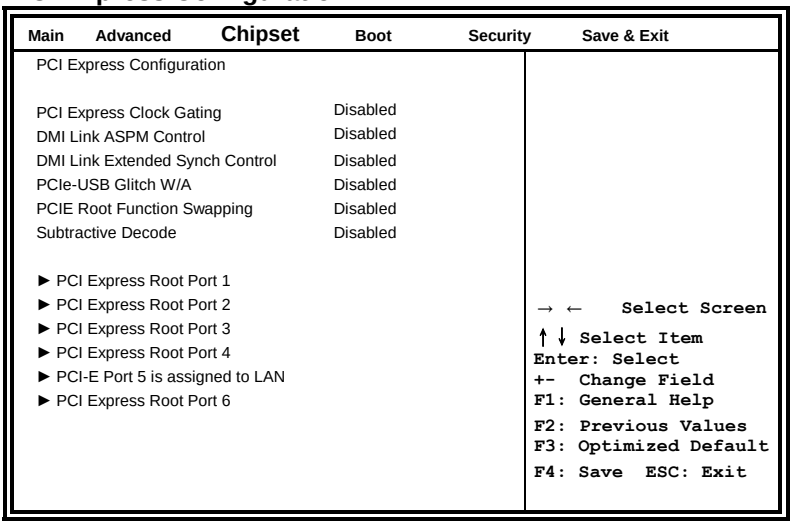
Wake on LAN

Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

SLP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.

PCI Express Configuration



PCI Express Clock Gating

Enable or disable PCI Express Clock Gating for each root port

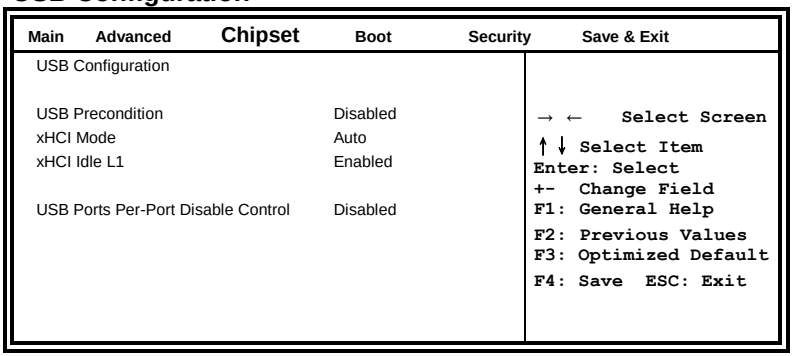
DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI link.

PCIe-USB Glitch W/A

PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG port.

USB Configuration



USB Precondition

Precondition work on USB host controller and root ports for faster enumeration.

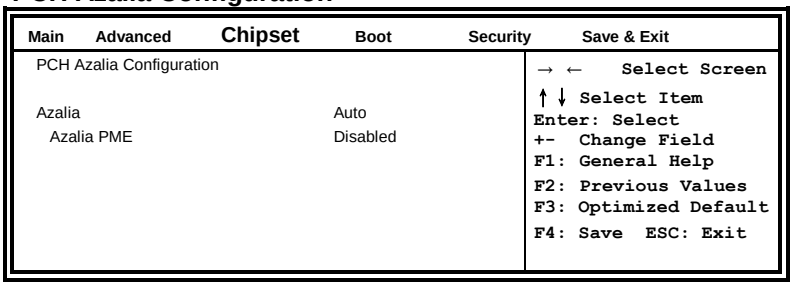
xHCI Mode

Mode of operation of xHCI controller.

USB Ports Per-Port Disable Control

Control each of the USB ports (0~13) disabling.

PCH Azalia Configuration



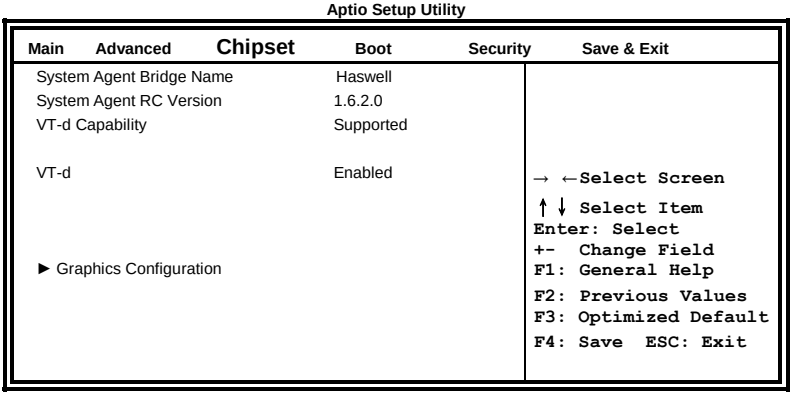
Azalia

Control Detection of the Azalia device.
Disabled = Azalia will be unconditionally be disabled.
Enabled = Azalia will be unconditionally be enabled.
Auto = Azalia will be enabled if present, disabled otherwise.

Azalia PME

Enable or disable power management capability of the audio controller.

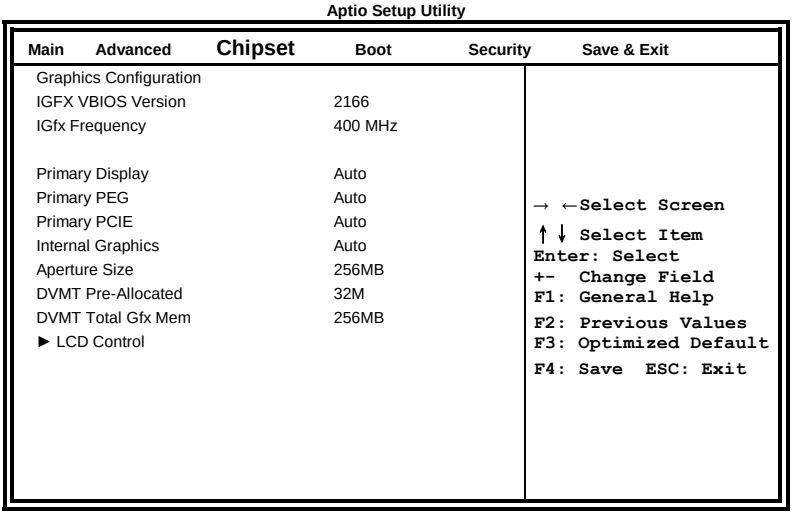
System Agent (SA) Configuration



VT-d

Check to enable VT-d function on MCH.

Graphics Configuration



Primary Display

Select which of IGFX/PEG/PCI graphics device should be primary display or select SG for switchable Gfx.

Primary PEG
Select PEGO/PEG1/PEG2/PEG3 Graphics device should be Primary PEG.

Primary PCIE
Select PCIE0/PCIE1/PCIE2/PCIE3/PCIE4/PCIE5/PCIE6PCIE7 Graphics device should be primary PCIE.

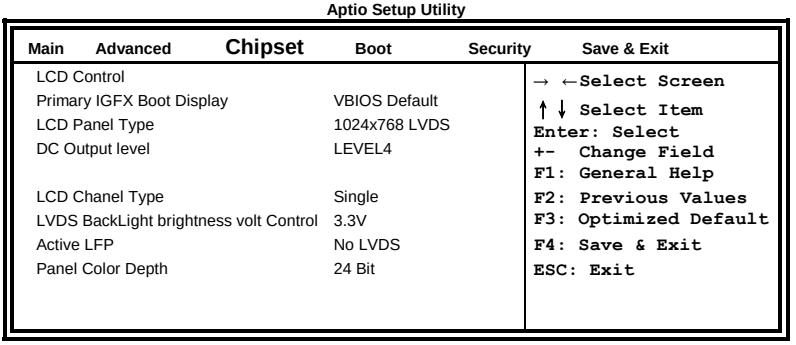
Internal Graphics
Keep IGD enabled based on the setup options.

DVMT Pre-Allocated
Select DVMT 5.0 Pre-Allocated (Fixed) graphics memory size used by the internal graphics device.

DVMT Total Gfx Mem
Select DVMT 5.0 total graphics memory size used by the internal graphics device.

LCD Control
Select the Video Device that will be activated during POST. This has no effect if external graphics present. Secondary booty display selection will appear based on your selection. VGA modes will be supported only on primary display.

LCD Control



Primary IGFX Boot Display

Select the Video Device, which will be activated during POST. This has no effect if external graphics present.
Secondary boot display selection will appear based on your selection. VGA modes will be supported only on primary display.

LCD Panel Type

Select LCD panel used by Internal Graphics Device by selecting the appropriate setup item: 640x480 LVDS ~ 2048x1536 LVDS.

DC Output level

Backlight Brightness Control

LCD Chanel Type

Select LCD Chanel Type

LVDS Back Light Brightness Volt Control

LVDS Back Light Volt Control: 3.3V, 5V

Active LFP

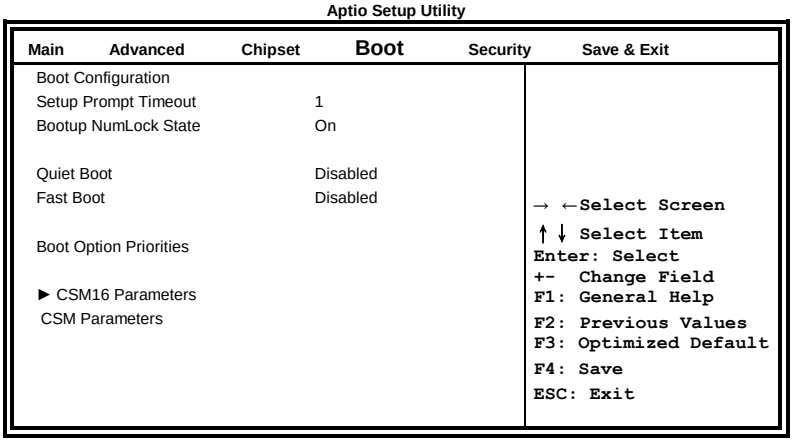
Select the Active LFP Configuration.
No LVDS: VBIOS does not enable LVDS.
Int-LVDS: VBIOS enables LVDS driver by Integrated encoder.
SDVO LVDS: VBIOS enables LVDS driver by SDVO encoder.
eDP Port-A: LFP Driven by Int-DisplayPort encoder from Port-A.

Panel Color Depth

Select the LFP Panel Color Depth: 18 Bit, 24 Bit.

Boot Settings

This section allows you to configure the boot settings.



Setup Prompt Timeout

Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables/Disables Quiet Boot option.

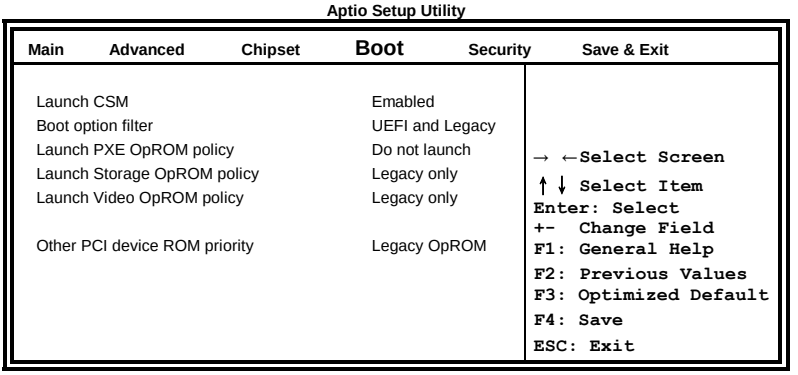
Fast Boot

Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Boot Option Priorities

Sets the system boot order.

CSM parameters
OpROM execution, boot options, filter, etc.



Launch CSM
This option controls if CSM will be launched.

Boot option filter
This option controls what devices system can boot to.

Launch PXE OpROM policy
Controls the execution of UEFI and Legacy PXE OpROM.

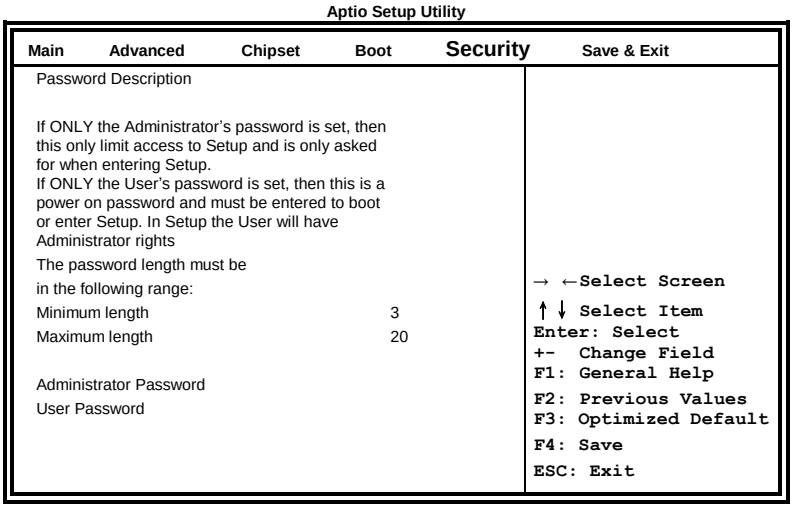
Launch Storatge OpROM policy
Controls the execution of UEFI and Legacy Storage OpROM.

Launch Video OpROM policy
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI device ROM priority
For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



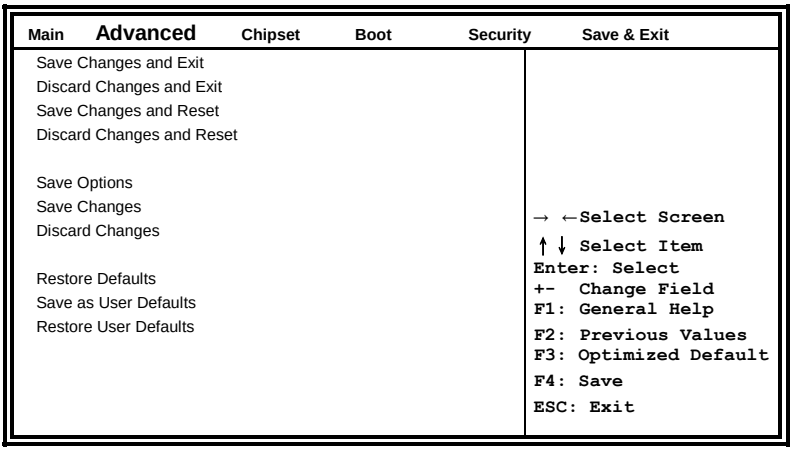
Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings



Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the board. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

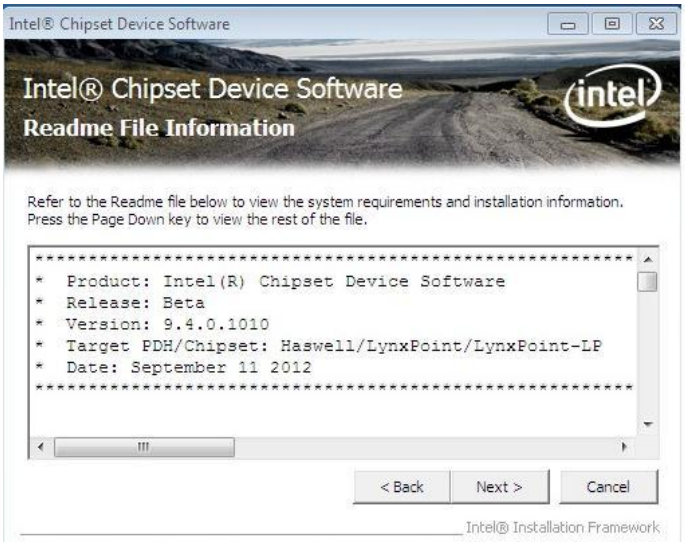
1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Intel(R) Chipset Software Installation Utility.***

3. When the Welcome screen to the Intel® Chipset Device Software appears, click ***Next*** to continue.

4. Click ***Yes*** to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click ***Next*** to continue the installation.



6. The Setup process is now complete. Click ***Finish*** to restart the computer and for changes to take effect.

VGA Drivers Installation

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Intel(R) Core(TM) i3/i5/i7 Graphics Driver.***

3. When the Welcome screen appears, click ***Next*** to continue.

4. Click ***Yes*** to to agree with the license agreement and continue the installation.

5. On the screen shown below, click ***Install*** to continue.

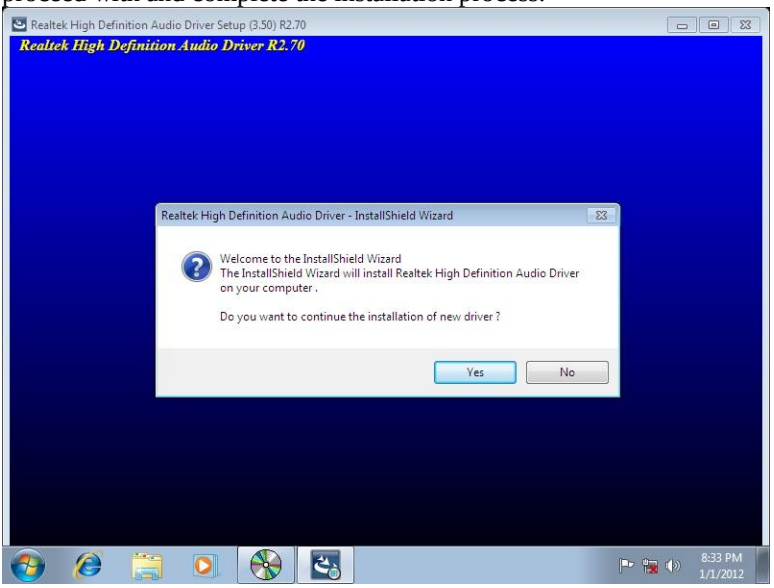
6. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Realtek HD Audio Driver Installation

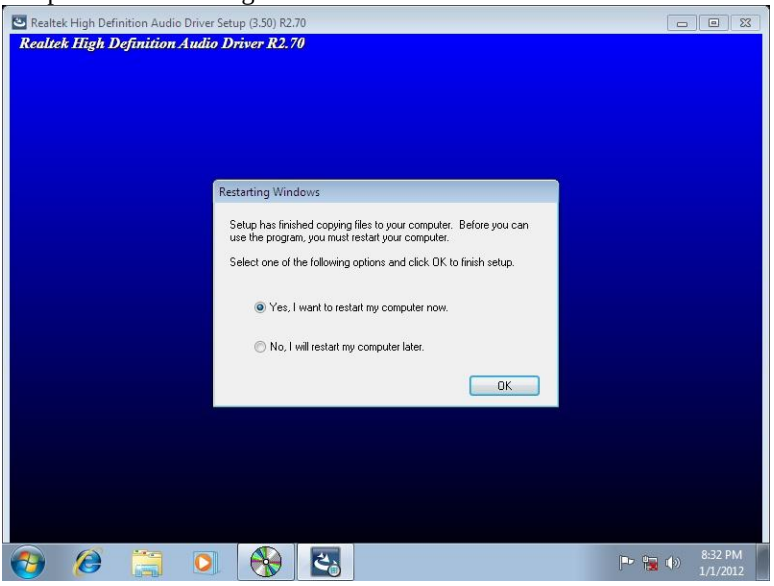
1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Realtek High Definition Audio Driver.***

3. On the Welcome to the InstallShield Wizard screen, click ***Yes*** to proceed with and complete the installation process.



4. The InstallShield Wizard Complete. Click ***Finish*** to restart the computer and for changes to take effect.

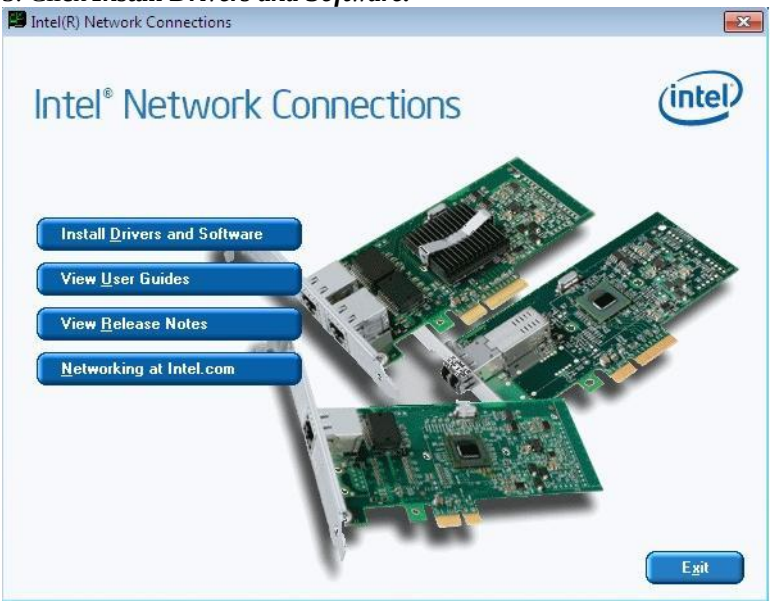


LAN Drivers Installation

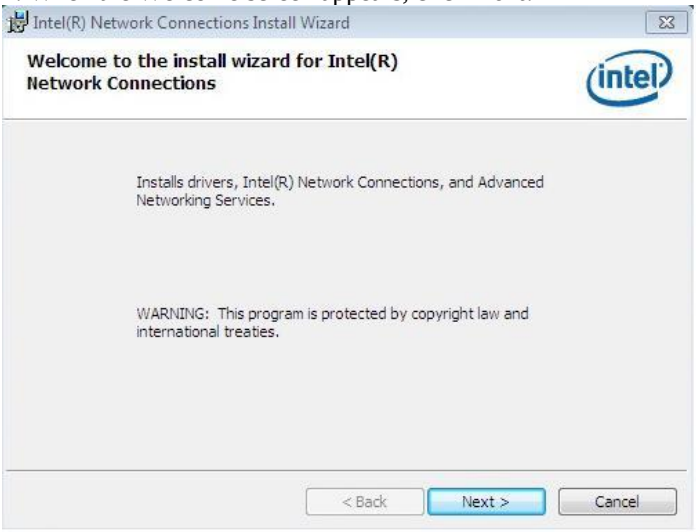
1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Intel(R) PRO LAN Network Driver.***

3. Click ***Install Drivers and Software.***

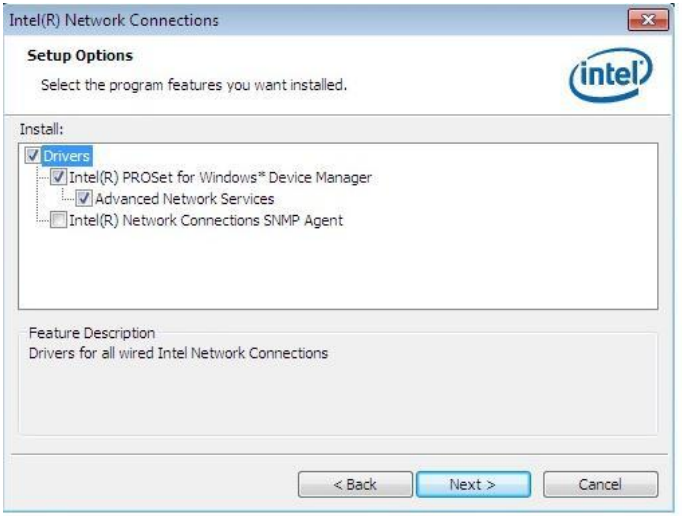


4. When the Welcome screen appears, click ***Next***.

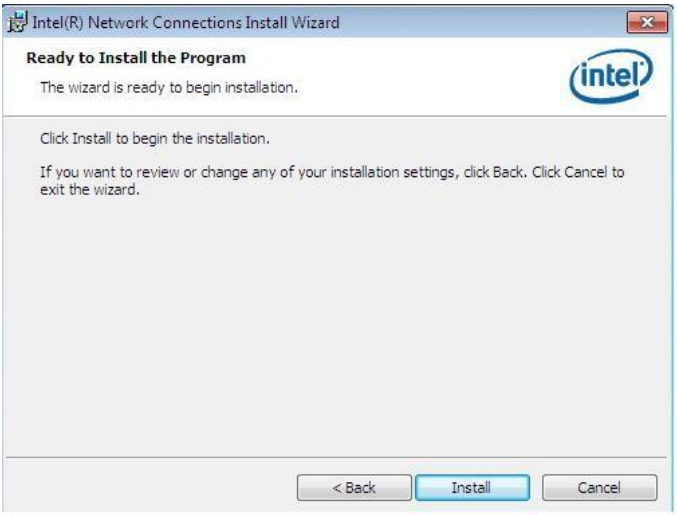


5. Click ***Next*** to to agree with the license agreement.

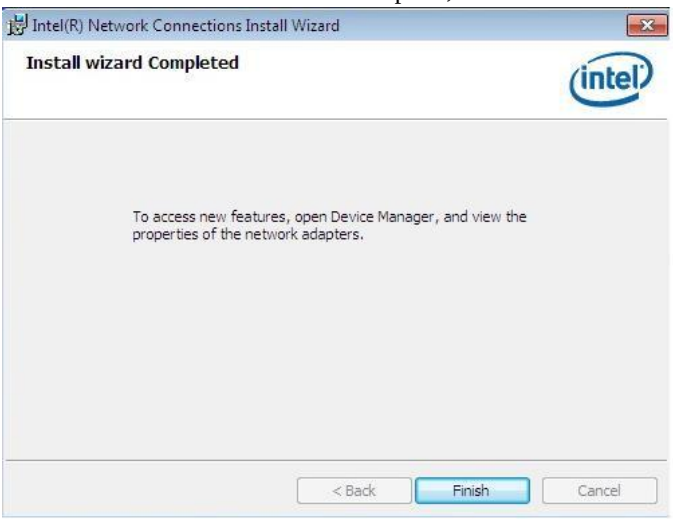
6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.



7. The wizard is ready to begin installation. Click ***Install*** to begin the installation.



8. When InstallShield Wizard is complete, click ***Finish***.

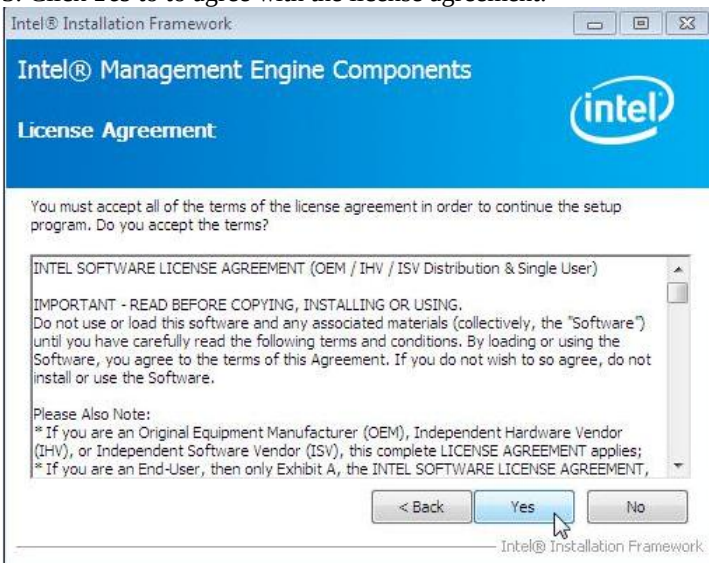


Intel® Management Engine Interface

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers*** and then ***Intel(R) AMT 9.5 Drivers***.

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click ***Next***.

3. Click ***Yes*** to to agree with the license agreement.



4. When the Setup Progress screen appears, click ***Next***. Then, click ***Finish*** when the setup progress has been successfully installed.

Intel® USB 3.0 Drivers

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Intel(R) USB 3.0 Drivers.***

3. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click ***Next***.

4. Click ***Yes*** to to agree with the license agreement and continue the installation.

5. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

6. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
000h - 01Fh	DMA Controller #1
020h - 021h	Interrupt Controller #1
040h - 043h	Timer
060h - 060h	Keyboard Controller
070h - 077h	Real Time Clock, NMI
081h - 091h	DMA Page Register
0A0h – 0A1h	Interrupt Controller #2
081h - 091h	DMA Controller #2
040h – 05Fh	SMBus Controler
2F8h - 2FFh	Serial Port #2(COM2)
3C0h- 3DFh	Graphics adapter Controller
D000 - FFFh	PCI-e Root Ports
3F8h - 3FFh	Serial Port #1(COM1)

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer Output
IRQ1	Keyboard
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ8	Real Time Clock
IRQ10	SMBus Controller
IRQ19	SATA AHCI Controller

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "6106"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
                                                        unsigned char bBuf;
                                                      unsigned char bTime;
                                                        char **endptr;

//                                                          char SIO;

                                                    printf("6106 watch dog program\n");



                                                bTime = strtol (argv[1], endptr, 10);
                                          printf("System will reset after %d seconds\n", bTime);

                                                  if (bTime)
                                                    {
                                                   else
                                                    {

                                                if (bTime > 0 && bTime < 256)
                                                    {

          A=2;

           unsigned char result;
           Set_6106_LD(0x08);

           gotoxy(1,12);


                                                                }
```

```
                                                                    return 0;
}
//---------------------------------------------------------------------------
void EnableWDT(int interval)
{
                                                                    unsigned char bBuf;

                                                                    Set_6106_LD(0x08);
                                                                    Set_6106_Reg(0x30, 0x01);

                                                                    Set_6106_Reg(0xF1, interval);

}
//---------------------------------------------------------------------------
void DisableWDT(void)
{
                                                                    unsigned char bBuf;

                                                                    Set_6106_LD(0x08);
                                                                    Set_6106_Reg(0x30, 0x00);

}
//---------------------------------------------------------------------------




//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "6106.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int 6106_BASE;
void Unlock_6106 (void);
void Lock_6106 (void);
//---------------------------------------------------------------------------
unsigned int Init_6106(void)
{
        unsigned int result;
        unsigned char ucDid;

        6106_BASE = 0x4E;
        result = 6106_BASE;

        ucDid = Get_6106_Reg(0x20);
        if (ucDid == 0x07)                                      //6106
        {       goto Init_Finish;       }

        6106_BASE = 0x2E;
        result = 6106_BASE;

        ucDid = Get_6106_Reg(0x20);
        if (ucDid == 0x07)                                      //6106
        {       goto Init_Finish;       }

        6106_BASE = 0x00;
        result = 6106_BASE;

Init_Finish:
        return (result);
```

```
}
//---------------------------------------------------------------------------
void Unlock_6106 (void)
{
        outportb(6106_INDEX_PORT, 6106_UNLOCK);
        outportb(6106_INDEX_PORT, 6106_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_6106 (void)
{
        outportb(6106_INDEX_PORT, 6106_LOCK);
}
//---------------------------------------------------------------------------
void Set_6106_LD( unsigned char LD)
{
        Unlock_6106();
        outportb(6106_INDEX_PORT, 6106_REG_LD);
        outportb(6106_DATA_PORT, LD);
        Lock_6106();
}
//---------------------------------------------------------------------------
void Set_6106_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_6106();
        outportb(6106_INDEX_PORT, REG);
        outportb(6106_DATA_PORT, DATA);
        Lock_6106();
}
//---------------------------------------------------------------------------
unsigned char Get_6106_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_6106();
        outportb(6106_INDEX_PORT, REG);
        Result = inportb(6106_DATA_PORT);
        Lock_6106();
        return Result;
}
//---------------------------------------------------------------------------
```