MX255D

3rd Generation Intel® Atom™ D2550 Fanless Mini ITX Motherboard (Cedar Trail Platform) supports 12V DC Power

bcm

ADVANCED
RESEARCH

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Revision History

Revision	Revision History	Date
1.1	Production release	08/31/2012
1.2	Update operating temperature	10/16/2012

Safety Instructions

- Always read the safety instructions carefully.
- Keep this User's Manual for future reference.
- Keep this equipment away from humidity.
- Lay this equipment on a reliable flat surface before setting it up.
- The openings on the enclosure are for air convection hence protects the equipment from overheating. DO NOT COVER THE OPENINGS.
- Make sure the voltage of the power source and adjust properly 110/220V before connecting the equipment to the power inlet.
- Place the power cord such a way that people can not step on it. Do not place anything over the power cord.
- Always Unplug the Power Cord before inserting any add-on card or module.
- All cautions and warnings on the equipment should be noted.
- Never pour any liquid into the opening that could damage or cause electrical shock.
- If any of the following situations arises, get the equipment checked by service personnel:
  ○ The power cord or plug is damaged.
  ○ Liquid has penetrated into the equipment.
  ○ The equipment has been exposed to moisture.
  ○ The equipment does not work well or you can not get it work according to User's Manual.
  ○ The equipment has dropped and damaged.
  ○ The equipment has obvious sign of breakage.
- DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT UNCONDITIONED, STORAGE TEMPERATURE ABOVE 60°C (140°F), IT MAY DAMAGE THE EQUIPMENT.

CAUTION: Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer.

警告使用者:

這是甲類資訊產品，在居住的環境中使用時，可能會造成無線電干擾，在這種情況下，使用者會被要求採取某些適當的對策。

廢電池請回收
For better environmental protection, waste batteries should be collected separately for recycling or special disposal.

CE Conformity

Hereby, we declare that this device is in compliance with the essential safety requirements and other relevant provisions set out in the European Directive.

FCC-B Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the measures listed below:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/television technician for help.

NOTICE 1

The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

NOTICE 2

Shielded interface cables and AC power cord, if any, must be used in order to comply with the emission limits.

VOIR LA NOTICE D'INSTALLATION AVANT DE RACCORDER AU RESEAU.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1. this device may not cause harmful interference, and

2. this device must accept any interference received, including interference that may cause undesired operation.

WEEE Statement

ENGLISH

Under the European Union ("EU") Directive on Waste Electrical and Electronic Equipment, Directive 2002/96/EC, which takes effect on August 13, 2005, products of "electrical and electronic equipment" cannot be discarded as municipal waste anymore and manufacturers of covered electronic equipment will be obligated to take back such products at the end of their useful life.

DEUTSCH

Gemäß der Richtlinie 2002/96/EG über Elektro- und Elektronik-Altgeräte dürfen Elektround Elektronik-Altgeräte nicht mehr als kommunale Abfälle entsorgt werden. Wir haben europaweit verschiedene Sammel- und Recyclingunternehmen beauftragt, die in die Europäische Union in Verkehr gebrachten Produkte, am Ende seines Lebenszyklus zurückzunehmen. Bitte entsorgen Sie dieses Produkt zum gegebenen Zeitpunkt ausschliesslich an einer lokalen Altgerätesammelstelle in Ihrer Nähe.

FRANÇAIS

Au sujet de la directive européenne (EU) relative aux déchets des équipement électriques et électroniques, directive 2002/96/EC, prenant effet le 13 août 2005, que les produits électriques et électroniques ne peuvent être déposés dans les décharges ou tout simplement mis à la poubelle. Les fabricants de ces équipements seront obligés de récupérer certains produits en fin de vie. Par conséquent vous pouvez retourner localement ces matériels dans les points de collecte.

РУССКИЙ

В соответствии с директивой Европейского Союза (ЕС) по предотвращению загрязнения окружающей среды использованным электрическим и электронным оборудованием (директива WEEE 2002/96/EC), вступающей в силу 13 августа 2005 года, изделия, относящиеся к электрическому и электронному оборудованию, не могут рассматриваться как бытовой мусор, поэтому производители вышеперечисленного электронного оборудования обязаны принимать его для переработки по окончании срока службы.

ESPAÑOL

Bajo la directiva 2002/96/EC de la Unión Europea en materia de desechos y/o equipos electrónicos, con fecha de rigor desde el 13 de agosto de 2005, los productos clasificados como "eléctricos y equipos electrónicos" no pueden ser depositados en los contenedores habituales de su municipio, los fabricantes de equipos electrónicos, están obligados a hacerse cargo de dichos productos al termino de su período de vida.

NEDERLANDS

De richtlijn van de Europese Unie (EU) met betrekking tot Vervuiling van Electrische en Electronische producten (2002/96/EC), die op 13 Augustus 2005 in zal gaan kunnen niet

meer beschouwd worden als vervuiling. Fabrikanten van dit soort producten worden verplicht om producten retour te nemen aan het eind van hun levenscyclus.

SRPSKI

Po Direktivi Evropske unije ("EU") o odbačenoj ekektronskoj i električnoj opremi, Direktiva 2002/96/EC, koja stupa na snagu od 13. Avgusta 2005, proizvodi koji spadaju pod "elektronsku i električnu opremu" ne mogu više biti odbačeni kao običan otpad i proizvođači ove opreme biće prinuđeni da uzmu natrag ove proizvode na kraju njihovog uobičajenog veka trajanja.

POLSKI

Zgodnie z Dyrektywą Unii Europejskiej ("UE") dotyczącą odpadów produktów elektrycznych i elektronicznych (Dyrektywa 2002/96/EC), która wchodzi w życie 13 sierpnia 2005, tzw. "produkty oraz wyposażenie elektryczne i elektroniczne " nie mogą być traktowane jako śmieci komunalne, tak więc producenci tych produktów będą zobowiązani do odbierania ich w momencie gdy produkt jest wycofywany z użycia.

TÜRKÇE

Avrupa Birliği (AB) Kararnamesi Elektrik ve Elektronik Malzeme Atığı, 2002/96/EC Kararnamesi altında 13 Ağustos 2005 tarihinden itibaren geçerli olmak üzere, elektrikli ve elektronik malzemeler diğer atıklar gibi çöpe atılamayacak ve bu elektonik cihazların üreticileri, cihazların kullanım süreleri bittikten sonra ürünleri geri toplamakla yükümlü olacaktır.

ČESKY

Podle směrnice Evropské unie ("EU") o likvidaci elektrických a elektronických výrobků 2002/96/EC platné od 13. srpna 2005 je zakázáno likvidovat "elektrické a elektronické výrobky" v běžném komunálním odpadu a výrobci elektronických výrobků, na které se tato směrnice vztahuje, budou povinni odebírat takové výrobky zpět po skončení jejich životnosti.

MAGYAR

Az Európai Unió ("EU") 2005. augusztus 13-án hatályba lépő, az elektromos és elektronikus berendezések hulladékairól szóló 2002/96/EK irányelve szerint az elektromos és elektronikus berendezések többé nem kezelhetőek lakossági hulladékként, és az ilyen elektronikus berendezések gyártói kötelessé válnak az ilyen termékek visszavételére azok hasznos élettartama végén.

ITALIANO

In base alla Direttiva dell'Unione Europea (EU) sullo Smaltimento dei Materiali Elettrici ed Elettronici, Direttiva 2002/96/EC in vigore dal 13 Agosto 2005, prodotti appartenenti alla categoria dei Materiali Elettrici ed Elettronici non possono più essere eliminati come rifiuti municipali: i produttori di detti materiali saranno obbligati a ritirare ogni prodotto alla fine del suo ciclo di vita.

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Chapter 1
Overview

Thank you for choosing the MX255D, an excellent industrial computer board from BCM.

Based on the innovative **Intel® NM10** chipset for optimal system efficiency, the MX255D accommodates the **Intel® Cedarview-D** processor and supports up to 2 DDR3 1066MHz Unbuffered, Non-ECC SO-DIMM slots to provide the maximum of 4GB memory capacity.

In the advanced-level and mid-range market segment, the MX255D provides a high-performance solution for today's front-end and general purpose workstation, as well as in the future.

Mainboard Specifications

CPU	■ Intel Cedarview-D D2550 processor
Chipset	■ North Bridge: integrated with CPU ■ South Bridge: Intel NM10 chipset
Memory	■ 2 DDR3 1066MHz Unbuffered, non-ECC SO-DIMM slots, supporting the maximum of 4GB
LAN	■ 2 Intel 82574L GbE controllers
SATA	■ 2 SATA 3Gb/s ports by Intel NM10
Audio	■ HDA Codec by Realtek® ALC887 or ALC886 ■ Compliant with Azalia 1.0 specs ■ With amplifier
Graphics	■ Intel 3650 series / 3600 series integrated Graphics Engine ■ Resolution up to 1920 x 1200 pixels
CF	■ 1 CompactFlash socket by JMicron JMB368
Back Panel I/O	■ 1 DC power jack ■ 1 RS-232/422/485 serial port (COM1) ■ 1 RS-232 serial port (COM2) ■ 1 VGA port ■ 1 DVI-D port ■ 2 Gigabit LAN jacks ■ 4 USB 2.0 ports ■ 1 Line-In audio jack ■ 1 Line-Out audio jack ■ 1 Mic-In audio jack

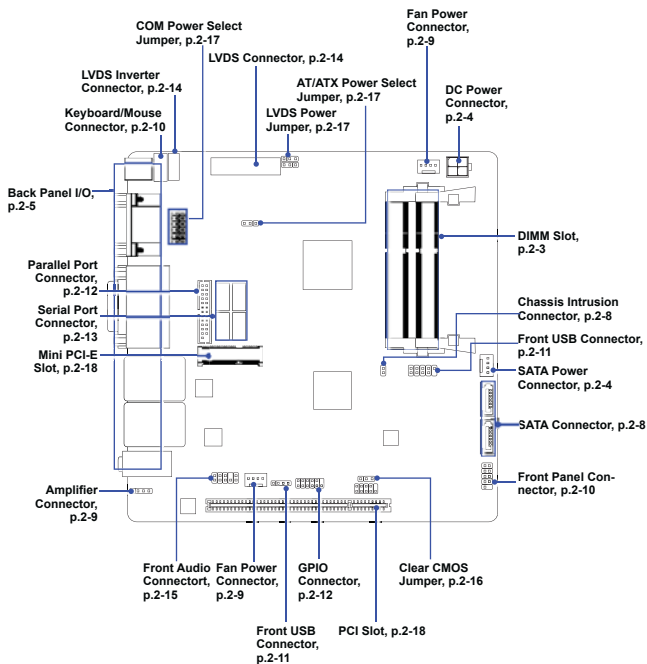| **Onboard Connectors/ Pinheaders**	■ 2 SATA 3Gb/s ports ■ 2 USB 2.0 pinheaders (3 ports) ■ 1 LVDS connector ■ 1 LVDS inverter connector ■ 4 serial port connectors ■ 6 serial port power select jumpers ■ 1 parallel port connector ■ 1 keyboard/mouse connector ■ 1 GPIO connector ■ 1 amplifier pinheader ■ 1 chassis intrusion pinheader ■ 1 front audio connector ■ 1 SPDIF out connector
Slot	■ 1 32-bit/33MHz PCI slot ■ 1 mini PCI-E slot ■ 1 CompactFlash socket
Form Factor	■ Mini-ITX: 170mm x 170mm

Environmental	■ Operating Temperature:
	   • A system fan is required for 45C to 60C
	   • For fanless solution: 0C to 45C
	■ Storage Temperature: -20°C to 80°C
	■ Humidity: 5% ~ 90% RH, Non-Condensing

Mainboard Layout
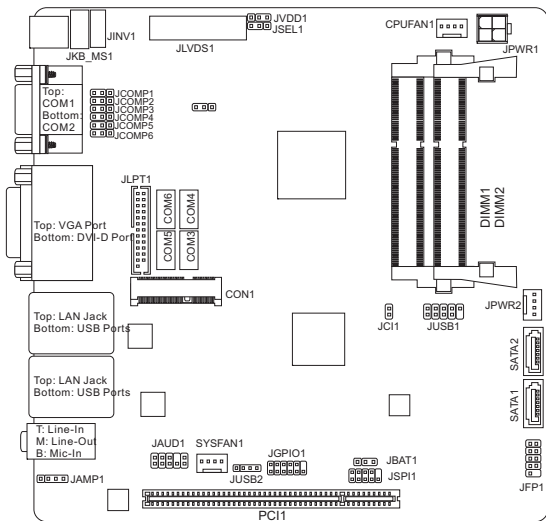
Chapter 2
Hardware Setup

This chapter provides you with the information on mainboard hardware configurations. Incorrect setting of jumpers and connectors may damage your mainboard. Please pay special attention not to connect these headers in wrong direction. DO NOT adjust any jumper while the mainboard is powered on.

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Memory

INSTALLING MEMORY MODULES

1. Locate the SO-DIMM slot. Align the notch on the DIMM with the key on the slot and insert the DIMM into the slot.

2. Push the DIMM gently downwards until the slot levers click and lock the DIMM in place.

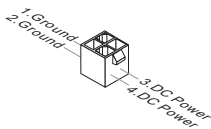3. To uninstall the DIMM, flip the slot levers outwards and the DIMM will be released instantly.

Important

You can barely see the golden finger if the memory module is properly inserted in the DIMM slot.

Power Supply

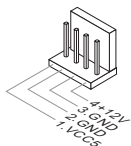### DC POWER CONNECTOR: JPWR1

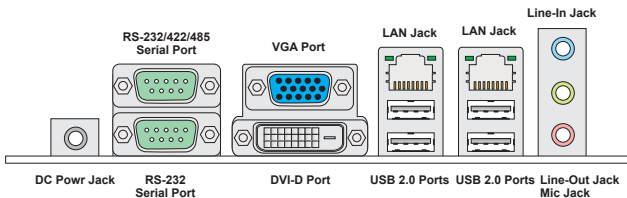This DC-In connector provides 12V power input.

1. Ground
2. Ground
3. DC Power
4. DC Power

SATA Power Connector: JPWR2

This DC-In connector provides DC power output for SATA devices.

4. +12V
3. GND
2. GND
1. VCC5

Back Panel I/O

RS-232/422/485 Serial Port · VGA Port · LAN Jack · LAN Jack · Line-In Jack

DC Powr Jack · RS-232 Serial Port · DVI-D Port · USB 2.0 Ports · USB 2.0 Ports · Line-Out Jack · Mic Jack

▶ **DC Power Jack**

▶ **COM1: RS-232/422/485 Serial Port**

The serial port is a 16550A high speed communications port that sends/ receives 16 bytes FIFOs. You can attach a serial mouse or other serial devices directly to the connector.

RS-232

PIN	SIGNAL	DESCRIPTION
1	DCD	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Signal Ground
6	DSR	Data Set Ready
7	RTS	Request To Send
8	CTS	Clear To Send
9	VCC_COM1	Voltage select setting by jumper

RS-422

PIN	SIGNAL	DESCRIPTION
1	422 TXD-	Transmit Data, Negative
2	422 RXD+	Receive Data, Positive
3	422 TXD+	Transmit Data, Positive
4	422 RXD-	Receive Data, Negative
5	GND	Signal Ground
6	NC	No Connection
7	NC	No Connection
8	NC	No Connection
9	NC	No Connection

RS-485

PIN	SIGNAL	DESCRIPTION
1	485 TXD-	Transmit Data, Negative
2	NC	No Connection
3	485 TXD+	Transmit Data, Positive
4	NC	No Connection
5	GND	Signal Ground
6	NC	No Connection
7	NC	No Connection
8	NC	No Connection
9	NC	No Connection

▶ **COM2: RS-232 Serial Port**

The serial port is a 16550A high speed communications port that sends/ receives 16 bytes FIFOs. You can attach a serial mouse or other serial devices directly to the connector.

▶ **VGA Port**

The DB15-pin female connector is provided for monitor.

▶ **DVI-D Port**

The DVI-D (Digital Visual Interface-Digital) connector allows you to connect an LCD monitor. It provides a high-speed digital interconnection between the computer and its display device. To connect an LCD monitor, simply plug your monitor cable into the DVI connector, and make sure that the other end

of the cable is properly connected to your monitor (refer to your monitor manual for more information.)

▶ **USB 2.0 Port**

The USB (Universal Serial Bus) port is for attaching USB devices such as keyboard, mouse, or other USB-compatible devices.

▶ **LAN Jack**

The standard RJ-45 LAN jack is for connection to the Local Area Network (LAN). You can connect a network cable to it.

Activity Indicator ─────── ┌─────┐ ─────── Speed Indicator

|		Left LED	Right LED
		Active LED	100M/1000M Speed LED
LED Color		Yellow	Green/Orange
10M Cable Plug-in	No Transmission	Yellow (Lighting)	OFF
	Transmission	Yellow (Blinking)	OFF
100M Cable Plug-in	No Transmission	Yellow (Lighting)	Green (Lighting)
	Transmission	Yellow (Blinking)	Green (Lighting)
1000M Cable Plug-in	No Transmission	Yellow (Lighting)	Orange (Lighting)
	Transmission	Yellow (Blinking)	Orange (Lighting)
In S3/S4/S5 Standby State		Yellow (Lighting)	OFF

▶ **Audio Jack**
  - **Line-In (Blue)** - for external CD player or other audio devices
  - **Line-Out (Green)** - for speakers or headphones
 - **Mic-In (Pink)** - for microphones

Connector

CHASSIS INTRUSION CONNECTOR: JCI1

This connector is provided to connect the chassis intrusion switch cable. If the chassis is opened, the chassis intrusion mechanism will be activated. The system will record this status and show a warning message on the screen. To clear the warning, you must enter the BIOS utility and clear the record.

2. Ground
1. CINTRU
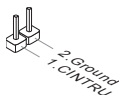
Serial ATA Connector: SATA1 ~ SATA2

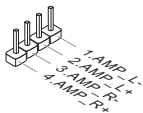This connector is a high-speed Serial ATA interface port. Each connector can connect one Serial ATA device.
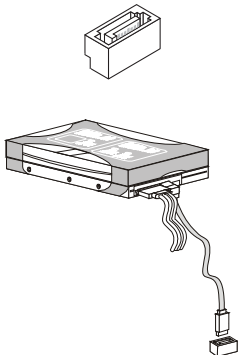
Important

*Please do not fold the Serial ATA cable into 90-degree angle. Otherwise,*

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AUDIO AMPLIFIER CONNECTOR: JAMP1

The JAMP1 is used to connect audio amplifiers to enhance audio performance.

1. AMP_L-
2. AMP_L+
3. AMP_R-
4. AMP_R+

Fan Power Connector: CPUFAN1, SYSFAN1

The fan power connector supports system cooling fan with +12V. When connecting the wire to the connectors, always note that the red wire is the positive and should be connected to the +12V; the black wire is Ground and should be connected to GND. If the mainboard has a System Hardware Monitor chipset onboard, you must use a specially designed fan with speed sensor to take advantage of the CPU fan control.
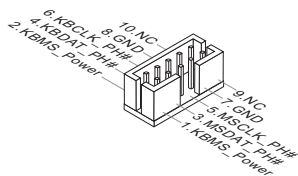
1. Ground
2. +12V
3. Sensor
4. Control
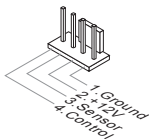
Important

- *Please refer to the recommended CPU fans at processor's official website or consult the vendors for proper CPU cooling fan.*

- *Fan cooler set with 3- or 4-pin power connector are both available for CPUFAN1.*
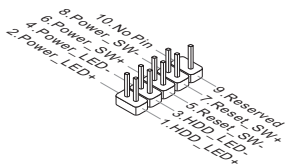
KEYBOARD/MOUSE CONNECTOR: JKB_MS1

This connector is used to connect PS/2 keyboard & mouse.

6. KBCLK_ PH#
8. GND
10. NC
4. KBDAT_ PH#
2. KBMS_ Power

9. NC
7. GND
5. MSCLK_ PH#
3. MSDAT_ PH#
1. KBMS_ Power

Front Panel Connector: JFP1

This front panel connector is provided for electrical connection to the front panel switches & LEDs and is compliant with Intel Front Panel I/O Connectivity Design Guide.

8. Power_ SW-
10. No Pin
6. Power_ SW+
4. Power_ LED-
2. Power_ LED+

9. Reserved
7. Reset_ SW+
5. Reset_ SW-
3. HDD_ LED-
1. HDD_ LED+

FRONT USB CONNECTOR: JUSB1, JUSB2

This connector, compliant with Intel I/O Connectivity Design Guide, is ideal for connecting high-speed USB interface peripherals such as USB HDD, digital cameras, MP3 players, printers, modems and the like.
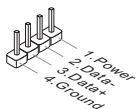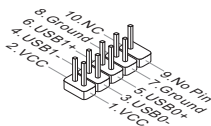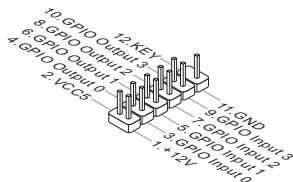

Important

Note that the pins of VCC and GND must be connected correctly to avoid possible damage.
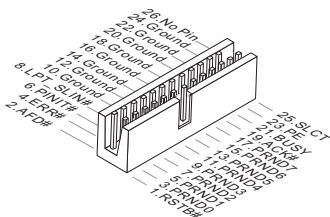
GPIO CONNECTOR: JGPIO1

This connector is provided for the General-Purpose Input/Output (GPIO) peripheral module.

```
10. GPIO Output 3    12. KEY
8. GPIO Output 2
6. GPIO Output 1         11. GND
4. GPIO Output 0         9. GPIO Input 3
2. VCC5                  7. GPIO Input 2
                         5. GPIO Input 1
           1. +12V       3. GPIO Input 0
```

Parallel Port Connector: JLPT1

The mainboard provides a 26-pin header for connection to an optional parallel port bracket. The parallel port is a standard printer port that supports Enhanced Parallel Port (EPP) and Extended Capabilities Parallel Port (ECP) mode.

```
26. No Pin
24. Ground
22. Ground
20. Ground
18. Ground
16. Ground
14. Ground
12. Ground        25. SLCT
10. LPT SLIN#     23. PE
8. LPT SLIN#      21. BUSY
6. ERR#           19. ACK#
4. PINT#          17. PRND7
2. AFD#           15. PRND6
                  13. PRND5
                  11. PRND4
                  9. PRND3
                  7. PRND2
                  5. PRND1
                  3. PRND0
                  1. RSTB#
```

RS-232 SERIAL PORT CONNECTOR: COM3, COM4, COM5, COM6

This connector is a 16550A high speed communications port that sends/receives 16 bytes FIFOs. You can attach a serial device to it through an optional serial port bracket.
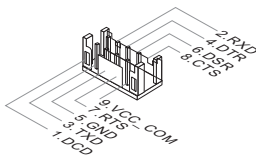
PIN	SIGNAL	DESCRIPTION
1	DCD	Data Carrier Detect
2	RXD	Receive Data
3	TXD	Transmit Data
4	DTR	Data Terminal Ready
5	GND	Signal Ground
6	DSR	Data Set Ready
7	RTS	Request To Send
8	CTS	Clear To Send
9	VCC_COM	12V or 5V power output, selected by JCOMP

LVDS Connector: JLVDS1

The LVDS (Low Voltage Differential Signal) connector provides a digital interface typically used with flat panels. After connecting an LVDS interface flat panel to the JLVDS1, be sure to check the panel datasheet and set the JVDD1 jumper to proper power voltage.
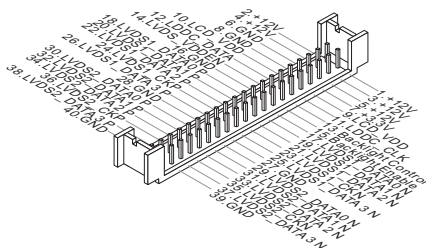
LCD Inverter Connector: JINV1

The connector is provided for LCD backlight options.
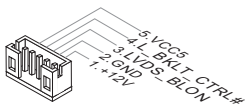
FRONT AUDIO CONNECTOR: JAUD1

This connector allows you to connect the front panel audio and is compliant with Intel® Front Panel I/O Connectivity Design Guide.

Jumper

CLEAR CMOS JUMPER: JBAT1
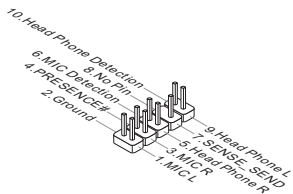
There is a CMOS RAM onboard that has a power supply from an external battery to keep the data of system configuration. With the CMOS RAM, the system can automatically boot OS every time it is turned on. If you want to clear the system configuration, set the jumper to clear data.

1 ▢▢ ▢	1 ▢▢ ▢	1 ▢ ▢▢
JBAT1	Normal	Clear CMOS

Important

You can clear CMOS by shorting 2-3 pin while the system is off. Then return to 1-2 pin position. Avoid clearing the CMOS while the system is on; it will damage the mainboard.

COM POWER SELECT JUMPER: JCOMP1 ~ JCOMP6

These jumpers are used to select the pin 9 power voltage of the COM1 ~ COM6 serial ports.

JCOMP1~6   +5V   +12V

LVDS Power Jumper: JVDD1

The LVDS power jumper allows users to select the operation voltage of the LVDS flat panel.

JVDD1   3V   5V

AT/ATX Select Jumper: J1

This jumper allows users to select between AT and ATX power.

J1   AT   ATX
(Default)

Slot

MINI PCI-E (PERIPHERAL COMPONENT INTERCONNECT EXPRESS) SLOT

The Mini PCI-E slot is provided for wireless LAN card, TV tuner card, and Robson NAND Flash card.

PCI (PERIPHERAL COMPONENT INTERCONNECT) SLOT

The PCI slot supports LAN card, SCSI card, USB card, and other add-on

COMPACTFLASH SOCKET

This socket supports CompactFlash cards.
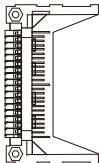
Important

When adding or removing expansion cards, make sure that you unplug the power supply first. Meanwhile, read the documentation for the expansion card to configure any necessary hardware or software settings for the expansion card, such as jumpers, switches or BIOS configuration.

Chapter 3
BIOS Setup

This chapter provides information on the BIOS Setup program and allows you to configure the system for optimum use.

You may need to run the Setup program when:

- An error message appears on the screen during the system booting up, and requests you to run SETUP.
- You want to change the default settings for customized features.

Entering Setup

Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <DEL> key to enter Setup.

PRESS DEL TO ENTER SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system by turning it OFF and On or pressing the RESET button. You may also restart the system by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys.

CONTROL KEYS

← →	Select Screen
↑↓	Select Item
+ -	Change Field
Tab	Select Field
F1	General Help
F10	Save and Exit
Esc	Exit

GETTING HELP

After entering the Setup menu, the first menu you will see is the Main Menu.

Main Menu

The main menu lists the setup functions you can make changes to. You can use the arrow keys (↑↓) to select the item. The on-line description of the highlighted setup function is displayed at the bottom of the screen.

Sub-Menu

If you find a right pointer symbol ▶ appears to the left of certain fields that means a sub-menu can be launched from this field. A sub-menu contains additional options for a field parameter. You can use arrow keys (↑↓) to highlight the field and press <Enter> to call up the sub-menu. Then you can use the control keys to enter values and move from field to field within a sub-menu. If you want to return to the main menu, just press the <Esc >.

GENERAL HELP <F1>

The BIOS setup program provides a General Help screen. You can call up this screen from any menu by simply pressing <F1>. The Help screen lists the appropriate keys to use and the possible selections for the highlighted item. Press <Esc> to exit the Help screen.

The Menu Bar
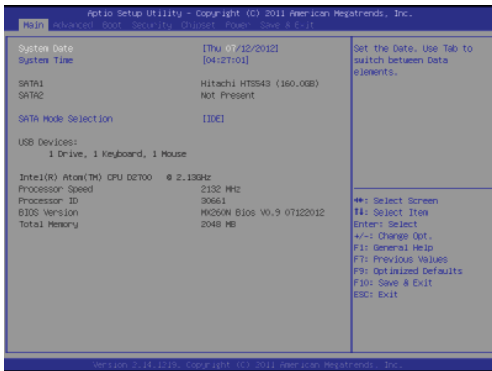
▶ **Main**

Use this menu for basic system configurations, such as time, date etc.

▶ **Advanced**

Use this menu to set up the items of special enhanced features.

▶ **Boot**

Use this menu to specify the priority of boot devices.

▶ **Security**

Use this menu to set supervisor and user passwords.

▶ **Chipset**

This menu controls the advanced features of the onboard Northbridge and Southbridge.

▶ **Power**

Use this menu to specify your settings for power management.

▶ **Exit**

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.

Main
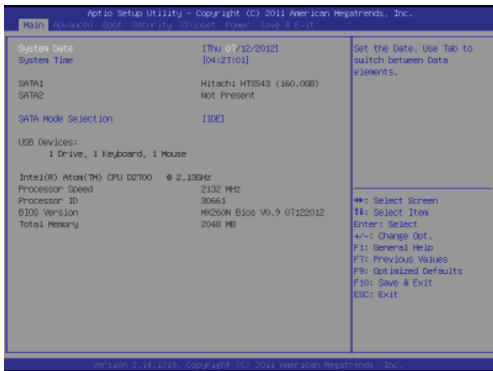
▶ **System Time**

This setting allows you to set the system time. The time format is <Hour> <Minute> <Second>.

▶ **System Date**

This setting allows you to set the system date. The date format is <Day>, <Month> <Date> <Year>.

▶ **SATA1, SATA2**

[Type]	Press PgUp/<+> or PgDn/<-> to select [Manual], [None] or [Auto] type. Note that the specifications of your drive must match with the drive table. The hard disk will not work properly if you enter improper information for this category. If your hard disk drive type is not matched or listed, you can use [Manual] to define your own drive type manually.

| [LBA/Large Mode]	Enabling LBA causes Logical Block Addressing to be used in place of Cylinders, Heads and Sectors
[Block (Multi-Sector Transfer)]	Any selection except Disabled determines the number of sectors transferred per block
[PIO Mode]	Indicates the type of PIO (Programmed Input/Output)
[DMA Mode]	Indicates the type of Ultra DMA
[S.M.A.R.T.]	This allows you to activate the S.M.A.R.T. (Self-Monitoring Analysis & Reporting Technology) capability for the hard disks. S.M.A.R.T is a utility that monitors your disk status to predict hard disk failure. This gives you an opportunity to move data from a hard disk that is going to fail to a safe place before the hard disk becomes offline.
[32 Bit Data Transfer]	Enables 32-bit communication between CPU and IDE controller

▶ **SATA Mode Selection**

This setting specifies the SATA controller mode.

Advanced
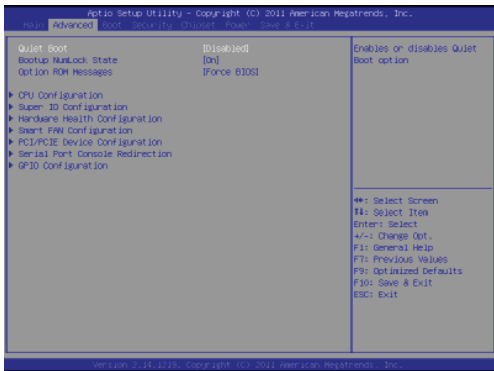
▸ **Quick Boot**

Enabling this setting will cause the BIOS power-on self test routine to skip some of its tests during bootup for faster system boot.

▸ **Bootup Num-Lock**

This setting is to set the Num Lock status when the system is powered on. Setting to [On] will turn on the Num Lock key when the system is powered on. Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

▸ **Option ROM Messages**

This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

‣ **CPU Configuration**
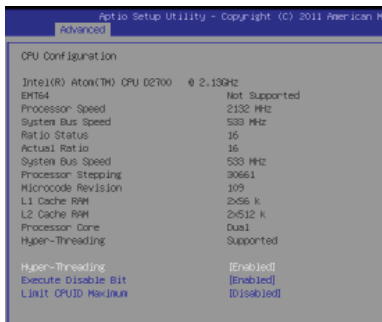
‣ **Hyper-Threading**

The processor uses Hyper-Threading technology to increase transaction rates and reduces end-user response times. The technology treats the two cores inside the processor as two logical processors that can execute instructions simultaneously. In this way, the system performance is highly improved. If you disable the function, the processor will use only one core to execute the instructions. Please disable this item if your operating system doesn't support HT Function, or unreliability and instability may occur.

‣ **Execute Disable Bit**

Intel's Execute Disable Bit functionality can prevent certain classes of malicious "buffer overflow" attacks when combined with a supporting operating system. This functionality allows the processor to classify areas in memory by where application code can execute and where it cannot. When a malicious worm attempts to insert code in the buffer, the processor disables code execution, preventing damage or worm propagation.

‣ **Limit CPUID Maximum**

The Max CPUID Value Limit BIOS feature allows you to circumvent problems with older operating systems that do not support the Intel Pentium 4 processor with Hyper-Threading Technology. When enabled, the processor will limit the maximum CPUID input value to 03h when queried, even if the processor supports a higher CPUID input value.

When disabled, the processor will return the actual maximum CPUID input value of the processor when queried.

▶ **Super IO Configuration**

▶ **Serial Port 1/ 2/ 3/ 4/ 5/ 6/ Parallel Port Address**

Select an address for the specified serial/parallel port.

▶ **Change Settings Serial Port 1/ 2/ 3/ 4/ 5/ 6 /Parallel Port**

This setting is used to change the address & IRQ settings of the specified serial port.

▶ **Mode Select**

Select an operation mode for the serial port 1.

▶ **Watch Dog**

You can enable the system watch-dog timer, a hardware timer that generates a reset when the software that it monitors does not respond as expected each time the watch dog polls it.

▸ **Hardware Health Configuration**

These items display the current status of all monitored hardware devices/components such as voltages, temperatures and all fans' speeds.
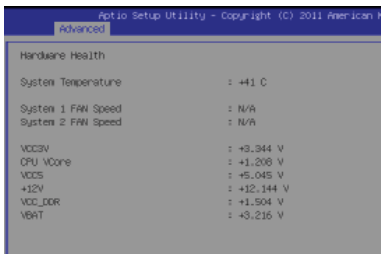
▸ **Smart Fan Configuration**
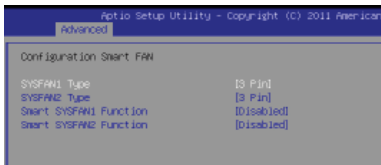
▸ **SYSFAN1 / 2 Type**

This setting specifies the fan type.

▸ **Smart SYSFAN1 / 2 Function**

This setting enables/disables the Smart Fan function. Smart Fan is an excellent feature which will adjust the CPU/system fan speed automatically depending on the current CPU/system temperature, avoiding the overheating to damage your system.

▸ **PCI/PCIE Device Configuration**
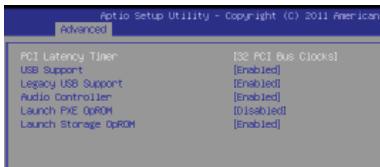
▸ **PCI Latency Timer**

This item controls how long each PCI device can hold the bus before another takes over. When set to higher values, every PCI device can conduct transactions for a longer time and thus improve the effective PCI bandwidth. For better PCI performance, you should set the item to higher values.

▸ **USB Support**

This setting enables/disables the onboard USB controller.

▸ **Legacy USB Support**

Set to [Enabled] if you need to use any USB 1.1/2.0 device in the operating system that does not support or have any USB 1.1/2.0 driver installed, such as DOS and SCO Unix.

▸ **Audio Controller**

This setting enables/disables the onboard audio controller.

▸ **Launch PXE OpROM / Launch Storage OpROM**

This setting enables/disables the initialization of the onboard LAN Boot ROM during bootup. Selecting [Disabled] will speed up the boot process.

▸ **Console Redirection**

▸ **Console Redirection Settings**

Console Redirection operates in host systems that do not have a monitor and keyboard attached. This setting enables/disables the operation of console redirection. When set to [Enabled], BIOS redirects and sends all contents that should be displayed on the screen to the serial COM port for display on the terminal screen. Besides, all data received from the serial port is interpreted as keystrokes from a local keyboard.

▸ **GPIO Configuration**
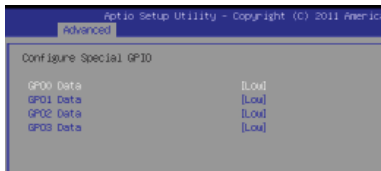
▸ **GPO 1/2/3/4 Data**

This setting specifies the GPO data.
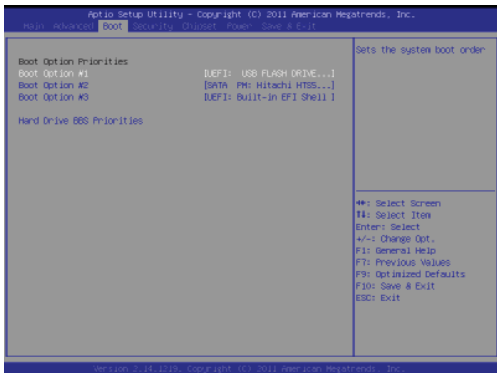
Boot

▶ **Boot Option #1 / 2 / 3**

This setting allows users to set the sequence of boot devices where BIOS attempts to load the disk operating system.

▶ **Hard Drive BBS Priorities**

This setting allows users to set the priority of the specified devices. First press <Enter> to enter the sub-menu. Then you may use the arrow keys (↑ ↓) to select the desired device, then press <+>, <-> or <PageUp>, <Page-Down> key to move it up/down in the priority list.

Security

▶ **Administrator Password**

Administrator Password controls access to the BIOS Setup utility.

▶ **User Password**

User Password controls access to the system at boot and to the BIOS Setup utility.

▶ **Chassis Intrusion**

The field enables or disables the feature of recording the chassis intrusion status and issuing a warning message if the chassis is once opened. To clear the warning message, set the field to [Reset]. The setting of the field will automatically return to the default value later.

▸ **Trusted Computing**

▸ **TCG/TPM Support**

This setting controls the Trusted Platform Module (TPM) designed by the Trusted Computing Group (TCG). TPMs are special-purpose integrated circuits (ICs) built into a variety of platforms to enable strong user authentication and machine attestation - essential to prevent inappropriate access to confidential and sensitive information and to protect against compromised networks.

Chipset

▶ **IGFX - Boot Type**

Use the field to select the type of device you want to use as the boot display of the system.

▶ **DP Panel Type**

This setting allows you to set your preferences for the boot display device.

▶ **Fixed Graphics Memory Size**

This setting specifies the size of system memory allocated for video memory.

Power
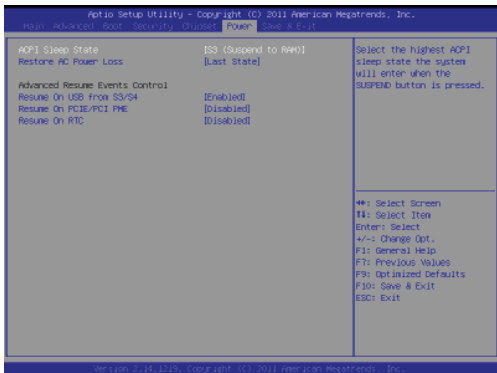
▶ **ACPI Sleep State**

This item specifies the power saving modes for ACPI function. If your operating system supports ACPI, you can choose to enter the Standby mode in S1 (POS) or S3 (STR) fashion through the setting of this field.

▶ **Restore on AC Power Loss**

This setting specifies whether your system will reboot after a power failure or interrupt occurs. Available settings are:

[Power Off]	Leaves the computer in the power off state.
[Power On]	Leaves the computer in the power on state.
[Last State]	Restores the system to the previous status before power failure or interrupt occurred.

▶ **Resume On USB from S3/S4**

The item allows the activity of the USB device to wake up the system from S3/S4 sleep state.

▶ **Resume On PCIE/PCI PME**

This field specifies whether the system will be awakened from power saving modes when activity or input signal of onboard PCIE/PCI PME is detected.This field specifies whether the system will be awakened from power saving modes when activity or input signal of onboard LAN/mini PCI-E is detected.

▶ **Resume On RTC Alarm**

When [Enabled], your can set the date and time at which the RTC (real-time clock) alarm awakens the system from suspend mode.

Exit

▸ **Save Changes and Exit**
Save changes to CMOS and exit the Setup Utility.

▸ **Discard Changes and Exit**
Abandon all changes and exit the Setup Utility.

▸ **Restore Defaults**
Restore the factory defaults.

▸ **Save as User Defaults**
Save all changes as user defaults.

▸ **Restore User Defaults**
Restore the preset user defaults.
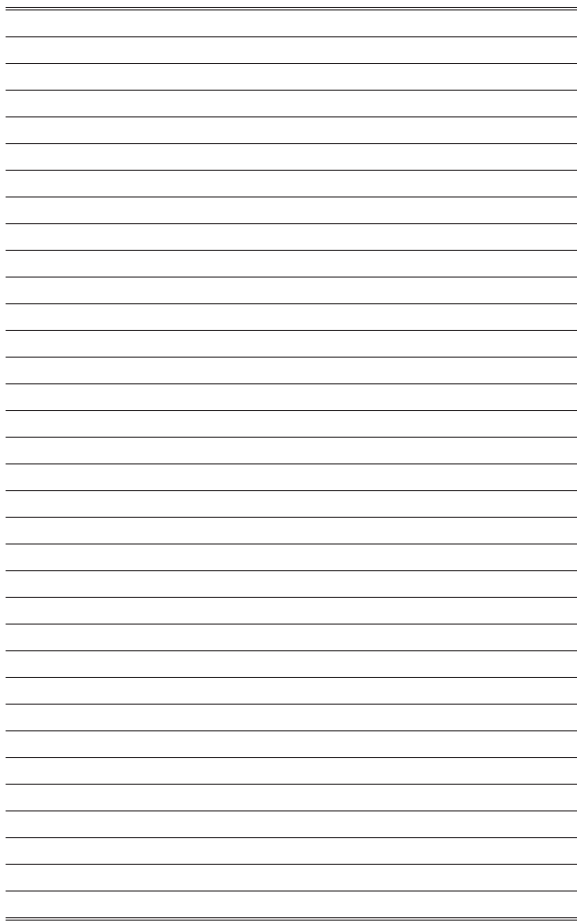
Chapter 4
System Resources

This chapter provides information on system resources.

AMI POST Code

Bootblock Initialization Code Checkpoints

The Bootblock initialization code sets up the chipset, memory and other components before system memory is available. The following table describes the type of checkpoints that may occur during the bootblock initialization portion of the BIOS:

Checkpoint	Description
Before D1	Early chipset initialization is done. Early super I/O initialization is done including RTC and keyboard controller. NMI is disabled.
D1	Perform keyboard controller BAT test. Check if waking up from power management suspend state. Save power-on CPUID value in scratch CMOS.
D0	Go to flat mode with 4GB limit and GA20 enabled. Verify the bootblock checksum.
D2	Disable CACHE before memory detection. Execute full memory sizing module. Verify that flat mode is enabled.
D3	If memory sizing module not executed, start memory refresh and do memory sizing in Bootblock code. Do additional chipset initialization. Re-enable CACHE. Verify that flat mode is enabled.
D4	Test base 512KB memory. Adjust policies and cache first 8MB. Set stack.
D5	Bootblock code is copied from ROM to lower system memory and control is given to it. BIOS now executes out of RAM.
D6	Both key sequence and OEM specific method is checked to determine if BIOS recovery is forced. Main BIOS checksum is tested. If BIOS recovery is necessary, control flows to checkpoint E0. See Bootblock Recovery Code Checkpoints section of document for more information.
D7	Restore CPUID value back into register. The Bootblock-Runtime interface module is moved to system memory and control is given to it. Determine whether to execute serial flash.
D8	The Runtime module is uncompressed into memory. CPUID information is stored in memory.
D9	Store the Uncompressed pointer for future use in PMM. Copying Main BIOS into memory. Leaves all RAM below 1MB Read-Write including E000 and F000 shadow areas but closing SMRAM.

POST Code Checkpoints

The POST code checkpoints are the largest set of checkpoints during the BIOS pre-boot process. The following table describes the type of checkpoints that may occur during the POST portion of the BIOS:

Checkpoint	Description
03	Disable NMI, Parity, video for EGA, and DMA controllers. Initialize BIOS, POST, Runtime data area. Also initialize BIOS modules on POST entry and GPNV area. Initialized CMOS as mentioned in the Kernel Variable "wCMOSFlags."
04	Check CMOS diagnostic byte to determine if battery power is OK and CMOS checksum is OK. Verify CMOS checksum manually by reading storage area. If the CMOS checksum is bad, update CMOS with power-on default values and clear passwords. Initialize status register A. Initializes data variables that are based on CMOS setup questions. Initializes both the 8259 compatible PICs in the system
05	Initializes the interrupt controlling hardware (generally PIC) and interrupt vector table.
06	Do R/W test to CH-2 count reg. Initialize CH-0 as system timer. Install the POSTINT1Ch handler. Enable IRQ-0 in PIC for system timer interrupt. Traps INT1Ch vector to "POSTINT1ChHandlerBlock."
08	Initializes the CPU. The BAT test is being done on KBC. Program the keyboard controller command byte is being done after Auto detection of KB/MS using AMI KB-5.
0A	Initializes the 8042 compatible Key Board Controller.
0B	Detects the presence of PS/2 mouse.
0C	Detects the presence of Keyboard in KBC port.
0E	Testing and initialization of different Input Devices. Also, update the Kernel Variables. Traps the INT09h vector, so that the POST INT09h handler gets control for IRQ1. Uncompress all available language, BIOS logo, and Silent logo modules.

Checkpoint	Description
13	Early POST initialization of chipset registers.
24	Uncompress and initialize any platform specific BIOS modules.
30	Initialize System Management Interrupt.
2A	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
2C	Initializes different devices. Detects and initializes the video adapter installed in the system that have optional ROMs.
2E	Initializes all the output devices.
31	Allocate memory for ADM module and uncompress it. Give control to ADM module for initialization. Initialize language and font modules for ADM. Activate ADM module.
33	Initializes the silent boot module. Set the window for displaying text information.
37	Displaying sign-on message, CPU information, setup key message, and any OEM specific information.
38	Initializes different devices through DIM. See DIM Code Checkpoints section of document for more information.
39	Initializes DMAC-1 & DMAC-2.
3A	Initialize RTC date/time.
3B	Test for total memory installed in the system. Also, Check for DEL or ESC keys to limit memory test. Display total memory in the system.
3C	Mid POST initialization of chipset registers.
40	Detect different devices (Parallel ports, serial ports, and coprocessor in CPU, … etc.) successfully installed in the system and update the BDA, EBDA…etc.
50	Programming the memory hole or any kind of implementation that needs an adjustment in system RAM size if needed.
52	Updates CMOS memory size from memory found in memory test. Allocates memory for Extended BIOS Data Area from base memory.
60	Initializes NUM-LOCK status and programs the KBD typematic rate.
75	Initialize Int-13 and prepare for IPL detection.
78	Initializes IPL devices controlled by BIOS and option ROMs.
7A	Initializes remaining option ROMs.
7C	Generate and write contents of ESCD in NVRam.

Checkpoint	Description
84	Log errors encountered during POST.
85	Display errors to the user and gets the user response for error.
87	Execute BIOS setup if needed / requested.
8C	Late POST initialization of chipset registers.
8E	Program the peripheral parameters. Enable/Disable NMI as selected
90	Late POST initialization of system management interrupt.
A0	Check boot password if installed.
A1	Clean-up work needed before booting to OS.
A2	Takes care of runtime image preparation for different BIOS modules. Fill the free area in F000h segment with 0FFh. Initializes the Microsoft IRQ Routing Table. Prepares the runtime language module. Disables the system configuration display if needed.
A4	Initialize runtime language module.
A7	Displays the system configuration screen if enabled. Initialize the CPU's before boot, which includes the programming of the MTRR's.
A8	Prepare CPU for OS boot including final MTRR values.
A9	Wait for user input at config display if needed.
AA	Uninstall POST INT1Ch vector and INT09h vector. Deinitializes the ADM module.
AB	Prepare BBS for Int 19 boot.
AC	End of POST initialization of chipset registers.
B1	Save system context for ACPI.
00	Passes control to OS Loader (typically INT19h).

Resource List

ICH8M GPIO

GPIO	Alt Func	Pin	I/O/NC	Power	Tol	Default	Rickles Signal Name
GPIO[0]	BMBUSY#	AG12	I/O	VCC3p3	3.3	GPI	NC
GPIO[1]	TACH1	AJ8	I/O	VCC3p3	3.3	GPI	NC
GPIO[2]	PIRQE#	F8	I/OD	VCC5	5	GPI	RS232_EN_1
GPIO[3]	PIRQF#	G11	I/OD	VCC5	5	GPI	RS422_EN#_1
GPIO[4]	PIRQG#	F12	I/OD	VCC5	5	GPI	RS485_EN#_1
GPIO[5]	PIRQH#	B3	I/OD	VCC5	5	GPI	AUXGPO_OE#
GPIO[6]	TACH2	AJ9	I/O	VCC3p3	3.3	GPI	NC
GPIO[7]	TACH3	AH9	I/O	VCC3p3	3.3	GPI	NC
GPIO[8]	unmuxed	AE16	I/O	VccSus3p3	3.3	GPI	SIO_PME#
GPIO[9]	WOL_EN	AG19	I/O	VccSus3p3	3.3	GPI	NC
GPIO[10]	ALERT#	AJ24	I/O	VccSus3p3	3.3	GPI	MPCIE1_PWRON
GPIO[11]	SMBALERT#	AG22	I/O	VccSus3p3	3.3	Native	AMP_DISABLE#
GPIO[12]	ENERGY_DETECT	AC19	I/O	VccSus3p3	3.3	Native	NC
GPIO[13]	GLAN_DOCK#	AH21	I/O	VccSus3p3	3.3	Native	NC
GPIO[14]	AC_PRESENT	AF22	I/O	VccSus3p3	3.3	GPI	LAN_DISABLE_N
GPIO[15]	STP_PCI#	AE20	I/O	VccSus3p3	3.3	Native	PM_STP_PCI#
GPIO[16]	DPRSLPVR	AJ14	I/O	VCC3p3	3.3	Native	DPRSLPVR_SB_GPIO16
GPIO[17]	TACH0	AG8	I/O	VCC3p3	3.3	GPI	SPI_WP#
GPIO[18]	UNMUXED	AH12	I/O	VCC3p3	3.3	GPO	NC
GPIO[19]	SATA1GP	AJ10	I/O	VCC3p3	3.3	GPI	SATA1GP_SB_GPIO19
GPIO[20]	unmuxed	AE11	I/O	VCC3p3	3.3	GPO	SPI_HOLD_GPIO20#
GPIO[21]	SATA0GP	AJ12	I/O	VCC3p3	3.3	GPI	SATA0GP_SB_GPIO21
GPIO[22]	SCLOCK	AG10	I/O	VCC3p3	3.3	GPI	NC
GPIO[23]	LDRQ1#	E6	I/O	VCC3p3	3.3	Native	PRES3
GPIO[24]	MEM_LED	AJ27	I/O	VccSus3p3	3.3	GPO	USB_EN#
GPIO[25]	STP_CPU#	AG18	I/O	VccSus3p3	3.3	Native	PM_STP_CPU#
GPIO[26]	S4_STATE	AH27	I/O	VccSus3p3	3.3	GPI	NC
GPIO[27]	unmuxed	AH25	I/O	VccSus3p3	3.3	GPO	CPUFAN_SET#
GPIO[28]	unmuxed	AD16	I/O	VccSus3p3	3.3	GPO	SYSFAN_SET#
GPIO[29]	OC#5	AG17	I/O	VccSus3p3	3.3	Native	USB_OC#4
GPIO[30]	OC#6	AD12	I/O	VccSus3p3	3.3	Native	USB_OC#6
GPIO[31]	OC#7	AJ18	I/O	VccSus3p3	3.3	Native	USB_OC#6
GPIO[32]	CLKRUN#	AH11	I/O	VCC3p3	3.3	GPO	P_CLKRUN#
GPIO[33]	HDA_DOCK_EN#	AE10	I/O	VCC3p3	3.3	GPO	PRES1
GPIO[34]	HDA_DOCK_RST#	AG14	I/O	VCC3p3	3.3	GPO	PRES2
GPIO[35]	SATACLKREQ#	AG13	I/O	VCC3p3	3.3	GPO	NC
GPIO[36]	SATA2GP	AF11	I/O	VCC3p3	3.3	GPI	SATA2GP_SB_GPIO36
GPIO[37]	unmuxed	AG11	I/O	VCC3p3	3.3	GPI	SATA3GP_SB_GPIO37
GPIO[38]	SLOAD	AF9	I/O	VCC3p3	3.3	GPI	ATADET0
GPIO[39]	SDATAOUT0	AJ11	I/O	VCC3p3	3.3	GPI	NC
GPIO[40]	OC1#	AG16	I/O	VccSus3p3	3.3	Native	USB_OC#0
GPIO[41]	OC2#	AG15	I/O	VccSus3p3	3.3	Native	USB_OC#2
GPIO[42]	OC3#	AE15	I/O	VccSus3p3	3.3	Native	USB_OC#4
GPIO[43]	OC4#	AF15	I/O	VccSus3p3	3.3	Native	USB_OC#4
GPIO[44]	NA	NA	NA	NA	NA	NA	NA
GPIO[45]	NA	NA	NA	NA	NA	NA	NA
GPIO[46]	NA	NA	NA	NA	NA	NA	NA
GPIO[47]	NA	NA	NA	NA	NA	NA	NA
GPIO[48]	SDATAOUT1	AD10	I/O	VCC3p3	3.3	GPI	NC
GPIO[49]	CPUPWRGD	AG29	I/O	V_FSB_VTT	VTT	Native	H_PWRGD
GPIO[50]	REQ1#	E18	I/O	VCC3p3	3.3	Native	NC
GPIO[51]	GNT1	C18	I/O	VCC3p3	3.3	Native	NC
GPIO[52]	REQ2#	B19	I/O	VCC3p3	3.3	Native	NC
GPIO[53]	GNT2	F18	I/O	VCC3p3	3.3	Native	NC
GPIO[54]	REQ3#	A11	I/O	VCC3p3	3.3	Native	NC
GPIO[55]	GNT3	C10	I/O	VCC3p3	3.3	Native	NC

SIO GPIO

GPIO	Alt Func	PIN	Usage	Input/Output	NOTES
GPIO00	GPIO00/SPI_CLK	52	AUX_GPIO0	INPUT	GPIO Input
GPIO01	GPIO01/SPI_CS0#	53	AUX_GPIO1	INPUT	GPIO Input
GPIO02	GPIO02/SPI_MISO	54	AUX_GPIO2	INPUT	GPIO Input
GPIO03	GPIO03/SPI_MOSI	55	AUX_GPIO3	INPUT	GPIO Input
GPIO04	GPIO04/SPI_CSI	56	AUX_GPIO4	OUTPUT	GPIO Output
GPIO05	GPIO05/SOUT6	57	SOUT6		
GPIO06	GPIO06/SIN6	58	SIN6		
GPIO07	GPIO07/RTS6	59	RTS6#		
GPIO10	GPIO10/LED_VSB	65	LED_VSB		
GPIO11	GPIO11/LED_VCC	66	LED_VCC		
GPIO12	GPIO12/SOUT5	67	SOUT5		
GPIO13	GPIO13/SIN5	68	SIN5		
GPIO14	GPIO14/RTS5	69	RTS5		
GPIO15	GPIO15/WDTRST#	70	WDT#		
GPIO16	GPIO16/BEEP	71	BEEP		
GPIO17	GPIO17/PECI	72	H_DPRSTP#		
GPIO20	GPIO20/ALERT#	76	AUXGPI_OE#	OUTPUT	GPIO intput enable default:1
GPIO21	GPIO21/ATXPG_IN	77	ATX_PWR_OK		
GPIO22	GPIO22/PWSIN#	78	PWRBTIN		
GPIO23	GPIO23/PWSOUT#	79	PSOUT#		
GPIO24	GPIO24/S3#	80	SLP_S3#		
GPIO25	GPIO25/PS_ON#	81	PS_ON#		
GPIO26	GPIO26/PWOK	82	PWRGD_PS		
GPIO27	GPIO27/RSMRST#	83	RSMRST#		
GPIO30	GPIO30/DCD3#	36	DCD3#		
GPIO31	GPIO31/RI3#	37	RI3#		
GPIO32	GPIO32/CTS3#	38	CTS3#		
GPIO33	GPIO33/DTR3#	39	DTR3#		
GPIO34	GPIO34/RTS3#	40	RTS3#		
GPIO35	GPIO35/DSR3#	41	DSR3#		
GPIO36	GPIO36/SOUT3	42	SOUT3		
GPIO37	GPIO37/SIN3	43	SIN3		
GPIO40	GPIO40/DCD4#	44	DCD4#		
GPIO41	GPIO41/RI4#	45	RI4#		
GPIO42	GPIO42/CTS4#	46	CTS4#		
GPIO43	GPIO43/DTR4#	47	DTR4#		
GPIO44	GPIO44/RTS4#	48	RTS4#		
GPIO45	GPIO45/DSR4#	49	DSR4#		
GPIO46	GPIO46/SOUT4	50	SOUT4		
GPIO47	GPIO47/SIN4	51	SIN4		
GPIO50	GPIO50	9	AUX_GPIO5	OUTPUT	GPIO Output
GPIO51	GPIO51	10	AUX_GPIO6	OUTPUT	GPIO Output
GPIO52	GPIO52	11	AUX_GPIO7	OUTPUT	GPIO Output
GPIO53	GPIO53/DCD6#	12	DCD6#		
GPIO54	GPIO54/RI6#	13	RI6#		
GPIO55	GPIO55/CTS6#	14	CTS6#		
GPIO56	GPIO56/DTR6#	15	DTR6#		
GPIO57	GPIO57/DSR6#	557	DSR6#		
GPIO60	GPIO60/DCD5#	17	DCD5#		
GPIO61	GPIO61/RI5#	18	RI5#		
GPIO62	GPIO62/CTS5#	19	CTS5#		
GPIO63	GPIO62/DTR5#	20	DTR5#		

GPIO Programming

Please refer to the "F81865 Super IO spec" for the GPIO pin function:

"Pin3-GPI00"	Status:addr F2 bit0
"Pin4-GPO04"	Status:addr F2 bit4, Setting:addr F1 bit4
"Pin5-GPI01"	Status:addr F2 bit1
"Pin6-GPO50"	Status:addr A2 bit0, Setting:addr A1 bit0
"Pin7-GPI02"	Status:addr F2 bit2
"Pin8-GPO51"	Status:addr A2 bit1, Setting:addr A1 bit1
"Pin9-GPI03"	Status:addr F2 bit3
"Pin10-GPO52"	Status:addr A2 bit2, Setting:addr A1 bit2

Note: GPIO pin connection design with 4 input and 4 output pins.
      GPI is design for input, GPO is design for output

Example 1: Read data from GPIO "Pin3-GPI00",
          // the "Pin3-GPI00" status value is at address F2 bit 0,

Step 1. Enable SIO configuration mode without timeout in between commands
        Out(0x4e, 0x87); // (port, value), 0x4e for index
        Out(0x4e, 0x87);

Step 2. Select LDN06 (GPIO) (LDN: Logic device number)
        Out(0x4e, 0x07); // select entry page, 0x4e for index
        Out(0x4f, 0x06); // select LDN06, 0x4f for data

Step 3. Set address to 0xF2
        Out(0x4e, 0xF2); // 0x4e for index

Step 4. Get input data from port 0x4f
        if (Inp(0x4f) & 0x01) !=0) // 0x4f for data, & 0x01 for bit0 of GPI00 input data
        value = "high";
        else
        value = "low";

Example 2: Set GPIO "Pin4-GPO04" output to "high",
      // the "Pin4-GPO04" output setting is at address F1 bit 4,

Step 1. Enable SIO configuration mode without timeout in between commands
      Out(0x4e, 0x87); // (port, value), 0x4e for index
      Out(0x4e, 0x87);

Step 2. Select LDN06 (GPIO) (LDN: Logic device number)
      Out(0x4e, 0x07); // select entry page, 0x4e for index
      Out(0x4f, 0x06); // select LDN06,   0x4f for data

Step 3. Set address to 0xF1
      Out(0x4e, 0xF1); //0x4e for index

Step 4. Get data from port 0x4f (Save current state)
      Byte tmp = Inp(0x4f); //Read current data for adding the output in bit4

Step 5. Write data to port 0x4f (only set bit 4 to "high" and write back)
      Out(0x4f, tmp|0x10); //0x4f for data

Example 3: Set GPIO "Pin4-GPO04" output to "low",
      // the "Pin4-GPO04" output setting is at address F1 bit 4,

Step 1. Enable SIO configuration mode without timeout in between commands
      Out(0x4e, 0x87); // (port, value), 0x4e for index
      Out(0x4e, 0x87);

Step 2. Select LDN06 (GPIO) (LDN: Logic device number)
      Out(0x4e, 0x07); // select entry page, 0x4e for index
      Out(0x4f, 0x06); // select LDN06,   0x4f for data

Step 3. Set address to 0xF1
      Out(0x4e, 0xF1); //0x4e for index

Step 4. Get data from port 0x4f (Save current state)

Byte tmp = Inp(0x4f);   //Read current data for adding the output in bit4

Step 5. Write data to port 0x4f (only set bit 4 to "low" and write back)

Out(0x4f, tmp&0xEF);