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SPECIFICATION

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3Y POWER TECHNOLOGY
3Y Power Technology, Inc.

µRP1H-300 (YH-5301E)

Power Distribution Board Specification

µRP1U 300W DC-DC Switching Power Distribution Board
80Plus Silver compliant

[This Document describes the specification of a switching power supply complying to industrial standards, namely Server System Infrastructure (SSI) specification.]

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Basic Specification

- DC to DC switching power distribution board
- Dimension: 41.5mm (height) x 106mm (width) x 260.5mm (length)
- 12V main input and 5Vsb auxilary input
- Allows AC and DC input power module with the complying power bus
- Max. ouput of the PDB is 300W combined.
- Must meet class B EMI compliance in chassis
- Three main outputs +12V, 3.3V, 5V and one auxilary output +5Vsb
- Traditional and green redundant support
- Hot-Swap function support for the pwer modules
- Passive cooled with PWM FAN of power modules
- Operation Temperature range: -5℃ ~ 50℃ @ full loa d
- Power Supply Management Controler (PSMC) for Smart Monitoring and control of the power supply
- EEPROM for FRU information
- i2c-Bus compliant communication bus (SDA, SCL) at 100kHz
- PS_Alert# , PWOK#, Buzzer signaling
- Protections: OCP,OVP, OPP, UVP, OTP, SCP, FFP,
- Safety Compliance: BSMI, CB, CE, CCC, cUL, UL, TÜV
- Envirnmental Compliance: ROHS, WEEE, REACH

1. REVISION LOG

This section contains the release history of this document:

Date	Section	Revision	Issue
2011/12/2		0.0	Original release
2012/2/10		0.1	Modify PWOK hold up time .
2012/3/22		0.2	3.1.7. Input Power Factor Correction update to 0.9/0.8/0.7 for system .
2012/5/11		0.3	5.3. Over Temperature Protection (OTPAR) Critical Tenv 58C Critical Tcomp 88C
2012/8/9	3.1.4	0.4	Input current peak power 400W
	2.1		Modify Dimension
	10.2		Outline Dimensions
2012/10/25		0.5	2.1.1 Connector Definition 12Vsb change to 5Vsb.
2012/12/25	10.1.1	0.6	Modify Model Label
2012/12/25	2.3.2	0.6	3700M change to 5000M
2012/12/25	2.3.4	0.6	3700M change to 5000M
2012/12/25	7.1	0.6	3700M change to 5000M
2013/3/15	2.3.1	0.7	DEL PEAK W .derating
	3.1.11.	0.7	Modify Performance Criteria of EMI
	6.1.2	0.7	SDA/SCL noise is 300mV

APPROVE		CHECK		PREPARE	

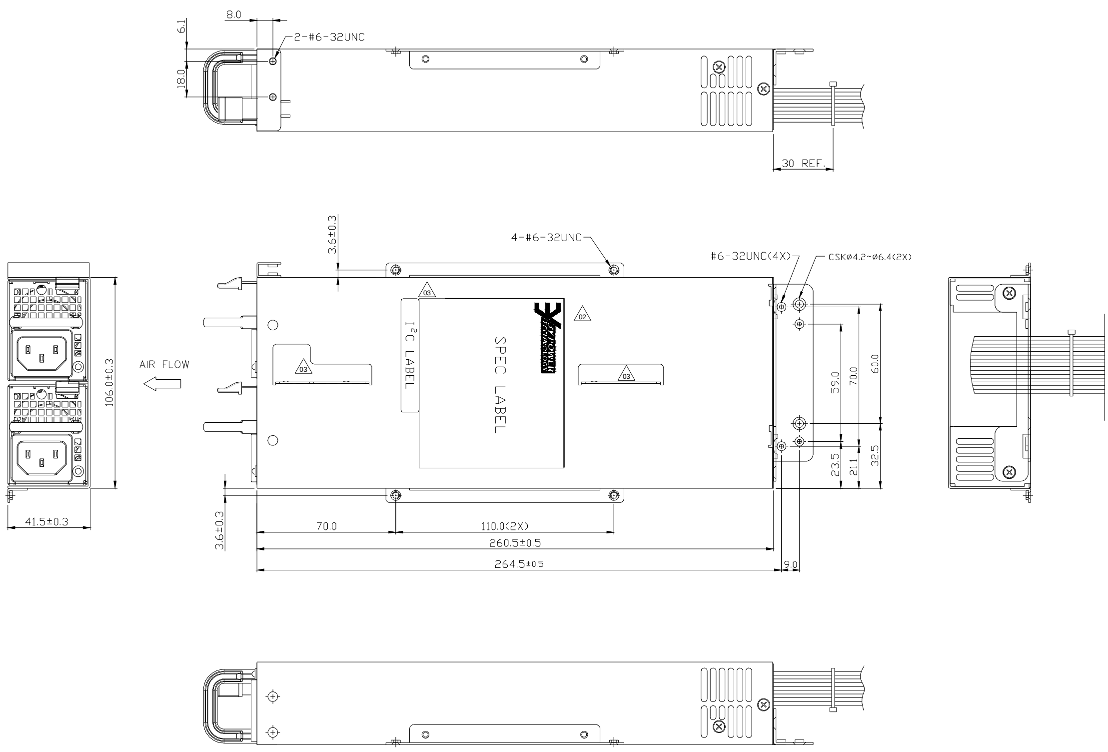
2. GENERAL SCOPE

This specification describes the performance characteristic of a 300W AC-DC switching power distribution board (PDB) with a +12V main DC input and a +5Vsb auxiliary input. The PDB will switch into 3.3V and 5V main output and distribute 12V along with 5Vsb auxiliary. The PDB shall be able to operate with a single power supply module, or in a N+1 parallel hot-plug able operation with active load sharing in a N+1 redundant configuration. Mixed operation of different input type power modules (AC-DC) is allowed.

2.1. Mechanical Overview

The physical size of the PDB enclosure is intended to accommodate power supplies with a power range of up to 300watts. The physical size is 41.5mm x 106mm x 260.5mm (height x width x length).
The power supply, which mates into this PDB, shall have a card edge for the DC outputs and signal pins, mating with Molex LPH series connector.
Input power plugs directly into the external face of the power supply module.

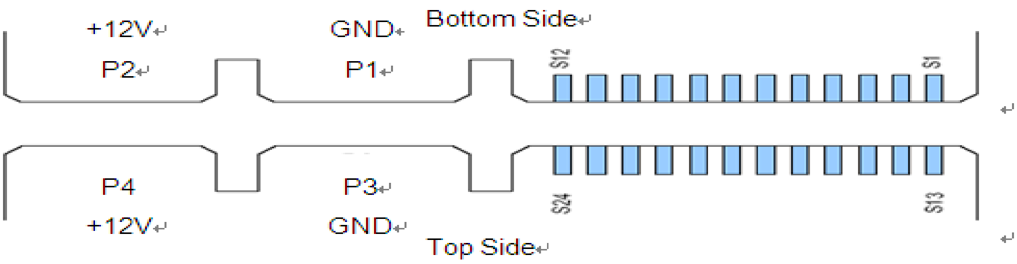
Figure 1 – PDB Dimension



2.1.1. DC Input Connector

The power supply shall have a card edge to mate with the Molex Low Profile Hybrid (LPH) Interconnect system. The Matting connector at PDB side is Molex PN 45984-4343.

Figure 2 – Card Edge Pin Out Location



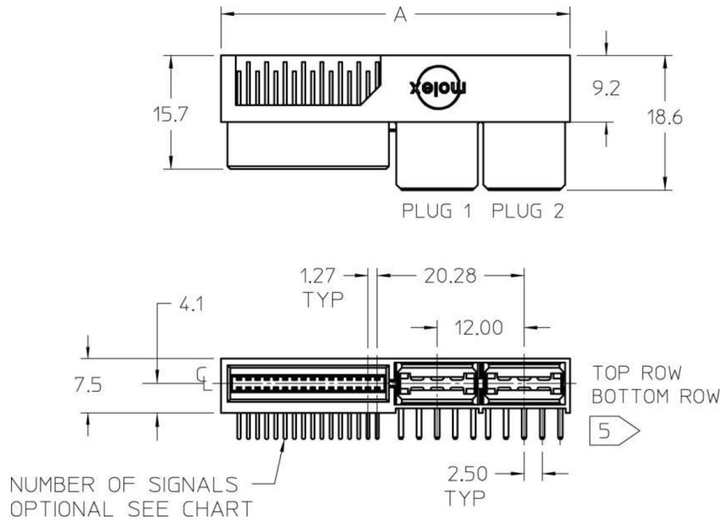
Pin Assignment :

- P1~4,: Power Circuits
- S1 ~ S24: Signal Circuits

Table 1 – Card Edge Pin Out Definition

Pin Name	Signal Name	Function
P1 Bottom	RTN GND	+12V return
P2 Bottom	Main_output	+12V
P3 Top	RTN GND	+12V return
P4 Top	Main_output	+12V
S1	Main_output Sense	+12VS
S2	GND Sense	+12V RTN Sense
S3	+MO IS	+12V Main output Current share bus
S4	SMB_Alert TTL	SMB_Alert for failure notification
S5	SDA	I2c Data signal
S6	SCL	I2c Clock signal
S7	+ PS_Kill	In order to switch of the Main output (shorter)
S8	PSON	Power enable input
S9	PWOK	Pwr OK output
S10	A1	I2c address bit 1
S11	Stby_Output	+5Vsb
S12	Stby_Output	+5Vsb
S13	reserved	reserved
S14	Present#	Power supply present
S15	A0	I2c address bit 0
S16	A2	I2c address bit 2 (DGND, as 1+1 only)
S17	Vs	Reserved for Factory use (+15Vcc)
S18	EEPROM_WP	EEPROM write protection
S19	Input_OK#	Input present signal
S20	grRD#	Green Redundancy input
S21	PDB-Fail	PDB Fail
S22	Vs	Reserved for factory use (NC)
S23	Stby_Output	+5Vsb
S24	Stby_Output	+5Vsb

Figure 3 – PDB Mating Connector



2.1.2. Handle Retention Mechanism

The power supply module shall have a handle to assist extraction. The module shall be able to be inserted and extracted without the assistance of tools. The power supply shall have a retention mechanism, which retains the power supply into the PDB cage or enclosure during all mechanical shock (50G) and vibration testing.
The handle shall protect the operator from any burn hazard through the use of Industrial designed plastic handle or equivalent approved material.

2.2. Buzzer Sound and Identification

The PDB shall have a Buzzer for indication of the power system status.
The buzzer is driven by an internal circuitry and should sound in a N+1 configuration even without AC power.
The Buzzer function can be switched off by hardware or i2c command.
Connector for disabling Buzzer is: TDB
I2C command for disabling Buzzer is: TDB
The BUZZER TYPE: TDB or equal.

Table 2 – Buzzer Status Information

Power system condition	PDB Buzzer
No AC power to all PSU	OFF
No AC power to one PSU only	0.5Hz buzzing
AC present/only standby output on	OFF
Power supply DC output ON and OK	OFF
One power module failure	1Hz buzzing
PDB fail	Steady buzzing

2.3. Enviornmental Requirements

The PDB shall operate within all specified limits over specified conditions in 2.3.
The defined operation condition include temperature, humidity, altitude, shock and vibration.

2.3.1. Temperature and Humidity Requirements

The PDB shall operate within all specified limits over T_{op} temperature range and specified humidity Range. All airflow shall pass through the PDB and not over the exterior surfaces of the PDB cage.

The power supply shall withstand thermal storage specified in $T_{non\text{-}OP}$ without any damage.

Table 3 – Temperature Requirements

Item	Description	MIN	MAX		Unit
T_{OP}	Operating temperature range.	-5	50		℃
ΔT	Max temperature rise across power supply		15		℃
$T_{non\text{-}OP}$	Non-Operating temperature range.	-40	70		℃
$T_{\Delta\ change}$	Rate of temperature change.		10		℃/hrs
H_{OP}	Operating humidity range, non condensing		85		%
$H_{non\text{-}OP}$	Non-Operating humidity range, non condensing		95		%

2.3.2. Altitude Requirements

The PDB shall operate within all specified limits over A_{op} Altitude range. The change pressure condition shall not harm the PDB and the operation within specified regulations shall be assured.

The PDB shall withstand Altitude storage specified in $A_{non\text{-}OP}$ without any damage.

Table 4 – Altitude Requirements

Item	Description	MIN	MAX	Unit
A_{OP}	Operating Altitude range.	0	5000	m
$A_{non\text{-}OP}$	Non-Operating Altitude range.	0	15000	m

2.3.3. Vibration and shock Requirements

The PDB shall operate within all specified limits over G_{op} Shock Vibration range.

The PDB shall withstand Shock Vibration storage specified in $G_{non\text{-}OP}$ without any damage.

Table 5 – Shock Vibration Requirements

Item	Description	MIN	MAX	Unit
G_{OP}	Operating Shock Vibration range.	0.01@10Hz	0.02@20Hz	G^2/Hz
$G_{non\text{-}OP}$	Non-Operating Shock Vibration range.	0.02@20Hz	0.02@1kHz	G^2/Hz
S_{OP}	Acceleration Shock while operation.		10	G
$S_{non\text{-}OP}$	Acceleration Shock non-operation		50	G

2.3.4. Airflow Requirements

The PDB shall be passively cooled through the air flow provided by the power module. The airflow direction shall be in either direction (inside out, pulling or outside in, pushing).

The airflow shall be increased according to specification in Table 6. The conditions must be satisfied under the maximum inlet temperature and altitude limits as specified in the table.

All airflow shall pass through the PDB and not over the exterior surfaces of the power subsystem..

Table 6 – Airflow and Thermal Requirements

Operation Condition	Load (W)	Minimum Requirement Airflow (CFM)	Maximum System Temp. (℃)	Maximum Inlet Temp. (℃)	Altitude
1	Acoustic- Idle 120W (40%)	TBD	25	45	900
2	Acoustic - Operating 180W (60%)	TBD	25	45	900
3	Performance – Max T 300W (100%)	TBD	35	50	900
4	Performance – Max Altitude 300W (100%)	TBD	28	43	5000

Figure 4 – PS Impedance Requirement

TBD

2.3.5. Acoustic Requirements

The PDB airflow shall be provided by the system or power module side. The Fan's installed into the power module shall not exceed the below requirements noise requirements.

Table 6 – Acoustic Requirements

Operating Condition	Volumetric Flow, stand alone (CFM)	Inlet Temperature Condition (℃)	% of Maximum Loading Condition	LwAd(BA)
Idle	TBD	50	40	4.7
Operating	TBD	50	60	5.2
Maximum	TBD	50	100	6.2

3. ELECTRICAL PERFORMANCE

3.1. Power Input Specification

3.1.1. Power Bus and Signal Connector

The PDB shall have a common Power Bus and signal connector complying to Molex LPH interconnect series. The exact PN for the interconnect is Molex PN 45984-4343.

The Pin definition shall comply with chapter 2.1 and shall provide 12VDC as main input and 5VsbDC as auxiliary input.

3.1.2. Power Inlet connector

The PDB has no direct power AC inlet connector. The power inlet shall be found at the power module. Dependant on the input power version, it shall comply to below requirements:

1. AC Version : Comply with IEC 320 C-14 power inlet connector specification. This inlet shall be rated for operation at 15A/250VAC.

3.1.3. Input voltage and frequency specification for the Power Module

The power modules inserted into the PDB shall operate within all specified limits over the following input range. The power supply shall power off if the AC or DC input is below V_{low_limit} and shall start (auto recover) if $V_{recover}$ is reached. Input of voltages below $V_{recover}$ shall not cause any damage to the power supply module nor the PDB, including the input fuse.

The PDB shall supply the full output power, as long the power supply module is operating within specifications.

Table 7 – Rated output power for each input voltage range

Parameter	Minimum input	Rated Input	Maximum input	$VAC_{recover}$	VAC_{low_limit}
115 VAC	$90V_{rms}$	$100\text{-}127V_{rms}$	$132V_{rms}$	85VAC ±5VAC	75VAC ±5VAC
230 VAC	$180V_{rms}$	$200\text{-}240V_{rms}$	$264V_{rms}$		
Frequency	47Hz	50/60Hz	63Hz		

3.1.4. Input current

The maximum input current defines the maximum possible output current, to ensure the proper function of the PDB to meet all defined specifications.

Table 8 – Maximum input current

Input voltage	Input current	Inrush current	Max power	Peak power
90-132VAC	5A*	40A*	300W	400W
180-264VAC	3A*	60A*	300W	400W

*:single power supply module

3.1.5. Line Fuse

The power supply module inserted to the PDB shall incorporate one input fuse on the line side for input over-current protection to prevent damage to the power supply and PDB, to meet product safety requirements. Fuses should be slow blow type or equivalent to prevent nuisance trips. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.1.6. Line inrush

The power supply module must meet inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition, during repetitive ON/OFF cycling of AC , and over the specified temperature range (T_{OP}). The peak Inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The maximum AC line inrush current for this power module is defined in the complying specification and is dependent on power module utilized.

Inrush current shall be measured at an ambient temperature of 25 deg C after the input voltage has been removed from the power supply for a minimum of 10 minutes.

3.1.7. Input Power Factor Correction (only AC input)

The input Power Factor shall be greater than 0.90/115Vac and 0.90/230Vac (show the below actual PF curve)over all input voltages at loads greater than 100% of the power supply's rated output, and meet Energy start 4.0 level .

Table 9 – Power Factor Correction

Input voltage	20% loading	50% loading	100% loading
115VAC	0.70	0.80	0.90
230VAC	0.70	0.80	0.90

3.1.8. Line dropout

An Line dropout is a transient condition defined as the Input to the power supply module drops to 0 VAC at any phase of the AC line for any length of time. During an AC dropout the power supply and PDB must meet dynamic voltage regulations requirements. An AC line dropout of any duration shall not cause dripping of the control signals and protection circuits. If the AC dropout lasts longer than the holdup time, the power supply system should recover when VAC meets $VC_{recover}$ and meet all turn on requirements. A Input dropout of any length shall not cause any damage to the power supply system.

Table 10 – Holdup time until Power output goes out of regulations

Loading	Main output	Standby output
50%	24mS	
80%	20mS	
100%	16mS	70mS

3.1.9. Efficiency

The minimum efficiency of the power system measured at an input voltage of 115V or 230V and the maximum load shall be 80%.

3.1.10. Susceptibility Requirements

The power supply system with the PDB shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter, which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 12 – Performance criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec. limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.1.10.1. Electrical Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024:1998 using the IEC 61000-4-2:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

3.1.10.2. Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-4:1995 test standard and performance criteria B define in Annex B of CISPR 24.

3.1.10.3. Radiated Immunity

The power supply shall comply with the limits defined in EN55024:1998 using the IEC61000-4-3:1995 test standard and performance criteria A defined in Annex B of CISPR 24.

3.1.10.4. Surge Immunity

The power supply shall be tested with the system for immunity to AC Ringwave and AC Unidirectional wave, both up to 2kV, per EN55024:1998, EN 61000-4-5:1995 and ANSI C62.45:1992.
The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.
The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in Annex B f CISPR 24.

3.1.10.5. AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions.

“Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions.

“Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.
The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 13 – AC Line SAG transient performance.

AC Line Sag (10sec interval between each sagging)				
Duration	**Sag**	**Operating AC voltage**	**Line frequency**	**Performance criteria**
Continuous	10%	Nominal AC voltage	50/60Hz	No loss of function or performance
0 to AC cycle	100%	Nominal AC voltage	50/60Hz	Loss of function or performance is acceptable, self recoverable
>1 AC cycles	>10%	Nominal AC voltage	50/60Hz	Loss of function acceptable, self recoverable
0 to 1/2 AC cycle	30%	Mid-point of nominal AC voltage	50/60Hz	No loss of function or performance

Table 14 – AC Line SURGE transient performance.

AC Line Surge				
Duration	**Surge**	**Operating ac voltage**	**Line frequency**	**Performance criteria**
Continuous	10%	Nominal AC voltage	50/60Hz	No loss of function or performance
0 to 1/2 AC cycle	30%	mid-point of nominal AC voltage	50/60Hz	No loss of function or performance

3.1.10.6. AC line fast transient (EFT) specification

The power supply shall meet the EN61000-4-5 directive and any additional requirements in IEC1000-4-5:1995 and the level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.

The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

3.1.11. Electromagnetic Compatibility Requirements for AC input supplies

Category	Standard	Frequency	Level / Limits	**Performance Criteria 1**
Radiated Emissions	EN 55022	30M -1GHz	Class B	3dB Margin
	CFR 47, Part 15, Subpart B	30M-1GHz >1GHz (see standard)	Class B	
	Additional requirements for DT	1.0 - 10.7GHz	70dBuV/m Pk	
		1.24 - 1.3GHz	50dBuV/m Pk	
		1.7 - 1.92GHz	50dBuV/m Pk	
		10.7 - 18GHz	85dBuV/m Pk	
	GR 1089, Issue 4	10k-10GHz, E-Field and H-Field	Section 3.2.1	
Conducted Emissions	EN 55022	150k-30MHz	Class B	3dB Margin
	GR 1089, Issue 4, Section 3.2.2	150k-30MHz	Voltage, Table 3-3&4	
		10k-30MHz	Current, Table 3-5	
AT&T NEDS (Network Equipment Development Stands)	ATT 801-900-160 (Dec 2003)		See standard	
Radiated Immunity	EN 61000-4-3	80M-2GHz	10 V/meter	A
	Additional requirements for BT and DT.	806 – 960 MHz	20 V/meter	A
		1700 – 2025 MHz		
		2100 – 2200 MHz		
		2500 – 2690 MHz		
		880 - 915 MHz	50 V/meter	A
		1710 - 1785 MHz	35 V/meter	A
		1920 - 1980 MHz	50 V/meter	A
		2400 - 2483 MHz	12 V/meter	A
		5150 - 5350 MHz		
		5725 - 5820 MHz		
	GR 1089, Issue 4	10 KHz – 10GHz	8.5 V/meter Section 3.3.1	A
ESD	EN 61000-4-2		8 KV contact, 15KV Air	B
Electrical Fast Transient	EN 61000-4-4		+/- 2 KV	B
Conducted Susceptibility	EN 61000-4-6	150 KHz – 80 MHz	10Vrms	A
	GR 1089, Issue 4	10 KHz – 30 MHz	Section 3.3.2 Table 3-11	A
Voltage Dips and Sags 2	EN 61000-4-11	>95% reduction for	10mS	B
		>30% reduction for	500mS	C
		>95% reduction for	500mS	C

3.1.12. Power Recovery

The PDB shall recover automatically (auto recover) after an input power failure. Input power failure is defined to be any loss of Input power that exceeds the dropout criteria.

3.1.13. Voltage Brown Out

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

In addition the power supply shall meet the following requirements:

A continuous input voltage below the nominal input range shall not damage the power supply or cause overstress to any power supply component. The power supply must be able to return to normal power up state after a brownout (Sag) condition. During brownout test of defined input range @ 300W with 3mins ramp, input current shall never exceed fuse and shall not blow the fuse.

3.1.14. Line Leakage Current

The maximum leakage current to ground for each power supply shall be 3.5mA when tested at 240VAC.

3.2. DC output voltages

3.2.1. Grounding

The output ground of the pins of the power supply provides the output power return path. The ground output at the PDB shall be connected to the safety ground (power supply enclosure) and PCB card edge. This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply system shall be provided with a reliable protective earth ground. All secondary circuits and D2D shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 1.0mΩ. This path may be used to carry DC-current.

3.2.2. Output rating

The following table defines the power and current rating of the 300W PDB. The combined output power of all outputs shall not exceed the rated output power. The power supply system must meet both static and dynamic voltage regulation requirements.

The utilized power module defines the maximum output power of the PDB. In a mixed operation, the power module with the lower output power shall define the maximum output limit in order to achieve safe redundant operation. In case the max output limit in a 1+0 had been exceeded, the power module shall latch OCP or OPP event. In a 1+1 operation, the current will be shared and redundancy function will be changed to forced current share mode, if the max. output rating of the lower power module had been exceeded.

The maximum combined steady output power shall be 300W, no matter how the current draw will be combined.

Table 15 – Output Power and Current Ratings

OUTPUT	NOM VOLT	OUTPUT CURRENT			UNITS	CONDITION
		MIN	MAX	Peak		
1	+3.3V	0	20 #a	24	A	combined #a & #b power≦140W
2	+5V	0	20 #b	24	A	
3	+12V	0	24	31.7	A	
4	-12V	0	0.5	N/A	A	
5	$+5V_{sb}$	0	3	4	A	

3.2.3. Remote Sense

The PDB shall have remote sense for the +3.3V (3.3VS) and return (ReturnS) if the server signal connector (i2c connector) is implemented. The remote sense return (ReturnS) is used to regulate out ground drops for all output voltages; +3.3V, +5V, +12V$_{1,2,3,4}$, -12V, and +5Vsb. The 3.3V remote sense (3.3VS) is used to regulate out drops in the system for the +3.3V output. The remote sense input impedance to the PDB must be greater than 200W on 3.3.VS and ReturnS. This is the value of the resistor connecting the remote sense to the output voltage internal to the PDB. Remote sense shall be able to regulate out a minimum of 200mV drop on the +3.3V output. The remote sense return (ReturnS) shall be able to regulate out a minimum of 200mV drop in the power ground return. The current in any remote sense line shall be less than 5mA to prevent voltage sensing errors. The PDB shall operate within specification over the full range of voltage drops from the PDB's output connector to the remote sense points.

3.2.4. Auxilary Output (Standby)

The 5Vsb output shall be present when an input voltage greater than $V_{recover}$ is applied to the power module.

3.2.5. No load operation

The power supply system shall meet all requirements except for the transient loading requirements when operated at no load on all outputs.

3.2.6. Peak load operation

The power supply shall be capable to hold the peak loading requirements for at least 15mS without going out of regulation or shutting down. Each output slew rate 0.05A/uS ,5Vsb minimum 0.3A .

3.2.7. Voltage Regulation

The power supply shall meet the Voltage regulation when operating at steady state condition , dynamic ,peak load , Hot swap conditions must be meet +/- 5% . These limits include the peak-peak ripple/noise.

The regulation of Table 16 shall be measured at the output connector of the power supply, subject to the dynamic loading conditions in paragraph 3.2.7.

Table 16 – Output Voltage regulation

		Output voltage limits(V_{dc})			
Output	**Minimum**	**Nominal**	**Maximum**	**Unit**	**Tolerance**
+3.3V	+3.135	+3.3	3.47	V_{rms}	+5/-5%
+5V	4.75	+5.0	5.25	V_{rms}	+5/-5%
+12V$_{1,2,3,4}$	+11.64	+12.0	+12.60	V_{rms}	+5/-3%
-12V	-11.40	-12.0	-13.08	V_{rms}	+9/-5%
+5Vsb	4.75	5	5.25	V_{rms}	+5/-5%

3.2.8. Ripple and Noise Regulation

Ripple and Noise is defined in table 17. Ripple and Noise shall be measured over a Bandwidth of 0Hz to 20MHz at the power supply output connector. A 0.1µF ceramic capacitor and 47µF of tantalum capacitor shall be placed at each point of measurement. The measurement points shall be as close as possible to the point of load.
The ripple and noise specification shall be met over all load ranges and any line voltages with 1+N power supplies in parallel operation.

Table 17– Ripple and Noise Regulation

Output	+3.3V	+5V	+12V	-12V	5VSB
Maximum ripple/noise	50mVp-p	50mVp-p	120mVp-p	120mVp-p	50mVp-p

3.2.9. Dynamic loading

The power supply shall operate within specified limits and meet regulation requirements for step loading and capacitive loading specified below.

The load transient repetition rate shall be tested between 50Hz to 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load and the MAX load.

This shall be tested with no additional bulk capacitance added to the load.

Table 18 – Transient Load Requirements

Output	Δ Step size	Slew Rate	Capacitive Load
+3.3V	30% of max. load	0.5A/ μsec	1000μF
+5V	30% of max. load	0.5A/ μsec	1000μF
+12V	65% of max. load	0.5A/ μsec	2200μF
+5VSB	25% of max. load	0.5A/ μsec	1μF

3.2.10. Capacitive load

The power supply shall operate within specifications over the capacitive loading ranges defined below in table 19.

Table 19 – Capacitive Loading Conditions

Output	Min	Max
+3.3V	10μF	12,000μF
+5V	10μF	12,000μF
+12V	10μF	11,000μF
-12V	1μF	350μF
+5VSB	1μF	350μF

3.2.11. Maximum load change

The power supply shall continue to operate normally when there is a step change ≤ 1 A/μsec. between minimum load and maximum load.

3.2.12. Close loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of: 45 degrees phase margin and -12dB gain margin is required. Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

3.2.13. Residual Voltage Immunity in Standby mode

The power supply should be immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on/off. The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when Input voltage is applied.

3.2.14. Common Mode Noise

The Common Mode noise on any output shall not exceed 350mV pk-pk over the frequency band of 10Hz to 200MHz. Measurement shall be made across a 100Ω resistor across the DC outputs, including ground at the DC output connector and chassis ground (power sub system enclosure),

3.2.15. Soft starting

The power supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the Input line or any power supply components at any specified Input line or load condition.

3.2.16. Hot Swap Requirements

Hot Swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic and zero loading conditions. The power supply can be hot swapped by the following method:

Extraction: The power supply may be removed from the system while operating with PSON# asserted, while in standby mode with PSON# de-asserted or with no AC applied. No connector damage should occur during un-mating of the power supply from the power distribution board (PDB).

Insertion: The power supply may be inserted into the system with PSON# asserted, with PSON# de-asserted or with no AC power present for that supply. No connector damage should occur due to the mating of the output and input connector.

In general a failed (of by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply will get turned on into standby or Power On mode once inserted.

3.2.17. Load sharing control

The +12 V output shall have active load sharing provided by inserted power modules. When operating at 50% of full load, the output current of any 1+1 power supplies shall be within (+/-10%). For example, if power supply #1 is operating at 12A, then all other power supplies within the system shall be operating between 10.8A to 13.2A (+/- 10% of 12A).

All current sharing functions shall be implemented internal to the power supply module by making use of the 12VLS signal. The PDB (Housing Back Plane, for example YH-Part), shall connect the 12VLS signals between the power supplies together. The power supply shall be able to share with up to 1+N supply in parallel.

The failure of a power supply shall not affect the load sharing or output voltages of the other supplies still operating. The power supplies must be able to load share with 100mV of drop between different power supply's output.

If the load sharing is disabled by shorting the load share bus to ground, the power supply shall continue to operate within regulation limits for loads less than or equal to the rating of one power supply.

Table 20 - Load share bus output characteristics

Item	Description	Min	Nominal	Max	Units
V_{share}; I_{out}=Max.	Voltage of load share bus at specified max output current		6		V
$\triangle V_{share}/\triangle I_{out}$	Slope of load share bus voltage with changing load		$6/I_{outmax}$		V/A
I_{share}SINK	Amount of current the load share bus output from each power supply is allowed to sink		1.5		mA
I_{share}SOURCE	Amount of current the load share bus output from each power supply needs to source		1.5		mA
T_{share}; I_{out}=Max.	Delay from output voltages in regulation to load sharing active with maximum load of one power supply and two power supplies in parallel. (remote on/off only)			100	msec

3.3. Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 0.2 to 70ms. For 5Vsb, it is allowed to rise from 0.2 to 25ms. All main outputs shall rise positive monotonically and have a slop value between 0 V/mS to 0.1V/mS.

For 5Vsb output any 5ms segment of the 10% to 90% rise time waveform, a straight line draw between the end points of the waveform segment must have s slope ≥ [Vout, nominal /20]V/mS.

Each output voltage shall reach regulation within 50mS (T_{vout_on}) of each other during turn on of the power supply system. Each output voltage shall fall out of regulation within 400mS (T_{vout_off}) of each other during turn off.

Table below shows the timing requirements for the power supply being turned on and off via the input power, with PSON held low and the PSON signal, with the input power applied.

3.3.1. Output Voltage Timing

The timing of signals and outputs are specified in below Table 13 and illustrated in Figure 1.

Table 21 - Turn on/off timing

Turn on	Description	Min	Max	Units
$T_{vout\ rise}$	Output voltage rise time for all main output	0.2	70	msec
	Output voltage rise time for auxiliary output 5Vsb	0.2	25	msec
$T_{vout\ on}$	All main outputs must be within regulation of each other within this time		50	msec
$T_{vout\ off}$	All main outputs must leave regulation within this time.		400	msec
$T_{sb\_on\_delay}$	Delay from AC being applied to 5VSB being within regulation		1500	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltage being within regulation		2500	msec
T_{vout_holdup}	Time all main output 12VI voltages stay within regulation after loss of AC.	16		msec
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	15		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits	5	400	msec
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		50	msec
T_{pwok_on}	Delay from output voltage(3.3V, 5V, 12V, -12V) within regulation limits to PWOK asserted at turn on	100	500	msec
T_{pwok_off}	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1		msec
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal	100		msec
T_{sb_vout}	Delay from 5Vsb being in regulation to main output being in regulation at AC turn on.	50	1000	msec
T_{5Vsb_holdup}	Time the 5Vsb output voltage stays within regulation after loss of AC	70		msec

Figure 5 – Output Voltage timing

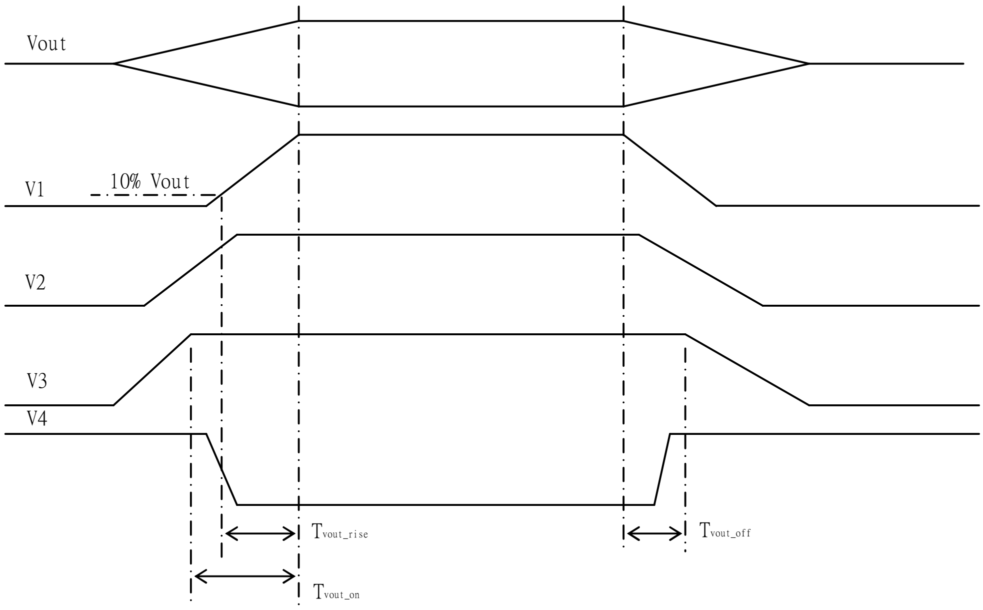
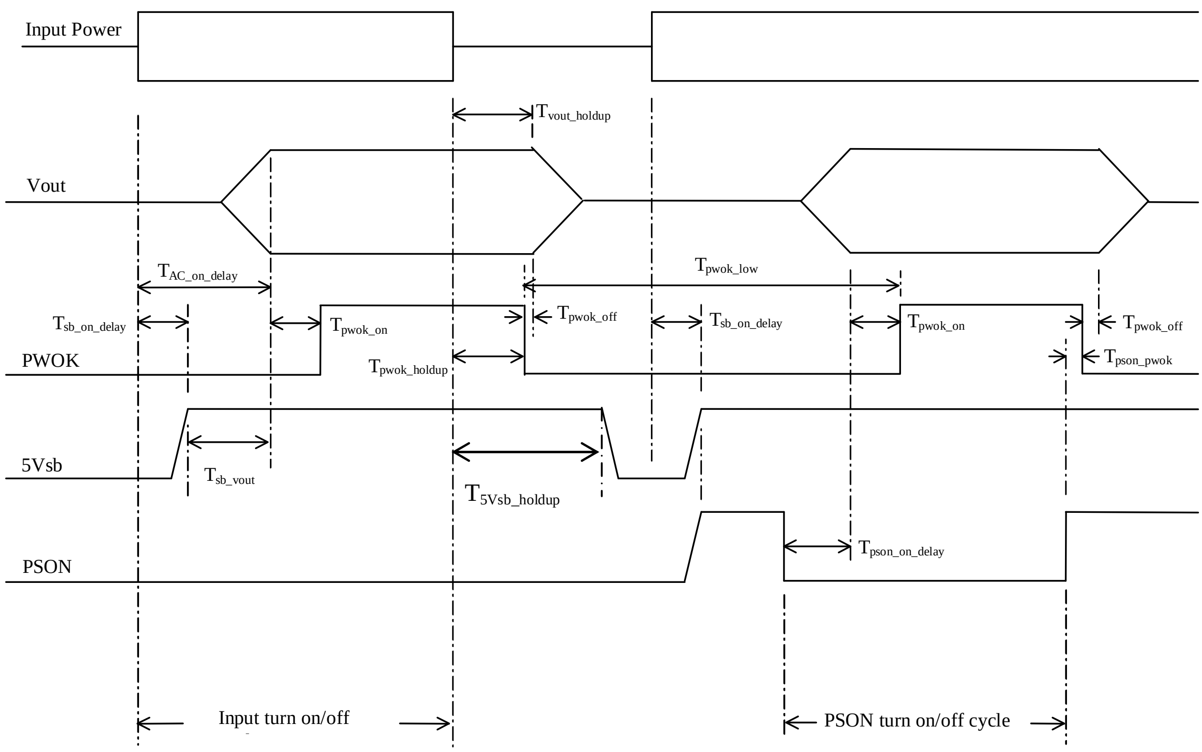


Figure 6 – Turn On/Off Timing (Power Supply Signals)



3.3.2. Overshoot

Any output overshoot at turn on shall be less than 5% of the nominal output value. Any overshoot shall recover to within the specified regulation in less than 0.5mS

3.3.3. Undershoot

Any output shall not undershoot at turn on or off cycle under any circumstances.

3.3.4. Temperature coefficient

After operating for 30 minutes or longer at 25°C a mbient, the output voltages shall not change by more than ± 0.05 % per degree C for any given line and load conditions.

3.4. Control and Indicator functions

The following section define the input and output signals from the power supply.
Signals that can be defined as low true use the following convention:
Signal# = low true.

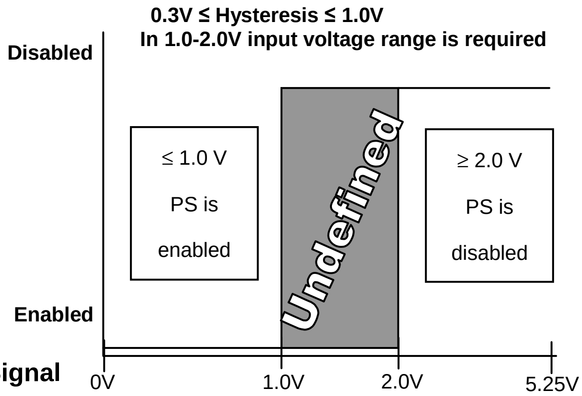
3.4.1. PSON# Input Signal (Power supply enable)

The PSON# signal is required to remotely turn on/off the main output of the power supply.
PSON# is and active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off.
PSON# is pulled to a standby voltage by a pull-up resistor internal to the power supply.
See Table 22.

Table 22 – PS ON# signal characteristics

Signal Type	**Accepts an open collector/drain input from the system. Pul-up to Vsb located in the power supply.**	
PSON# = Low	ON	
PSON# = High or Open	OFF	
PSON# = Low, PSKILL = Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, V_{pson} = low		4mA
Power up delay: $T_{pson\_on\_delay}$	5ms	400ms
PWOK delay: T_{pson_pwok}		50ms

Figure 7 – PSON# Signal Characteristic



3.4.2. PSKILL Input Signal

The purpose of the PSKILL pin is to allow for hot swapping of the power supply. The PSKILL pin on the power supply is shorter than the other signal pins. When a power supply is operating in parallel with other power supplies and then extracted from the system, the PSKill pin will quickly turn off the main output to prevent arcing of the DC output contacts. T_{PSKill} is the minimum time delay from the PSKill pin un-mating to when the power pins un-mate. The power supply must discharge its output inductor within this time from the un-mating of PSKill pin. When the PSKill signal pin is not pulled down or left open (power supply is extracting from the system or had not been inserted to the system), the power supply should shut down regardless of the condition of the PSON# signal.

The mating pin of this signal in the system shall be tied to ground. Internal to the power supply, the PSKILL pin shall be connected to a standby voltage through a pull-up resistor. Upon receiving a LOW state signal at the PSKILL pin, a PSON# signal shall enable the power supply to turn on.
See Table 23.

Table 23 – PSKILL signal characteristics

Signal Type (Input Signal to Supply)	**Accepts a ground input from the system. Pull- up to Vsb located in the power supply.**	
PSKILL = Low, PSON# = Low	ON	
PSKILL = Low or Open, PSON# = Open	OFF	
PSKILL = Open , PSON# = Low	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	0.4V
Logic level high (power supply OFF)	2.4V	5.25V
Source current, V_{pskill} = low		4mA
Delay from PSKILL=High to power supply turned off (T_{PSKill})		100µsec

3.4.3. Power OK (PG or PWOK) Output Signal

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, a internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.
See Table 24.

Table 24 – PWOK signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to Vsb located in power supply.**	
PWOK=High	Power Good	
PWOK=Low	Power Not Good	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{source} = 200µA	2.4V	5.25V
Sink current, PWOK=low		4mA
Source current, PWOK=high		2mA
PWOK delay: T_{pwok_on}	100ms	500ms
PWOK rise and fall time		100µsec
Power down delay: T_{pwok_off}	1ms	200ms

3.4.4. SMBAlert# (PSAlert) Output Signal Pin

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

3.4.4.1. Smart Ride-Through (SmaRT)

SMBAlert# will also be asserted in case of a input power lost.
This function is part of the Smart ride-through (SmaRT) function in order to throttle the system and start up all put in greenRedundancy™ held power supplies.
The SMBAlert# needs to be asserted up on input power lost according to below table.

3.4.4.2. Thermal CLST

SMBAlert# shall also be utilized for warning of critical thermal component temperatures. The Thermal CLST shall assert when the component temperature, which shall be reported by a dedicated thermal probe, is reaching below specified ΔT to critical shut down. The power supply shall report the temperature in addition to Thermal CLST through PMBus to the system, in order to increase fan speed to cool down environmental temperature.

This signal is to be asserted in parallel with LED turning solid red or blinking red/blue.
See Table 25.

Table 25 – PSAlert# signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to Vsb located in power supply.**	
Alert#=High	Power OK	
Alert#=Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{sink} = 50µA	2.4V	3.46V
Sink current, Alert#=low		4mA
Sink current, Alert#=high		50µA
50µA rise and fall time		100µsec
SmaRT input power fail assertion		2msec
Thermal CLST ΔT to critical thermal	10℃	

3.4.5. Power Distribution Board Fail (B/P Fail) Input Signal Pin

This signal pin sense is a signal pin from the PDB, to remotely shut of the main output of the power supply in a critical or failed state situation caused by the PDB. B/P_Fail will be asserted when the PDB or the system experience any problem like over-current, over-voltage, under-voltage, short-circuit, over-temperature or the system operating in environmental condition exceeding the operation conditions.
The power Supply will latch off and the LED will indicate solid “RED”.
When the B/P_Fail signal had been de-asserted the power supply will recover, if the PSON# signal is still asserted.
See Table 26.

Table 26 – B/P_Fail signal characteristics

Signal Type	**Accepts an open collector/drain input from the system. Pull-up to Vsb located in the power supply.**	
B/P_Fail = Low or Open	ON	
B/P_Fail = High	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, V_{pson} = low		4mA
B/P_Fail delay: T_{B/P_Fail_Off}		100µsec

4. Energy Saving Features

4.1. greenRedundancy™ Operation

The PDB shall support greenRedundancy and standard redundant operation. In greenRedundancy operation the PDB can put power module into standby, while the active power supply will provide the entire power output to the PDB. This function is for optimizing the power system efficiency and shall not affect the standard redundancy function of the entire power sub system.

4.1.1. greenRedundancy™ and standard redundancy operation support

The PDB shall support standard redundant (all power module in a N+1 configuration are active) and greenRedundancy™ (when a sufficient number of power modules in a N+1 configuration providing the entire power output, while other are in standby, to achieve the highest power sub system efficiency). **This feature shall be provided via SMBus on the PDB or baseboard**.

4.1.2. greenRedundancy™ Disabling

The greenRedundancy™ feature can be disabled on the PDB or baseboard via hardware or firmware.

HW – via short jumper to provide a logic low to the greenRedundancy™ circuitry.

FW – via PMBus command to the PSMC.

4.1.3. greenRedundancy™ Power Module Steady State

1. Output caps pre-charge state: PS output filter capacitors of the power supply module operating in greenRedundancy™ mode shall stay charged at main output level +5/-10% level at any time when active power supply is OK.
2. Output load state while in greenRedundancy™ standby state: All Fans and preloading resistors need to be disconnected from the main output by an switch and can be activated by PSON. This shall minimize the power dissipation of the power supply in standby mode.
3. PFC disable state: PFC has to be disabled in the greenRedundancy™ Standby power module in order to minimize the power dissipation.

4.1.4. greenRedundancy™ Power Module Start Up requirements

The power module in greenRedundancy™ standby state shall ramp output load up to system level, as soon the active (hot) power module occurring any **Warning, Failure** or **Input power fault.**
The power module shall also be activated when the total power output reaches the greenRedundancy™ threshold (optimum efficiency) and also put back into greenRedundancy™ standby state, when the entire power sub system is ramping down and crossing the threshold, in order to provide optimum efficiency.
The power module need to comply with timings in below table to ensure a stable operation of the power sub system and common voltages.

Table 27 – Timing requirements for greenRedundancy™

Condition	Max	Unit
Any Warning, Failure or Input Power Fail	1	msec
Reaching greenRedundancy™ threshold	1	msec

4.1.5. greenRedundancy™ Signal requirements

a. A logic signal compatible with the PS_ON input must be asserted indicating that this condition has been reached.

b. A pin on the power supply output connector must be allocated for this signal (gRD Pin)

c. The signal generating circuit must incorporate hysteresis preventing it from oscillation under small 5% current variation.

4.1.6. greenRedundancy™ Active Module rotation

With N+1 power supplies installed in the PDB, which supports greenRedundancy™ functionality, the active power modules shall be switched every 168 hours (7 days). This function is utilized to increase the life of every installed power supply in the PDB and equals the active time among the installed power supplies.

4.1.7. greenRedundancy™ control circuitry

The PDB shall incorporate a control circuitry, which shall be able to provide following functions:

a. Continuously monitors main output level and disable power module soft start feature once the main output remains within output specification (12V±10%).
b. PWOK signal shall be de-asserted, when main output voltage drops below $UV_{main\_threshold}$ (11.6V), when it is in an operating active state. The de-assertion timing shall comply to below table.

Table 28 – greenRedundancy™ control circuit timing and thresholds

Condition	Nominal	Unit	Tolerance
Main output range	12	V	± 10%
$UV_{main\_threshold}$ (Main Output drop out threshold)	11.6	V	± 5%
$T_{UV\_PWOK\_OFF}$ (max. time for de-assert of PWOK up on main output drop)	100	µsec	

5. Protection circuits

Protection circuits inside the PDB shall cause only the main output to shutdown (latch off). If the power supply latches off due to a protection circuit assert, an Input Power cycle OFF for 15sec or a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

Specific protection circuits shall not latch, but auto recover when the latching reason had been cleared. This protection circuits will be written in cursive writing and will have a Auto Recover ($Output_{Ar}$) in the chapter name.

The auxiliary output shall not affected by any protection circuit, unless the auxiliary output itself is affected.

5.1. Over Voltage Protection (OVP$_{main}$ & *OVP$_{auxilary\ AR}$*)

All Over Voltage Condition shall be measured internal to the PDB on all outputs (Main and *Auxiliary Output$_{AR}$*) at the output connector. The PDB shall shutdown and latch off after an Over Voltage condition occurs on main outputs, *the auxiliary output shall be auto recover **(VsB$_{AR}$)** after the OVP had been removed*.
The voltages never shall exceed the maximum levels specified in below table when measured during any fail.

The PDB shall alert the system of the OCP/SCP condition via SMBAlert# and fail Buzzer indicator.
The latch on the main output can be cleared by asserting the PSON# signal or by an Input Power interruption.

Table 29 - Over Voltage Protection requirements

Output	Min	Max	Units
Main (+3.3V)	3.9	4.5	VOLTS
Main (+5V)	5.7	6.5	VOLTS
Main (+12V)	13.3	15.6	VOLTS

5.2. Over Current and Short Circuit Protection (OCP/SCP$_{main}$ & *OCP/SCP$_{auxilary\ AR}$*)

The Over Current Condition shall be measured internal to the PDB on all outputs (Main and *Auxiliary Output$_{AR}$*), and preventing outputs to exceed current limits specified in below table. The PDB shall shutdown and latch off after an Over Current condition on main outputs, *the auxiliary output shall be auto recover **(VsB$_{AR}$)** after the OCP/SCP had been removed.*

The latch on the main output can be cleared by asserting PSON# signal or by an Input Power interruption.
The PDB shall alert the system of the OCP/SCP condition via SMBAlert# and fail LED indicator.
The PDB shall not be damaged from repeated power cycling in this condition.

Table 30 – Over Current/Short Circuit Protection

Output	Over Current limit
Main (+3.3V)	110% MIN.; MAX. (28A)
Main (+5V)	110% MIN.; MAX. (28A)
Main (+12V)	110% MIN.; MAX. (35.2A)

5.3. Over Temperature Protection (OTP_{AR})

The PDB shall have a thermal sensors to measure the environmental (T_{env}). The thermal sensor shall be part of a protection circuit to protected against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In an critical Over temperature condition, specified in below table, the power system shall be shutdown with the exception of the ***auxiliary output (VsB_{AR})***.

The Thermal CLST shall be part of the ***OTP_{AR}***.

The PDB shall alert the system of the ***OTP_{AR}*** condition via SMBAlert[#] and Buzzer. The PDB will auto recover the power system from this condition, when the temperature is dropping within specification again. If the ***OTP_{AR}*** is caused due to a defective fan in the power module, than the defective module shall latch off and not auto recover.

Table 31 – *Over Temperature Protection$_{AR}$*

Condition	Warning in ℃	Critical in℃	Timing for SMBAlert[#]/LED
T_{env}	-	58	1msec
T_{comp}		88	1msec
Thermal CLST	-		100µsec

The thermal sensors shall have an accuracy of max. 1℃ per step and a tolerance of ± 10%.

5.4. Fan Failure Protection$_{AR}$

The power supply module shall have a circuit internal to monitor the power module internal fan. The fan failure protection shall monitor the fan speed and should assert SMBAlert[#] and fail LED signal in case the fan Rotation Per Minute (RPM) drop lower threshold or set PWM Δ as defined in below table. In case of a critical event the power module shall de-assert the PWOK and shut of the main output.

The protection circuit shall shutoff the main outputs only and let them auto recover when the fan failure had been cleared.

The PDB shall not be affected from the shut down in a N+1 configuration and only assert the SMBAlert[#] and Buzzer.

Table 32 – *Fan Failure Protection$_{AR}$*

Condition	FAN RPM	PWM Δ	Timing for SMBAlert[#]/LED
Warning	2000	-15%	1sec
Critical	1500	- 25%	1sec

6. Power Supply Management

6.1. Hardware Layer

The serial bus communication devices for Power Supply Management Controller (PSMC) and Field Replacement Unit (FRU) in the power supply shall be compatible with both SMBus 2.0 "high power" and I2C Vdd based power and drive specification.

This bus shall operate at 3.3V but be tolerant to 5V pull-ups. The power supply should not have any internal pull-ups on the SMBus, pull-ups shall be located on system side.

Two pins are allocated on the power supply. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Both pins are bi-directional and are used to form a serial bus. The device(s) in the power supply shall be located at an address(s) determined by addressing pins A0 and A1 on the power supply module. The circuits inside the power supply shall derive their 3.3V power from the 5Vsb bus through a buffer. Device(s) shall be powered from the system side of the 5VSB or'ing device. No pull-up resistors shall be on SCL or SDA inside the power supply. The pull-up resistors should be located external to the power supply on system/application side.

6.1.1. Capancitance for SMBus

The recommended Capacitance per pin on SDA and SCL shall be 10pF, and is not allowed to exceed 40pF per pin. In an N+1 configuration of up to eight (8) power module with additional PDB, the total Capacitance of each Bus pin shall not exceed 400pF.

6.1.2. I2c Bus noise requirement

The power supplies i2c bus' SDA and SCL line shall be clean from noise, which might affect the proper function when utilized with other devices.

The maximum allowed line noise on SDA or SCL is 300mV.

6.1.3. Pull Ups

The main pull-ups are provided by the system and may be connected to 5V or 3.3V. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail. In case the power supply require pull-ups internal, the pull up resistance shall be very week on SDA or SCL.

6.2. Power Supply Management Controller (PSMC)

The PSMC device on the PDB shall derive its power of the 5Vsb output on the system side of the O'ring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBus™ Power System Management Protocol Specification Part I and Part II in Revision 1.2 or later

It shall be located at the address set by the A0 and A1 pins.

Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details on the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the housing.

Table 33 – PSMC Addressing for inserted power modules

PDB position and PSMC address	PM1 B0h/B1h	PM2 B2h/B3h	**PDB 4Ah/4Bh**
Pin A2/A1/A0	0/0/0	0/0/1	**None**

6.2.1. Related Documents

- PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.1 and 1.2
- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.1 and 1.2
- System Management Bus (SMBUS) Specification 2.0

6.2.2. Data Speed

The PSMC device on the PDB shall operate at the full 100kbps (100kHz) SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply is allowed to clock stretch while parsing a command or servicing multiple interrupts or NACK.

Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

The PSMC may support 400kbps (400kHz) PMBus speed.

6.2.3. Bus Errors

The PSMC shall support SMBus clock-low timeout ($T_{timeout}$). This capability requires the PSMC to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions within 10ms later. The total reset time from detection of the condition till restarted, ready to receive commands condition shall not exceed 35ms.

The device must recognize SMBus START and STOP conditions on ANY clock interval. The PSMC must not hang due to ‘runt clocks’, ‘runt data’, or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup. Or hold times that are shorter than the minimums specified by the SMBus specifications. The PSMC is not required to operate normally, but must return to normal operation once ‘in spec’ clock and data timing is again received. Note if the PSMC ‘misses’ a clock from the master due to noise or other bus errors, the device must continue to accept ‘in spec’ clocks and NACK. The PSMC is suppose to re-synch with the master on the next START or STOP condition.

6.2.4. General Call Address

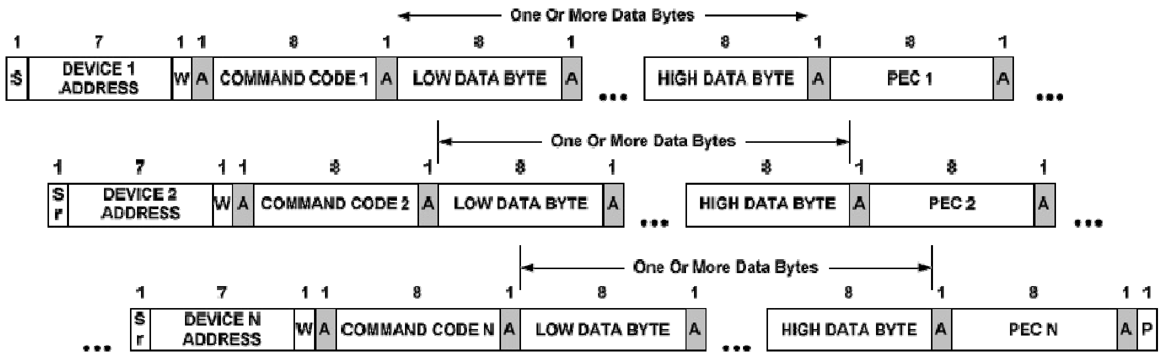
The PSMC shall respond to the General Call Address (00h) as well to its own physical address.

6.2.5. Group Command

The Group Command is used to send commands to more than one PMBus device at a time. The commands are sent in one continuous transmission. When the PSMC detect the STOP condition that ends the sending of commands, it shall begin executing the command which it received or NACK, if the command is not supported.

The Group Command Protocol is not allowed to be used with commands that require the PSMC to respond to the data (only WRITES).

Figure 8 – Group Command with PEC



6.2.6. Extended Command

The Extended Command protocol allows for an extra 256 command codes. This command is similar to the Block-Write/Block-Read Word process call in the SMBus Specification, but allows an maximum length of 256 command codes. The first byte (the low data byte) is a reserved value indicating that the extended command format is being used. The second byte (the high order byte) is the command to be executed. This allows the standard commands to be extended by PMBus and Manufacture specific commands.

Command Extension Codes:

1. MFR_SPECIFIC_COMMAND EXT: FEh
2. PMBUS_COMMAND EXT: FFh

Please see below illustration for utilization:

Figure 9 – Extended Command Write

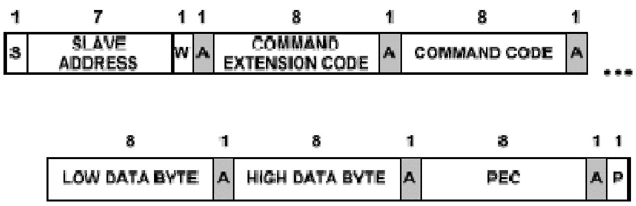
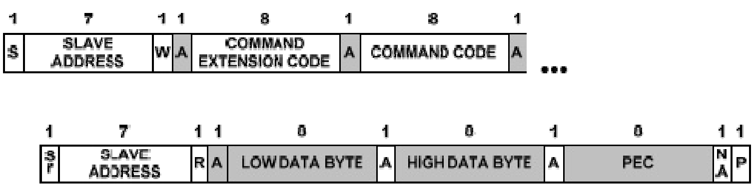


Figure 10 – Extended Command Read



6.2.7. Write Protection (WP)

The PDB shall have a hardware Pin for WP the memory of the PSMC for firmware updates and towards accidental EEPROM writes.

The WP is a active high signal and prevents any write to any memory. The WP needs to be pulled low in order to update the PSMC firmware or write to the EEPROM.

6.2.8. Firmware Updates

The PSMC shall support firmware updates over the SMBus. In order to perform Firmware Updates, the WP needs to be pulled low and appropriated Software tool are required to guaranty the successful update.

6.2.9. Sensor Accuracy

The sensor of the PSMC shall meet below accuracy requirements for sensor readings. The accuracy shall be meet at the specified environmental condition and the full range of rated input voltage.

Table 34 – Sensor Accuracy

Sensor	10% - 20% load	> 20% - 50% load	> 50% - 100% Load
Current	± 5%	± 2%	± 2%
Voltage	± 5%	± 2%	± 2%
Temperature	± 3℃ with Δ5%		
FAN	Provided by the power module		
Input Power	± 15%	± 5%	± 5%
	Provided by the power module		

6.2.10. PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose.
All Sensors shall continue to provide real time data as long as the PSMC device is powered.
This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Table 35 – PSMC Sensor list

Sensor	Description
V_{input}	Input Voltage
I_{input}	Input Current
P_{input}	Input Power
V_{output_main}	Output Voltage main output
I_{output_main}	Output Current main output
P_{output_main}	Output Power main output
V_{output_aux}	Output Voltage auxiliary output
I_{output_aux}	Output Current auxiliary output
P_{output_aux}	Output Power auxiliary output
T_{comp}	Component Temperature
T_{env}	Environmental Temperature
PDB_{fail}	PDB fail protection

6.3. Power Supply Field Replacement Unit (FRU)

The PDB shall support electronic access of FRU information over an I^2C bus. Five pins at the power supply connector are allocated for this. They are named SCL, SDA, A1, A0 and Write protect. SCL is serial clock. SDA is serial data. These two bidirectional signals from the basic communication lines over the I^2C bus. A0and A1 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I^2C address shall be per table below. The Write protection pin is to ensure that data will not accidentally overwritten.

The device used for this shall be powered from a 3.3V bias voltage derived from the +5 VSB output . No pull-up resistors shall be on SCL or SDA inside the power supply.

Table 33 - EEPROM Addressing

PDB position and FRU address	PM1 A0h/A1h	PM2 A2h/A3h	PM3 A4h/A5h	PM4 A6h/A7h	PM5 A8h/A9h	PM6 AAh/ABh	PDB ACh/ADh	PM8 AEh/AFh
Pin A2/A1/A0	0/0/0	0/0/1	0/1/0	0/1/1	1/0/0	1/0/1	1/1/0	1/1/1

6.3.1. FRU Data

The FRU Data format shall be compliant with the IPMI ver. 1.0 (per rev. 1.1 from Sep.25th , 1999) specification. The current version of these specification is available at http://developer.intel.com/design/servers/ipmi/specs.htm. The following is the exact listeng of the EEPROM content. During testing this should be followed and verified.

6.3.2. FRU Device protocol

The FRU device will implement the same protocols as the commonly used ATC24C02 device, including Byte Read, Sequential Read, Byte Write, and Page Read protocols.

6.3.3. FRU Data Format

The information to be contained in the FRU device is shown in the following table.

Table 33 - EEPROM Addressing

Area Type	Description
Common Header	As defined by the FRU document
Internal Use Area	Not required, do not reserve
Chassis Info Area	Not applicable, do not reserve
Board Info Area	Not applicable, do not reserve
Product Info Area	As defined by the IPMI FRU document. Product information shall be defined as follows:
Field Name	**Field Description**
Manufacturer Name	3Y Power
Product Name	YH-5301EAR
Product part/model number	Customer part number
Product Version	Customer current revision
Product Serial Number	{Defined at time of manufacture}
Asset Tag	{Not used, code is zero length byte}
FRU File ID	uRP1H300UHP20000Rxx
PAD Bytes	{Added as necessary to allow for 8-byte offset to next area}
Multi-Record Area	As defined by the IPMI FRU document. The following record types shall be used on this power supply: - Power Supply Information (Record Type 0x00) - DC Output (Record Type 0x01) No other record types are required for the power supply. Multi-Record information shall be defined as follows:
Field Name (PS Info)	**Field Information Definition**
Overall Capacity (watts)	300
Peak VA	
Inrush current (A)	0
Inrush interval (msec)	0
Low end input voltage range 1	90
High end input voltage range 1	264
Low end input voltage range 2	40
High end input voltage range 2	72
A/C dropout total. (msec)	20
Binary flags	Set for: Hot Swap support, Auto switch, and PFC
Peak Wattage	Set for: 400 Watts
Combined wattage	None
Predictive fail tach support	Supported
Field Name (Output)	Field Description: Two outputs are to be defined from #1 to #2, as follows: +12V and +5Vsb.
Output Information	Set for: Standby on +5Vsb, No Standby on all others.
All other output fields	Format per IPMI specification, using parameters in this specification.

7. ENVIRONMENTAL

The PDB shall operate normally, and sustain no damage as a result of the environmental conditions listed in this chapter.

7.1. Temperature

Operating Ambient, normal mode (inlet Air): -5℃ mi n/+50℃ max at 5000m above sea level.
(At full load, with a maximum rate of change of 5℃/10 minutes, but no more than 10℃/hr)
Operating Ambient, stand-by mode (inlet Air): -5℃ min/+50℃ max at 5000m above sea level.
Non-operating ambient: -40℃ to +70℃ (Maximum rat e of change shall be 20℃/hr)

7.2. Humidity

Operating: up to 85% relative humidity (non-condensing)
Non-operating: up to 95% relative humidity (non-condensing)
Note: 95% relative humidity is achieved with a dry bulb temperature of 55℃ and a wet bulb temperature of 54℃.

7.3. Altitude

A) Operation : sea level to 5000m

B) Non-Operation : sea level to 15200m

7.4. Vibration

A) Operation : 0.01G^2/Hz at 10Hz, 0.02G^2/Hz at 20Hz.

B) Non-Operation :

- **Sine sweep:** 5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15min at each of 3 resonant points;
- **Random profile:** 5Hz @ 0.01g^2/Hz to 20Hz @ 0.02g^2 (slope up): 20Hz to 500Hz @ 0.02g^2/Hz (flat); Input acceleration = 3.13gRMS; 10min. per axis for 3 axis on all samples

7.5. Mechanical Shock

A) Operation: 10G, no malfunction

B) Non operating: 50G Trapezoidal Wave, Velocity change = 4.3m/sec. Three drops in each of six directions are applied to each of the samples.

7.6. Thermal shock (Shipping)

Non-operating: -40℃ to +70℃, 50 cycles, 30℃/min. ≥ transition time ≥ 15℃/min., duration of exposure to temperature extremes for each half cycle shall be 30minutes.

7.7. Catastrophic Failure

The PDB shall be designed to fail without startling noise or excessive smoke.

7.8. EMI

The power supply shall comply with FCC part 15, CRISP 22 and EN55022; Class B for both conducted and radiated emissions with a 3dB margin. Test shall be conducted using a shielded DC output cable to a shielded load. The load shall be adjusted to 100% load. Test will be performed at 100VAC @ 50Hz, 120VAC @ 60Hz, and 230VAC @ 50Hz power.

The power supply shall comply with EN55024.

The power supply when installed in the system must meet the following all the immunity requirements when integrated into the end system.

7.9. Magnetic Leakage Fields

The PFC choke magnetic leakage field shall not cause any interference with a high resolution computer monitor placed next to or on top of the chassis.

7.10. Voltage Fluctuations and Flicker

The power supply shall meet the specified limits of EN61000-3-3, for voltage fluctuations and flicker for equipment ≤ 16 amps connected to low voltage distribution systems.

8. REGULATORY Requirements

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, residential, alarm systems, test equipment, etc.) other than ITE application, may require further evaluation.

8.1. Product Safety Compliance

A) UL 60950-1/CSA 60950-1 Edition 2 (USA/Canada)
B) EN60950-1 Edition 2 (Europe)
C) IEC60950-1 Edition 2 (International)
D) CB Certificate & Report, IEC60950-1 Edition 2 (report to include all country national deviations)
E) CE – Low Voltage Directive 2006/95/EC (Europe)
F) BSMI (Taiwan)
G) GB4943-CBCA Certification (China)

8.2. Product EMC Compliance – Class B Compliance

Note: The product is required to comply with Class B emission, as the system it is build into might be configured with the intend for commercial environment or home use. The Power supply is to have a minimum of 3dB margin to Class B Limits to support 3Y's Standard margin requirements.

A) FCC / ICES-003 Emission (USA/Canada) Verification
B) CRISP 22 – Emission (International)
C) EN55022 – Emission (Europe)
D) EN55024 – Immunity (Europe)
  - EN61000-4-2 Electrostatic Discharge
  - EN61000-4-3 Radiated RFI Immunity
  - EN61000-4-4 Electrical Fast Transients
  - EN61000-4-5 Electrical Surge
  - EN61000-4-6 RF Conducted
  - EN61000-4-8 Power Frequency Magnetic Fields
  - EN61000-4-11 Voltage Dips and Interruptions
E) EN61000-3-2 – Harmonics (Europe)
F) EN61000-3-3 – Voltage Flicker (Europe)
G) CE – EMC Directive 2004/108/EEC (Europe)
H) BSMI (Taiwan)
I) GB 9254 2008 (EMC) Certification (China)
J) GB 17625.1 – (Harmonics) CNCA Certification (China)

8.3. Maximum Leakage current to ground

3.5mA max for each power supply at 240Vac.

8.3.1. Hi-pot

The power supply module in the system shall be test at 1800Vac, with a trigger limit of 30mA.

8.4. Electrostatic Discharge (ESD)

In addition to IEC 801-2/ IEC1000-4-2, the following ESD tests shall be conducted. Each surface area of the system under test shall be subjected to twenty (20) successive static discharges, at each of the following voltages: 2kV , 3kV , 4kV , 5kV , 6kV , 7kV , 8kV , 10kV , 15kV.

Performance criteria:

a) All power system output shall continue to operate within the limits of this specification, without glitches or interruption, while the supply is operated as defined and subjected to 2kV through 15kV ESD pulses. The direct ESD event shall not cause any out of regulation condition. The power system shall withstand these tests without nuisance trips.

b) The power system, while operating as defined, shall not have a component failure when subjected to any discharge voltages up to and including 15kV. Component failure is defined as any malfunction of the power supply caused by component degradation or failure requiring component replacement to correct the problem.

8.5. Certifications / Registrations/ Declerations

A) UL Certification (US)
B) cUL Certification (Canada)
C) CB Certification & Report
D) FCC/ICES-003 Class B Attestation (USA/Canada)
E) TÜV Rheinland (Germany)
F) CE Declaration of Conformity (CENELEC Europe)
G) BSMI (Taiwan)
H) CCC / CNCA Certification (China)

8.6. Comonent Regulation Requirements

1. All Fans shall have the minimum certifications: UL and TÜV or VDE
2. All current limiting devices shall have UL and TÜV or VDE certifications and shall be suitable rated for the application where the device In its application complies with IEC60950.
3. All printed wiring boards shall be rated UL94V-0 and be sourced from a UL approved printing wiring board manufacturer.
4. All connectors shall be UL recognized and have a UL flame rating of UL94V-0
5. All wiring harnesses shall be sourced from a UL approved wiring harness manufacturer.
   SELV cable to be rated minimum 80V @ 120℃
6. Product safety label must be printed on UL approved label stock and printer ribbon.
   Alternatively labels can be purchased from a UL approved label manufacturer.
7. The product must be marked with the correct regulatory markings to support the certifications that are specified in this document.

8.6.1. Product Ecology Requirement

All materials, parts and subassemblies must not contain restricted materials as defined in directive 2002/95/EC, Restriction of Hazardous Substances (RoHS) 6/6.

All cords and cables shall contain <100ppm of cadmium.

All packing materials must be marked with applicable recycling logos for Europe (green dot) and Japan (Eco-marks), if sold as a retail product. All packing materials shall be recyclable.

9. Reliability / Waranty / Service

9.1. Component De-rating

The following component de-rating guidelines shall be followed:

1. Semiconductor junction temperature shall not exceed 115℃ with an ambient of 40℃. Any exceptions are subject to final approval.
2. Transformer temperature shall not exceed 115℃ w ith an ambient of 40℃. Any exceptions are subject to final approval.
3. Inductor case temperature shall not exceed 85% of rated temperature in ℃.
4. Capacitor case temperature shall not exceed 85% of rated temperature in ℃.
5. Resistor wattage de-rating shall be >30%.
6. Component voltage and current de-rating shall ≥ 20% at operating temperature. During abnormal conditions (such as a short circuit and the like) no de-rating is allowed as long as each component max rating is not exceeded. Any exception are subject to final approval.

9.2. Component Life requirement

All components life expectancy requirements in min. 3 years, calculated for 100% of max continues load @ 50℃ ambient temperature and @ 100VAC line voltage.

9.3. Mean Time between Failures (MTBF)

The power supply shall have a minimum MTBF at continuous operation of 200,000 hours calculated at 100%, according to BELL CORE TR-322 at 25℃ excludi ng the Fan MTBF, and at least 100,000 hours including the fan MTBF.

9.4. Warranty

The Warranty for the power supply is 36 months (three years) from production date code.

9.5. Serviceability

No troubleshooting by maintenance personnel is to be performed. Units shall be returned to 3Y Power for any troubleshooting, unless agreed by both parties.

The power supply will lose warranty if opened other than 3Y service personal or agreed by both parties.

10. MISCELLANEOUS

10.1. Marking

The PDB housing shall carry labels defined in this section.

10.1.1. Model label

Please refer to PLM system and check the label part number as below:

10.1.2. Notification of Hazard

The Power Supply shall carry a label warning towards hazardous voltages if the cover is removed.
It also should carry a non self troubleshoot marking in black on yellow ground,
as shown in below figure.

Figure 12 – Hazard Warning Label

10.1.3. Notification of Hot Surface

The Power Supply shall carry a label warning towards hot surface.
The marking shall be in black on yellow ground, as shown in below figure.

Figure 13 – Warning Hot Surface Label

10.1.4. Firmware ID Label (FW ID)

The Power Supply shall carry a Firmware ID label, which shall be human readable and in linear bar code Code 128 or QR-Code. The FW ID shall contain the product series name, wattage, FW ID, Sub ID and Revision complying with below figure.

Figure 14 – FW ID label

uRP1H301UHP20000A00

ABCDE	FFf	G	H	IIii	JJ	K	kk
Product Name	Output rating	Input type	System Type	Protocol Type	Prot. Subtype	FW Major Rev.	FW Minor Rev.

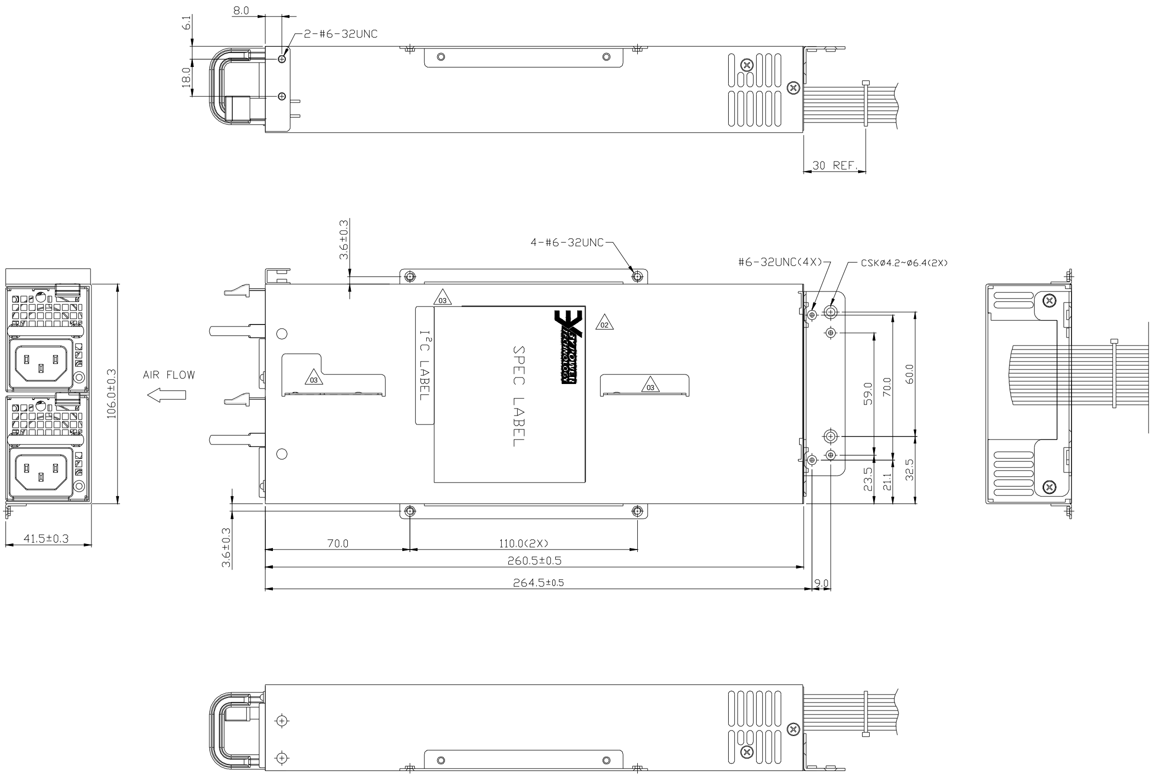
Definition

ABCDE	Product name reflects the Series name, for easy recognition of product series. E.g. SUNNY, OMEGA, JUNIP
FFf	Output rating (BB) is shown in dezimal notation with third digit (b) as dezimal exponent. E.g.: 651 = 65*10^1 = 650.
G	Represents the input version. A= AC-Input, D= DC-Input, U= Universal (PDB only)
H	Represents the System indicator. M = System Power Module, H = System Housing
IIiiJJ	EE = 1. digit: Protocol Type: e.g. "P" = PMBus, "S" = SMBus 2. digit: i2c byte length, "1" = 1-Byte data format, "2" = 2-Byte data format.yte; "2" = 2byte ee = Firmware protocol type coding, is reflected in numbers starting from "00", refer to table below for decoding FF = Protocol sub type, differed by characters of A-Z, 2-9, only inserted when Protocol has different settings in same HW & FW ID.
K	First letter of FW Rev. and the major rev. of the FW.
kk	"gg" = the sub Rev. indicator and will be upgraded when a minor function upgrade or bugfix will be released.

10.2. Outline Dimensions

The Power Supply shall have the dimension 106mm x 41.5mm x 260.5mm (WxHxL) without the card edge. Please see below Figure for details.

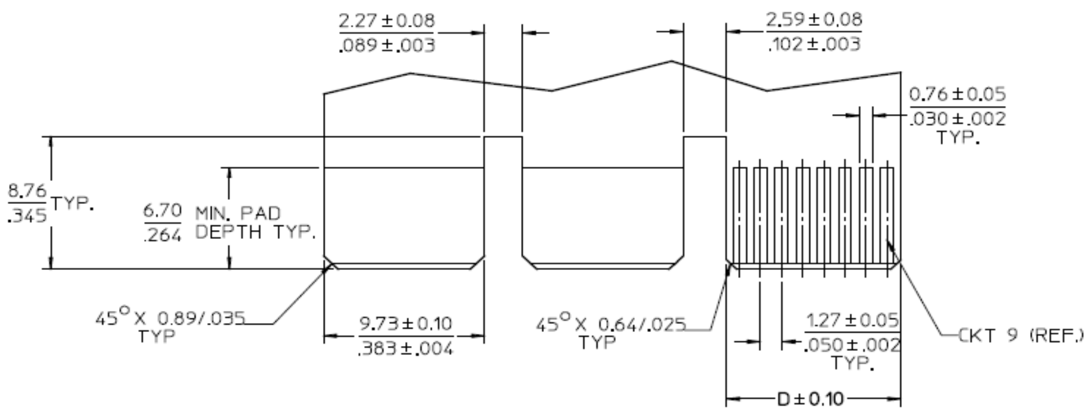
Figure 16 – Outline Drawing



10.2.1. Power Supply Card Edge Dimension

The Power Supply Card Edge shall comply with below specification.

Figure 17 – Card Edge Dimension



10.3. Packing

The Power Supply should be packed according to the description in this chapter.
The Packing for the power supply should be recyclable and has no metal parts to hold the packing.

10.3.1. Single Packing

TBD

10.3.1.1. Single Packing Label

TBD

10.3.2. Multi Packing

TBD

10.3.2.1. Multi Packing Label

TBD

10.3.3. Palletization

TBD

10.3.3.1. Pallet Label

TBD

11. PSMC Interface (PMBus – FW ID P20000)

Following Chapter provide details information of the utilized PSMC Interface protocol utilized. The Interface protocol can be recognized by it's ID.

By Default the PMBus shall be utilized to achieve the best compatibility with current applications.

A customization of the PSMC Interface is possible and would accordingly reflected in a different FW ID and different specification compared to the PMBus ones.

11.1. Data Formats

The Data format for Current, voltage, power, temperature, and fan speed shall use the PMBus linear format.

Linear data format: $X = Y \cdot 2^N$

X =the sensor value in volts, amps, watts, degrees C, or RPM
Y = mantissa
N = exponent. The exponents are fixed for each power supply and define the resolution for each sensor..

11.2. Power Sensors

The following PMBus commands shall be supported for the purpose of monitoring currents, voltages, and power. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output(s) of the power supply shall be zero amps and zero volts.

Table 34 – PMBus Sensor Commands

PMBus command	Description
READ_PIN	AC input power to the power supply in watts. This shall be monitored as close to the power supply's AC input connector as possible.
READ_FAN	Fan speed in RPM of fan sensor.
READ_IOUT	Output current in amps. For multi output power supplies the PAGE command shall be used to read the output currents. Smaller outputs like 5VSB that may not have a PMBus sensor may not support the READ_IOUT command.
READ_TEMP	Temperature in degrees C of temp sensor

11.2.1. VOUT_MODE

For reading output voltages the power supply shall support the VOUT_MODE command to report the output voltage formatting for the READ_VOUT command. The VOUT_MODE shall be set to Linear.

11.2.2. Sensor Averaging

The sensor registers for monitoring input/output power, current, and voltage shall contained averaged data, not instantaneous peak data. The power supply shall refresh the sensor data at a rate no slower than about once every second.

READ_IIN and READ_VIN shall contain RMS values over about a 1 second interval.

READ_PIN, READ_POUT, READ_IOUT, and READ_VOUT shall contain average values over about a 1 second interval.

11.3. Thermal management

The following command shall be supported for monitoring temperature, monitor fan speed, and controlling the power supply fan.

The fan monitoring shall be configured to provide a value in RPM. The fan control shall be in RPM. All temperature sensors and fans in the power supply shall be accessible via PMBus.

Command	Description
READ_TEMPERATURE_1, _2, _3	Returns the temperature in degrees C of temp sensor 1, 2, 3
READ_FAN_SPEED_1,_2,_3,_4	Returns the fan speed in RPM of fan sensor 1, 2, 3, 4
FAN_CONFIG_1_2	Returns the configuration of Fan 1 and Fan 2 in the power supply
FAN_CONFIG_3_4	Returns the configuration of Fan 3 and Fan 4 in the power supply
FAN_COMMAND_1, _2	Allows system to request fans in the power supply to be set to the defined RPM.
FAN_COMMAND_3, _4	The system cannot cause the power supply fan to run slower than the power supply needs for cooling.

FAN_CONFIG_1_2 & FAN_CONFIG_3, _4

Bit(s)	Meaning
7	Fan 1/3 presence
6	Fan 1/3 commanded in RPM
5:4	Not used
3	Fan 2/4 presence
2	Fan 2/4 commanded in RPM
1:0	Not used

11.4. Status commands

The following PMBus status commands shall be supported.

CLEAR_FAULTS
STATUS_WORD
STATUS_IOUT
STATUS_INPUT
STATUS_TEMPERATURE
STATUS_FANS_1_2
STATUS_FANS_3_4
STATUS_CML

11.5. Limit commands

The following PMBus commands shall be supported to allow the system to set warning limits. If one of the warning limits are exceeded the appropriate bit in the status register shall be set and the SMBAlert signal shall be asserted.

Command	Meaning
IOUT_OC_WARN_LIMIT	output over current warning limit
OT_WARN_LIMIT_1, _2, _3, _4	Over temperature warning limit for temp sensor n
IIN_OC_WARN_LIMIT	Input over current warning limit
POUT_OP_WARN_LIMIT	output over power warning limit
PIN_OP_WARN_LIMIT	Input over power warning limit

11.5.1. Default Limits for System Controllable Limits

The default values for system controllable limits shall be set to the power supplies maximum capabilities.

11.5.2. Manufacturer Controlled Limits

The limit for indicating a fan fault and warning condition is strictly controlled by the power supply manufacturer. No method shall be provided to allow the system to change these values.

All fault limits shall be set by the power supply manufacturer and is strictly controlled by the power supply manufacturer. No methods shall be provided to allow the system to change these values.

11.6. Faults and Error Correction

The power supply shall support PEC protocols as well as the STATUS_CML command to support error checking and handling. Unsupported commands may or may not respond with a NACK but must always set the communication error status bit in STATUS_CML.

11.7. Capability and inventory reporting

The follow commands shall be supported for discovery of the power supplies capabilities.

Command	Meaning
CAPABILITY	Defines the power supplies PEC support, bus speed, and support of SMBAlert
QUERY	Used to determine if the power supply supports a specific command. The PAGE command is used to QUERY a specific output of a multi output power supply

Revision and inventory information
PMBUS_REVISION
MFR_ID
MFR_MODEL
MFR_REVISION
MFR_LOCATION
MFR_DATE
MFR_SERIAL

Power supply ratings and capabilities
MFR_PIN_ACCURACY
MFR_VIN_MIN
MFR_VIN_MAX
MFR_IIN_MAX
MFR_PIN_MAX
MFR_VOUT_MIN
MFR_VOUT_MAX
MFR_IOUT_MAX
MFR_POUT_MAX
MFR_TAMBIENT_MAX
MFR_EFFICIENCY_LL
MFR_EFFICIENCY_HL

11.8. Write Protection

The WRITE_PROTECT command shall be supported in the following configurations. WRITE_PROTECT shall default to "1000 0000" to disable all commands but the WRITE_PROTECT when the power supply is powered off and back on.

Data Byte Value	Meaning
1000 0000	Disables all commands but the WRITE_PROTECT
0100 0000	Disables all commands but the WRITE_PROTECT and PAGE
0000 0000	Enables writes to all commands

11.9. Interrupts

The SMBAlert# side band interrupt signal shall be supported. The SMBAlert# signal shall assert as quickly as possible if any of the following events occur. It is desired to have less than a 2msec delay time for asserting the SMBAlert# signal whenever possible.

SMBAlert# assertion conditions
IOUT over current warning
IOUT over current fault
POUT over power warning
POUT over power fault
IIN over current warning
PIN over power warning
VIN under voltage warning
VIN under voltage fault
Power good de-asserts
Power supply failure

11.10. Firmware upgrade

The power supply module should support firmware upgrades via I2C bus.