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1. GENERAL DESCRIPTION

This specification describes the performance characteristics of a 650 watts hot swappable, 1+1 power system with +3.3V,+5V,+12V1,+12V2, +12V3,+12V4/0A, -12V main DC outputs, and 5V standby outputs. The system is configured to hold two identical 650W power supply modules, 3Y model YM-2651B.

2. ELECTRICAL PERFORMANCE

2.1 AC Input

2.1.1. Input voltage and frequency

The power system shall be capable of supplying full rated output power in the voltage range of 115V to 264V from a single phase source. The system shall operate at any input frequency between 47 Hz and 63 Hz. The nominal voltage is 115V for a voltage source with a 115-132V range, and is 230V for a voltage source with a 180-264V range.

2.1.2. Input current and inrush current

INPUT VOLTAGE	MAX INPUT CURRENT per power supply module	MAX INRUSH CURRENT per power supply module
115VAC	8-4A	40A
230VAC	8-4A	60A

Table 1: Input steady state and inrush current

2.2. Input Current Harmonics

The input current drawn on the power line shall not exceed the limits set by IEC 1000-3-2 when the system is operated within the voltage and frequency described in Sec. 2.1.1.

2.3. Input Power Factor

The minimum power factor at full load shall be 0.98/115V 60 Hz and 0.94/230V 50 Hz.

2.4. Power On Off Control

2.4.1. DC on/off control

The power supply shall have a TTL compatible input for on/off control of the output voltages. This input shall be driven by an external signal, *PSON, referenced to the output voltage common. The external circuit providing *PSON shall be capable of sinking 4mA.

The output voltages shall turn on when *PSON is low (less than or equal to 0.8 V). They shall turn off when *PSON is high (greater than or equal to 2.4V). *PSON shall have no control over the 5V standby output voltage.

2.5. Output

2.5.1. Power good(system Power good)

The Power good signal have redundant function, Power good shall be a TTL compatible signal capable of sinking 4mA and sourcing 2mA. Power good low shall be a maximum of 0.4V. Power good high shall be a minimum of 2.4V.

Power good shall change from low to high between 100 and 500ms after the output attains a static operating level within the regulation limit specified in Sec. 2.5.3.2.

Power good shall change from high to low at least 1 ms before All output falls below its specified lower regulation limit.

Power good rise time shall be less than 100us with a maximum capacitive load of 47pF across the power good signal.

2.5.2. Stand-by power

The system shall provide a standby output of 5V +/- 5% with a current sourcing capability of 3A. The ripple and noise of this output shall be less than 50mVp-p. The output shall be active whenever AC power is applied to the unit. *PSON shall have no effect on this output.

2.5.3. Dc power

2.5.3.1. Output current capacity

Each of the 1+1 redundant power supply module shall be capable of supplying the output currents of Table 2 subject to the listed conditions and a total output power of 650 watts. Due to the active current share, the actual maximum steady state current from each output shall be about half of the maximum current specified.

OUTPUT	NOM VOLT	OUTPUT CURRENT			UNITS	CONDITION
		MIN	MAX	Peak		
1	+3.3V	1.5	20 #a		A	combined #a & #b power≦140W
2	+5V	1.0	20 #b		A	
3	+12V1	0.5	16	18	A	
4	+12V2	0.5	16	18	A	
5	+12V3	1.0	16	18	A	
6	+12V4	0	0	0	A	
7	-12V	0	0.5		A	
8	$+5V_{sb}$	0.1	3		A	

Table 2: Output current

Note:
1. +3.3V,+5V,+12V1,+12V2,+12V3, combined max power 629W @ 25℃,Total power 650W @ 25℃
2. +3.3V,+5V,+12V1,+12V2,+12V3, combined max power 479W @ 40℃,Total power 500W @ 40℃

2.5.3.2. Output voltage and ripple

The power system shall meet the regulation, ripple, and noise requirements of Table 3 for all line, load, temperature, and environmental conditions.

Ripple and noise shall be measured with 0.1uF of ceramic capacitance and 47uF of tantalum capacitance on each of the power supply output connector terminal. The ripple and noise shall be met over all load ranges and AC line voltages with 1 to 2 power supplies in parallel operation. The output noise requirements shall apply over a 0Hz to 20MHz bandwidth.

	Output voltage limits(V_{dc})			Ripple & Noise
Output	Minimum	Nominal	Maximum	Maximum
+3.3V	3.14V	3.30V	3.47V	$50mV_{p-p}$
+5V	4.80V	5.00V	5.25V	$50mV_{p-p}$
12V1,12V2,12V3	11.64V	12.00V	12.36V	$120mV_{p-p}$
-12V	-11.40V	-12.00V	-12.60V	$120mV_{p-p}$
5VSB	4.75V	5.00V	5.25V	$50mV_{p-p}$

Table 3: Output voltage regulation and ripple

2.5.3.3. Output voltage rise time

The rise time shall be less than 50 ms measured from 10% to 90%.

2.5.3.4. Output voltage hold up time

Upon loss of the nominal input voltage, all outputs shall remain in regulation for at least 20ms.

2.5.3.5. Temperature coefficient

The output voltage change with temperature shall be +/-0.05% per degree C or less.

2.5.3.6. Transient response

The following shall apply to the 3.3V, 5V, and 12V1,+12V2, +12V3, outputs:

Output voltage for each output shall recover to within 1 % of its steady state level in less than 1 ms under the following conditions:

1. Load step see Table 4, step load size
2. Repetition rate of 10 ms with 50 % duty cycle
3. Current slew rate is 0.5A/us or less.
4. Ac input voltage range as specified in Sec. 2.1.1
5. Capacitive loads specified in Sec.2.5.4.9 shall not be applied.

Output	△Step Load Size	Load Slew Rate	Capacitive Load
+3.3V	30% of max load	0.5A/us	1000uF
+5V	30% of max load	0.5A/us	1000uF
12V1,12V2,12V3	60% of max load	0.5A/us	2200uF
+5VSB	25% of max load	0.5A/us	1uF

Table 4: Transient Load Requirements

2.5.3.7. Efficiency

The minimum efficiency of the power system measured at an input voltage of 115V or 230V and the maximum load shall be 80%.

2.5.3.8. Remote sensing

The power supply shall have remote sense (ReturnS) to compensate for output ground drops for output voltages; +3.3V, +5V, +12V. The power supply system output shall have remote sense (3.3VS, 5VS, 12VS) to compensate for drops in the system for the +3.3V, +5V, and +12V outputs. The remote sense input impedance to the power supply shall be greater than 200 ohms on 3.3VS, 5VS, 12VS and RetrunS. Remote sense shall be able to compensate for a minimum of 200mV drop on the +3.3V and +5V outputs. Remote sense shall be able to compensate for a minimum of 400mV drop on the +12V output. The remote sense return (RetunS) shall be able to compensate for a minimum of 200mV drop in the power ground return. The current in any remote sense line shall be less than 5mA to minimum voltage sensing errors.

2.5.3.9. Capacitive loads

The power supply shall be stable and meet all requirements, except dynamic loading requirements, with following capacitive loading ranges.
Note : Up to 10,000uF of the +12V capacitive loading may be on the +12V1 output.

OUTPUT	MIN	MAX	Units
+3.3V	10	12,000	uF
+5V	10	12,000	uF
+12V	10	11,000	uF
-12V	1	350	uF
+5VSB	1	350	uF

Table 5: Capacitive Loading Conditions

2.5.4. Output protection

2.5.4.1. Over voltage protection

The power supply over voltage protection shall be locally sensed in the hot swap modules. The power supply shall shutdown and latch off after an over voltage condition occurs. This latch shall be cleared by toggling the PSON$^{\#}$ signal or by an AC power interruption. Table 6 contains the over voltage limits. The values are measured at the output of the power supply's connectors. The voltage shall never exceed the maximum levels when measured at the power pins of the power supply connector during any single point of fail. The voltage shall never trip any lower than the minimum levels when measured at the power pins of the power pins of the power supply connector.

Output Voltage	MIN(V)	MAX(V)
+3.3V	3.9V	4.5V
+5V	5.7V	6.5V
12V1,+12V2,+12V3	13.3V	14.5V

Table 6 : Over Voltage Limits

2.5.4.2. Short circuit protection

A short circuit placed on any output shall cause no damage to the system.

2.5.4.3. Over current protection

The power supply shall have current limit to prevent the +3.3V,+5V,and +12V output from exceeding the values shown in Table7. If the current limits are exceeded, the power supply shall shutdown and latch off. The latch will be cleared by toggling the PSON# signal or by an AC power interruption. The power supply shall not be damaged from repeated power cycling in this condition. -12V and 5VSB shall be protected under over current or shorted conditions so that no damage can occur to the power supply.

Voltage	Over Current Limit (lout limit)
+3.3V	22A minimum; 30A maximum
+5V	22A minimum; 30A maximum
+12V1,12V2,12V3,	19A minimum; 24A maximum

Table 7: Over Current Protection

2.6. Fault indication

When one of the power supply module in the system fails to provide output, the system shall provide:

2.6.1. PSAlert# (option)

This signal indicates that the power supply is experiencing a problem that the user should investigate. The signal shall activate in the case of over temperature, general failure, over current, over voltage, and under voltage, This signal may also indicate the power supply is reaching it and of life or is operating an environment exceeding the specified limits.

Signal type (Active low)	Open collector/ drain output from power supply. Pull-up to VSB located in system	
Alert#=High	OK	
Alert#=Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, Isink=4mA	0V	0.4V
Logic level high voltage, Isink=50uA		5.25V
Sink current, Alert#=low		4mA
Source current, Alert#=high		50uA

Table 7: Alert# signal characteristics

2.6.2. Audible alarm

An audible alarm shall sound. This alarm can be turned off by an active low TTL compatible open collector signal applied to alarm reset *ALMRST.

2.6.3. Logic alarm

A TTL compatible, active high signal shall become active. Two such signals shall be provided, each corresponding to one of the 1+1 modules. Each is capable to sink 5mA and source 400uA.

2.6.4. Forced Load Sharing

The +12V outputs shall have forced load sharing for PSU module . The corresponding output shall share within (+/-6.5%) at full load when operated in a redundant 1+1 configuration. The 5VSB outputs shall not have forced load sharing between power module

Example of load share accuracy: Power supply #1 = 20A
Power supply #2 > 18.7A and < 21.3A

2.6.5. Load Sharing Signal

The power supplies load share shall use a single load share bus signal connected between each corresponding output. If the load sharing is disabled by shorting the bus to ground, the power system shall continue to operate within regulation limits for loads less than or equal to the full load rating of each power supply. The failure of one power supply shall not effect the output voltages of the other supply still operating.

2.7. Timing requirements

These are the timing requirements for the power assembly operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 200ms. The +3.3V, +5V and +12V output voltages should start to rise at about the same time. All outputs must rise monotonically. The +5V output needs to be greater than the +3.3V output during any point of the voltage rise. The +5V output must never be greater than the +3.3V output by more than 2.25V. Each output voltage shall reach regulation within 50mS (T_{vout_on}) of each other during turn on of the power supply. Each output voltage shall fall out of regulation within 400ms (T_{vout_off}) of each other during trun off. Figure 3 and Figure 4 show the turn on and turn off timing requirements. In Figure4 ,the timing is shown with both AC and PSON# controlling the ON/OFF of the power supply.

Item	Description	MIN	MAX	Units
$T_{vout\ rise}$	Output voltage rise time from each main output	5	50	m
$T_{vout\ \_on}$	All main outputs must be within regulation of each other within this time		50	ms
$T_{vout\ \_off}$	All main outputs must leave regulation within this time		400	ms

Table 8 : output voltage timing

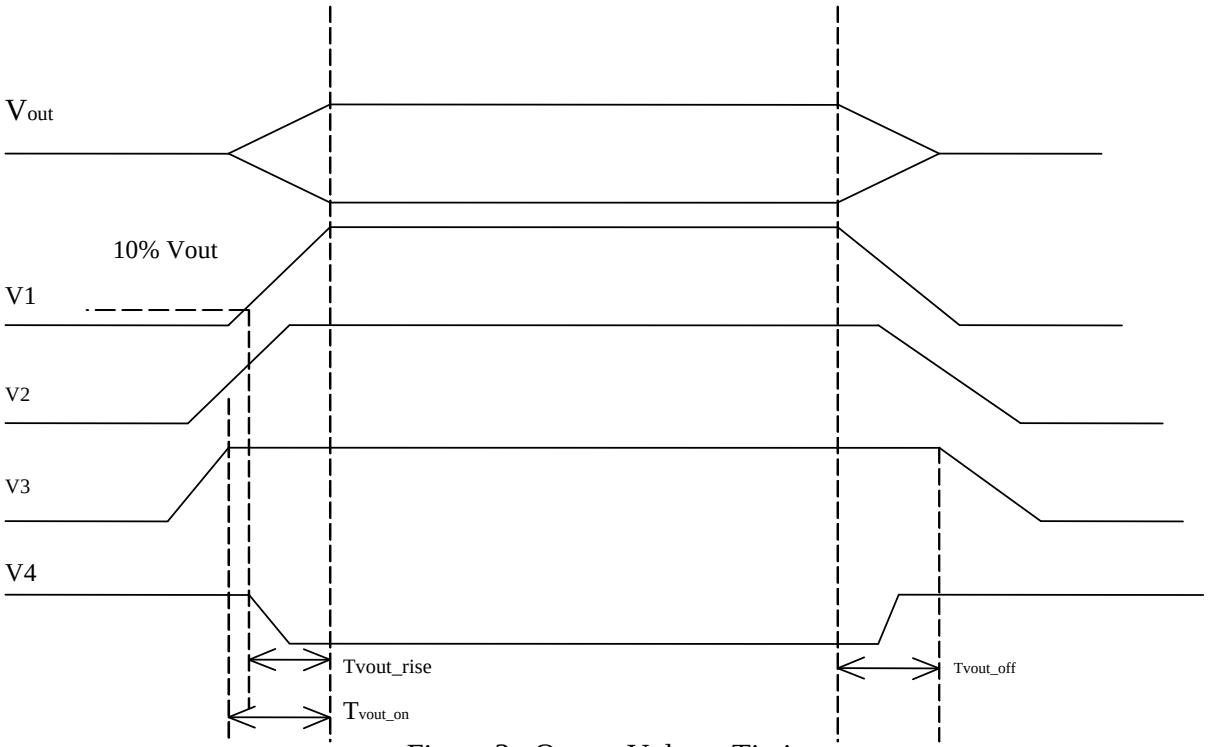


Figure 3 : Output Voltage Timing

Turn on	Description	Min	Max	Units
Tsb_on_delay	Delay from AC being applied to 5VSB being within regulation		1500	ms
Tac_on_delay	Delay from AC being applied to all output voltage being within regulation		2500	ms
Tvout_holdup	Time all output voltages stay within regulation after loss of AC	21		ms
Tpwok_holdup	Delay from loss of AC to deassertion of PWOK	20		ms
Tpson_on_delay	Delay from PSON# Active to output voltages within regulation limits	5	400	ms
Tpwok_on	Delay from output voltage(3.3V, 5V, 12V, -12V) within regulation limits to PWOK asserted at turn on	100	500	ms
Tpwok_off	Delay from PWOK deasserted to output voltages (3.3V, 5V, 12V, -12V) dropping out of regulation limits	1		ms
Tpwok_low	Duration of PWOK being in the deasserted state during an off/on cycle using AC or the PSON signal	100		ms
Tsb_vout	Delay from 5Vsb being in regulation to O/Ps being in regulation at AC turn on	50	1000	ms
Tsb_holdup	Time 5Vsb output voltage stays within regulation after loss of AC	70		ms

Table 9 : Turn on/off timing

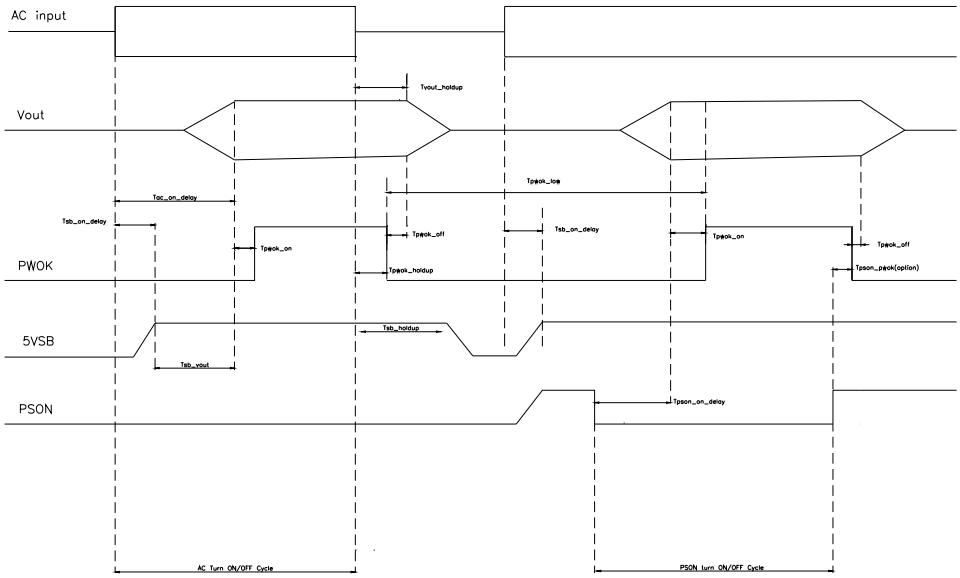


Figure 4: Turn on/off Timing

2.8. SMBus communication (option)

The serial bus communication devices for PSMI data in the power supply shall be compatible with both SMBUS and I2C Vdd based power and drive. This bus shall operate at 5V bus The SMBUS pull-ups are located on the motherboard and may be connected to 5V.

Two pins are allocated on the power supply. One pin is the serial clock (PSM clock). The second pin is used for serial data (PSM data). Both pins are bi-directional and are used to form a serial bus. The device(s) in the power supply shall be located at an address(s) determined by addressing pins A0 and A1 on the power supply module. The circuits inside the power supply shall derive their power from the 5VSB bus. Device(s)shall be powered from the system side of the 5VSB or'ing device. No pull-up resistors shall be on SCL or SDA inside the power supply. There pull-up resistors should be located external to the power supply.

2.9. Power supply management interface (option)

The PSMI device in the power supply shall derive its power off of the 5VSB output on the system side of the or'ing device and grounded to returns. It shall be located at an address set by the A0 and A1 pins. Refer to the PSMI specification posted on the www.ssiforum.org website for details on the power supply monitoring interface requirements. PSMI is a SMBus interface used to communicate power management information to the system

2.9.1. Power supply mangrement interface address (option)

PDB addressing A0/A1	0/0	0/1	1/0
Power supply PSMI device	(PSU1)B0h	(PSU2)B2h	(Power supply system)B4h

2.9.2. FRU data (option)

FRU data shall be stored starting in address location 8000h through 80FFh(ref). The FRU data format shall be compliant with the IPMI specifications. The current versions of these specification are available at: http://developer.intel.com/design/servers/ipmi/spec.htm

2.9.3. FRU data format (option)

The information to be contained in the FRU device is shown in the following table

Area type	Description
Common header	As defined by the FRU document
Internal use area	Not required, do not reserve
Chassis info area	Not required, do not reserve
Board info area	Not required, do not reserve

Table 10 : FRU device information

2.9.3.1. Product info area(option)

Implement as defined by the IPMI FRU document. Product information shall be defined as follows:

Field name	Field description
Manufacturer name	Formal name of manufacturer
Product name	Manufacturer’s model number
Product part/model number	Customer part number
Product version	Customer current revision
Product serial number	Defined at time of manufacture
Asset tag	Not used, code is zero length byte
FRU file ID	Not required
PAD bytes	Added as necessary to allow for 8-byte offset to next area

‘Table 11 : FRU device product information area

2.9.4. Multirecord area(option)

Implement as defined by the IPMI FRU document. The following record types shall be used on this power supply:

- Power supply information (Record type 0x00)
- DC output (Record type 0x01)
- No other record types are required for the power supply

Multi-Record information shall be defined as follows:

Field name (PS info)	Field information definition
Overall capacity (watts)	650
Peak VA	820
Inrush current (A)	60
Inrush interval (ms)	TBD
Low end input voltage range 1	90
High end input voltage range 1	132
Low end input voltage range 2	180
High end input voltage range 2	264
A/C dropout tol (ms)	20
Binary flags	Set for : Hot swap support, Autoswitch, and PFC
Peak wattage	TBD
Combined wattage	Set for 5V & 3.3V combined wattage of 140W
Predictive fail Tach support	Not supported, 00h value
Field name (output)	TBD
Output information	TBD
All other output fields	Format per IPMI specification, using parameters in the ERP12V specification

‘Table 12 : FRU device product information area

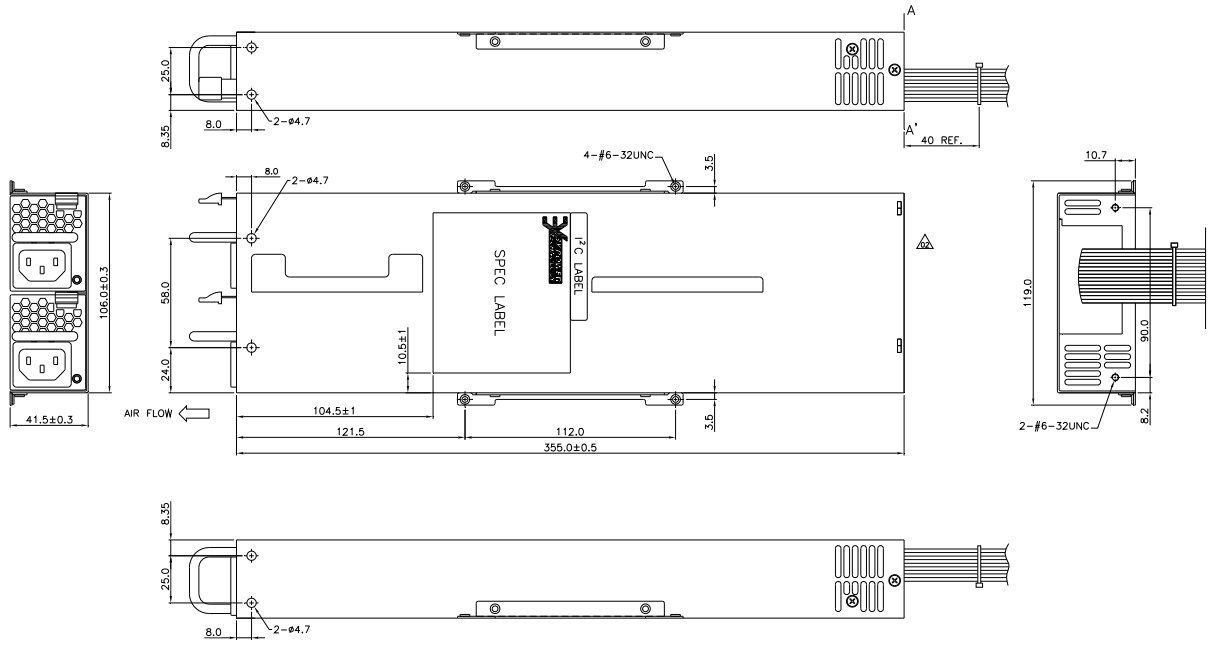
2.9.5. Power supply manager interface function (option)

Reference YH-8651AAR power supply manager interface function specification

3. MECHANICAL

3.1. Outside Dimension

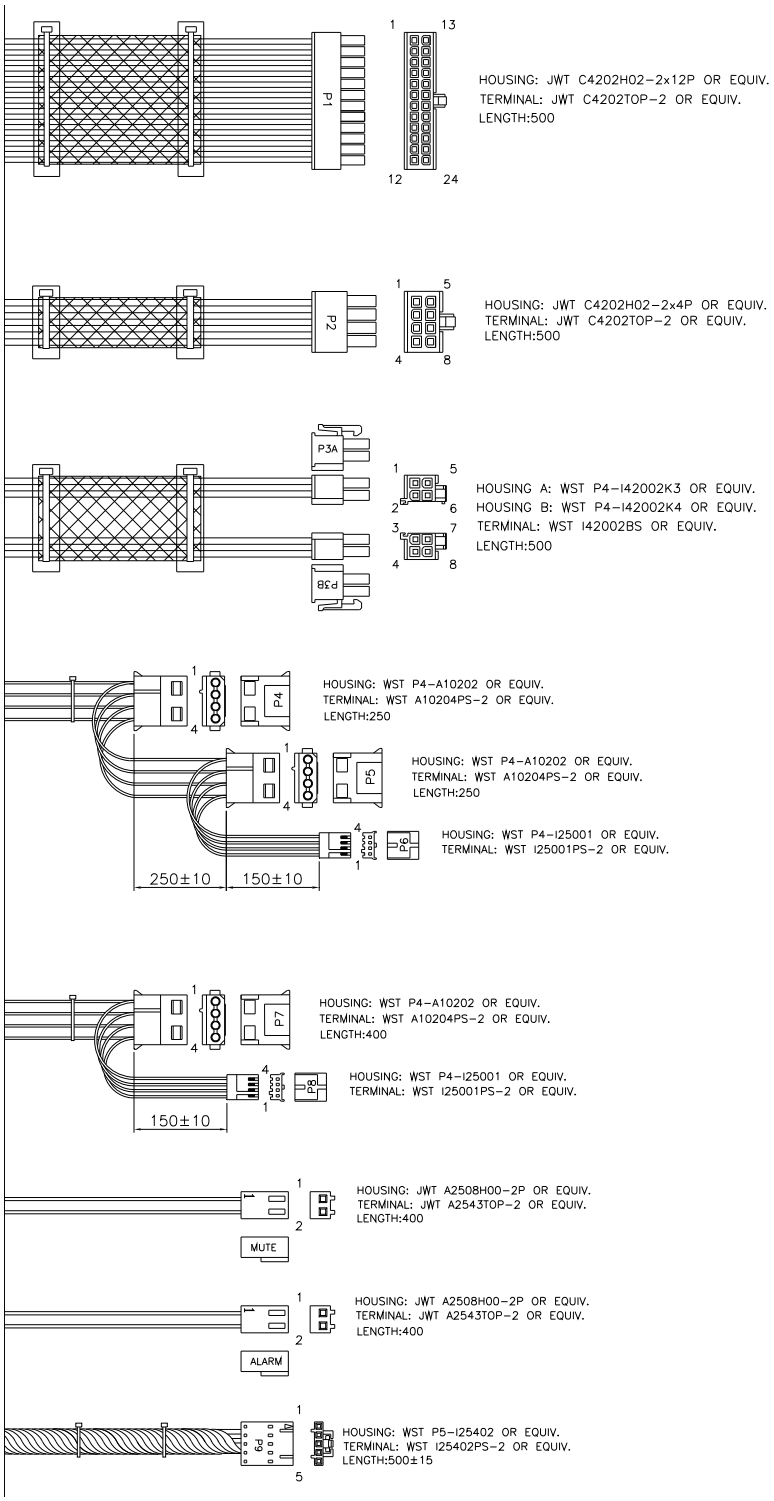
The casing dimension is W 106 mm x L 355 mm x H 41.5 mm



3.2. AC input connector

Each power module of the system shall have its own IEC 320 AC inlet.

3.3. Output cable connector



NOTES:

1. *OUTLINE DIMENSION : 41.5*106.0*355.0*
2. *IF CASE BY NCT PROCESS, THE TOLERENCE OF ALL DIMENSIONS MUST BE ENLARGED ±0.2 mm FOR CPK INSPECTION.*
3. *OUTPUT CONNECTOR & PIN ASSIGNMENT:*

	PIN NUM	PIN CON	COLOR	WIRE SPEC.
P1	1	+3.3V	ORANGE	UL1007 16AWG
		+3.3VS	ORANGE	UL1007 24AWG
	2	+3.3V	ORANGE	UL1007 16AWG
	3	GND	BLACK	UL1007 18AWG
	4	+5VS	RED	UL1007 24AWG
		+5V	RED	UL1007 18AWG
	5	GND	BLACK	UL1007 18AWG
		RS-GND	BLACK	UL1007 24AWG
	6	+5V	RED	UL1007 18AWG
	7	GND	BLACK	UL1007 18AWG
	8	PWR OK	GRAY	UL1007 24AWG
	9	+5VSB	PURPLE	UL1007 18AWG
	10	+12V3	YELLOW	UL1007 18AWG
		+12VS	YELLOW	UL1007 24AWG
	11	+12V3	YELLOW	UL1007 18AWG
	12	+3.3V	ORANGE	UL1007 16AWG
	13	+3.3V	ORANGE	UL1007 16AWG
	14	-12V	BLUE	UL1007 18AWG
	15	GND	BLACK	UL1007 18AWG
	16	PS-ON	GREEN	UL1007 24AWG
	17	GND	BLACK	UL1007 18AWG
	18	GND	BLACK	UL1007 18AWG
	19	GND	BLACK	UL1007 18AWG
	20	——	——	——
	21	+5V	RED	UL1007 18AWG
	22	+5V	RED	UL1007 18AWG
	23	+5V	RED	UL1007 18AWG
	24	GND	BLACK	UL1007 18AWG

	PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P2	1,2,3,4	GND	BLACK	UL1007 18AWG
	5,6,7,8	+12V1	YELLOW	

	PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P3 (P3A+P3B)	1,2,3,4	GND	BLACK	UL1007 18AWG
	5,6,7,8	+12V2	YELLOW	

	PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P4 P5	1	+12V2	YELLOW	UL1007 18AWG
	2	GND	BLACK	
	3	GND	BLACK	
	4	+5V	RED	
P6	1	+5V	RED	UL1007 22AWG
	2	GND	BLACK	
	3	GND	BLACK	
	4	+12V2	YELLOW	

	PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P7	1	+12V2	YELLOW	UL1007 18AWG
	2	GND	BLACK	
	3	GND	BLACK	
	4	+5V	RED	
P8	1	+5V	RED	UL1007 22AWG
	2	GND	BLACK	
	3	GND	BLACK	
	4	+12V2	YELLOW	

	PIN NUM	PIN CONN	COLOR	WIRE SPEC.
MUTE	1	ALARM MUTE (-)	BLACK	UL1007 24AWG
	2	ALARM MUTE (+)	YELLOW	

	PIN NUM	PIN CONN	COLOR	WIRE SPEC.
ALARM	1	TTL SIGNAL (-)	BLACK	UL1007 24AWG
	2	TTL SIGNAL (+)	RED	

	PIN NUM	PIN CONN	COLOR	WIRE SPEC.
P9	1	I^2CSCL	GRN/WHT	UL1007 24AWG
	2	I^2CSDA	YEL/WHT	
	3	PS_Alert	WHITE	
	4	GND	BLACK	
	5	——	——	

3.4. Grounding

The ground of the pins of the power assembly wire harness provides the power return path. The wire harness ground pins shall be connected to safety ground (power supply enclosure)

3.5. Temperature Range

Operating : 0 to 40 degrees C @500W
0 to 25 degrees C @650W
Storage : -40 to 70 degrees C

3.6. Humidity

The humidity range for both operating and storage shall be 5% to 90%,non - condensing.

4. REGULATORY

4.1 Safety Approval

UL, CUL, TUV, CE, CCC, CB

4.2. EMI

The system shall meet FCC class B, CISPR 22 class B.

4.3. Hi-pot

Each power supply module in the system shall be test at 1800Vac, with a trigger limit of 30mA.

4.4. Electrical Fast transient

The power supply shall comply with the surge voltage requirements of EN61000-4-5 level 3(2kV

Peak open circuit voltage from line/neutral to GND, and 1kV from line to neutral).

4.5. Surge immunity

The power supply shall operate normally when installed in a computer system and subjected to a power line noise described in EN61000-4-4, level 3 (2kV open circuit voltage). The test shall not cause any failure in the host computer system during line noise testing.

4.6. ESD

In addition to IEC 801-2/ IEC1000-4-2, the following ESD tests shall be conducted. Each surface area of the system under test shall be subjected to twenty (20) successive static discharges, at each of the following voltages: 2kV , 3kV , 4kV , 5kV , 6kV , 7kV , 8kV , 10kV , 15kV.

Performance criteria:

a) All power system output shall continue to operate within the limits of this specification, without glitches or interruption, while the supply is operated as defined and subjected to 2kV through 15kV ESD pulses. The direct ESD event shall not cause any out of regulation condition. The power system shall withstand these tests without nuisance trips.

b) The power system, while operating as defined, shall not have a component failure when subjected to any discharge voltages up to and including 15kV. Component failure is defined as any malfunction of the power supply caused by component degradation or failure requiring component replacement to correct the problem.

5. MISCELLANEOUS

5.1. Marking

5.1.1. Model label

6. RESTRICTION OF HAZARDOUS SUBSTANCE (ROHS) IN ELECTRICAL

The directive 2002/95/EC of the European Parliament and of the Council of the 27th January 2003, on the restriction of the use of certain hazardous substances in electrical and electronic equipment, requires the reduction of the substances Lead, Mercury, Cadmium, Hexavalent Chromium, Polybrominated Biphenyls (PBB), and Polybrominated Diphenyl Ethers (PBDE) in electronic products by July 1, 2006. Unless otherwise noted, all materials used will be compliant with this directive and any subsequent revisions or amendments.