VAST II (YH5851-xEARxAxD)

1U 1+1 Power Distribution Board

Specification

VAST II 850W AC-DC and DC-DC Switching Power Distribution Board

AC PSU has 80Plus Platinum compliant

AC + AC

DC + DC

Horizontal series

AC + DC (Mix)

[This Document describes the specification of a switching power supply complying to industrial standards, namely Server System Infrastructure (SSI) specification.]

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2. GENERAL SCOPE

This specification describes the performance characteristics of 850W AC-DC (YM-2851VCR) and DC-DC (YM-2851ECR) switching power distribution board (PDB) with a +12V main DC input and a +5Vsb auxiliary input. The PDB will switch into +3.3V, +5V and -12V main output and distribute +12V along with +5Vsb auxiliary. The PDB shall operate with a single power supply module (0+1) or redundant (1+1) configuration. Redundant configuration includes hot-pluggable and active load sharing features.

2.1. Features of PDB

Basic specification of PDB

Power	850W 1+1 redundant					
Dimension	Horizontal, 41.5mm(H) x 106mm(W) x 355mm(L)					
Outputs	+3.3V/25A$_{\#a}$	+5V/36A$_{\#b}$	-12V/0.5A	+12V/70A	+5Vsb/3A	#a + #b=210W
Regulation	±5%	±5%	+9/-5%	±5%	±5%	
Ripple/Noise	50mVp-p	50mVp-p	120mVp-p	120mVp-p	50mVp-p	
PSU	YM-2851VCR $_{80Plus\ Platinum\ compliant}$			YM-2851ECR		
PSU input range	AC $_{(C14)}$: 90 to 264VAC, 47Hz to 63Hz. HVDC $_{(C14)}$: 190 to 310VDC			DC $_{(Terminal)}$: -36 to -72VDC.		
Efficiency	Typ.>85% @115/230VAC, 850W			Typ.>85% @-48VDC, 850W.		
Power factor	Typ.>0.95 @115/230VAC, 850W			N/A		
Hold up time	Typ. 10ms$_{min.}$ @850W			Typ. 2ms$_{min.}$ @850W		
Operating Temp. and Humidity	-5 to 50 degree C. 95% $_{max.}$ Humidity.					
Protection	OVP, UVP, OCP, SCP, OTP, and Fan fail					
Outputs signal/TTL	Buzzer sound, buzzer reset, TTL, TTL1$_{\#option}$, TTL2$_{\#option}$, Alarm$_{\#option}$, PS-Alert, and PWOK.					
PSU module	Detail information reference AC or DC PSU specification.					

I²C

MCU Protocol	PMBus1.1$_{\#PDB}$
EEPROM	Follow IPMI

License

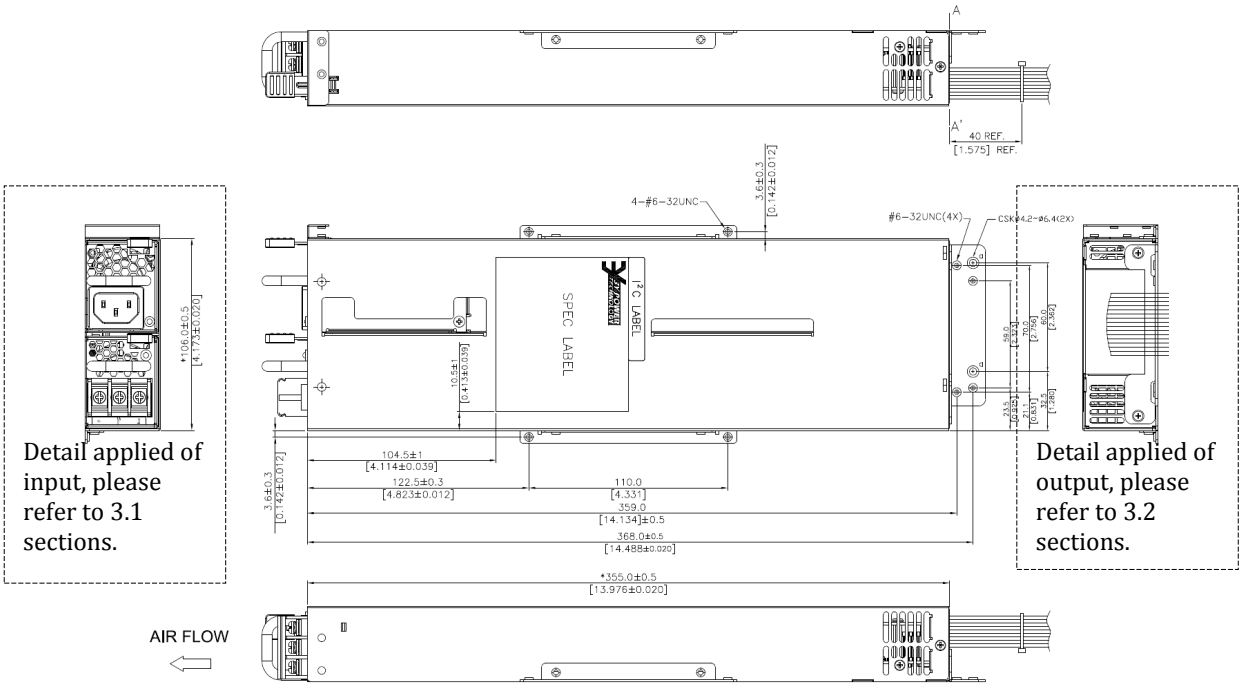
Safety/EMC	UL/cUL, TUV, CE, CB, FCC, BSMI$_{(without\ DC)}$, and CCC

2.2. Mechanical Overview

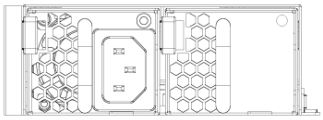
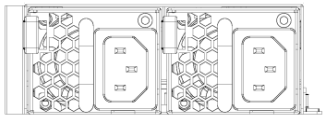
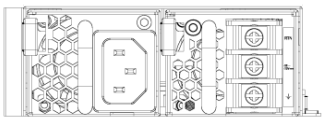
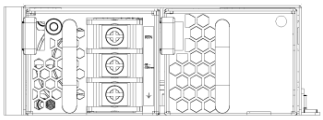
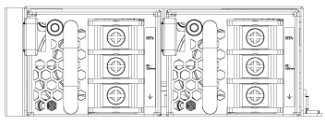
The physical size of the PDB enclosure is intended to accommodate power supplies with a power range of up to 850watts. The physical size is 41.5mm x 106mm x 355mm (height x width x length).

Input power plug(s) directly accesses to the front side of the power module(s).

Figure 1A – YH5851-xEARxAxD PDB Dimension



Power system assembly options

0 + 1 series	1 + 1 series	AC + DC mix series
 AC + dummy application 3Y Model name: 850W, YH5851-0EAR1A0D	 AC + AC application 3Y Model name: 850W, YH5851-1EAR2A0D	 AC + DC application 3Y Model name: 850W, YH5851-1EAR1A1D
 DC +dummy application 3Y Model name: 850W, YH5851-0EAR0A1D	 DC + DC application 3Y Model name: 850W, YH5851-1EAR0A2D	

Input type	Model name of 850W module
AC module name is	YM-2851VCR
DC module name is	YM-2851ECR

2.2.1. DC Output Connector

Figure 2

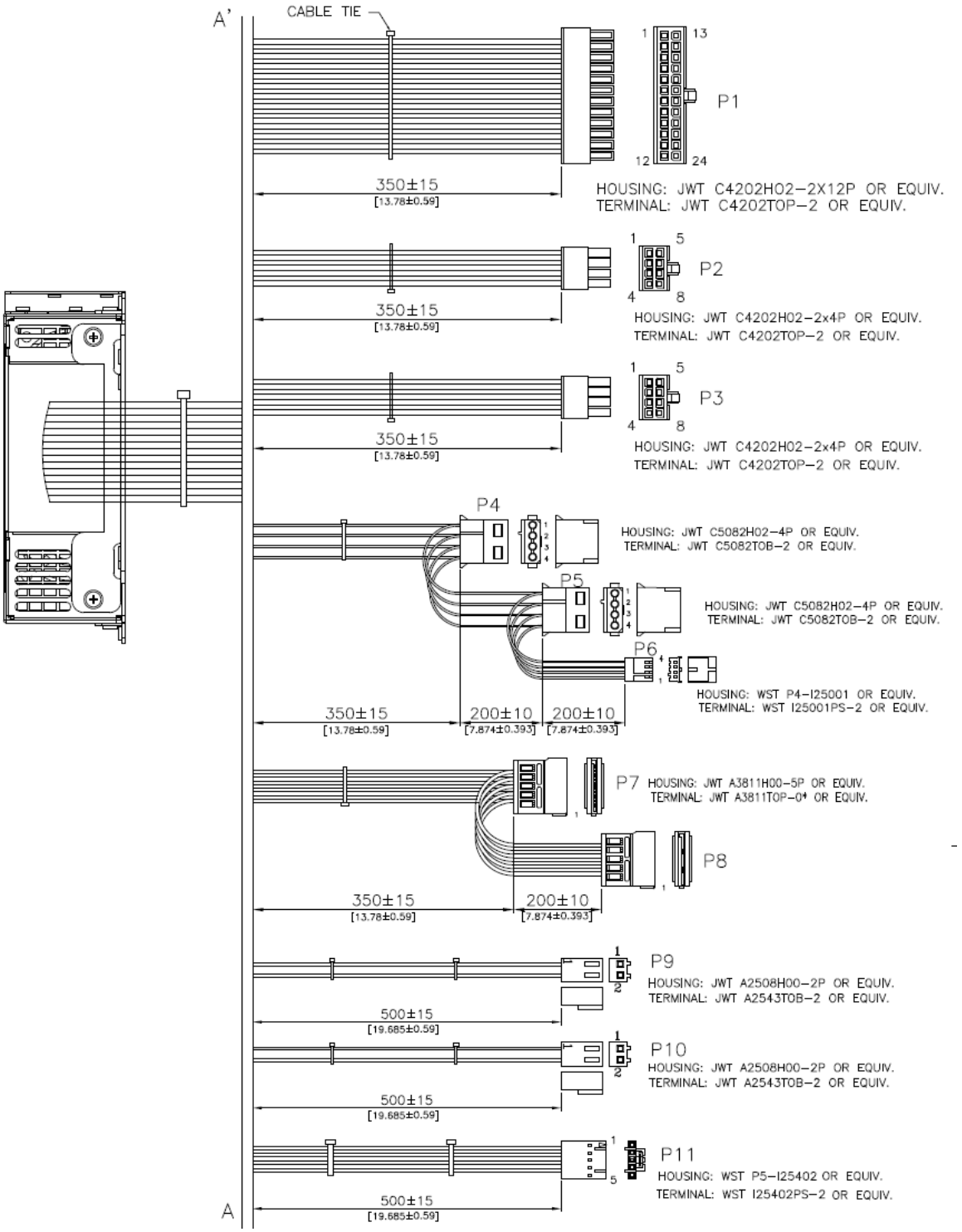


Table 1

NOTES:

1. OUTLINE DIMENSION : 355L*106W*41.5H mm (13.976L*4.173W*1.634H inch)
2. IF CASE BY NCT PROCESS, THE TOLERENCE OF ALL DIMENSIONS MUST BE ENLARGED ±0.2 mm FOR CPK INSPECTION.
3. OUTPUT CONNECTOR & PIN ASSIGNMENT:

P1

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	+3.3V	ORANGE	UL1007 18AWG
	+3.3VS	ORANGE	UL1007 24AWG
2	+3.3V	ORANGE	UL1007 18AWG
3	GND	BLACK	UL1007 18AWG
4	+5V	RED	UL1007 18AWG
	+5VS	RED	UL1007 24AWG
5	GND	BLACK	UL1007 18AWG
	RS-GND	BLACK	UL1007 24AWG
6	+5V	RED	UL1007 18AWG
7	GND	BLACK	UL1007 18AWG
8	PWOK	GRAY	UL1007 24AWG
9	+5VSB	PURPLE	UL1007 18AWG
10	+12V	YELLOW	UL1007 18AWG
	+12VS	YELLOW	UL1007 24AWG
11	+12V	YELLOW	UL1007 18AWG
12	+3.3V	ORANGE	UL1007 18AWG
13	+3.3V	ORANGE	UL1007 18AWG
14	-12V	BLUE	UL1007 18AWG
15	GND	BLACK	UL1007 18AWG
16	PS-ON	GREEN	UL1007 24AWG
17	GND	BLACK	UL1007 18AWG
18	GND	BLACK	UL1007 18AWG
19	GND	BLACK	UL1007 18AWG
20	——	——	——
21	+5V	RED	UL1007 18AWG
22	+5V	RED	UL1007 18AWG
23	+5V	RED	UL1007 18AWG
24	GND	BLACK	UL1007 18AWG

P2 P3

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	GND	BLACK	UL1007 18AWG
2	GND	BLACK	UL1007 18AWG
3	GND	BLACK	UL1007 18AWG
4	GND	BLACK	UL1007 18AWG
5	+12V	YELLOW	UL1007 18AWG
6	+12V	YELLOW	UL1007 18AWG
7	+12V	YELLOW	UL1007 18AWG
8	+12V	YELLOW	UL1007 18AWG

P4

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	+12V	YELLOW	UL1007 18AWG
2	GND	BLACK	UL1007 18AWG
3	GND	BLACK	UL1007 18AWG
4	+5V	RED	UL1007 18AWG

P5

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	+12V	YELLOW	UL1007 18AWG
2	GND	BLACK	UL1007 18AWG
3	GND	BLACK	UL1007 18AWG
4	+5V	RED	UL1007 18AWG

P6

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	+5V	RED	UL1007 22AWG
2	GND	BLACK	UL1007 22AWG
3	GND	BLACK	UL1007 22AWG
4	+12V	YELLOW	UL1007 22AWG

P7

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	+12V	YELLOW	UL1007 18AWG
2	GND	BLACK	UL1007 18AWG
3	+5V	RED	UL1007 18AWG
4	GND	BLACK	UL1007 18AWG
5	+3.3V	ORANGE	UL1007 18AWG

P8

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	+12V	YELLOW	UL1007 18AWG
2	GND	BLACK	UL1007 18AWG
3	+5V	RED	UL1007 18AWG
4	GND	BLACK	UL1007 18AWG
5	+3.3V	ORANGE	UL1007 18AWG

P9

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	TTL SIGNAL (-)	BLACK	UL1007 24AWG
2	TTL SIGNAL (+)	RED	UL1007 24AWG

P10

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	MUTE (-)	BLACK	UL1007 24AWG
2	MUTE (+)	YELLOW	UL1007 24AWG

P11

PIN NUM	PIN CON	COLOR	WIRE SPEC.
1	SCL	GRN/WHT	UL1007 24AWG
2	SDA	YEL/WHT	UL1007 24AWG
3	PS_ALERT	WHITE	UL1007 24AWG
4	GND	BLACK	UL1007 24AWG
5	———	———	———

2.3. Buzzer Sound and Identification

The PDB provides audio buzzer to indicate DC input power failure from power module(s) when power module(s) is installed..

The buzzer is driven by an internal circuitry and should sound in an 1+1 configuration even without AC or DC power.

The buzzer function can be switched off by hardware.

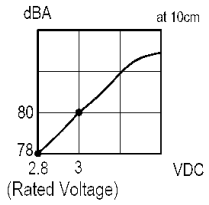
Audio buzzer could be switch off by shorted (pull low) mute connector (P10) (refer to 2.1.1)

The buzzer type (Vender): AX-1003-LF (ADVANCED) or equal.

Resonant frequency (rated voltage 3V) is: 2,700+/-300 Hz

Audio volume: 78dBA (minimum) with distance at 10cm/rated voltage 2.8V; 80dBA (minimum) with distance at 10cm/rated voltage 3V.

Frequency response curve



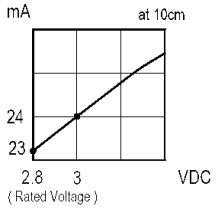


Table 2 – Buzzer Status Information

Power system condition	PDB Buzzer
No input AC or DC power to all PSU	OFF
No input AC or DC power to one PSU only	2Hz buzzing
Input AC or DC present/only standby output on	OFF
Power supply DC output ON and OK	OFF
One power module failure	1Hz buzzing
PDB fail	Steady buzzing

2.4. Enviornmental Requirements

The PDB shall operate within all specified limits over specified conditions in 2.4.1.

The defined operation conditions include temperature, humidity, altitude, shock and vibration.

2.4.1. Temperature and Humidity Requirements

The PDB shall operate normally within all specified limits of operating temperature and humidity range. All airflow shall pass through the PDB and not over the exterior surfaces of the PDB cage.

The power supply shall withstand thermal storage specified in $T_{non\text{-}OP}$ without any damage.

Table 3 – Temperature Requirements

Item	Description	MIN	MAX	Unit
T_{OP}	Operating temperature range.	-5	50	°C
ΔT	Max temperature rise across power supply		15	°C
$T_{non\text{-}OP}$	Non-Operating temperature range.	-40	70	°C
T_{Δ_change}	Rate of temperature change.		10	°C/hrs
H_{OP}	Operating humidity range, non condensing		85	%
$H_{non\text{-}OP}$	Non-Operating humidity range, non condensing		95	%

2.4.2. Altitude Requirements

The PDB shall operate normally within all specified limits of Altitude range.. The change pressure condition shall not harm the PDB and the operation within specified regulations shall be assured.

The PDB shall withstand Altitude storage specified in $A_{non\text{-}OP}$ without any damage.

Table 4 – Altitude Requirements

Item	Description	MIN	MAX	Unit
A_{OP}	Operating Altitude range.	0	5,000	m
$A_{non\text{-}OP}$	Non-Operating Altitude range.	0	15,000	m

2.4.3. Vibration and shock Requirements

The PDB shall operate within all specified limits of Shock vibration range.

The PDB shall withstand Shock Vibration storage specified in $G_{non\text{-}OP}$ without any damage.

Table 5 – Shock Vibration Requirements

Item	Description	MIN	MAX	Unit
G_{OP}	Operating Shock Vibration range.	0.01@10Hz	0.02@20Hz	G^2/Hz
G_{non-OP}	Non-Operating Shock Vibration range.	0.02@20Hz	0.02@1kHz	G^2/Hz
S_{OP}	Acceleration Shock while operation.		10	G
S_{non-OP}	Acceleration Shock non-operation		50	G

2.4.4. Acoustic Requirements

The PDB airflow shall be provided by the fan installed in the system or power module(s). The Fan's installed into the power module shall not exceed the below requirements noise requirements.

Table 6 – Acoustic Requirements

Operating Condition	Volumetric Flow, stand alone (CFM)	% of Maximum Loading Condition	Noise level (db)
Idle	7.927	40	42.3
Operating	11.786	60	50.6
Maximum	19.959	100	62.7

3. ELECTRICAL PERFORMANCE

3.1. Power Input Specification

3.1.1. Power Bus and Signal Connector

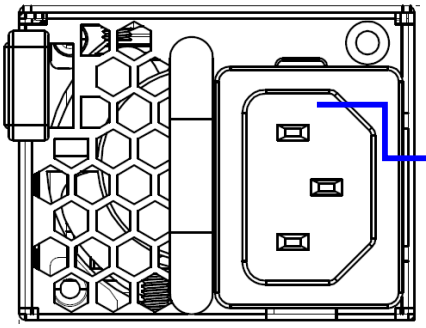
The PDB shall have a common Power Bus and signal connector complying to FCI interconnect series. The exact PN for the interconnect is FCI(10118868-003LF) & OUPIIN(9302-4S24H08P11ACB30DA)

The Pin definition shall comply with chapter 2.1 and shall provide +12VDC as main input and +5VsbDC as auxiliary input.

3.1.2. Power Inlet connector

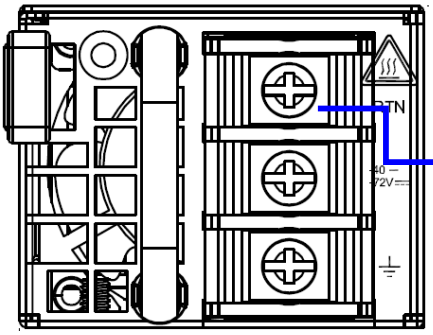
The PDB has no direct power AC or DC inlet connector. The power inlet shall be found at the power module. Depends on types of input power, the inlet connector shall comply requirements as below:

AC Version: Comply with IEC60320 C-14 (ST-01A-BTT, SOLTEAM) power inlet connector specification. This inlet shall be rated for operation at 12.5A, 420VDC/VAC (LITTELFUSE).



Terminal NO.	Function
L / N	90~264VAC 190~310VDC
FG	FG

DC Version: Comply with DT-66-C11W-03 (DINKLE) connector specification. This connector shall be rated for operation at 25A/125VDC (LITTELFUSE).



Terminal NO.	Function	Polarity
T1	RTN	Positive pole
T2	-36- -72VDC	Negative pole
T3	FG	

3.1.3. Efficiency

The minimum efficiency of the power system measured at a AC input voltage of 115VAC/230VAC, or DC input voltage of -48VDC and the maximum load shall be 84%. Including five combined conditions.

3.1.4. Suspeceptibility Requirements

The power supply system with the PDB shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter, which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 7 – Performance criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec. limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.1.4.1. Electrical Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024 using the IEC 61000-4-2 test standard and performance criteria B defined in Annex B of CISPR 24.

3.1.4.2. Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024 using the IEC 61000-4-4 test standard and performance criteria B define in Annex B of CISPR 24.

3.1.4.3. Radiated Immunity

The power supply shall comply with the limits defined in EN55024 using the IEC61000-4-3 test standard and performance criteria A defined in Annex B of CISPR 24.

3.1.4.4. Line Surge Immunity

Each AC power supply shall meet the EN61000-4-5 directive and any additional requirements in IEC61000-4-5 and the Level 3 requirements for surge-withstand capability (2KV peak open circuit voltage from line/neutral to GND, and 1Kv from line to neutral) with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not cause any damage to the power supply.
- The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

Each DC power supply module shall meet the 500VDC peak open circuit voltage from -48VDC/RTN to GND, and 250VDC from -48VDC to RTN.

3.1.4.5. AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions.

“Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions.

“Surge” will be defined as a condition of AC line voltage rising above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 8 – AC Line SAG transient performance.

AC Line Sag (10sec interval between each sagging)				
Duration	**Sag**	**Operating AC voltage**	**Line frequency**	**Performance criteria**
Continuous	10%	Nominal AC voltage	50/60Hz	No loss of function or performance
0 to AC cycle	100%	Nominal AC voltage	50/60Hz	Loss of function or performance is acceptable, self-recoverable
>1 AC cycles	>10%	Nominal AC voltage	50/60Hz	Loss of function acceptable, self-recoverable
0 to 1/2 AC cycle	30%	Mid-point of nominal AC voltage	50/60Hz	No loss of function or performance

Table 9 – AC Line SURGE transient performance.

AC Line Surge				
Duration	**Surge**	**Operating ac voltage**	**Line frequency**	**Performance criteria**
Continuous	10%	Nominal AC voltage	50/60Hz	No loss of function or performance
0 to 1/2 AC cycle	30%	mid-point of nominal AC voltage	50/60Hz	No loss of function or performance

3.1.5. PDB Power Recovery

The PDB shall recover automatically (auto recover) after an input power failure. Input power failure is defined to be any loss of input power that exceeds the dropout criteria.

3.2. DC output voltages

3.2.1. Grounding

The output ground pins provides output power return path. The ground pins at the PDB shall be connected to

the safety ground (power supply enclosure) and PCB card edge. This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply system shall be provided a reliable protective earth ground. All secondary and D2D circuits shall be connected to protective earth ground. Resistance from ground (returns) to chassis shall not exceed DC 0.1Ω/AC 0.1 Ω. This path may be used to carry DC-current.

3.2.2. Output rating

The following table defines the power and current rating of the 850W PDB. All combinations of output power rails shall not exceed the maximum power rating as below table listed. The power supply system must meet both static and dynamic voltage regulation requirements.

The utilized power module defines the maximum output power of the PDB. In a mixed operation, the power module with the lower output power shall define the maximum output limit in order to achieve safe redundant operation. In the case of the maximum output power exceeded limitation at 0+1 operating condition, the power module shall latch off by OCP or OPP function. In 1+1 operating condition, active current share will force power supply activate the current share mode if output current on one of the power module exceed the maximum output rating.

The maximum combined steady output power shall be 850W when operate input voltage range from 90-264VAC,-36 - -72VDC, any output current combinations shall not effect.

Table 10– Output Power and Current Ratings

Output	Nom. voltage	Output current			Units	Condition
		MIN	MAX	Peak		
1	+3.3V	0	25 #a	N/A	A	Combined #a and #b power≦210W
2	+5V	0	36 #b	N/A	A	
3	-12V	0	0.5	N/A	A	
4	+12V	Follow PSU			A	
5	$5V_{sb}$	Follow PSU			A	

3.2.3. Voltage Regulation

The power supply shall meet the Voltage regulation when operating at steady state condition, dynamic, peak load, Hot swap conditions must be meet +/- 5%. These limits include the peak-peak ripple/noise.

The regulation of Table 11 shall be measured at the output connector of the power supply, subject to the dynamic loading conditions in paragraph 3.2.6.

Table 11 – Output Voltage regulation

Output	Output voltage limits(VDC)				
	Minimum	Nominal	Maximum	Unit	Tolerance
+3.3V	+3.135	+3.3	+3.47	V_{rms}	+5/-5%
+5V	+4.75	+5.0	+5.25	V_{rms}	+5/-5%
+12V	+11.4	+12.0	+12.6	V_{rms}	+5/-5%
-12V	-11.40	-12.0	-13.08	V_{rms}	+9/-5%
+5Vsb	+4.75	+5	+5.25	V_{rms}	+5/-5%

3.2.4. Ripple and Noise Regulation

Ripple and Noise is defined in table 12. Ripple and Noise shall be measured over a bandwidth of 0Hz to 20MHz at the power supply output connector. A 0.1μF ceramic capacitor and 10μF of tantalum capacitor shall be placed at each point of measurement. The measurement points shall be as close as possible to the point of load.

The ripple and noise shall follow specification under all defined load ranges and line defined regulation range with 1+1 power supplies in parallel operation.

Table 12– Ripple and Noise Regulation

Output	+3.3V	+5V	+12V	-12V	5VSB
Maximum ripple/noise	50mVp-p	50mVp-p	Follow PSU	120mVp-p	Follow PSU
Guarantee at load range	0-25A	0-36A	0-70A	0-0.5A	0-3A

3.2.5. Dynamic loading

The power supply shall operate within specified limits and meet regulation requirements for step loading and capacitive loading specified below.

The load transient repetition rate shall be tested between 50Hz to 5kHz at duty cycles ranging from 10%-90%. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load and the MAX load.

This shall be tested with no additional bulk capacitance added to the load.

Table 13 – Transient Load Requirements

Output	Δ Step size	Slew Rate	Capacitive Load
+3.3V	30% of max. load	0.5A/ μsec	1,000μF
+5V	30% of max. load	0.5A/ μsec	1,000μF
+12V	Follow PSU	Follow PSU	Follow PSU
+5Vsb	Follow PSU	Follow PSU	Follow PSU

3.2.6. Capacitive load

The power supply shall operate within specifications over the capacitive loading ranges defined below in table 14.

Table 14 – Capacitive Loading Conditions

Output	Min.	Max.
+3.3V	10μF	12,000μF
+5V	10μF	12,000μF
-12V	1μF	350μF
+12V	Follow PSU	Follow PSU
+5VSB	Follow PSU	Follow PSU

3.2.7. Maximum load change

The power supply shall continue to operate normally when there is a step change ≤ 1A/μsec, between minimum load and maximum load.

3.2.8. Close loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions including capacitive load ranges. A minimum of: 45 degrees phase margin and -10dB gain margin is required.

Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

3.2.9. Hot Swap Requirements

Hot Swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified. The hot swap test must be conducted when the system is operating under static, dynamic and zero loading conditions. The power supply can be hot swapped by the following method:

Extraction: The power supply may be removed from the system while operating with PSON# asserted, while in standby mode with PSON# de-asserted or with no AC applied. No connector damage should occur during un-mating of the power supply from the power distribution board (PDB).

Insertion: The power supply may be inserted into the system with PSON# asserted, with PSON# de-asserted or with no AC power present for that supply. No connector damage should occur due to the mating of the output and input connector.

In general a failed (of by internal latch or external control) supply may be removed, then replaced with a good power supply, however, hot swap needs to work with operational as well as failed power supplies. The newly inserted power supply will be turned on into standby or Power On mode once inserted.

3.2.10. Load sharing control

Follow PSU requirement.

3.3. Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 0.2 to 50ms. For +5Vsb, it is allowed to rise from 0.2 to 70ms. All main outputs shall rise positive monotonically and have a slop value between 0 V/ms to 0.1V/ms.

For 5Vsb output any 5ms segment of the 10% to 90% rise time waveform, a straight line draw between the end points of the waveform segment must have s slope ≥ [Vout, nominal /20]V/ms.

Each output voltage shall reach regulation within 50ms (T_{vout_on}) of during turn on of the power supply system. Each output voltage shall fall out of regulation within 400ms (T_{vout_off}) of during turn off.

Table below shows the timing requirements for the power supply being turned on and off via the input power, with PSON held low and the PSON signal, with the input power applied.

3.3.1. Output Voltage Timing

The timing of signals and outputs are specified in below Table 15 and illustrated in Figure 3, 4.

Table 15 - Turn on/off timing

Turn on	Description	Min	Max	Units
$T_{vout\ rise}$	Output voltage rise time for all main output	0.2	50	msec
	Output voltage rise time for auxiliary output 5Vsb	0.2	70	
$T_{vout\ on}$	All main outputs must be within regulation of each other within this time		50	
$T_{vout\ off}$	All main outputs must leave regulation within this time.		400	
$T_{sb\_on\_delay}$	Delay from AC or DC being applied to 5Vsb being within regulation		1500	
$T_{ac\_on\_delay}$	Delay from AC or DC being applied to all output voltage being within regulation		2500	
T_{vout_holdup}	Time all main output 12V voltages stay within regulation after loss of AC.	10		
	Time all main output 12V voltages stay within regulation after loss of DC.	2		
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	9		
	Delay from loss of DC to de-assertion of PWOK	1		
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limit	5	400	
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		50	
T_{pwok_on}	Delay from output voltage(3.3V, 5V, 12V, -12V) within regulation limits to PWOK asserted at turn on	100	500	
T_{pwok_off}	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1		
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal	100		
T_{sb_vout}	Delay from 5Vsb being in regulation to main output being in regulation at AC or DC turn on.	50	1000	
T_{5Vsb_holdup}	Time the 5Vsb output voltage stays within regulation after loss of AC or DC	70		

Figure 3 – Output Voltage timing

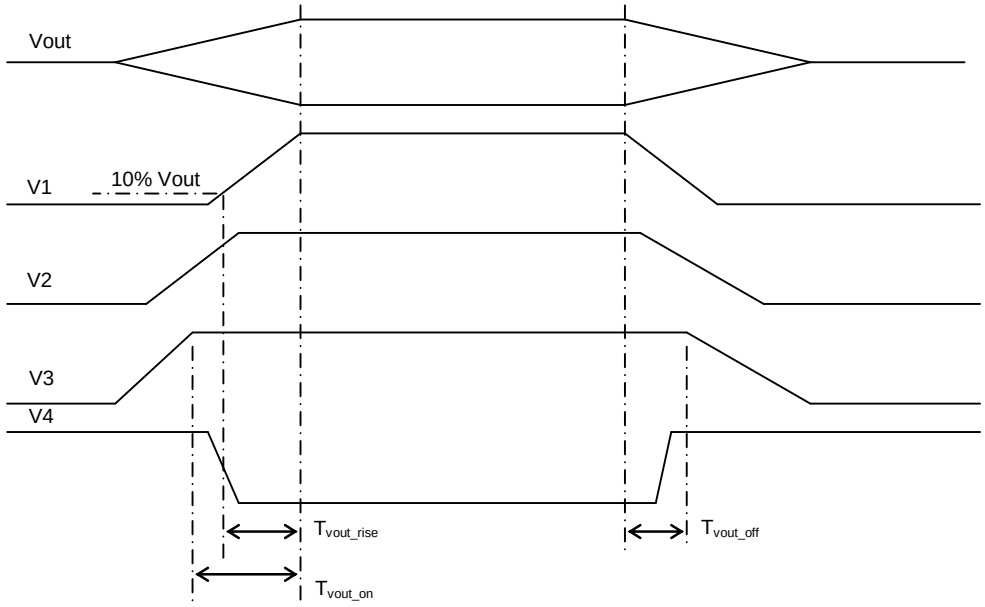
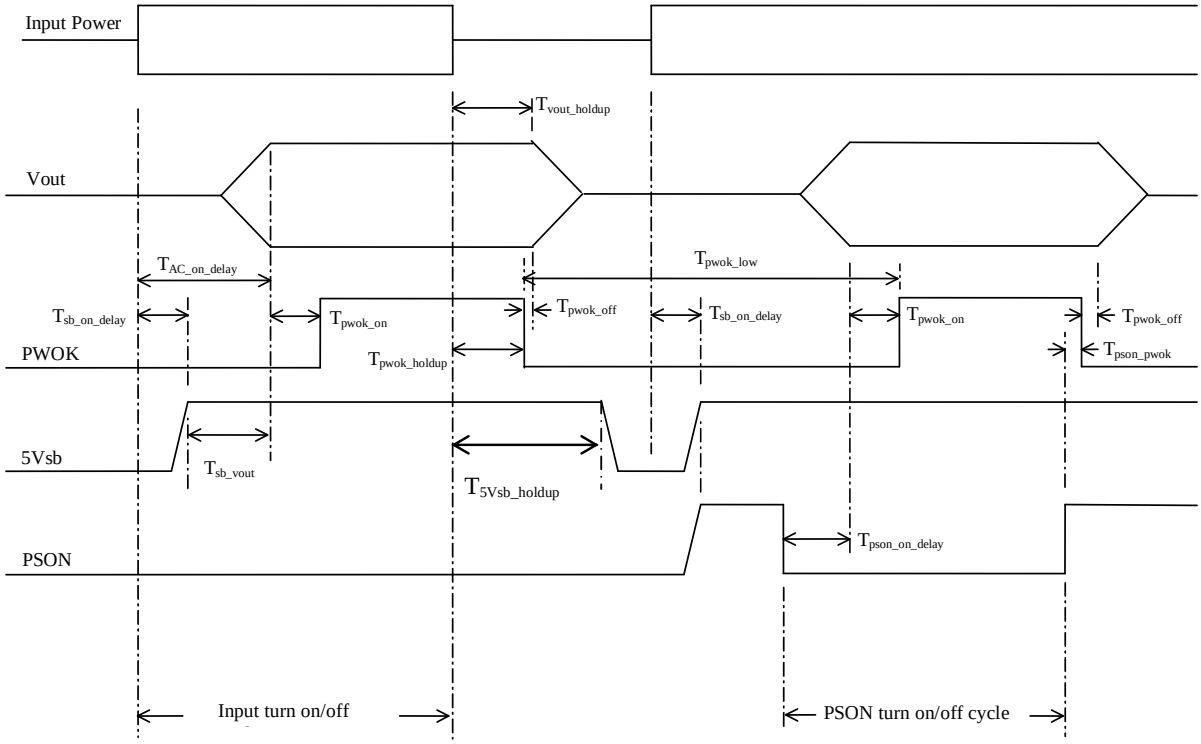


Figure 4 – Turn On/Off Timing (Power Supply Signals)



3.3.2. Overshoot

Any output overshoot at turn on shall be less than 5% of the nominal output value. Any overshoot shall recover to within the specified regulation in less than 0.5ms.

3.3.3. Undershoot

Any output shall not undershoot at turn on or off cycle under any circumstances.

3.3.4. Temperature coefficient

After operating for 30 minutes or longer at 25° C ambient, the output voltages shall not change by more than ± 0.05 % per degree C for any given line and load conditions.

3.4. Control and Indicator functions

The following sections define the input and output signals from the power supply.

Signals that can be defined as low true use the following convention:

Signal# = low true.

3.4.1. PSON# Input Signal (Power supply enable)

The PSON# signal is required to remotely turn on/off the main output of the power supply.

PSON# is and active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off.

PSON# is pulled to a standby voltage by a pull-up resistor internal to the power supply. See Table 16.

Table 16 – PS ON# signal characteristics

Signal Type	**Accepts an open collector/drain input from the system. Pul-up to Vsb located in the power supply.**	
PSON# = Low	ON	
PSON# = High or Open	OFF	
PSON# = Low, PSKILL = Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	1.0V
Logic level high (power supply OFF)	2.0V	5.25V
Source current, V_{pson} = low		1.4mA
Power up delay: $T_{pson\_on\_delay}$	5ms	400ms
PWOK delay: T_{pson_pwok}		50ms

Figure 5 – PSON# Signal Characteristic

3.4.2. Power OK (PG or PWOK) Output Signal

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, an internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit. See Table 17.

Table 17 – PWOK signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to Vsb located in power supply.**	
PWOK=High	Power Good	
PWOK=Low	Power Not Good	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{source} = 200μA	2.4V	5.25V
Sink current, PWOK=low		4mA
Source current, PWOK=high		200uA
PWOK delay: T_{pwok_on}	100ms	500ms
PWOK rise and fall time		100μsec
Power down delay: T_{pwok_off}	1ms	200ms

3.4.3. SMBAlert# (PSAlert) Output Signal Pin

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to critical events or warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

3.4.3.1. Thermal CLST(Close Loop system Throtting)

SMBAlert# shall also be utilized for warning of critical thermal component temperatures. The Thermal CLST(Close Loop system Throtting) shall assert when the component temperature, which shall be reported by a dedicated thermal probe, is reaching limitation of specified ΔT. The power supply shall report the temperature in addition to Thermal CLST(Close Loop system Throtting) through PMBus to the system, in order to increase fan speed to cool down environmental temperature.

This signal is to be asserted in parallel with LED turning solid red or blinking Red/Green or Red/Blue. See Table 18.

Table 18 – PSAlert# signal characteristics

Signal Type	Open collector/drain output from power supply. Pull-up to Vsb located in power supply.	
Alert#=High	Power OK	
Alert#=Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{sink} = 50μA	2.0V	3.46V
Sink current, Alert#=low		4mA
Sink current, Alert#=high		50μA
50μA rise and fall time		100μsec
Smart input power fail assertion		2msec
Thermal CLST ΔT to critical thermal	10°C	

3.4.4. Output TTL signal

TTL are power supply status signal and shall be pulled HIGH or LOW by the power supply to indicate that all inputs or outputs are within power supply action conditions. The standard PDB provides a single TTL outputs signal. The PDB could be provides maximum 3 channels to external TTL output signal required. The TTL, TTL1, TTL2, and Alarm signals could be defined from MCU adjust to require channel or disable. TTL outputs signal with different colors as the identification. Everyone TTL outputs signal are open collector output from power supply and pull up to Vsb located in power supply.

The TTL voltage level, source current and active conditions table

Channel name		TTL		TTL1		TTL2		Alarm	
Status		Total power good status		Module 1 status		Module 2 status		Total power fail status	
Support/Do not support		Support		Do not support		Do not support		Do not support	
Output cable number		P9		Reserved		Reserved		Reserved	
Pin number		1	2	1	2	1	2	1	2
Wire color		Black	Red	Black	White	Black	Blue	Black	Orange
Voltage level	Max.	0.4V	3.46V	0.4V	3.46V	0.4V	3.46V	0.4V	3.46V
	Min.	0V	2V	0V	2V	0V	2V	0V	2V
Maximum source current			5mA		5mA		5mA		5mA
Action conditions									
NO.	Description								
1	Without anyone module input.		Low		Low		Low		Low
2	Module 1 with AC or DC input, but without PS-ON, anyone module 2 without AC or DC input at housing.		Low		Low		Low		Low
3	Module 2 with AC or DC input, but without PS-ON, anyone module 1 without AC or DC		Low		Low		Low		Low

	input at housing.								
4	Module 1 and 2 with AC or DC input at PS-ON on stage.		High		High		High		Low
5	Module 1 with AC or DC input, and PS-ON, module 2 in the housing but without Ac or DC input.		Low		High		Low		Low
6	Module 2 with AC or DC input, and PS-ON, module 1 in the housing but without Ac or DC input.		Low		Low		High		Low
7	Module 1 with AC or DC input at PS-ON on stage, but without module 2.		High		High		Low		Low
8	Module 2 with AC or DC input at PS-ON on stage, but without module 1.		High		Low		High		Low
9	Module 1 happen OVP, UVP, OCP, OTP, and Fan fail… failure conditions, but module 2 working is normal.		Low		Low		High		High
10	Module 2 happen OVP, UVP, OCP, OTP, and Fan fail… failure conditions, but module 1 working is normal.		Low		High		Low		High
11	When anyone PDB happen OVP, UVO, OCP, and OTP… failure conditions.		Low		Low		Low		High

4. Protection circuits

Protection circuits (functions) inside the PDB shall turn off (latch off) the main output. If the power supply latches off due to a protection circuit assert, an input Power cycle OFF for 15sec or a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

4.1. Over Voltage Protection (OVP_{main} & $OVP_{auxilary\ AR}$)

All Over Voltage Condition shall be measured internal to the PDB on all outputs (Main and *Auxiliary Output*$_{AR}$) at the output connector. The PDB shall shutdown and latch off after an Over Voltage condition occurs on main output, *the auxiliary output shall be hiccup mode* ***(VsB$_{AR}$)*** *after the OVP had been removed*.

The voltages shall never exceed the maximum levels specified in below table when measured during any fail.

The PDB shall alert the system of the OCP/SCP condition via SMBAlert# and fail buzzer indicator.

The latch on the main output can be cleared by asserting the PSON# signal or by an input Power interruption.

Table 19 - Over Voltage Protection requirements

Output	Min	Max	Units
Main (+3.3V)	3.9	4.5	VOLTS
Main (+5V)	5.7	6.5	VOLTS
Main (+12V)	13.3	15.6	VOLTS

4.2. Over Current and Short Circuit Protection (OCP/SCP$_{main}$ & *OCP/SCP$_{auxilary\ AR}$*)

The Over Current Condition shall be measured internal to the PDB on all outputs (Main and *Auxiliary Output$_{AR}$*), and preventing outputs to exceed current limits specified in below table. The PDB shall shutdown and latch off when Over Current condition occur at main outputs, *the auxiliary output shall be hiccup mode* ***(VsB$_{AR}$)*** *after the OCP/SCP had been removed.*

The latch on the main output can be cleared by asserting PSON# signal or by an input Power interruption.

The PDB shall alert the system of the OCP/SCP condition via SMBAlert# and fail LED indicator.

The PDB shall not be damaged from repeated power cycling in this condition.

Table 20 – Over Current/Short Circuit Protection

Output	Over Current limit
Main (+3.3V)	110% MIN.; 150%MAX.
Main (+5V)	110% MIN.; 150%MAX.
Main (+12V)	110% MIN.; 150% MAX.

4.3. Over Temperature Protection (OTP$_{AR}$)

The PDB shall have thermal sensors to measure the environmental (T_{env}). The thermal sensor shall be part of a protection circuit to protect against over temperature conditions caused by loss of fan cooling or excessive ambient temperature. In a critical over temperature condition, specified in below table, the power system shall shutdown with the exception of the ***auxiliary output (VsB$_{AR}$)***.

The Thermal CLST shall be part of the ***OTP$_{AR}$***.

The PDB shall alert the system of the ***OTP$_{AR}$*** condition via SMBAlert# and buzzer. The PDB outputs will auto recover, after temperature drops into specification defined range. Power supply will not automatically recover and will latch off when the OTP is triggered by defective fan (fan fail).

Table 21 – Over Temperature ProtectionAR of PDB

Condition	Warning in °C	Critical in°C	Timing for SMBAlert#/LED
T_{env}	65	70	1msec
T_{comp}	84	89	1msec

The thermal sensors shall have an accuracy of max. 1°C per step and a tolerance of ± 10%.

5. Power Supply Management

5.1. Hardware Layer

The serial bus communication devices for Power Supply Management Controller (PSMC) and Field Replacement Unit (FRU) in the power supply shall be compatible with both SMBus 2.0 “high power” and I²C Vdd based power and drive specification.

This bus shall operate at +3.3V but be tolerant to +5V pull-ups. The power supply should not have any internal pull-ups on the SMBus, pull-ups shall be located on system side.

Two pins are allocated on the power supply. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Both pins are bi-directional and are used to form a serial bus. The device(s) in the power supply

shall be located at an address(s) determined by addressing pins A0 and A1 on the power supply module. The circuits inside the power supply shall derive their +3.3V power from the +5Vsb bus through a buffer. Device(s) shall be powered from the system side of the +5Vsb OR'ing device. No pull-up resistors shall be on SCL or SDA inside the power supply. The pull-up resistors should be located external to the power supply on system/application side.

5.1.1. Capancitance for SMBus

The recommended Capacitance per pin on SDA and SCL shall be 10pF, and is not allowed to exceed 40pF per pin. In a 1+1 configuration of up to two (2) power modules with additional PDB, the total Capacitance of each Bus pin shall not exceed 400pF.

5.1.2. I²C Bus noise requirement

The power supplies I²C bus's SDA and SCL line shall be clean from noise, which might affect the proper function when utilized with other devices.

The maximum allowed line noise on SDA or SCL is 350mV under 20MHz bandwidth condition.

5.1.3. Pull Ups

The main pull-ups are provided by the system and may be connected to +5V or +3.3V. For the system design, the main pull-ups shall be located external to the power supply and derive their power from the standby rail. In case the power supply requires pull-ups internal, the pull up resistance shall be relatively much weaker than system pull up resistance on SDA or SCL lines.

5.2. Power Supply Management Controller (PSMC)

The PSMC device on the PDB shall derive its power of the +5Vsb output on the system side of the OR'ing device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBus™ Power System Management Protocol Specification Part I and Part II in Revision 1.2 or later.

It shall be located at the address set by the A0, A1, and A2 pins.

Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details on the power supply monitoring interface requirements and refer to followed section of supported features. The below table reflect the power module addresses complying with the position in the housing.

Table 22 – PSMC Addressing for inserted power modules

PDB position and PSMC address	PM1 B0h/B1h	PM2 B2h/B3h	PDB 4Ah/4Bh
Pin A2/A1/A0	0/0/0	0/0/1	None

5.2.1. Related Documents

- PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.1.
- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.1.
- System Management Bus (SMBUS) Specification 2.0

5.2.2. Data Speed

The PSMC device on the PDB shall operate at the full 100kbps (100kHz) SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply is allowed to clock stretch while parsing a command or servicing multiple interrupts or NACK.

Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

5.2.3. Bus Errors

The PSMC shall support SMBus clock-low timeout ($T_{timeout}$). This capability requires the PSMC to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions within 10ms later. The total reset time from detection of the condition till restarted, ready to receive commands condition shall not exceed 35ms.

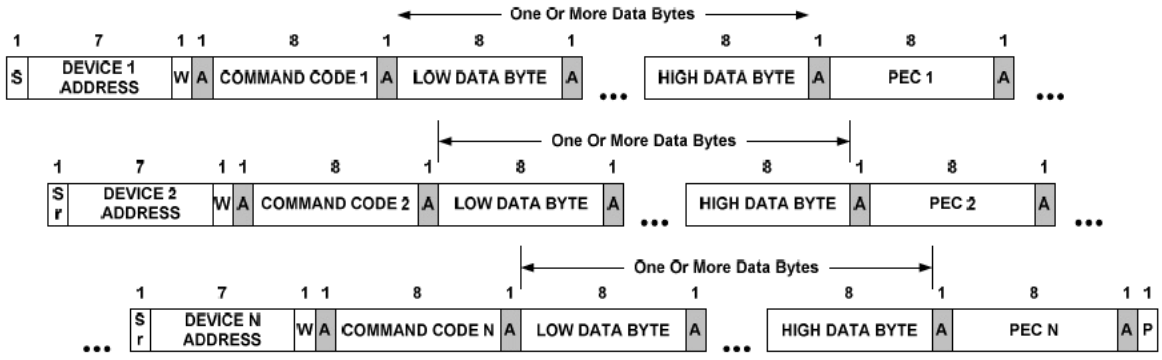
The device must recognize SMBus START and STOP conditions on ANY clock interval. The PSMC must not hang due to 'runt clocks', 'runt data', or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup. Or hold times that are shorter than the minimums specified by the SMBus specifications. The PSMC is not required to operate normally, but must return to normal operation once 'in spec' clock and data timing is again received. Note if the PSMC 'misses' a clock from the master due to noise or other bus errors, the device must continue to accept 'in spec' clocks and NACK. The PSMC is supposed to re-synch with the master on the next START or STOP condition.

5.2.4. Group Command

The Group Command is used to send commands to more than one PMBus device at a time. The commands are sent in one continuous transmission. When the PSMC detect the STOP condition that ends the sending of commands, it shall begin executing the command which it received or NACK, if the command is not supported.

The Group Command Protocol is not allowed to be used with commands that require the PSMC to respond to the data (only WRITES).

Figure 6 – Group Command with PEC



5.2.5. Extended Command

The Extended Command protocol allows for an extra 256 command codes. This command is similar to the Block-Write/Block-Read Word process call in the SMBus Specification, but allows an maximum length of 256

command codes. The first byte (the low data byte) is a reserved value indicating that the extended command format is being used. The second byte (the high order byte) is the command to be executed. This allows the standard commands to be extended by PMBus and Manufacture specific commands.

Command Extension Codes:

1. MFR_SPECIFIC_COMMAND EXT: FEh
2. PMBUS_COMMAND EXT: FFh

Please see below illustration for utilization:

Figure 7 – Extended Command Write

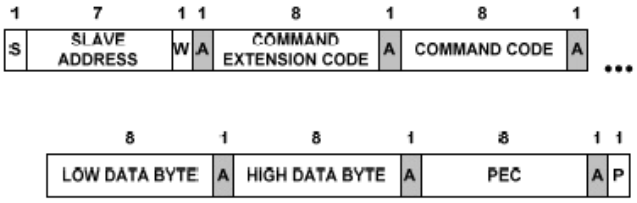
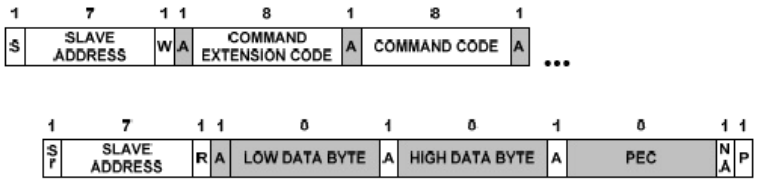


Figure 8 – Extended Command Read



Note: Not all PMBus functions are supported.

5.2.6. Write Protection (WP)

The PDB shall have a hardware pin for WP the memory of the PSMC for firmware updates and towards accidental EEPROM writes.

The WP is an active high signal and prevents any write to any memory. The WP needs to be pulled low in order to update the PSMC firmware or write to the EEPROM.

5.2.7. Firmware Updates

The PSMC shall support firmware updates over the SMBus. In order to perform firmware updates, the WP needs to be pulled low and appropriated Software tool are required to guaranty the successful update.

5.2.8. Sensor Accuracy

The sensor of the PSMC shall meet below accuracy requirements for sensor readings. The accuracy shall be meet at the specified environmental condition and the full range of rated input voltage.

Table 23 – Sensor Accuracy

Sensor	10% - 20% load	> 20% - 50% load	> 50% - 100% Load
Current	± 10%	± 5%	± 5%
Voltage	± 10%	± 5%	± 5%
Temperature	± 3°C with Δ5%		
FAN	Provided by the power module		
Input Power	± 10%	± 5%	± 5%
	Provided by the power module		

5.2.9. PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose.

All Sensors shall continue to provide real time data as long as the PSMC device is powered.

This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Table 24 – PSMC Sensor list

Sensor	Description
V_{input}	Input Voltage
I_{input}	Input Current
P_{input}	Input Power
V_{output_main}	Output Voltage main output
I_{output_main}	Output Current main output
P_{output_main}	Output Power main output
V_{output_aux}	Output Voltage auxiliary output
I_{output_aux}	Output Current auxiliary output
T_{comp}	Component Temperature
T_{env}	Environmental Temperature

5.3. Power Supply Field Replacement Unit (FRU)

The PDB shall support electronic access of FRU information over an I^2C bus. Five pins at the power supply connector are allocated for this. They are named SCL, SDA, A1, A0 and Write protect. SCL is serial clock. SDA is serial data. These two bidirectional signals from the basic communication lines over the I^2C bus. A0and A1 are input address lines to the power supply. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I^2C address shall be per table below. The Write protection pin is to ensure that data will not accidentally overwritten.

The device used for this shall be powered from a +3.3V bias voltage derived from the +5VSB output. No pull-up resistors shall be on SCL or SDA inside the power supply.

Table 25 - EEPROM Addressing

PDB position and FRU address	PM1 A0h/A1h	PM2 A2h/A3h	PDB Ach
Pin A2/A1/A0	0/0/0	0/0/1	None

5.3.1. FRU Data

The FRU Data format shall be compliant with the IPMI ver. 1.0 (per rev. 1.1 from Sep.25th , 1999) specification. The current version of these specification is available at http://developer.intel.com/design/servers/ipmi/specs.htm. The following is the exact listing of the EEPROM content. During testing this should be followed and verified.

5.3.2. FRU Device protocol

The FRU device will implement the same protocols as the commonly used ATC24C02D or EQU device, including Byte Read, Sequential Read, Byte Write, and Page Read protocols.

5.3.3. FRU Data Format

The information to be contained in the FRU device is shown in the following table.

Table 26A - EEPROM Addressing of YH5851-xEARxAxD

Area Type	**Description**	
Common Header	As defined by the FRU document	
Internal Use Area	Not required, do not reserve	
Chassis Info Area	Not applicable, do not reserve	
Board Info Area	Not applicable, do not reserve	
Product Info Area	As defined by the IPMI FRU document. Product information shall be defined as follows:	
Field Name	**Field Description**	
Manufacturer Name	3Y Power	
Product Name	YH5851-1EAR2A0D	YH5851-1EAR0A2D
Product part/model number	Customer part number	
Product Version	Customer current revision	
Product Serial Number	{Defined at time of manufacture}	
Asset Tag	{Not used, code is zero length byte}	
FRU File ID		
PAD Bytes	{Added as necessary to allow for 8-byte offset to next area}	
Multi-Record Area	As defined by the IPMI FRU document. The following record types shall be used on this power supply: - Power Supply Information (Record Type 0x00) - DC Output (Record Type 0x01) No other record types are required for the power supply. Multi-Record information shall be defined as follows:	
Field Name (PS Info)	**Field Information Definition**	

	AC Module	DC Module
Overall Capacity (watts)	850	
Peak VA		
Inrush current (A)	60	100
Inrush interval (msec)		
Low end input voltage range 1	90	36
High end input voltage range 1		
Low end input voltage range 2		
High end input voltage range 2	264	72
A/C dropout total. (msec)	10	
Binary flags	Set for: Hot Swap support, Auto switch, and PFC	
Peak Wattage		
Combined wattage	None	
Predictive fail tech support	Supported	
Field Name (Output)	Field Description: Two outputs are to be defined from #1 to #2, as follows: +12V and +5Vsb.	
Output Information	Set for: Standby on +5Vsb, No Standby on all others.	
All other output fields	Format per IPMI specification, using parameters in this specification.	

6. ENVIRONMENTAL

The PDB shall operate normally, and sustain no damage as a result of the environmental conditions listed in this chapter.

6.1. Temperature

Operating Ambient, normal mode (inlet Air): -5°C min/+50°C max at 5,000m above sea level.

(At full load, with a maximum rate of change of 5°C/10 minutes, but no more than 10°C/hr)

Operating Ambient, stand-by mode (inlet Air): -5°C min/+50°C max at 5,000m above sea level.

Non-operating ambient: -40°C to +70°C (Maximum rate of change shall be 20°C/hr)

6.2. Humidity

Operating: up to 85% relative humidity (non-condensing)

Non-operating: up to 95% relative humidity (non-condensing)

Note: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

6.3. Altitude

A) Operation : sea level to 5,000m

B) Non-Operation : sea level to 15,200m

6.4. Vibration

A) Operation: 0.01G^2/Hz at 10Hz, 0.02G^2/Hz at 20Hz.

B) Non-Operation :

- **Sine sweep:** 5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15min at each of 3 resonant points;
- **Random profile:** 5Hz @ 0.01g^2/Hz to 20Hz @ 0.02g^2 (slope up): 20Hz to 500Hz @ 0.02g^2/Hz (flat);input acceleration = 3.13gRMS; 10min. per axis for 3 axis on all samples

6.5. Mechanical Shock

A) Operation: 10G, no malfunction

B) Non-operating: 50G Trapezoidal Wave, Velocity change = 4.3m/sec. Three drops in each of six directions are applied to each of the samples.

6.6. Thermal shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30minutes.

6.7. Catastrophic Failure

The PDB shall be designed to fail without startling noise or excessive smoke.

6.8. EMI

The power supply shall comply with FCC part 15, CRISP 22 and EN55022; Class A for both conducted and radiated emissions with a 3dB margin. Test shall be conducted using a shielded DC output cable to a shielded load. The load shall be adjusted to 100% load. Test will be performed at 100VAC @ 50Hz, 120VAC @ 60Hz, and 230VAC @ 50Hz power of AC power supplies, or at -48VDC of DC power supplies.

The power supply shall comply with EN55024.

The power supply when installed in the system must meet the following all the immunity requirements when integrated into the end system.

6.9. Voltage Fluctuations and Flicker

The power supply shall meet the specified limits of EN61000-3-3, for voltage fluctuations and flicker for equipment ≤ 16 amps connected to low voltage distribution systems.

7. REGULATORY Requirements

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, residential, alarm systems, test equipment, etc.) other than ITE application, may require further evaluation.

7.1. Product Safety Compliance

A) UL 60950-1/CSA 60950-1 Edition 2 (USA/Canada)

B) EN60950-1 Edition 2 (Europe)

C) IEC60950-1 Edition 2 (International)

D) CB Certificate & Report, IEC60950-1 Edition 2 (report to include all country national deviations)

E) CE – Low Voltage Directive 2006/95/EC (Europe)

F) BSMI (Taiwan) *Note: without DC power supplies

G) GB4943-CBCA Certification (China)

7.2. Product EMC Compliance

Note: The product is required to comply with Class A emission, as the system it is built into might be configured with the intend for commercial environment or home use. The Power supply have a minimum 3dB margin to Class A limits to meet 3Y's Standard margin requirements.

A) FCC / ICES-003 Emission (USA/Canada) Verification

B) CRISP 22 – Emission (International)

C) EN55022 – Emission (Europe)

D) EN55024 – Immunity (Europe)

- EN61000-4-2 Electrostatic Discharge
- EN61000-4-3 Radiated RFI Immunity
- EN61000-4-4 Electrical Fast Transients
- EN61000-4-5 Electrical Surge
- EN61000-4-6 RF Conducted
- EN61000-4-8 Power Frequency Magnetic Fields
- EN61000-4-11 Voltage Dips and Interruptions

E) EN61000-3-2 – Harmonics (Europe)

F) EN61000-3-3 – Voltage Flicker (Europe)

G) CE – EMC Directive 2004/108/EEC (Europe)

H) BSMI (Taiwan) *Note: without DC power supplies

I) GB 9254 2008 (EMC) Certification (China)

J) GB 17625.1 – (Harmonics) CNCA Certification (China)

7.3. Maximum Leakage current to ground

The maximum leakage current to ground for each power supply module shall be 3.5mA when tested at 240VAC.

7.3.1. HI-POT

The AC power supply module in the system shall be test at 1,800VAC, with a trigger limit of 30mA.

The DC power supply module in the system shall be test at 2,250VDC, with a trigger limit of 30mA.

7.4. Electrostatic Discharge (ESD)

In addition to IEC61000-4-2, the following ESD tests shall be conducted. Each surface area of the system under

test shall be subjected to twenty (20) successive static discharges, at each of the following voltages: 2kV, 3kV, 4kV, 5kV, 6kV, 7kV, 8kV, 10kV, 15kV.

Performance criteria:

A) All power system output shall continue to operate within the limits of this specification, without glitches or interruption, while the supply is operated as defined and subjected to 2kV through 15kV ESD pulses. The direct ESD event shall not cause any out of regulation condition. The power system shall withstand these tests without nuisance trips.

B) The power system, while operating as defined, shall not have a component failure when subjected to any discharge voltages up to and including 15kV. Component failure is defined as any malfunction of the power supply caused by component degradation or failure requiring component replacement to correct the problem.

7.5. Certifications / Registrations/ Declerations

A) UL Certification (US)

B) cUL Certification (Canada)

C) CB Certification & Report

D) FCC/ICES-003 Class B Attestation (USA/Canada)

E) TÜV Rheinland (Germany)

F) CE Declaration of Conformity (CENELEC Europe)

G) BSMI (Taiwan) *Note: without DC power supplies

H) CCC / CNCA Certification (China)

7.6. Comonent Regulation Requirements

1. All Fans shall have the minimum certifications: UL and TÜV or VDE
2. All current limiting devices shall have UL and TÜV or VDE certifications and shall be suitable rated for the application where the device in its application complies with IEC60950.
3. All printed wiring boards shall be rated UL94V-0 and be sourced from a UL approved printing wiring board manufacturer.
4. All connectors shall be UL recognized and have a UL flame rating of UL94V-0
5. All wiring harnesses shall be sourced from a UL approved wiring harness manufacturer.
6. Product safety label must be printed on UL approved label stock and printer ribbon.
7. Alternatively labels can be purchased from a UL approved label manufacturer.
8. The product must be marked with the correct regulatory markings to support the certifications that are specified in this document.

7.6.1. Product Ecology Requirement

All materials, parts and subassemblies must not contain restricted materials as defined in directive

2002/95/EC, Restriction of Hazardous Substances (RoHS) 6/6.

All cords and cables shall contain <100ppm of cadmium.

All packing materials must be marked with applicable recycling logos for Europe (green dot) and Japan (Eco-marks), if sold as a retail product. All packing materials shall be recyclable.

8. Reliability / Waranty / Service

8.1. Component De-rating

The component de-rating guidelines shall be followed by 3Y guidelines.

8.2. Component Life requirement

All components life expectancy requirements in min. 3 years, calculated for 100% of max continues load @ 50°C ambient temperature and @ 100VAC line voltage of AC, or @-48VDC input voltage of DC.

8.3. Mean Time between Failures (MTBF)

The power supply shall have a minimum MTBF at continuous operation of 200,000 hours calculated at 100%, according to BELL CORE TR-322 at 25°C excluding the Fan MTBF, and at least 100,000 hours including the fan MTBF.

8.4. Warranty

The Warranty for the power supply is 36 months (three years) from production date code.

8.5. Serviceability

No troubleshooting by maintenance personnel is to be performed. Units shall be returned to 3Y Power for any troubleshooting, unless agreed by both parties.

The power supply will lose warranty if opened other than 3Y service personal or agreed by both parties.