電氣規格書

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FSP1200-50FS

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全漢企業股份有限公司
FSP TECHNOLOGY INC.

SPECIFICATION

FSP1200-50FS

2U 1200W Redundant Power Supply

Revision 1.2

April.11.2018

全漢企業股份有限公司
FSP GROUP FSP TECHNOLOGY INC.

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1. REVISION LOG

This section contains the release history of this document:

Date	Revision	Section	Issue
2018/4/11	1.0		Origin
2018/6/1	1.1		Revise 3.2.2 Output rating Revise 3.4.1 PSON# Input Signal (Power supply enable)

APPROVE		CHECK		PREPARE	

2. GENERAL SCOPE

This specification describes the performance characteristic of a 550W AC-DC switching redundant power supply. The power supply shall be able to operate as a single supply or in a 1+1 parallel hot-plug able operation with active load sharing in a 1+1 redundant configuration.

2.1 Mechanical Overview

The physical size of the power supply enclosure is intended to accommodate the power range of up to 550W. The physical size is 83.8mm x 76mm x 250mm (height x width x length).

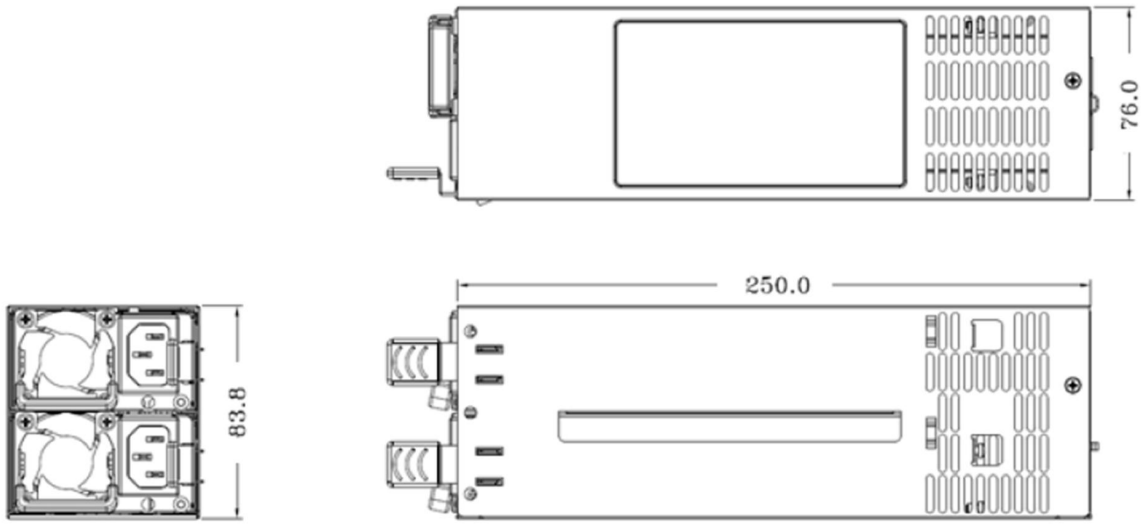

Figure 1 – Power Supply Dimension

2.2 LED Marking and Identification

The power supply shall have two LED for indication of the power supply status.

Table 1 – LED Status Information

Power supply condition	Power supply LED
Output ON and OK	Solid Green
No AC power to all power supplies	OFF
AC present/only standby output on	1Hz Blink Green
AC cord unplugged or AC power lost; with a second power supply in parallel still with AC input power.	Solid Amber
Power supply warning events where the power supply continues to operate; high temp, high power, high current, slow fan.	1Hz Blink Amber
Power supply critical event causing a shutdown failure; OCP, OVP, UVP	1Hz Blink Green
Power supply critical event causing a shutdown failure; OTP, Fan Fail	Solid Amber
Power supply FW update mode of Module	2Hz Blink Green
Power supply FW update mode of Housing	1Hz Blink Green

Note: Blink frequency: 1Hz (0.5 sec ON / 0.5sec OFF)；2Hz (0.25 sec ON / 0.25sec OFF)

2.3 Environmental Requirements

The power supply shall operate within all specified limits over specified conditions in 2.3.

The defined operation condition include temperature, humidity, altitude, shock and vibration.

2.3.1 Temperature and Humidity Requirements

The power supply shall operate within all specified limits over T_{op} temperature range and specified humidity Range. All airflow shall pass through the power supply and not over the exterior surfaces of the power supply.

The power supply shall withstand thermal storage specified in $T_{non\text{-}OP}$ without any damage.

Table 2 – Temperature Requirements

Item	Description	MIN	MAX	Unit
T_{OP}	Operating temperature range.	0	55	℃
$T_{non\text{-}OP}$	Non-Operating temperature range.	-40	70	℃
H_{OP}	Operating humidity range, non-condensing		90	%
$H_{non\text{-}OP}$	Non-Operating humidity range, non-condensing		95	%

2.3.2 Altitude Requirements

The power supply shall operate within all specified limits over A_{op} Altitude range. The change pressure condition shall not harm the power supply and the operation within specified regulations shall be assured.

The power supply shall withstand Altitude storage specified in $A_{non\text{-}OP}$ without any damage.

Table 3 – Altitude Requirements

Item	Description	MIN	MAX	Unit
A_{OP}	Operating Altitude range.	0	5000	m
$A_{non\text{-}OP}$	Non-Operating Altitude range.	0	15000	m

3. ELECTRICAL PERFORMANCE

3.1 AC power Input Specification

3.1.1 AC Inlet connector

The power supply shall incorporate an AC input connector complying with IEC 320 C-14 power inlet connector specification. This inlet shall be rated for operation at 10A/250VAC.

3.1.2 Input voltage and frequency specification

The power supply shall operate within all specified limits over the following input range. Harmonic distortions of up to 10% of the rated line voltage must not cause the power supply to go out of specified limits.

The power supply shall power off if the AC input is below 75 ±5Vac and shall start (auto recover) if AC input is exceed 85 ±4Vac.

The power supply shall supply the full output power in the voltage range of 90VAC to 264VAC.

Table 4 – Rated output power for each input voltage range

Parameter	Minimum input	Rated Input	Maximum input
115 VAC	$90V_{rms}$	$100\text{-}127V_{rms}$	$140V_{rms}$
230 VAC	$180V_{rms}$	$200\text{-}240V_{rms}$	$264V_{rms}$
Frequency	47Hz	50/60Hz	63Hz

3.1.3 HVDC Input voltage

The power supply supports High Voltage Direct Current (HVDC) input. Allowed HVDC input range as shown in below table. The power supply shall operate within all specified limits, when HVDC input meet requirements defined in this chapter.

Table 5 – HVDC input voltage range

Parameter	Minimum input	Rated Input	Maximum input
HVDC(240)	180V	240V	310V

3.1.4 Input current

The maximum input current defines the maximum possible input current to ensure the proper function of the power supply to meet all defined specifications.

Table 6 – Maximum input current

Input voltage	Input current	Max power
90VAC	14A	1000W
100-127VAC	12A	1000W
180VAC	8A	1200W
200-240VAC	7A	1200W
264VAC	5.2A	1200W
240VDC	6A	1200W

3.1.5 AC Line Fuse

The power supply shall incorporate one input fuse on the line side for input over-current protection to prevent damage to the power supply and meet product safety requirements. AC inrush current shall not cause the AC line fuse to blow under any conditions. All protection circuits in the power supply shall not cause the AC fuse to blow unless a component in the power supply has failed. This includes DC output load short conditions.

3.1.6 AC line inrush

AC line inrush current shall not exceed 55A peak, for up to one-quarter of the AC cycle, after which, the input current should be no more than the specified maximum input current. The peak inrush current shall be less than the ratings of its critical components (including input fuse, bulk rectifiers, and surge limiting device).

The power supply must meet the inrush requirements for any rated AC voltage, during turn on at any phase of AC voltage, during a single cycle AC dropout condition as well as upon recovery after AC dropout of any duration, and over the specified temperature range (Top).

3.1.7 Input Power Factor Correction

The input Power Factor shall be greater than 0.95 at 50% loading (show the below Table 7).

Table 7 – module Power Factor Correction

Output power	10% load	20% load	50% load	100% load
Power factor	> 0.90	> 0.96	> 0.98	> 0.99
Input conditions	200VAC to 240VAC & 50Hz / 60Hz			

3.1.8 AC line dropout

An AC line dropout is a transient condition defined as the AC input to the power supply drops to 0 VAC at any phase of the AC line for any length of time. During an AC dropout the power supply must meet dynamic voltage regulations requirements. An AC line dropout of any duration shall not cause dripping of the control signals and protection circuits. If the AC dropout lasts longer than the holdup time, the power supply should recover when VAC meets $VAC_{recover}$ and meet all turn on requirements.

An input dropout of any length shall not cause any damage to the power supply.

Table 8 – Hold-up time until Power output goes out of regulations

Loading	Main output	Standby output
100%	12mS	70mS

3.1.9 Efficiency

The redundant power supply module efficiency should meet at least Climate Saver 3 / 80Plus Platinum rating, specified in below table. The efficiency should be measured at 230VAC and with external fan power according to Climate Saver / 80Plus efficiency measurement specifications (CSCI-09-10)

Table 9 – module efficiency requirements

Efficiency Std.	20% load (12V is 8.8A,12vsb is 0.42A)	50% load (12V is 22A,12vsb is 1.05A)	100% load (12V is 44A,12vsb is 2.1A)
Platinum	90%	94%	91%

3.1.10 Susceptibility Requirements

The power supply shall meet the following electrical immunity requirements when connected to a cage with an external EMI filter, which meets the criteria defined in the SSI document EPS Power Supply Specification.

Table 10 – Performance criteria

Level	Description
A	The apparatus shall continue to operate as intended. No degradation of performance.
B	The apparatus shall continue to operate as intended. No degradation of performance beyond spec. limits.
C	Temporary loss of function is allowed provided the function is self-recoverable or can be restored by the operation of the controls.

3.1.10.1 Electrical Discharge Susceptibility

The power supply shall comply with the limits defined in EN 55024:1998 using the IEC 61000-4-2:1995 test standard and performance criteria B defined in Annex B of CISPR 24.

3.1.10.2 Fast Transient/Burst

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-4:1995 test standard and performance criteria B define in Annex B of CISPR 24.

3.1.10.3 Radiated Immunity

The power supply shall comply with the limits defined in EN55024:1998 using the IEC61000-4-3:1995 test standard and performance criteria A defined in Annex B of CISPR 24.

3.1.10.4 Surge Immunity

The power supply shall be tested with the system for immunity to AC Ring wave and AC Unidirectional wave, both up to 2kV(Differential mode 1K,Common mode 2K), per EN55024:1998, EN 61000-4-5:1995 and ANSI C62.45:1992.

The pass criteria include: No unsafe operation is allowed under any condition; all power supply output voltage levels to stay within proper spec levels; No change in operating state or loss of data during and after the test profile; No component damage under any condition.

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-5:1995 test standard and performance criteria B defined in Annex B f CISPR 24.

3.1.10.5 AC Line Transient Specification

AC line transient conditions shall be defined as “sag” and “surge” conditions.

“Sag” conditions are also commonly referred to as “brownout”, these conditions will be defined as the AC line voltage dropping below nominal voltage conditions.

“Surge” will be defined to refer to conditions when the AC line voltage rises above nominal voltage.

The power supply shall meet the requirements under the following AC line sag and surge conditions.

Table 11 – AC Line SAG transient performance.

AC Line Sag (10sec interval between each sagging)				
Duration	**Sag**	**Operating AC voltage**	**Line frequency**	**Performance criteria**
0 to 1/2 AC cycle	95%	Nominal AC voltage	50/60Hz	No loss of function or performance
>1 AC cycles	>30%	Nominal AC voltage	50/60Hz	Loss of function acceptable, self-recoverable

Table 12 – AC Line SURGE transient performance.

AC Line Surge				
Duration	**Surge**	**Operating ac voltage**	**Line frequency**	**Performance criteria**
Continuous	10%	Nominal AC voltage	50/60Hz	No loss of function or performance
0 to 1/2 AC cycle	30%	mid-point of nominal AC voltage	50/60Hz	No loss of function or performance

3.1.10.6 AC line fast transient (EFT) specification

The power supply shall meet the EN61000-4-5 directive and any additional requirements in IEC1000-4-5:1995 and the level 3 requirements for surge-withstand capability, with the following conditions and exceptions:

- These input transients must not cause any out-of-regulation conditions, such as overshoot and undershoot, nor must it cause any nuisance trips of any of the power supply protection circuits.
- The surge-withstand test must not produce damage to the power supply.
- The supply must meet surge-withstand test conditions under maximum and minimum DC-output load conditions.

3.1.11 Power Recovery

The power supply shall recover automatically (auto recover) after an AC power failure. AC power failure is defined to be any loss of AC power that exceeds the dropout criteria.

3.1.12 Voltage Brown Out

The power supply shall comply with the limits defined in EN55024:1998 using the IEC 61000-4-11:1995 test standard and performance criteria C defined in Annex B of CISPR 24.

In addition the power supply shall meet the following requirements:

A continuous input voltage below the nominal input range shall not damage the power supply or cause overstress to any power supply component. The power supply must be able to return to normal power up state after a brownout (Sag) condition. During brownout test from 120VAC to 0VAC @ 1200W with 3mins ramp, input current shall never exceed fuse and shall not blow the fuse.

3.1.13 AC Line Leakage Current

The maximum leakage current to ground for each power supply shall be 3.5mA when tested at 264Vac/63Hz.

3.2 DC output voltages

3.2.1 Grounding

The output ground of the pins of the power supply provides the output power return path. The ground output at the PCB card edge shall be connected to the safety ground (power supply enclosure). This grounding should be well designed to ensure passing the max allowed Common Mode Noise levels.

The power supply shall be provided with a reliable protective earth ground. All secondary circuits shall be connected to protective earth ground. Resistance of the ground returns to chassis shall not exceed 100 mΩ (Test Conditions 40A for 120sec). This path may be used to carry DC-current.

3.2.2 Output rating

The following table defines the power and current rating of the 550W power supply. The combined output power of all outputs shall not exceed the rated output power. The power supply must meet both static and dynamic voltage regulation requirements.

Table 13 – Output Power and Current Ratings

<table>
<tr><th>Output</th><th>Minimum Current(A)</th><th>Maximum Current(A)</th><th colspan="2">Output Power(W)</th></tr>
<tr><td>+12V</td><td>0.5A</td><td>80.5A for 90~180Vrms
97A for 180~264Vrms</td><td>966W for 90~180Vrms
1164W for 180~264Vrms</td><td rowspan="5">1000W for 90~180Vrms
1200W for 180~264Vrms</td></tr>
<tr><td>+5V</td><td>0A</td><td>30A</td><td rowspan="2">180W</td></tr>
<tr><td>+3.3V</td><td>0A</td><td>30A</td></tr>
<tr><td>-12V</td><td>0A</td><td>0.3A</td><td>3.6W</td></tr>
<tr><td>+5Vsb</td><td>0A</td><td>5A</td><td>25W</td></tr>
</table>

3.2.3 Auxiliary Output (Standby)

The 5Vsb output shall be present when an AC input greater than $V_{recover}$ is applied.

3.2.4 No load operation

The power supply shall meet all requirements except for the transient loading requirements when operated at no load on all outputs.

3.2.5 Voltage Regulation

The power supply shall meet the Voltage regulation under all operating conditions (AC line, transient loading, output

loading). These limits include the peak-peak ripple/noise. The regulation of Table 14 shall be measured at the output connector of the power supply, subject to the dynamic loading conditions in paragraph 3.2.7.

Table 14 – Output Voltage regulation

Output	Minimum	Nominal	Maximum	Unit
+12V	11.4	12.0	12.6	Vdc
+5V	4.75	5.0	5.25	Vdc
+3.3V	3.135	3.3	3.465	Vdc
-12V	-11.40	-12.0	-12.6	Vdc
+5Vsb	4.75	5.0	5.25	Vdc

3.2.6 Ripple and Noise Regulation

Ripple and Noise is defined in table 15. Ripple and Noise shall be measured over a Bandwidth of 20Hz to 20MHz at the power supply output connector. A 0.1μF ceramic capacitor and 10μF of tantalum capacitor shall be placed at each point of measurement. The measurement points shall be as close as possible to the point of load.

The ripple and noise specification shall be met over all load ranges and AC line voltages with 1+1 power supplies in parallel operation.

Table 15– Ripple and Noise Regulation

Output	Maximum	Unit
+12V	120	mV
+5V	50	mV
+3.3V	50	mV
-12V	120	mV
+5Vsb	50	mV

3.2.7 Dynamic loading

The power supply shall operate within specified limits and meet regulation requirements for step loading and capacitive loading specified below.

The load transient repetition rate shall be tested between 50Hz to 5kHz at duty cycles ranging. The load transient repetition rate is only a test specification. The Δ step load may occur anywhere within the MIN load and the MAX load.

This shall be tested with no additional bulk capacitance added to the load.

Table 16 – Transient Load Requirements

Output	Δ Step size	Slew Rate	Capacitive Load
+3.3V	30% OF MAX.	0.25A/μs	2200μF
+5V	30% OF MAX.	0.25A/μs	2200μF
+12V	60% OF MAX.	0.25A/μs	4700μF
+5Vsb	25% OF MAX.	0.25A/μs	100μF

Note: For dynamic conditions +12V min. loading is 1A.

3.2.8 Capacitive load

The power supply shall operate within specifications over the capacitive loading ranges defined below in table 17.

Table 17 – Capacitive Loading Conditions

Output	Min	Max
+3.3V	10μF	12,000μF
+5V	10μF	12,000μF
+12V	10μF	11,000μF
-12V	1μF	350μF
+5Vsb	1μF	350μF

3.2.9 Close loop stability

The power supply shall be unconditionally stable under all line/load/transient load conditions. A minimum of: 45 degrees phase margin and -12dB-gain margin is required.

Closed-loop stability must be ensured at the maximum and minimum loads as applicable.

3.2.10 Residual Voltage Immunity in Standby mode

The power supply should be immune to any residual voltage placed on its outputs (typically a leakage voltage through the system from standby output) up to 500mV. There shall be no additional heat generated nor stressing of any internal components with this voltage applied to any individual or all outputs simultaneously. It also should not trip the protection circuits during turn on/off.

The residual voltage at the power supply outputs for no load condition shall not exceed 100mV when AC voltage is applied.

3.2.11 Soft starting

The power supply shall contain control circuit which provides monotonic soft start for its outputs without overstress of the AC line or any power supply components at any specified AC line or load condition.

3.2.12 Hot Swap Requirements

Hot swapping a power supply is the process of inserting and extracting a power supply from an operating power system. During this process the output voltages shall remain within the limits with the capacitive load specified.

The hot swap test must be conducted when the system is operating under static, dynamic, and zero loading conditions. The power supply shall use a latching mechanism to prevent insertion and extraction of the power supply when the AC power cord is inserted into the power supply.

3.2.13 Load sharing control

The +12 V output shall have active load sharing. When operating at 50% of full load, the output current of any 1+1 power supplies shall be within (+/-10%). For example, if power supply #1 is operating at 20A, then all other power supplies within the system shall be operating between 18A to 22A (+/- 10% of 20A).

All current sharing functions shall be implemented internal to the power supply by making use of the SBus signal. The power distribution board (PDB), must connect the SBus signals between the power supplies together. The power supply shall be able to share with up to 1+N supply in parallel.

The failure of a power supply shall not affect the load sharing or output voltages of the other supplies still operating. The power supplies must be able to load share with 100mV of drop between different power supply's output.

If the load sharing is disabled by shorting the load share bus to ground, the power supply shall continue to operate within regulation limits for loads less than or equal to the rating of one power supply.

Table 18 - Load share bus output characteristics

Item	Description	Min	Nominal	Max	Units
V_{share}; I_{out}=Max.	Voltage of load share bus at specified max output current		8		V
$\Delta V_{share}/\Delta I_{out}$	Slope of load share bus voltage with changing load		$8/I_{outmax}$		V/A

3.3 Timing Requirements

These are the timing requirements for the power supply operation. The output voltages must rise from 10% to within regulation limits (T_{vout_rise}) within 5 to 70ms. For +5Vsb, it is allowed to rise from 1 to 25ms. All outputs must rise monotonically. Table below shows the timing requirements for the power supply being turned on and off via the AC input, with PSON held low and the PSON signal, with the AC input applied.

3.3.1 Output Voltage Timing

The timing of signals and outputs are specified in below Table 19 and illustrated in Figure 2.

Table 19 - Turn on/off timing

Turn on	Description	Min	Max	Units
$T_{vout\ rise}$	Output voltage rise time for all main output	10	70*	Msec
$T_{sb\_on\_delay}$	Delay from AC being applied to 5Vsb being within regulation		1500	msec
$T_{ac\_on\_delay}$	Delay from AC being applied to all output voltage being within regulation		3000	msec
T_{vout_holdup}	Time all main output 12VI voltages stay within regulation after loss of AC.	11		msec
T_{pwok_holdup}	Delay from loss of AC to de-assertion of PWOK	10		msec
$T_{pson\_on\_delay}$	Delay from PSON# active to output voltages within regulation limits	5	400	msec
T_{pson_pwok}	Delay from PSON# deactivate to PWOK being de-asserted.		50	msec
T_{pwok_on}	Delay from output voltage(12V) within regulation limits to PWOK asserted at turn on	100	500	msec
T_{pwok_off}	Delay from PWOK de-asserted to output voltages dropping out of regulation limits.	1		msec
T_{pwok_low}	Duration of PWOK being in the de-asserted state during an off/on cycle using AC or the PSON signal	100		msec
T_{sb_vout}	Delay from 5Vsb being in regulation to main output being in regulation at AC turn on.	50	1000	msec
T_{5Vsb_holdup}	Time the 5Vsb output voltage stays within regulation after loss of AC	70		msec

*T_{vout_rise} :The 5Vsb output rise time shall be 1ms to 25ms.

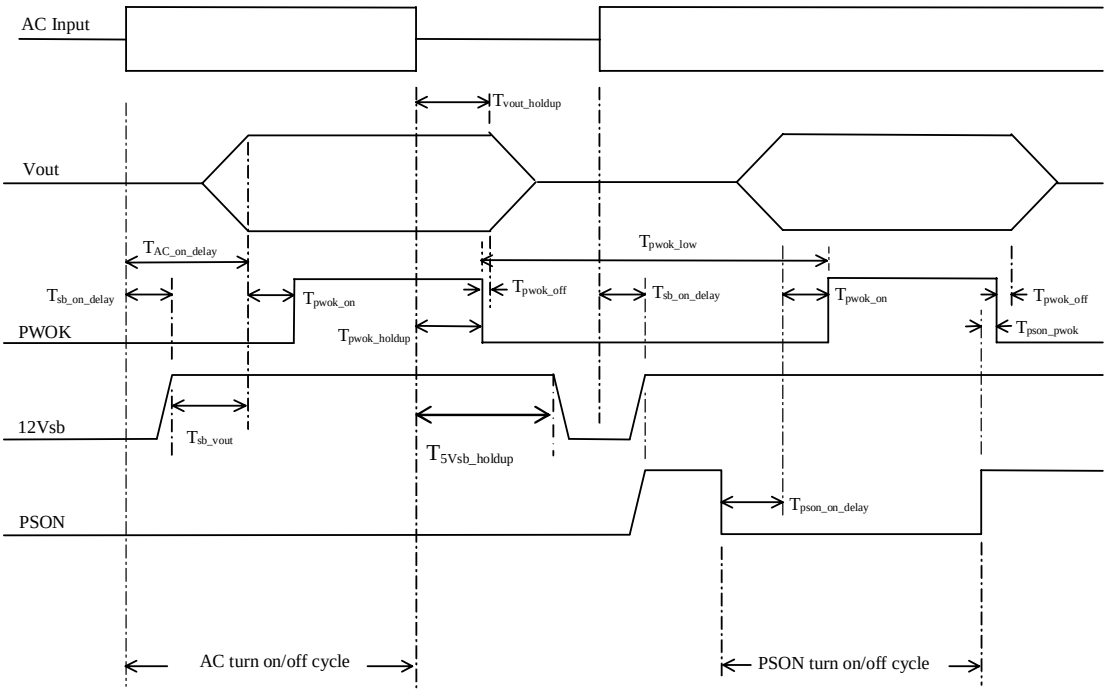

Figure 2 – Turn On/Off Timing (Power Supply Signals)

3.3.2 Overshoot

Any output overshoot at turn on shall be less than 10% of the nominal output value.

3.3.3 Undershoot

Any output shall not undershoot at turn on or off cycle under any circumstances.

3.3.4 Temperature coefficient

After operating for 30 minutes or longer at 25° C ambient, the output voltages shall not change by more than ± 0.05 % per degree C for any given line and load conditions.

3.4 Control and Indicator functions

The following section define the input and output signals from the power supply.

Signals that can be defined as low true use the following convention:

Signal$^{\#}$ = low true.

3.4.1 PSON$^{\#}$ Input Signal (Power supply enable)

The PSON$^{\#}$ signal is required to remotely turn on/off the main output of the power supply.

PSON$^{\#}$ is and active low signal that turns on the main output power rail. When this signal is not pulled low by the system or left open, the outputs (except the Standby output) turn off.

PSON$^{\#}$ is pulled to a standby voltage by a pull-up resistor internal to the power supply.

See Table 20.

Table 20 – PS ON# signal characteristics

Signal Type	**Accepts an open collector/drain input from the system. Pull-up to +5V located in the power supply**.	
PSON# = Low	ON	
PSON# = High or Open	OFF	
	MIN	MAX
Logic level low (power supply ON)	0V	0.6V
Logic level high (power supply OFF)	2.0V	3.46V
Source current, V_{pson} = low		4mA
Power off delay: $T_{pson\_off\_delay}$		5ms
Power up delay: $T_{pson\_on\_delay}$	5ms	400ms
PWOK delay: T_{pson_pwok}		5ms

3.4.2 Power OK (PG or PWOK) Output Signal

PWOK is a power good signal and shall be pulled HIGH by the power supply to indicate that all outputs are within regulation limits. When any output voltage falls below regulation limits, a internal failure or when AC power has been removed for a time sufficiently long, so that power supply operation is no longer guaranteed, PWOK will be de-asserted to a LOW state. The start of the PWOK delay time shall inhibited as long as any power supply output is in current limit.

See Table 21.

Table 21 – PWOK signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to +5V located in power supply.**	
PWOK=High	Power Good	
PWOK=Low	Power Not Good	
	MIN	MAX
Logic level low voltage, I_{sink}=400μA	0V	0.4V
Logic level high voltage, I_{source} = 200μA	2.4V	5.25V
Sink current, PWOK=low		400μA
Source current, PWOK=high		2mA
PWOK delay: T_{pwok_on}	100ms	500ms
PWOK rise and fall time		100μs
Power down delay: T_{pwok_off}	1ms	

3.4.3 SMBAlert# (PSAlert) Output Signal Pin

This signal indicates that the power supply is experiencing a problem that the user should investigate. This shall be asserted due to Critical events or Warning events. The signal shall activate in the case of critical component temperature reached a warning threshold, general failure, over-current, over-voltage, under-voltage, failed fan. This signal may also indicate the power supply is reaching its end of life or is operating in an environment exceeding the specified limits.

This signal is to be asserted in parallel with LED turning solid amber or blinking amber/green.

See Table 22.

Table 22 – SMBAlert# signal characteristics

Signal Type	**Open collector/drain output from power supply. Pull-up to +5V located in power supply.**	
Alert#=High	Power OK	
Alert#=Low	Power Alert to system	
	MIN	MAX
Logic level low voltage, I_{sink}=4mA	0V	0.4V
Logic level high voltage, I_{source} = 50μA	2.4V	5.25V
Sink current, Alert#=low		4mA
Source current, Alert#=high		50μA
Rise and fall time		100μs

3.4.4 12V_{RS} and Return Sense

The power supply has remote sense return (Return Sense) to regulate out ground drops for all output voltages. The power supply uses remote sense to regulate out drops in the system for the main outputs. The +12V output only uses remote sense with reference to the Return Sense signal. The remote sense input impedance to the power supply must be greater than 10Ω on the main outputs and is 10Ω on Return Sense. These are the values of the resistors connecting the remote senses to the output voltage internal to the power supply. Remote sense is able to regulate out a minimum of 300mV of drop on the +12V output. The remote sense return is able to regulate out drops of 300mV as well. The current in any remote sense line shall be less than 5mA to prevent voltage sensing errors. The power supply operates within specification over the full range of voltage drops from the power supply's output connector to the remote sense points.

3.4.5 SDA and SCL

One pin is the serial clock (SCL), and the other pin is used for serial data (SDA). The SCL and SDA signals are pulled up by system, both pins are bi-directional, open drain signals, and are used to form a serial bus

3.4.6 PS_H

PS_H signal indicates that the power supply is experiencing a problem that the user should investigate. The power is ok, when standby mode, PS_H signal is "High" state, pson mode, PS_H signal is "Low" state. The signal shall activate in the case of general failure, over-current, over-voltage, under-voltage, failed fan. PS_H signal from Low to High.

3.4.7 PS_L

PS_L signal indicates that the power supply is experiencing a problem that the user should investigate. The power is ok, when standby mode, PS_L signal is "Low" state, pson mode, PS_L signal is "High" state. The signal shall activate in the case of general failure, over-current, over-voltage, under-voltage, failed fan. PS_L signal from High to Low.

4. Protection circuits

Protection circuits inside the power supply shall cause only the main output to shutdown (latch off). If the power supply latches off due to a protection circuit assert, an Input Power cycle OFF for 15sec or a PSON# cycle HIGH for 1sec shall be able to reset the power supply.

Specific protection circuits shall not latch, but auto recover when the latching reason had been cleared. This protection circuits will be written in cursive writing and will have an Auto Recover in the chapter name.

The auxiliary output shall not affected by any protection circuit, unless the auxiliary output itself is affected.

4.1 Over Voltage Protection (OVP_{main} & $OVP_{auxilary}$)

All Over Voltage Condition shall be measured internal to the power supply on all outputs (Main and Auxiliary Output) at the card edge output. The power supply shall shutdown and latch off after an Over Voltage condition occurs on main outputs, the auxiliary output shall be auto recover after the OVP had been removed.

The voltages never shall exceed the maximum levels specified in below table when measured during any fail.

Table 23 - Over Voltage Protection requirements

Output Voltage	MIN (V)	MAX (V)
+12 V	13.3	14.5
+5 V	5.7	6.5
+3.3 V	3.9	4.5
-12 V	-13.3	-14.5
+5Vsb	5.7	6.5

4.2 Over Current and Short Circuit Protection (OCP/SCP_{main} & $OCP/SCP_{auxilary}$)

The Over Current Condition shall be measured internal to the power supply on all outputs (Main and Auxiliary Output), and preventing outputs to exceed current limits specified in below table. The power supply shall shutdown and Auto Recovery after an over current condition on Main and Auxiliary Outputs, and shall be Auto Recovery when OCP/SCP condition is removed.

The power supply shall alert the system of the OCP/SCP condition via SMBAlert#.

The power supply shall not be damaged from repeated power cycling in this condition.

Table 24 – Over Current/Short Circuit Protection

Voltage	Over Current Limit (Iout limit)
+12 V	110% minimum; 150% maximum
+5 V	110% minimum; 150% maximum
+3.3 V	110% minimum; 150% maximum

5. Power Supply Management

5.1 Hardware Layer

The serial bus communication devices for Power Supply Management Controller (PSMC) and Field Replacement Unit (FRU) in the power supply shall be compatible with both SMBus 2.0 “high power” and I^2C Vdd based power and drive specification.

This bus shall operate at 3.3V but be tolerant to 5V pull-ups. The power supply should not have any internal pull-ups on the SMBus, pull-ups shall be located on system side.

Two pins are allocated on the power supply. One pin is the serial clock (SCL). The second pin is used for serial data (SDA). Both pins are bi-directional and are used to form a serial bus. The circuits inside the power supply shall derive their 3.3V power from the 5Vsb bus through a buffer. Device(s) shall be powered from the system side of the 5Vsb oring device. The pull-up resistors shall be on SCL or SDA inside the power supply.

5.2 Power Supply Management Controller (PSMC)

The PSMC device in the power supply shall derive its power of the 5Vsb output on the system side of the oring device and shall be grounded to return. It shall be compatible with SMBus specification 2.0 and PMBus™ Power System Management Protocol Specification Part I and Part II in Revision 1.2.

Refer to the specification posted on www.ssiforum.org and www.pmbus.org website for details on the power supply monitoring interface requirements and refer to followed section of supported features.

5.2.1 Related Documents

- PMBus™ Power System Management Protocol Specification Part I – General Requirements, Transport And Electrical Interface; Revision 1.1 and 1.2
- PMBus™ Power System Management Protocol Specification Part II – Command Language; Revision 1.1 and 1.2
- System Management Bus (SMBUS) Specification 2.0

5.2.2 Data Speed

The PSMC device in the power supply shall operate at the full 100kbps (100kHz) SMBus speed and avoid using clock stretching that can slow down the bus. For example, the power supply is allowed to clock stretch while parsing a command or servicing multiple interrupts or NACK.

Unsupported commands may respond with a NACK but must always set the communication error status bit in STATUS_CML.

5.2.3 Bus Errors

The PSMC shall support SMBus clock-low timeout ($T_{timeout}$). This capability requires the PSMC to abort any transaction and drop off the bus if it detects the clock being held low for >25ms, and be able to respond to new transactions within

10ms later. The total reset time from detection of the condition till restarted, ready to receive commands condition shall not exceed 35ms.

The device must recognize SMBus START and STOP conditions on ANY clock interval. The PSMC must not hang due to ‘runt clocks’, ‘runt data’, or other out-of-spec bus timing. This is defined as signals, logic-level glitches, setup. Or hold times that are shorter than the minimums specified by the SMBus specifications. The PSMC is not required to operate normally, but must return to normal operation once ‘in spec’ clock and data timing is again received. Note if the PSMC ‘misses’ a clock from the master due to noise or other bus errors, the device must continue to accept ‘in spec’ clocks and NACK. The PSMC is supposed to re-synch with the master on the next START or STOP condition.

5.2.4 Write byte/word

The first byte of a Write Byte/Word access is the command code. The next one or two bytes, respectively, are the data to be written. In this example the master asserts the slave device address followed by the write bit. The device acknowledges and the master delivers the command code. The slave again acknowledges before the master sends the data byte or word (low byte first). The slave acknowledges each byte, and the entire transaction is finished with a STOP condition.

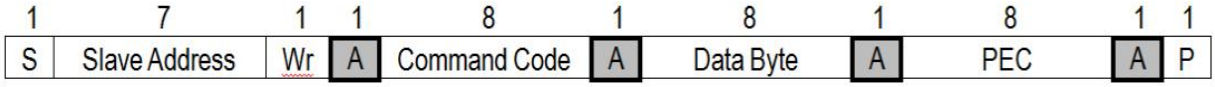

Figure 3 –Write byte protocol with PEC

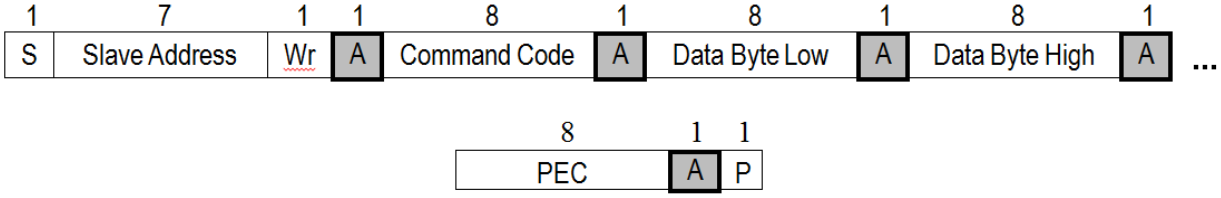

Figure 4 –Write Word Protocol with PEC

5.2.5 Read byte/word

Reading data is slightly more complicated than writing data. First the host must write a command to the slave device. Then it must follow that command with a repeated START condition to denote a read from that device’s address. The slave then returns one or two bytes of data.

Note that there is no STOP condition before the repeated START condition, and that a NACK signifies the end of the read transfer.

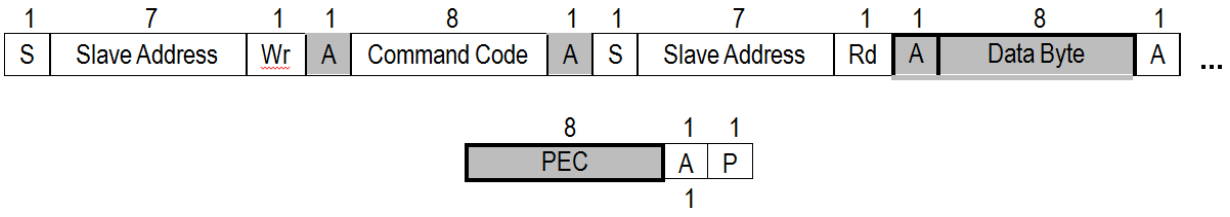

Figure 5 –Read byte protocol with PEC

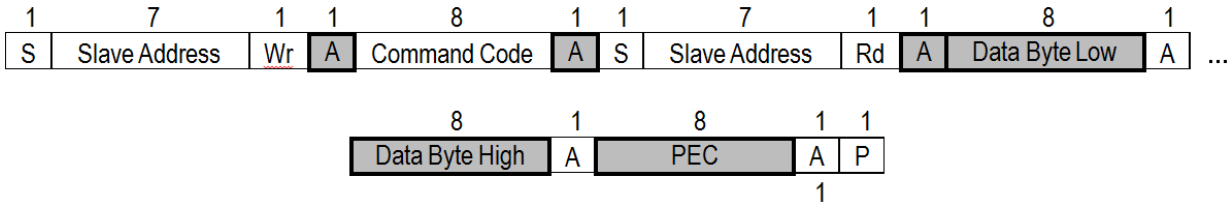

Figure 6–Read word protocol with PEC

5.2.6 Block write/read

The Block Write begins with a slave address and a write condition. After the command code the host issues a byte count which describes how many more bytes will follow in the message. If a slave has 20 bytes to send, the byte count field will have the value 20 (14h), followed by the 20 bytes of data. The byte count does not include the PEC byte. The byte count may not be 0. A Block Read or Write is allowed to transfer a maximum of 32 data bytes.

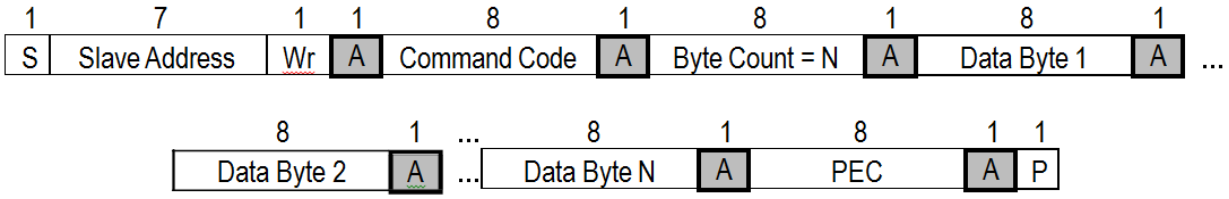

Figure 7 –Block Write with PEC

A Block Read differs from a block write in that the repeated START condition exists to satisfy the requirement for a change in the transfer direction. A NACK immediately preceding the STOP condition signifies the end of the read transfer.

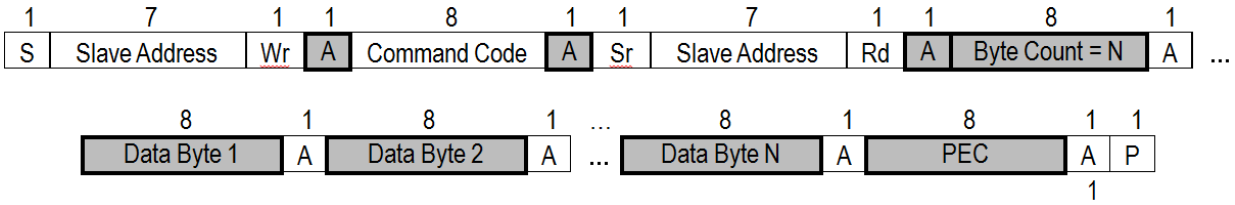

Figure 8 –Block Read with PEC

5.2.7 Sensor Accuracy

The sensor of the PSMC shall meet below accuracy requirements for sensor readings. The accuracy shall be meet at the specified environmental condition and the full range of rated input voltage.

- READ_VOUT
- READ_IOUT
- READ_POUT

Table 27 – Sensor Accuracy

	Required Accuracy (+/-x% of equipment reading)(Vin range=100v-240v)		
Sensor	**< 10% load**	**10% - 20% load**	**> 20% - 100% load**
Pout	± 10W	± 10W	± 5%
Vout	± 5%		
Iout	NA	± 10%	± 5%

5.2.8 PSMC Sensors

Sensors shall be available to the PSMC for monitoring purpose.

All Sensors shall continue to provide real time data as long as the PSMC device is powered.

This means in standby and operation mode, while in standby the main output(s) of the power supply shall read zero Amps and Volts.

Table 29 – PSMC Sensor list

Sensor	Description
V_{output_main}	Output Voltage main output
I_{output_main}	Output Current main output
P_{output_main}	Output Power main output
V_{output_aux}	Output Voltage auxiliary output
I_{output_aux}	Output Current auxiliary output
P_{output_aux}	Output Power auxiliary output

5.3 Power Supply Field Replacement Unit (FRU)

The power supply shall support electronic access of FRU information over an I^2C bus. Two pins will be allocated for the FRU information on the Power Supply connector. They are named SCL, SDA. SCL is serial clock. SDA is serial data. These two bidirectional signals from the basic communication lines over the I^2C bus. The backplane defines the state of these lines such that the address to the power supply is unique within the system. The resulting I^2C address shall be per table below. The Write protection pin is to ensure that data will not accidentally overwritten.

The device used for this shall be powered from a 3.3V bias voltage derived from the 12Vsb output. The pull-up resistors shall be on SCL or SDA inside the power supply.

Table 30 - FRU Signals

	MCU Address	
	PMBus	**IPMI FRU**
PSU - 1	B0	A0
PSU - 2	B2	A2
Housing	4A	AC

5.3.1 FRU Data

The FRU Data format shall be compliant with the IPMI ver. 1.0 (per rev. 1.1 from Sep.25th , 1999) specification. The current version of these specification is available at http://developer.intel.com/design/servers/ipmi/specs.htm.

5.3.2 FRU Device protocol

The FRU device will implement the same protocols as the commonly used memory device, including Byte Read, Sequential Read, Byte Write, and Page Read protocols.

Table 31 - EEPROM Addressing

Item	Address	Byte Value (hex)	Description	Area
0	00H	01	Common Header	Format Version Number
1	01H	00	Internal Use Area	
2	02H	00	Chassis Info Area	
3	03H	00	Board Info Area	
4	04H	01	Product Info Area	
5	05H	0C	Multi Record Info Area	
6	06H	00	PAD Area	
7	07H	F2	Common Header Checksum (Total Of Bytes)	
8	08H	01	Product Area Format Version	Product Information Area
9	09H	0B	Product Area Length	
10	0AH	19	Language Code	
11	0BH	C9	**Manufacturer Name** type/length byte	
12	0CH	46	Manufacturer Name bytes	F
13	0DH	53	Manufacturer Name bytes	S
14	0EH	50	Manufacturer Name bytes	P
15	0FH	20	Manufacturer Name bytes	
16	10H	47	Manufacturer Name bytes	G
17	11H	52	Manufacturer Name bytes	R
18	12H	4F	Manufacturer Name bytes	O
19	13H	55	Manufacturer Name bytes	U
20	14H	50	Manufacturer Name bytes	P
21	15H	CC	**Product Name** type/length byte	
22	16H	46	Product Name bytes	F
23	17H	53	Product Name bytes	S
24	18H	50	Product Name bytes	P
25	19H	31	Product Name bytes	1
26	1AH	32	Product Name bytes	2
27	1BH	30	Product Name bytes	0
28	1CH	30	Product Name bytes	0
29	1DH	2D	Product Name bytes	-
30	1EH	35	Product Name bytes	5
31	1FH	30	Product Name bytes	0
32	20H	46	Product Name bytes	F
33	21H	53	Product Name bytes	S
34	22H	CA	**Product Part/Model Number** type/length byte	
35	23H	20	Product Part Number bytes	**Need be consistent with SPEC label**

36	24H	20	Product Part Number bytes	**Need be consistent with SPEC label**
37	25H	20	Product Part Number bytes	**Need be consistent with SPEC label**
38	26H	20	Product Part Number bytes	**Need be consistent with SPEC label**
39	27H	20	Product Part Number bytes	**Need be consistent with SPEC label**
40	28H	20	Product Part Number bytes	**Need be consistent with SPEC label**
41	29H	20	Product Part Number bytes	**Need be consistent with SPEC label**
42	2AH	20	Product Part Number bytes	**Need be consistent with SPEC label**
43	2BH	20	Product Part Number bytes	**Need be consistent with SPEC label**
44	2CH	20	Product Part Number bytes	**Need be consistent with SPEC label**
45	2DH	C2	**Product Version** type/length byte	
46	2EH	20	Product Version	**Need be consistent with BOM**
47	2FH	20	Product Version	**Need be consistent with BOM**
48	30H	CC	**Product Serial Number** type/length byte	
49	31H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
50	32H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
51	33H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
52	34H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
53	35H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
54	36H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
55	37H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
56	38H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
57	39H	20	Product Serial Number bytes	**Need be consistent with SPEC label**
58	3AH	20	Product Serial Number bytes	**Need be consistent with SPEC label**
59	3BH	20	Product Serial Number bytes	**Need be consistent with SPEC label**
60	3CH	20	Product Serial Number bytes	**Need be consistent with SPEC label**
61	3DH	CA	**Asset Tag** type/length byte	**Production Date**
62	3EH	30	Asset Tag	Year
63	3FH	30	Asset Tag	Year
64	40H	30	Asset Tag	Year
65	41H	30	Asset Tag	Year
66	42H	2F	Asset Tag	/
67	43H	30	Asset Tag	Month
68	44H	30	Asset Tag	Month
69	45H	2F	Asset Tag	/
70	46H	30	Asset Tag	Day
71	47H	30	Asset Tag	Day
72	48H	D0	**FRU File ID** type/length byte	
73	49H	20	FRU File ID bytes.	**Need be consistent with SPEC label**
74	4AH	20	FRU File ID bytes.	**Need be consistent with SPEC label**
75	4BH	20	FRU File ID bytes.	**Need be consistent with SPEC label**
76	4CH	20	FRU File ID bytes.	**Need be consistent with SPEC label**
77	4DH	20	FRU File ID bytes.	**Need be consistent with SPEC label**
78	4EH	20	FRU File ID bytes.	**Need be consistent with SPEC label**
79	4FH	20	FRU File ID bytes.	**Need be consistent with SPEC label**
80	50H	20	FRU File ID bytes.	**Need be consistent with SPEC label**
81	51H	20	FRU File ID bytes.	**Need be consistent with SPEC label**
82	52H	20	FRU File ID bytes.	**Need be consistent with SPEC label**
83	53H	20	FRU File ID bytes.	**Need be consistent with SPEC label**
84	54H	20	FRU File ID bytes.	**Need be consistent with SPEC label**

85	55H	20	FRU File ID bytes.	**Need be consistent with SPEC label**
86	56H	20	FRU File ID bytes.	**Need be consistent with SPEC label**
87	57H	20	FRU File ID bytes.	**Need be consistent with SPEC label**
88	58H	20	FRU File ID bytes.	**Need be consistent with SPEC label**
89	59H	C1	no more info fields	
90	5AH	00	PAD	
91	5BH	00	PAD	
92	5CH	00	PAD	
93	5DH	00	PAD	
94	5EH	00	PAD	
95	5FH	20	Product Info Area Checksum (Sum Of Bytes)	
96	60H	00	**Record Type ID**	**Power Supply Information**
97	61H	02	End of List/Record Format Version	
98	62H	18	Record Length	
99	63H	92	Record Checksum (zero checksum)	
100	64H	54	Header Checksum (zero checksum)	
101	65H	26	Overall Capacity in Watts (LSB)	550W
102	66H	02	Overall Capacity in Watts (MSB)	550W
103	67H	FF	Peak VA	
104	68H	FF	Peak VA	
105	69H	37	Inrush current	55A
106	6AH	05	Inrush interval in ms.	5ms
107	6BH	28	Low end Input voltage range 1 (10mV ,LSB)	90V
108	6CH	23	Low end Input voltage range 1 (10mV ,MSB)	90V
109	6DH	B0	High end Input voltage range 1 (10mV ,LSB)	140V
110	6EH	36	High end Input voltage range 1 (10mV ,MSB)	140V
111	6FH	50	Low end Input voltage range 2 (10mV ,LSB)	180V
112	70H	46	Low end Input voltage range 2 (10mV ,MSB)	180V
113	71H	20	High end Input voltage range 2 (10mV ,LSB)	264V
114	72H	67	High end Input voltage range 2 (10mV ,MSB)	264V
115	73H	2F	Low end Input frequency range	47Hz
116	74H	3F	High end Input frequency range	63Hz
117	75H	0C	A/C dropout tolerance in ms	12mS
118	76H	1B	Binary flags	
119	77H	5D	Peak Wattage(LSB)	605W
120	78H	C2	Peak Wattage(MSB) – Hold up time in seconds	12S
121	79H	00	Combined Wattage	7:4 – Voltage 1；3:0 – Voltage 2
122	7AH	00	Combined Wattage (LSB)	
123	7BH	00	Combined Wattage (MSB)	
124	7CH	0A	Predictive fail tachometer lower threshold (RPS)	
125	7DH	01	**Record Type ID**	**12V Output Record**
126	7EH	02	End of List/Record Format Version	
127	7FH	0D	Record Length	
128	80H	EB	Record Checksum (zero checksum)	
129	81H	05	Header Checksum (zero checksum)	
130	82H	01	Output Information	
131	83H	B0	Nominal voltage (10 mV) (LSB)	1200mV
132	84H	04	Nominal voltage (10 mV) (MSB)	1200mV

133	85H	74	Maximum negative voltage (10 mV) (LSB)	1140mV
134	86H	04	Maximum negative voltage (10 mV) (MSB)	1140mV
135	87H	EC	Maximum positive voltage (10 mV) (LSB)	1260mV
136	88H	04	Maximum positive voltage (10 mV) (MSB)	1260mV
137	89H	78	Ripple and Noise (1mV) (LSB)	120mV
138	8AH	00	Ripple and Noise (1mV) (MSB)	120mV
139	8BH	F4	Minimum current draw (mA)	500mA
140	8CH	01	Minimum current draw (mA)	500mA
141	8DH	E0	Maximum current draw (mA)	44000mA
142	8EH	AB	Maximum current draw (mA)	44000mA
143	8FH	01	**Record Type ID**	**5V Output Record**
144	90H	02	End of List/Record Format Version	
145	91H	0D	Record Length	
146	92H	7E	Record Checksum (zero checksum)	
147	93H	72	Header Checksum (zero checksum)	
148	94H	02	Output Information	
149	95H	F4	Nominal voltage (10 mV) (LSB)	500mV
150	96H	01	Nominal voltage (10 mV) (MSB)	500mV
151	97H	DB	Maximum negative voltage (10 mV) (LSB)	475mV
152	98H	01	Maximum negative voltage (10 mV) (MSB)	475mV
153	99H	0D	Maximum positive voltage (10 mV) (LSB)	525mV
154	9AH	02	Maximum positive voltage (10 mV) (MSB)	525mV
155	9BH	32	Ripple and Noise (1mV) (LSB)	50mV
156	9CH	00	Ripple and Noise (1mV) (MSB)	50mV
157	9DH	00	Minimum current draw (mA)	0mA
158	9EH	00	Minimum current draw (mA)	0mA
159	9FH	20	Maximum current draw (mA)	20000mA
160	A0H	4E	Maximum current draw (mA)	20000mA
161	A1H	01	**Record Type ID**	**3.3V Output Record**
162	A2H	02	End of List/Record Format Version	
163	A3H	0D	Record Length	
164	A4H	7D	Record Checksum (zero checksum)	
165	A5H	73	Header Checksum (zero checksum)	
166	A6H	03	Output Information	
167	A7H	4A	Nominal voltage (10 mV) (LSB)	330mV
168	A8H	01	Nominal voltage (10 mV) (MSB)	330mV
169	A9H	39	Maximum negative voltage (10 mV) (LSB)	313mV
170	AAH	01	Maximum negative voltage (10 mV) (MSB)	313mV
171	ABH	5A	Maximum positive voltage (10 mV) (LSB)	346mV
172	ACH	01	Maximum positive voltage (10 mV) (MSB)	346mV
173	ADH	32	Ripple and Noise (1mV) (LSB)	50mV
174	AEH	00	Ripple and Noise (1mV) (MSB)	50mV
175	AFH	00	Minimum current draw (mA)	0mA
176	B0H	00	Minimum current draw (mA)	0mA
177	B1H	20	Maximum current draw (mA)	20000mA
178	B2H	4E	Maximum current draw (mA)	20000mA
179	B3H	01	**Record Type ID**	**-12V Output Record**
180	B4H	02	End of List/Record Format Version	
181	B5H	0D	Record Length	

182	B6H	76	Record Checksum (zero checksum)	
183	B7H	7A	Header Checksum (zero checksum)	
184	B8H	04	Output Information	
185	B9H	50	Nominal voltage (10 mV) (LSB)	-1200mV
186	BAH	FB	Nominal voltage (10 mV) (MSB)	-1200mV
187	BBH	8C	Maximum negative voltage (10 mV) (LSB)	-1140mV
188	BCH	FB	Maximum negative voltage (10 mV) (MSB)	-1140mV
189	BDH	14	Maximum positive voltage (10 mV) (LSB)	-1260mV
190	BEH	FB	Maximum positive voltage (10 mV) (MSB)	-1260mV
191	BFH	78	Ripple and Noise (1mV) (LSB)	120mV
192	C0H	00	Ripple and Noise (1mV) (MSB)	120mV
193	C1H	00	Minimum current draw (mA)	0mA
194	C2H	00	Minimum current draw (mA)	0mA
195	C3H	2C	Maximum current draw (mA)	300mA
196	C4H	01	Maximum current draw (mA)	300mA
197	C5H	01	**Record Type ID**	**5Vsb Output Record**
198	C6H	82	End of List/Record Format Version	
199	C7H	0D	Record Length	
200	C8H	BA	Record Checksum (zero checksum)	
201	C9H	B6	Header Checksum (zero checksum)	
202	CAH	85	Output Information	
203	CBH	F4	Nominal voltage (10 mV) (LSB)	500mV
204	CCH	01	Nominal voltage (10 mV) (MSB)	500mV
205	CDH	DB	Maximum negative voltage (10 mV) (LSB)	475mV
206	CEH	01	Maximum negative voltage (10 mV) (MSB)	475mV
207	CFH	0D	Maximum positive voltage (10 mV) (LSB)	525mV
208	D0H	02	Maximum positive voltage (10 mV) (MSB)	525mV
209	D1H	32	Ripple and Noise (1mV) (LSB)	50mV
210	D2H	00	Ripple and Noise (1mV) (MSB)	50mV
211	D3H	00	Minimum current draw (mA)	0mA
212	D4H	00	Minimum current draw (mA)	0mA
213	D5H	A0	Maximum current draw (mA)	4000mA
214	D6H	0F	Maximum current draw (mA)	4000mA
215	D7H	FF		
216	D8H	FF		
217	D9H	FF		
218	DAH	FF		
219	DBH	FF		
220	DCH	FF		
221	DDH	FF		
222	DEH	FF		
223	DFH	FF		
224	E0H	FF		
225	E1H	FF		
226	E2H	FF		
227	E3H	FF		
228	E4H	FF		
229	E5H	FF		
230	E6H	FF		

231	E7H	FF		
232	E8H	FF		
233	E9H	FF		
234	EAH	FF		
235	EBH	FF		
236	ECH	FF		
237	EDH	FF		
238	EEH	FF		
239	EFH	FF		
240	F0H	FF		
241	F1H	FF		
242	F2H	FF		
243	F3H	FF		
244	F4H	FF		
245	F5H	FF		
246	F6H	FF		
247	F7H	FF		
248	F8H	FF		
249	F9H	FF		
250	FAH	FF		
251	FBH	FF		
252	FCH	FF		
253	FDH	FF		
254	FEH	FF		
255	FFH	FF		

6. ENVIRONMENTAL

The power supply shall operate normally, and sustain no damage as a result of the environmental conditions listed in this chapter.

6.1 Temperature

Operating Ambient, normal mode (inlet Air): 0°C min/+55°C max at 5000m above sea level.

(At full load, with a maximum rate of change of 5°C/10 minutes, but no more than 10°C/hr)

Operating Ambient, stand-by mode (inlet Air): -5°C min/+50°C max at 5000m above sea level.

Non-operating ambient: -40°C to +70°C (Maximum rate of change shall be 20°C/hr)

6.2 Humidity

Operating: 5%- 90% relative humidity (non-condensing)

Non-operating: 5%- 95% relative humidity (non-condensing)

Note: 95% relative humidity is achieved with a dry bulb temperature of 55°C and a wet bulb temperature of 54°C.

6.3 Altitude

A) Operation : sea level to 5000m

B) Non-Operation : sea level to 15000m

6.4 Vibration

A) Operation : $0.01g^2/Hz$ at 5 Hz sloping to $0.02g^2/Hz$ at 20 Hz, and maintaining $0.02g^2/Hz$ from 20 Hz to 500 Hz. The area under the PSD curve is 3.13gRMS. The duration shall be 20 minutes per axis for all three axes on all samples.

B) Non-Operation :

- **Sine sweep:** 5Hz to 500Hz @ 0.5gRMS at 0.5 octave/min; dwell 15min at each of 3 resonant points;

6.5 Mechanical Shock

A) Operation: 10G, 4.3 mSec, no malfunction

B) Non-operating: 50G Trapezoidal Wave, Velocity change = 4.3m/sec. Three drops in each of six directions are applied to each of the samples.

6.6 Thermal shock (Shipping)

Non-operating: -40°C to +70°C, 50 cycles, 30°C/min. ≥ transition time ≥ 15°C/min., duration of exposure to temperature extremes for each half cycle shall be 30minutes.

6.7 Catastrophic Failure

The power supply shall be designed to fail without startling noise or excessive smoke.

6.8 EMI

The power supply shall comply with FCC part 15, CRISP 22 and EN55-22; Class B for both conducted and radiated emissions with a 3dB margin. Test shall be conducted using a shielded DC output cable to a shielded load. The load shall be adjusted to 100% load. Test will be performed at 115VAC @ 60Hz and 230VAC @ 50Hz power.

The power supply shall comply with EN55024.

The power supply when installed in the system must meet the following all the immunity requirements when integrated into the end system.

6.9 Magnetic Leakage Fields

The PFC choke magnetic leakage field shall not cause any interference with a high resolution computer monitor placed next to or on top of the chassis.

6.10 Voltage Fluctuations and Flicker

The power supply shall meet the specified limits of EN61000-3-3, for voltage fluctuations and flicker for equipment ≤ 16 amps connected to low voltage distribution systems.

7. REGULATORY Requirements

Intended Application – This product was evaluated as Information Technology Equipment (ITE), which may be installed in offices, schools, computer rooms, and similar commercial type locations. The suitability of this product for other product categories and environments (such as: medical, industrial, telecommunications, NEBS, residential, alarm systems, test equipment, etc.) other than ITE application, may require further evaluation.

7.1 Product Safety Compliance

A) UL 62368-1/CSA 62368-1 Edition 2 (USA/Canada)

B) EN62368-1 Edition 2 (Europe)

C) IEC62368-1 Edition 2 (International)

D) CB Certificate & Report, IEC62368-1 Edition 2 (report to include all country national deviations)

E) CE – Low Voltage Directive 2006/95/EC (Europe)

F) GB4943-CBCA Certification (China)

7.2 Product EMC Compliance – Class B Compliance

Note: The product is required to comply with Class B emission, as the system it is build into might be configured with the intend for commercial environment or home use. The Power supply is to have a minimum of 3dB margin to Class B Limits to support FSP's Standard margin requirements.

A) FCC / ICES-003 Emission (USA/Canada) Verification

B) CRISP 22 – Emission (International)

C) EN55022 – Emission (Europe)

D) EN55024 – Immunity (Europe)

- EN61000-4-2 Electrostatic Discharge
- EN61000-4-3 Radiated RFI Immunity
- EN61000-4-4 Electrical Fast Transients
- EN61000-4-5 Electrical Surge
- EN61000-4-6 RF Conducted
- EN61000-4-8 Power Frequency Magnetic Fields
- EN61000-4-11 Voltage Dips and Interruptions

E) EN61000-3-2 – Harmonics (Europe)

F) EN61000-3-3 – Voltage Flicker (Europe)

G) CE – EMC Directive 2004/108/EEC (Europe)

H) JEIDA (Japan)

I) AS/NZS CISPR 22 (Australia / New Zealand)

J) GB 9254 2008 (EMC) Certification (China)

K) GB 17625.1 – (Harmonics) CNCA Certification (China)

7.3 Maximum AC Leakage current to ground

3.5mA max for each power supply at 264Vac/63Hz.

7.3.1 Hi-pot

The power supply module in the system shall be test at 1800Vac, with a trigger limit of 30mA.

7.4 Electrostatic Discharge (ESD)

In addition to IEC 801-2/ IEC1000-4-2, the following ESD tests shall be conducted. Each surface area of the system under test shall be subjected to twenty (20) successive static discharges, at each of the following voltages: 15kV.

Performance criteria:

A) All power system output shall continue to operate within the limits of this specification, without glitches or interruption, while the supply is operated as defined and subjected to 2kV through 15kV ESD pulses. The direct ESD event shall not cause any out of regulation condition. The power system shall withstand these tests without nuisance trips.

B) The power system, while operating as defined, shall not have a component failure when subjected to any discharge voltages up to and including 15kV. Component failure is defined as any malfunction of the power supply caused by component degradation or failure requiring component replacement to correct the problem.

7.5 Certifications / Registrations/ Declarations

A) UL Certification (US)

B) CB Certification & Report

C) TÜV Rheinland (Germany)

D) CE Declaration of Conformity (CENELEC Europe)

E) CCC / CNCA Certification (China)

7.6 Component Regulation Requirements

1. All Fans shall have the minimum certifications: UL and TÜV or VDE
2. All current limiting devices shall have UL and TÜV or VDE certifications and shall be suitable rated for the application where the device In its application complies with IEC62368.
3. All printed wiring boards shall be rated UL94V-0 and be sourced from a UL approved printing wiring board manufacturer.
4. All connectors shall be UL recognized and have a UL flame rating of UL94V-0
5. All wiring harnesses shall be sourced from a UL approved wiring harness manufacturer.

   SELV cable to be rated minimum 80V @ 120°C
6. Product safety label must be printed on UL approved label stock and printer ribbon.

   Alternatively labels can be purchased from a UL approved label manufacturer.
7. The product must be marked with the correct regulatory markings to support the certifications that are specified in this document.

7.6.1 Product Ecology Requirement

All materials, parts and subassemblies must not contain restricted materials as defined in directive 2002/95/EC, Restriction of Hazardous Substances (RoHS) 6/6.

All cords and cables shall contain <100ppm of cadmium.

All packing materials must be marked with applicable recycling logos for Europe (green dot) and Japan (Eco-marks), if sold as a retail product. All packing materials shall be recyclable.

8. Reliability / Warranty / Service

8.1 Mean Time between Failures (MTBF)

The power supply shall have a minimum MTBF at continuous operation of 200,000 hours calculated at 100%, according to BELL CORE TR-322 at 25°C excluding the Fan MTBF, and at least 100,000 hours including the fan MTBF.

8.2 Warranty

The Warranty for the power supply is 36 months (three years) from production date code.

8.3 Serviceability

No troubleshooting by maintenance personnel is to be performed. Units shall be returned to FSP Power for any troubleshooting, unless agreed by both parties.

The power supply will lose warranty if opened other than FSP service personal or agreed by both parties.

9. PSMC Interface

Following Chapter provide details information of the utilized PSMC Interface protocol utilized. The Interface protocol can be recognized by its ID.

By Default the PMBus shall be utilized to achieve the best compatibility with current applications.

A customization of the PSMC Interface is possible and would accordingly reflected in a different FW ID and different specification compared to the PMBus ones.

9.1 PMBus Data Formats

The Linear Data Format is a two byte value with:

An 11 bit, two's complement mantissa and

A 5 bit, two's complement exponent (scaling factor).

The format of the two data bytes is illustrated in Figure 9

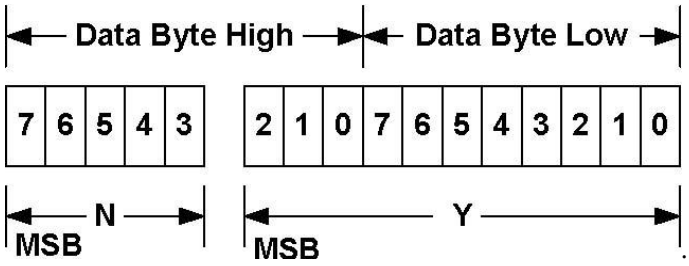

Figure 9. Linear Format Data Bytes

The relation between Y, N and the "real world" value is:

$X = Y \cdot 2^N$

Where, as described above:

X is the "real world" value being communicated

Y is an 11 bit, two's complement integer; and

N is a 5 bit, two's complement integer.

Devices that use the Linear format must accept and be able to process any value of N.

9.2 Power Sensors

The following PMBus commands shall be supported for the purpose of monitoring currents, voltages, and power. All sensors shall continue providing real time data as long as the PMBus device is powered. This means in standby mode the main output(s) of the power supply shall be zero amps and zero volts.

Table 33– PMBus Command Summary supported

Command Code	Name	Type	Bytes	Value	Conditions
00h	PAGE	R/W	1		
01h	OPERATION	R/W	1		
02h	ON_OFF_CONFIG	R/W	1		
03h	CLEAR_FAULTS	Send Byte	0		
05h	PAGE_PLUS_WRITE	Block W			
06h	PAGE_PLUS_READ	BW-BR process call			
19h	CAPABILITY	R	1	90h	
1Ah	QUERY	BW-BR process call			
1Bh	SMBALERT_MASK	BW-BR process call	2		
20h	VOUT_MODE	R	1	17h	
30h	COEFFICIENTS	BW-BR process call	5		
4Ah	IOUT_OC_WARN_LIMIT	R/W	2	101.8A	
79h	STATUS_WORD	R	2		
7Ah	STATUS_VOUT	R	1		
7Bh	STATUS_IOUT	R	1		
87h	READ_EOUT	Block R	6		
8Bh	READ_VOUT	R	2		
8Ch	READ_IOUT	R	2		
96h	READ_POUT	R	2		
98h	PMBUS_REVISION	R	1	22h	PMBus 1.2
99h	MFR_ID	Block R	9	FSP GROUP	
A2h	CALIBRATION OUTPUT CURRENT_1	R			
AAh	CALIBRATION OUTPUT CURRENT_2	R			
AFh	CALIBRATION OUTPUT CURRENT_3	W	1		
D9h	MFR_EEPROM_WRITE	Block W			
F8h	BOOTLOADER COMMAND	Block W			For FW boot loader
F9h	BOOTLOADER OPERTAION	W	1		For FW boot loader
FAh	BOOTLOADER CHECK SUM	R	1		For FW boot loader

9.2.1 PAGE Command (00h)

Page member :

- READ_IOUT
- READ_VOUT
- STATUS_IOUT
- STATUS_VOUT
- IOUT_OC_WARN_LIMIT

Page list of Housing:

PAGE	OUTPUT	Description
00h	12v1	Supported, Default for single 12v output
01h	12v2	--
02h	12v3	--
03h	12v4	--
04h	12v5	--
05h	12v6	--
06h-0fh	Reserved	--
10h	5v	Supported
11h	3.3v	Supported
12h-1fh	Reserved	--
20h	5vsb	Supported
21h	3.3vsb	--
22h	-12v	Supported
23h	12vsb	--
24h-2fh	Reserved	--
30h	48v	--
31h	24v	--
32h-3fh	Reserved	--

Note: “ -- ” is Not supported

9.2.2 Operation Command (01h)

Operation Notice：

This function is only supported for module operation only without PDB.

If utilized while inserted in a PDB without function support, utilization of this function might cause Unexpected side effects.

Operation command Default Value is 0x80h.

Bits [7:6]	Bits [5:4]	Bits [3:2]	Bits [1:0]	Unit On Or Off	Margin State	Description	Supported
00	XX	XX	XX	Immediate Off (No Sequencing)	N/A	Immediate turn-off	Ok
01	XX	XX	XX	Soft Off (With Sequencing)	N/A	turn-off delay and fall time	--
10	00	XX	XX	On (turn-on)	Off	Immediate turn-on	Ok
10	01	01	XX	On	Margin Low (Ignore Fault)	Margin Low (Ignore Fault)	--
10	01	10	XX	On	Margin Low (Act On Fault)	Margin Low (Act On Fault)	--
10	10	01	XX	On	Margin High (Ignore Fault)	Margin High (Ignore Fault)	--
10	10	10	XX	On	Margin High (Act On Fault)	Margin High (Act On Fault)	--

Note: " -- " is Not supported

9.2.3 ON_OFF_CONFIG Command (02h)

Operation Notice：

This function is only supported for module operation only without PDB.

If utilized while inserted in a PDB without function support, utilization of this function might cause Unexpected side effects.

ONOFF_CONFIG command Default value is 0x15h.

Bit	Purpose	Bit Value	Meaning	Default value	Supported
7:5	Reserved	Reserved	Reserved	Reserved	Reserved
4	Sets the default to either operate any time power is present or for the on/off to be controlled by CONTROL pin and serial bus commands	0	Unit powers up any time power is present regardless of state of the CONTROL pin	1	Ok
		1	Unit does not power up until commanded by the CONTROL pin and OPERATION command (as programmed in bits [3:0]).		
3	Controls how the unit responds to commands received via the serial bus	0	Unit ignores the on/off portion of the OPERATION command from serial bus	0	Ok
		1	To start, the unit requires that that the on/off portion of the OPERATION command is instructing the unit to run. Depending on bit [2], the unit may also require the CONTROL pin to be asserted for the unit to start and energize the output.		
2	Controls how the unit responds to the CONTROL pin	0	Unit ignores the CONTROL pin (on/off controlled only the OPERATION command)	1	Ok
		1	Unit requires the CONTROL pin to be asserted to start the unit. Depending on bit [3], the		

			OPERATION command may also be required to instruct the device to start before the output is energized.		
1	Polarity of the CONTROL pin	0	Active low (Pull pin low to start the unit)	0	--
		1	Active high (Pull high to start the unit)		
0	CONTROL pin action when commanding the unit to turn off	0	Use the programmed turn off delay (Section 16.5) and fall time (Section 16.6)	1	--
		1	Turn off the output and stop transferring energy to the output as fast as possible. The device's product literature shall specify whether or not the device sinks current to decrease the output voltage fall time.		

Note: " -- " is Not supported

9.2.3.1 ON_OFF_CONFIG command operation note

Setting type	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Data value	Description[1]	Supported
1	0	X	X	X	0	0x00	If AC ok, turn-on power + DLY	--
2	0	X	X	X	1	0x01	If AC ok, turn-on power	OK
3	1	0	0	X	X	0x10	null	--
4	1	0	1	0	0	0x14	HW + LO + DLY	--
5	1	0	1	0	1	0x15	HW + LO	OK
6	1	0	1	1	0	0x16	HW + HI + DLY	--
7	1	0	1	1	1	0x17	HW + HI	--
8	1	1	0	X	0	0x18	SW + DLY	--
9	1	1	0	X	1	0x19	SW	OK
10	1	1	1	0	0	0x1C	HW + LO + SW + DLY	--
11	1	1	1	0	1	0x1D	HW + LO + SW	OK
12	1	1	1	1	0	0x1E	HW + HI + SW + DLY	--
13	1	1	1	1	1	0x1F	HW + HI + SW	--

Note: " -- " is Not supported

[1] :

X = don't care

HW = turn-on/off by control pin

HI = control pin active high turn-on power

LO = control pin active low turn-on power

SW = turn-on/off by operation command

DLY = turn-off delay

9.2.4 CLEAR_FAULTS Command (03h)

Operation Notice：

Null.

Power clear faults methods

The Power have four methods can be clear PMBus faults.

Method	Description
1	PMBus clear faults command
2	PMBus operation RESET[1]
3	PS RESET[1]
4	AC RESET[1]

[1] : RESET mean is Turn-OFF → Turn-ON

9.2.5 VOUT_MODE Command (20h)

The data bytes for the VOUT_MODE and VOUT_COMMAND when using the Linear voltage data format are shown in Figure 10.

Note that the VOUT_MODE command is sent separately from output voltage related commands and only when the output voltage format changes.

VOUT_MODE is not sent every time an output voltage command is sent.

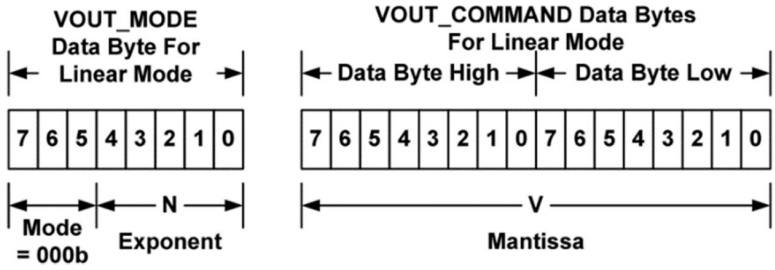

Figure 10. Linear Data Format Data Bytes

The Mode bits are set to 000b.

The Voltage, in volts, is calculated from the equation:

Voltage = $V \cdot 2^N$

Where:

Voltage is the parameter of interest in volts;

V is a 16 bit unsigned binary integer; and

N is a 5 bit two’s complement binary integer.

9.2.6 STATUS_WORD Command (79h)

STATUS_WORD Command：

Byte	Bit Number	Status Bit Name	Meaning	Supported
Low	7	BUSY	A fault was declared because the device was busy and unable to respond.	--
	6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.	Ok
	5	VOUT_OV	An output overvoltage fault has occurred	Ok
	4	IOUT_OC	An output overcurrent fault has occurred	Ok
	3	VIN_UV	An input under voltage fault has occurred	--
	2	TEMPERATURE	A temperature fault or warning has occurred	--
	1	CML	A communications, memory or logic fault has occurred	--
	0	NONE OF THE ABOVE	A fault or warning not listed in bits [7:1] of this byte has occurred	--
High	7	VOUT	An output voltage fault or warning has occurred	Ok
	6	IOUT/POUT	An output current or output power fault or warning has occurred	Ok
	5	INPUT	An input voltage, input current, or input power fault or warning has occurred	--
	4	MFR	A manufacturer specific fault or warning has occurred	--
	3	POWER_GOOD#	The POWER_GOOD signal, if present, is negated	Ok
	2	FANS	A fan or airflow fault or warning has occurred	--
	1	OTHER	A bit in STATUS_OTHER is set	--
	0	UNKNOWN	A fault type not given in bits [15:1] of the SATUS_WORD has been detected	--

9.2.7 STATUS_VOUT Command (7Ah)

Bit	Meaning	Supported
7	VOUT Over voltage Fault	Ok
6	VOUT Over voltage Warning	Ok
5	VOUT Under voltage Warning	Ok
4	VOUT Under voltage Fault	Ok
3	VOUT_MAX Warning (An attempt has been made to set the output voltage to value higher than allowed by the VOUT_MAX command	--
2	TON_MAX_FAULT	--
1	TOFF_MAX Warning	--
0	VOUT Tracking Error	--

9.2.8 STATUS_IOUT Command (7Bh)

Bit	Meaning	Supported
7	IOUT Over current Fault	Ok
6	IOUT Over current And Low Voltage Shutdown Fault	--
5	IOUT Over current Warning	Ok
4	IOUT Under current Fault	--
3	Current Share Fault	--
2	Power Limiting	--
1	POUT Over power Fault	--
0	POUT Over power Warning	--

9.2.9 Bootloader Function(F8h, F9h, FAh)

Command	Operation	Function
F8h	00	Enter user mode
	01	Enter boot mode
F9h	00	Write hex data
	01	Erase hex data
FAh		Read hex data checksum

Bootloader Flow:

STEP 1	0x4A 0xF8 0x01	Boot mode command
STEP 2	0x4A 0xF9 0x01	Erase RAM command
STEP 3	Wait 2000ms	Erase Time
STEP 4 STEP 5 STEP 6 Replay 4~6 STEP	0x4A 0xF9 0x00 Wait 1ms 32 bytes data	Write command Wait 1ms Write Data
STEP 7	Consecutive 32 data is 0xFF	Write to finish
STEP 8	Wait 140ms	Wait 140ms
STEP 9	0x4A 0xF8 0x00	Go to User mode
STEP 10	0x4A 0x00 0x00	Go to User mode
STEP 11	Wait 2000ms	Go to User mode Time
STEP 12	Read 0x4A 0xFA	Verify Checksum
		Finish

9.3 Firmware Protection

9.3.1 Firmware Protection

1. Vout Over Voltage

Output voltage	Warning threshold	Protect threshold
12V	13.2V	13.8V
5V	5.5V	6.1V
3.3V	3.63V	3.9V
-12V	-13.2V	-13.8V
5Vsb	--	6.1V

2. Vout Under Voltage

Output voltage	Warning threshold	Protect threshold
12V	10.8V	9V
5V	4.5V	3.5V
3.3V	2.97V	2.2V
-12V	-10.8V	-9V
5Vsb	--	3.5V

3. Iout Over Current

Output voltage	Warning threshold	Protect threshold
12V	101.8A	106.7A
5V	30A	33A
3.3V	30A	33A
5Vsb	5A	5.5A maximum