innodisk

The Total Solution For Industrial Flash Storage

Approval Sheet

Customer	
Product Number	**M3XT-8GSSDLPC-E**
Module speed	**PC3-12800**
Pin	**240pin**
Cl-tRCD-tRP	**11-11-11**
Operating Temp	**0℃~85℃**
Date	**6th April 2022**

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			CL	tRCD	tRP
		CL=7	CL=9	CL=11			
PC3-12800	**P**	1066	1333	1600	11	11	11

- 240-pin eXtreme Rugged Dual In-Line Memory Module
- Intend for PC3-12800 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.35 Volt (-0.067/+0.1V), 1.5 Volt (-0.075/+0.075V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs (TC ≤ +85°C)
- 16/10/2 Addressing (row/column/rank)-8GB
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 6,7,8,9,10,11
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant *(Section 11)*

2. Ordering Information

DDR3L XR-DIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M3XT-8GSSDLPC-E	8GB	PC3-12800	1Gx64	16	2	N

3. Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VSS	2	VSS	121	CK1_t	122	A1
3	VSS	4	VSS	123	CK1_n	124	VDD
5	DQ0	6	DQ4	125	VDD	126	CK0_t
7	DQ1	8	DQ5	127	VREFCA	128	CK0_c
9	VSS	10	VSS	129	PAR_IN	130	VDD
11	DQS0_c	12	DM0	131	VDD	132	EVENT_n
13	DQS0_t	14	VSS	133	A10/AP	134	A0
15	VSS	16	DQ6	135	BA0	136	VDD
17	DQ2	18	DQ7	137	VDD	138	BA1
19	DQ3	20	VSS	139	WE_n	140	VDD
21	VSS	22	DQ12	141	CAS_n	142	RAS_n
23	DQ8	24	DQ13	143	VDD	144	S0_n
25	DQ9	26	VSS	145	S1_n	146	VDD
27	VSS	28	DM1	147	ODT1	148	ODT0
29	DQS1_c	30	VSS	149	VDD	150	A13
31	DQS1_t	32	DQ14	151	S3_n/NC	152	VDD
33	VSS	34	DQ15	153	VSS	154	S2_n/NC
35	DQ10	36	VSS	155	DQ32	156	VSS
37	DQ11	38	DQ20	157	DQ33	158	DQ36
39	VSS	40	DQ21	159	VSS	160	DQ37
41	DQ16	42	VSS	161	DQS4_c	162	VSS
43	DQ17	44	VREFDQ	163	DQS4_t	164	DM4
45	VSS	46	NC(TEST)	165	VSS	166	VSS
47	DQS2_c	48	VSS	167	DQ34	168	DQ38
49	DQS2_t	50	DM2	169	DQ35	170	DQ39
51	VSS	52	VSS	171	VSS	172	VSS
53	DQ18	54	DQ22	173	DQ40	174	DQ44
55	DQ19	56	DQ23	175	DQ41	176	DQ45
57	VSS	58	VSS	177	VSS	178	VSS
59	DQ24	60	DQ28	179	DQS5_c	180	DM5
61	DQ25	62	DQ29	181	DQS5_t	182	VSS
63	VSS	64	VSS	183	VSS	184	DQ46
65	DQS3_c	66	DM3	185	DQ42	186	DQ47
67	DQS3_t	68	VSS	187	DQ43	188	VSS

69	VSS	**70**	DQ30	**189**	VSS	**190**	DQ52
71	DQ26	**72**	DQ31	**191**	DQ48	**192**	DQ53
73	DQ27	**74**	VSS	**193**	DQ49	**194**	VSS
75	VSS	**76**	CB4	**195**	VSS	**196**	DM6
77	CB0	**78**	CB5	**197**	DQS6_c	**198**	VSS
79	CB1	**80**	VSS	**199**	DQS6_t	**200**	DQ54
81	VSS	**82**	DM8	**201**	VSS	**202**	DQ55
83	DQS8_c	**84**	VSS	**203**	DQ50	**204**	VSS
85	DQS8_t	**86**	CB6	**205**	DQ51	**206**	DQ60
87	VSS	**88**	CB7	**207**	VSS	**208**	DQ61
89	CB2	**90**	VSS	**209**	DQ56	**210**	VSS
91	CB3	**92**	RESET_n	**211**	DQ57	**212**	DM7
93	VSS	**94**	ERR_OUT_n	**213**	VSS	**214**	VSS
95	VTT	**96**	VTT	**215**	DQS7_c	**216**	DQ62
97	CKE0	**98**	CKE1	**217**	DQS7_t	**218**	DQ63
99	VDD	**100**	VDD	**219**	VSS	**220**	VSS
101	BA2	**102**	A15	**221**	DQ58	**222**	VDDSPD
103	VDD	**104**	A14	**223**	DQ59	**224**	SA0
105	A11	**106**	VDD	**225**	VSS	**226**	SA1
107	A7	**108**	A12/BC	**227**	SA2	**228**	SCL
109	VDD	**110**	A9	**229**	VSS	**230**	SDA
111	A5	**112**	VDD	**231**	SATA_RX_p	**232**	VSS
113	A4	**114**	A8	**233**	SATA_RX_n	**234**	SATA_TX_n
115	VDD	**116**	A6	**235**	VSS	**236**	SATA_TX_p
117	A2	**118**	VDD	**237**	VTT	**238**	VSS
119	VDD	**120**	A3	**239**	VTT	**240**	VTT

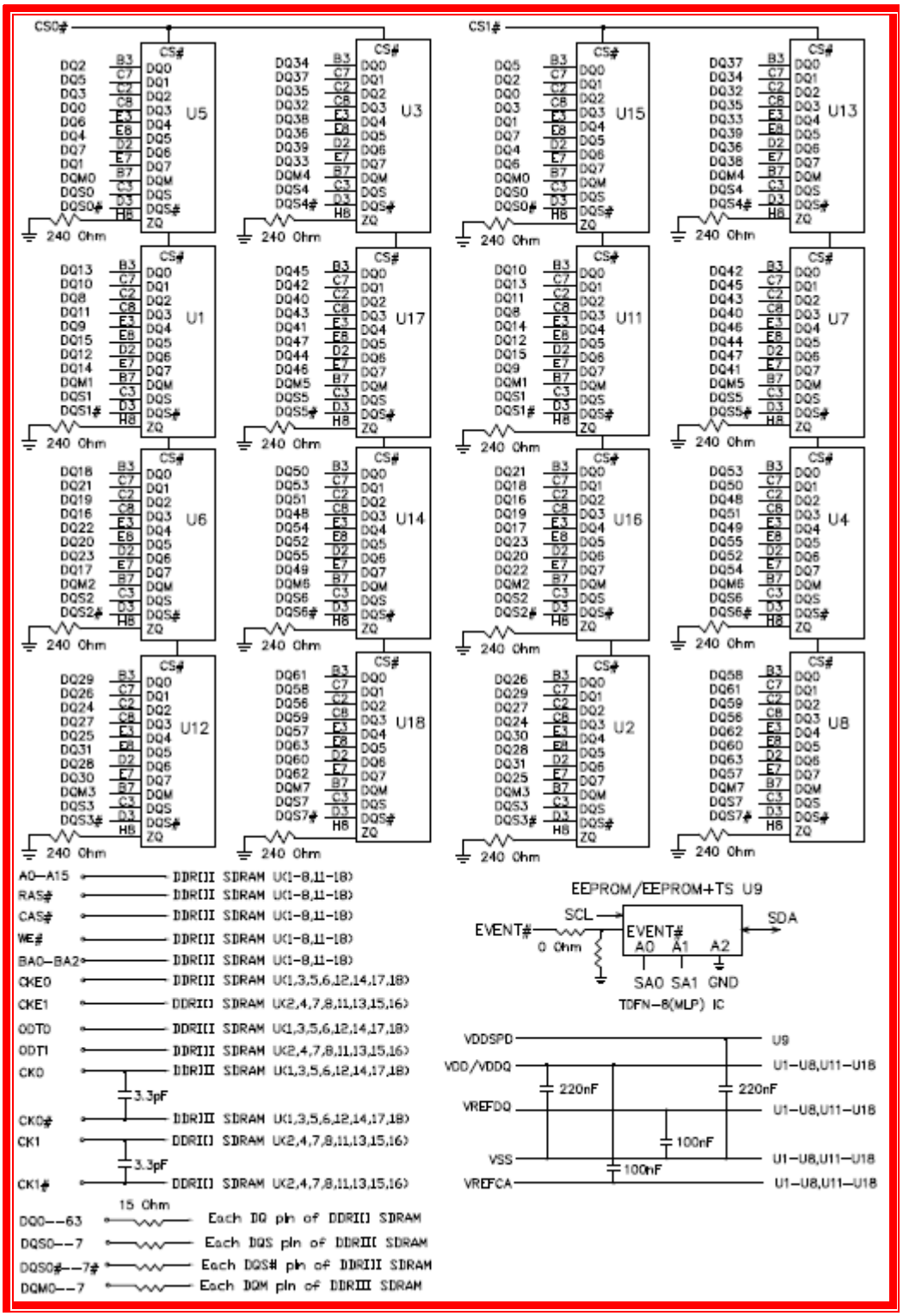
4. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 – A15	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 – BA2	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
RAS_n	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
CAS_n	SDRAM column address strobe	V_{DD}	Power Supply
WE_n	SDRAM write enable	V_{DDID}	V_{DD} Identification Flag
S0_n - /S3_n	DIMM Rank Select Lines	V_{DDQ}	SDRAM I/O Driver power supply
CKE0 – CKE1	SDRAM clock enable lines	V_{REFDQ}	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V_{REFCA}	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0_t–DQS8_t DQS0_c–DQS8_c	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	Reset_n	Reset enable
CK0_t–CK1_t CK0_c–CK1_c	Differential SDRAM Clocks	Event_n	Reserved for optional temperature-sensing hardware
PAR_IN	XR-RDIMM only: Parity bit for the Address and Control bus. (“1 “: Odd, “0 “:Even)	V_{TT}	SDRAM I/O termination supply.
ERR_OUT_n	RS_RDIMM only: Parity error detected on the Address and Control bus. A resistor may be connected from Err_Out_n bus line to VDD on the system planar to act as a pull up.	NC	Not connected
SATA_RX_p SATA_RX-n	Differential SATA Receive signal pair	SATA_TX_p SATA_TX-n	Differential SATA Transmit signal pair

5. Function Block Diagram:

- (8GB, 2 Ranks, 512Mx8 DDR3L SDRAMs)



6. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Operating Temp.	0 to 85	°C	1,2
		Extended Temp.	85 to 95	°C	1,3
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.8	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.8	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.8	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

7. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
Recommended DC Operating Conditions - DDR3L (1.35V) operation						
V_{DD}	Supply Voltage	1.283	1.35	1.45	V	1,2
VDDSPD	Supply Voltage	3	3.3	3.6	V	
V_{DDQ}	Supply Voltage	1.283	1.35	1.45	V	1,2
Recommended DC Operating Conditions - DDR3 (1.5V) operation						
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDSPD	Supply Voltage	3	3.3	3.6	V	
V_{DDQ}	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
V_{IH} (DC) DDR3L	DC Input High (Logic1) Voltage	VREF + 90	-	V_{DD}	mV	3
V_{IH} (DC) DDR3	DC Input High (Logic1) Voltage	VREF + 100		V_{DD}	mV	3
V_{IL} (DC) DDR3L	DC Input Low (Logic 0) Voltage	V_{SS}	-	V_{REF} - 90	mV	3
V_{IL} (DC) DDR3	DC Input Low (Logic 0) Voltage	V_{SS}		V_{REF} - 100	mV	3
V_{IH} (AC) DDR3L	AC Input High (Logic1) Voltage	V_{REF}+ 135	-	-	mV	3
V_{IH} (AC) DDR3	AC Input High (Logic1) Voltage	V_{REF}+ 150			mV	3
V_{IL} (AC) DDR3L	AC Input Low (Logic 0) Voltage	-	-	V_{REF} - 135	mV	3
V_{IL} (AC) DDR3	AC Input Low (Logic 0) Voltage			V_{REF} - 150	mV	3
V_{REFDQ} (DC)	Reference Voltage for DQ, DM inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
V_{REFCA} (DC)	Reference Voltage for ADD,CMD inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
Single Ended AC/DC Output Levels						
V_{OH} (DC)	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
V_{OM} (DC)	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
V_{OL} (DC)	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	
V_{OH} (AC)	AC output high measurement level (for output SR)	-	VTT + 0.1 x VDDQ	-	V	6

$V_{OL\ (AC)}$	AC output low measurement level (for output SR)		VTT - 0.1 x VDDQ	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
$V_{IHdiff\ DDR3L}$	Differential Input high	+0.18	-	Note 9	V	7
$V_{IHdiff\ DDR3}$	Differential Input high	+0.2		Note 9	V	7
$V_{ILdiff\ DDR3L}$	Differential Input logic Low	Note 9	-	-0.18	V	7
$V_{ILdiff\ DDR3}$	Differential Input logic Low	Note 9	-	-0.2	V	7
$V_{IHdiff(ac)\ DDR3L}$	Differential Input high ac	2* ($V_{IH\ (AC)}$- V_{REF})	-	Note 9	V	8
$V_{IHdiff(ac)\ DDR3}$	Differential Input high ac	2* ($V_{IH\ (AC)}$- V_{REF})	-	Note 9	V	8
$V_{ILdiff(ac)\ DDR3L}$	Differential Input logic Low ac	Note 9	-	2* (V_{REF}- $V_{IL\ (AC)}$)	V	8
$V_{ILdiff(ac)\ DDR3}$	Differential Input logic Low ac	Note 9	-	2* (V_{REF}- $V_{IL\ (AC)}$)	V	8
Differential AC and DC Output Levels						
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
4. Recommended DC Operating Conditions - DDR3 (1.5V) operation : The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV); Recommended DC Operating Conditions - DDR3L (1.35V) operation: The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV)
5. For reference: approx. VDD/2.
6. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2
7. Used to define a differential signal slew-rate.
8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.
10. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

8. Operating, Standby, and Refresh Currents

- 8GB XR-DIMM (2 Ranks, 512Mx8 DDR3L SDRAMs)

Symbol	Parameter/Condition		PC3-12800	Unit
I DD0	One bank; Active - Precharge		416	mA
I DD1	One bank; Active - Read - Precharge		576	mA
I DD2N	Precharge Standby Current		176	mA
IDD2NT	Precharge Standby ODT Current		208	mA
I DD2P	Precharge Power Down Current	Fast Mode	128	mA
	Precharge Power Down Current	Slow Mode	128	mA
I DD2Q	Pecharge Quiet Standby Current		160	mA
I DD3N	Active Standby Current		336	mA
I DD3P	Active Power-Down Current		160	mA
I DD4R	Operating Current Burst Read		1024	mA
I DD4W	Operating Current Burst Write		1008	mA
I DD5B	Burst Refresh Current		3040	mA
I DD6	Self-Refresh Current: Normal Temperature Range		192	mA
I DD7	Operating Bank Interleave Read Current		1936	mA
I DD8	RESET Low Current		240	mA

9. Timing Parameters

Symbol	Parameter	PC3-12800		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.25	<1.5	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-70	70	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-60	60	Ps
JIT (CC)	Cycle to Cycle Period Jitter	140		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	120		Ps
TERR (2per)	Cumulative error across 2 cycle	-103	103	Ps
TERR (3per)	Cumulative error across 3 cycle	-122	122	Ps
TERR (4per)	Cumulative error across 4 cycle	-136	136	Ps
TERR (5per)	Cumulative error across 5 cycle	-147	147	Ps
TERR (6per)	Cumulative error across 6 cycle	-155	155	Ps
TERR (7per)	Cumulative error across 7 cycle	-163	163	Ps
TERR (8per)	Cumulative error across 3 cycle	-169	169	Ps
TERR (9per)	Cumulative error across 4 cycle	-175	175	Ps
TERR (10per)	Cumulative error across 5 cycle	-180	180	Ps
TERR (11per)	Cumulative error across 6 cycle	-184	184	Ps
TERR (12per)	Cumulative error across 7 cycle	-188	188	Ps

TERR (nper)	Cumulative error across 13~50 cycle	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		Ps
Data Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDQSQ	DQS, DQS# to DQ skew, per group, per access	-	100	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-450	225	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	225	Ps
1.35V				
tDS(base) AC160	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC135		25	-	Ps
tDS(base) AC125		-	-	Ps
tDH(base) DC90	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	55	-	Ps
1.5V				
tDS(base) AC175	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC150		10	-	Ps
tDS(base) AC135		-	-	Ps
tDH(base) DC100	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	45	-	Ps
Data Strobe Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)

tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps
tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
Command and Address Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			

tCCD		4	-	nCK
tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	35	9 *tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	40	-	ns
1.35V				
tIS(base) AC160	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	60	-	Ps
tIS(base) AC135		185	-	Ps
tIS(base) AC125		-	-	Ps
tIH(base) DC90	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	130	-	Ps
1.5V				
tIS(base) AC175	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	45	-	Ps
tIS(base) AC150		170	-	Ps
tIS(base) AC135		-	-	Ps
tIS(base) AC125		-	-	Ps
tIH(base) DC100	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	120	-	Ps
Calibration Timing				

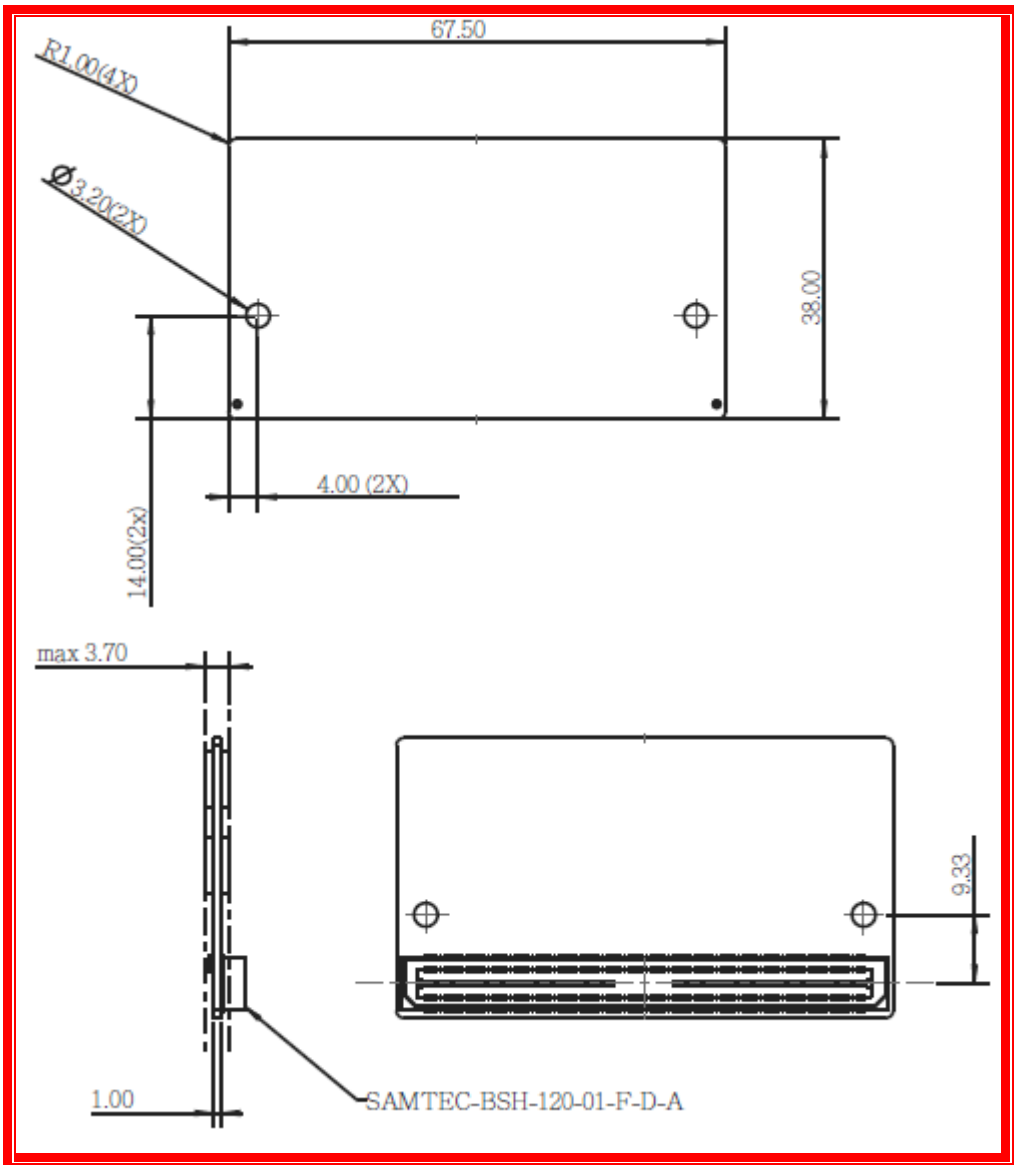
Symbol	Parameter	Min.	Max.	Unit
tZQinit	Power-up and RESET calibration time	512	-	nCK
tZQoper	Normal operation Full calibration time	256	-	nCK
tZQCS	Normal operation Short calibration time	64	-	nCK
Reset Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK,tRFC+10ns)	-	
Self Refresh Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC+10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE(min)+1tCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK, 10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK, 10ns)	-	
Power Down Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	

tCKE	CKE minimum pulse width	max(3nCK,5ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCKE(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns

tAON	RTT-turn-on	-225	225	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)
Write Leveling Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	165	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	165	-	ps
tWLO	Write leveling output delay	0	7.5	ns
tWLOE	Write leveling output error	0	2	ns

10. PACKAGE DIMENSION

- (8GB, 2 Ranks, 512Mx8 DDR3L base XR-DIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

11. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Page 1/1

Tel:(02)7703-3000 Internet: https://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

三、 本公司聲明我們的產品符合 RoHS 指令的附件中(7a)、(7c-I)允許豁免。
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.
※ (7a) Lead in high melting temperature type solders(i.e. lead-based alloys containing 85% by weight or more lead).
※ (7C-I) Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
鉛（Pb）	< 1000 ppm
汞（Hg）	< 1000 ppm
鎘（Cd）	< 100 ppm
六價鉻（Cr 6+）	< 1000 ppm
多溴聯苯（PBBs）	< 1000 ppm
多溴二苯醚（PBDEs）	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯（DEHP）	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯（BBP）	< 1000 ppm
鄰苯二甲酸二丁酯（DBP）	< 1000 ppm
鄰苯二甲酸二異丁酯（DIBP）	< 1000 ppm

立 保 證 書 人 (Guarantor)

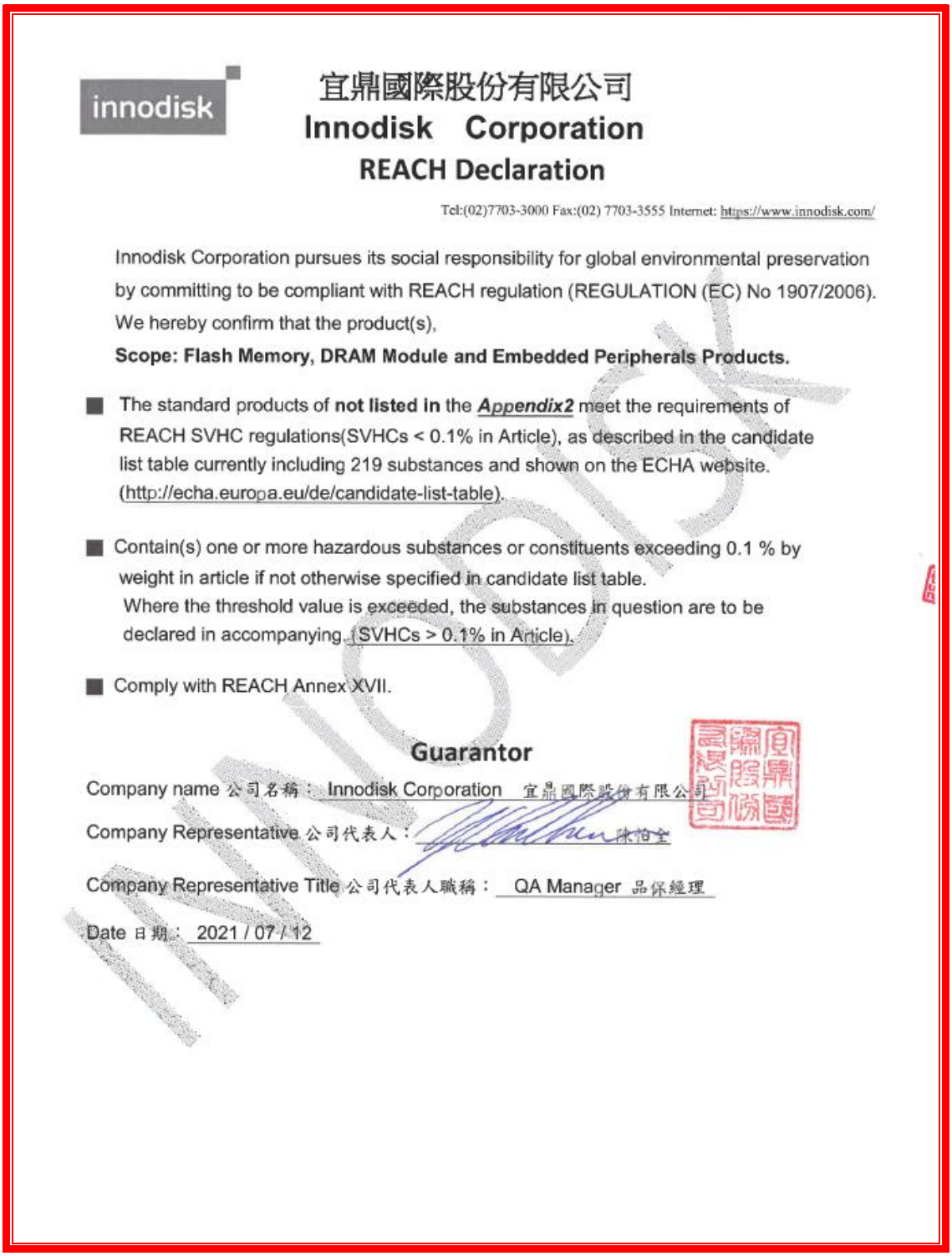
Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2020 / 03 / 03

12. REACH Declaration



宜鼎國際股份有限公司
Innodisk Corporation
REACH Declaration

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: https://www.innodisk.com/

Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006).
We hereby confirm that the product(s),
Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.

- The standard products of **not listed in** the ***Appendix2*** meet the requirements of REACH SVHC regulations(SVHCs < 0.1% in Article), as described in the candidate list table currently including 219 substances and shown on the ECHA website. (http://echa.europa.eu/de/candidate-list-table).
- Contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table.
  Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs > 0.1% in Article).
- Comply with REACH Annex XVII.

Guarantor

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： 陳柏全

Company Representative Title 公司代表人職稱： QA Manager 品保經理

Date 日期： 2021 / 07 / 12

13. Revision Log

Rev	Date	Modification
0.1	6th April 2022	Preliminary Edition
1.0	6th April 2022	Official released.