innodisk

The Total Solution For Industrial Flash Storage

Approval Sheet

Customer	
Product Number	**M4XI-AGS1QCSJ-C**
Module speed	**PC4-2400**
Pin	**300 pin**
Cl-tRCD-tRP	**17-17-17**
Operating Temp	**0℃~85℃**
Date	**14th May 2020**

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			CL	tRCD	tRP
		CL=13	CL=15	CL=17			
PC4-2400	**S**	1866	2133	2400	17	17	17

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- 300-pin eXtreme Rugged Dual in-line memory module (XRDIMM)
- Intend for PC4-2400 applications
- Inputs and Outputs are SSTL-12 compatible
- V_{DD}=V_{DDQ}= 1.2 Volt (1.14V~1.26V)
- V_{PP}=2.5 Volt (2.375V~2.75V)
- V_{DDSPD}=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Fly-By topology
- Terminated control, command and address bus
- Programmable /CAS Latency: 10,11,12,13,14,15,16,17,18
- On-die V_{REFDQ} generation and Calibration
- Temperature Sensor with EEPROM
- RoHS and Halogen free *(Section 11)*
- BSH-150-01-F-D-A connector

2. Ordering Information

DDR4 XRDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M4XI-AGS1QCSJ-C	16GB	PC4-2400	2Gx72	18	2	Y

3. Pin Configurations (Front side/Back side)

Pin	Odd-Row	Pin	Even-Row	Pin	Odd-Row	Pin	Even-Row
1	NC	2	NC	153	EVENT_N/NF	154	A1
3	NC	4	NC	155	VDD	156	VDD
5	NC	6	NC	157	CK1_T/NF	158	CK0_T
7	NC	8	NC	159	CK1_C/NF	160	CK0_C
9	NC	10	NC	161	VDD	162	VDD
11	NC	12	NC	163	A0	164	PARITY
13	NC	14	NC	165	A10/AP	166	BA1
15	NC	16	NC	167	VDD	168	VDD
17	NC	18	NC	169	BA0	170	CS0_N
19	NC	20	NC	171	RAS_N/A16	172	WE_N/A14
21	VSS	22	VSS	173	VDD	174	VDD
23	DQ4	24	DQ5	175	CAS_N/A15	176	ODT0
25	VSS	26	VSS	177	A13	178	CS1_N
27	DQ0	28	DQ1	179	VDD	180	VDD
29	VSS	30	VSS	181	C0/CS2_N/NC	182	ODT1
31	DM0_N/DBI0_N	32	DQS0_C	183	VREFCA	184	VDD
33	VSS	34	DQS0_T	185	SA2	186	C1/CS3_N/NC
35	DQ6	36	VSS	187	VSS	188	VSS
37	VSS	38	DQ7	189	DQ36	190	DQ37
39	DQ2	40	VSS	191	VSS	192	VSS
41	VSS	42	DQ3	193	DQ32	194	DQ33
43	DQ12	44	VSS	195	VSS	196	VSS
45	VSS	46	DQ13	197	DM4_N/DBI4_N	198	DQS4_C
47	DQ8	48	VSS	199	VSS	200	DQS4_T
49	VSS	50	DQ9	201	DQ39	202	VSS
51	DQS1_C	52	VSS	203	VSS	204	DQ38
53	DQS1_T	54	DM1_N/DBI1_N	205	DQ35	206	VSS
55	VSS	56	VSS	207	VSS	208	DQ34
57	DQ14	58	DQ15	209	DQ45	210	VSS
59	VSS	60	VSS	211	VSS	212	DQ44
61	DQ11	62	DQ10	213	DQ41	214	VSS
63	VSS	64	VSS	215	VSS	216	DQ40
65	DQ20	66	DQ21	217	DQS5_C	218	VSS
67	VSS	68	VSS	219	DQS5_T	220	DM5_N/DBI5_N
69	DQ16	70	DQ17	221	VSS	222	VSS

71	VSS	72	VSS	223	DQ47	224	DQ46
73	DM2_N/DBI2_N	74	DQS2_C	225	VSS	226	VSS
75	VSS	76	DQS2_T	227	DQ43	228	DQ42
77	DQ22	78	VSS	229	VSS	230	VSS
79	VSS	80	DQ23	231	DQ53	232	DQ52
81	DQ18	82	VSS	233	VSS	234	VSS
83	VSS	84	DQ19	235	DQ48	236	DQ49
85	DQ28	86	VSS	237	VSS	238	VSS
87	VSS	88	DQ29	239	DM6_N/DBI6_N	240	DQS6_C
89	DQ24	90	VSS	241	VSS	242	DQS6_T
91	VSS	92	DQ25	243	DQ54	244	VSS
93	DQS3_C	94	VSS	245	VSS	246	DQ55
95	DQS3_T	96	DM3_N/DBI3_N	247	DQ50	248	VSS
97	VSS	98	VSS	249	VSS	250	DQ51
99	DQ31	100	DQ30	251	DQ60	252	VSS
101	VSS	102	VSS	253	VSS	254	DQ61
103	DQ27	104	DQ26	255	DQ57	256	VSS
105	VSS	106	VSS	257	VSS	258	DQ56
107	CB4/NC	108	CB5/NC	259	DQS7_C	260	VSS
109	VSS	110	VSS	261	DQS7_T	262	DM7_N/DBI7_N
111	CB0/NC	112	CB1/NC	263	VSS	264	VSS
113	VSS	114	VSS	265	DQ63	266	DQ62
115	DM8_N/DBI8_N	116	DQS8_C	267	VSS	268	VSS
117	VSS	118	DQS8_T	269	DQ59	270	DQ58
119	CB6/NC	120	VSS	271	VSS	272	VSS
121	VSS	122	CB2/NC	273	SDA	274	SCL
123	CB7/NC	124	VSS	275	SA0	276	VDDSPD
125	VSS	126	CB3/NC	277	VTT	278	VPP
127	RESET_N	128	VSS	279	SA1	280	VPP
129	CKE1	130	CKE0	281	NC	282	NC
131	VDD	132	VDD	283	NC	284	NC
133	ACT_N	134	BG1	285	NC	286	NC
135	ALERT_N	136	BG0	287	NC	288	NC
137	VDD	138	VDD	289	NC	290	NC
139	A11	140	A12	291	NC	292	NC
141	A7	142	A9	293	NC	294	NC
143	VDD	144	VDD	295	NC	296	NC

145	A5	146	A8	297	NC	298	NC
147	A4	148	A6	299	NC	300	NC
149	VDD	150	VDD				
151	A2	152	A3				

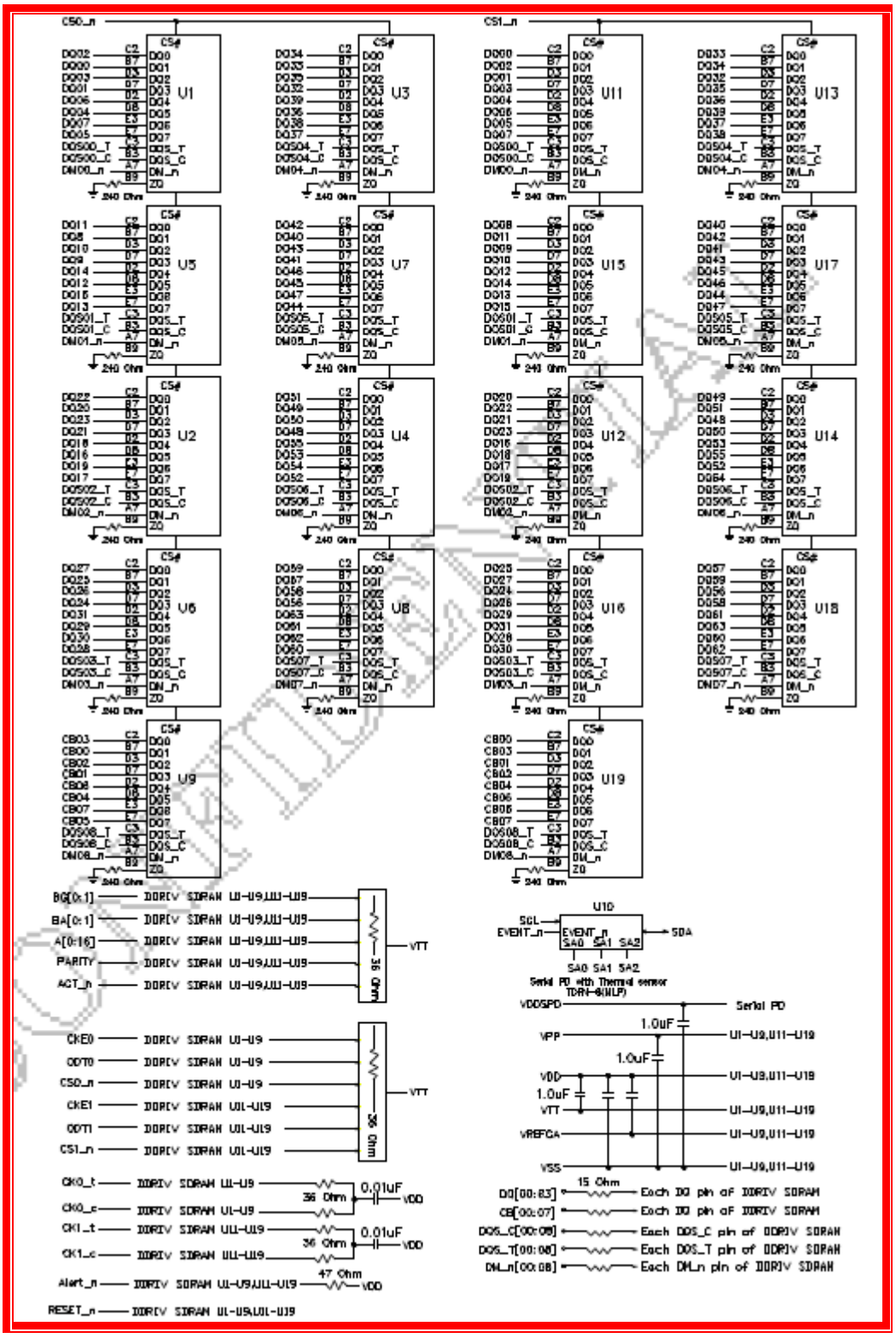
4. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0–A16	SDRAM address bus	SCL	I^2C serial bus clock for SPD/TS
BA0, BA1	SDRAM bank select	SDA	I^2C serial bus data line for SPD/TS
BG0, BG1	SDRAM bank group select	SA0–SA2	I^2C slave address select for SPD/TS
RAS_n	SDRAM row address strobe	PARITY	SDRAM parity input
CAS_n	SDRAM column address strobe	VDD	SDRAM I/O & core power supply
WE_n	SDRAM write enable	VPP	SDRAM activating power supply
CS0_n, CS1_n CS2_n, CS3_n	Rank Select Lines	C0, C1	Chip ID lines for 3DS components
CKE0, CKE1	SDRAM clock enable lines	VREFCA	SDRAM command/address reference supply
ODT0, ODT1	SDRAM on-die termination control lines	VSS	Power supply return (ground)
ACT_n	SDRAM activate	VDDSPD	Serial SPD/TS positive power supply
DQ0–DQ63	DIMM memory data bus	ALERT_n	SDRAM ALERT_n
CB0–CB7	DIMM ECC check bits (for x72 module)	VPP	SDRAM Activating Power Supply: 2.5V (2.375V min, 2.75V max)
DQS0_t–DQS8_t	SDRAM data strobes (positive line of differential pair)	RESET_n	Set SDRAMs to a Known State
DQS0_c–DQS8_c	SDRAM data strobes (negative line of differential pair)	EVENT_n	SPD signals a thermal event has occurred.
DM0_n–DM8_n, DBI0_n-DBI8_n	SDRAM data masks/data bus inversion (x8-based x72 DIMMs)	VTT	Termination supply for the Address, Command and Control bus
CK0_t, CK1_t	SDRAM clocks (positive line of differential pair)	NC	No connection
CK0_c, CK1_c	SDRAM clocks (negative line of differential pair)		

5. Function Block Diagram:

- (16GB, 2 Rank 1Gx8 DDR4 SDRAMs)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

6. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.3 to +1.5	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.3 to +1.5	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.3 to +1.5	V	4,6

Note:

1) Operating Temperature TOPER is the case surface temperature on the center/top side of the DRAM.

2) The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0-85°C under all operating conditions.

3) Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

7. Operating Condition

Symbol	Parameter	Min	Nom	Max	Units	Notes
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1
V_{PP}	DRAM activating power supply	2.375	2.5	2.75	V	2
$V_{REFCA(DC)}$	Input reference voltage command/ address bus	0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	V	3
V_{TT}	Termination Voltage	0.49 × VDD	0.5 × VDD	0.51 × VDD	V	4

Note:

1. VDDQ tracks with VDD; VDDQ and VDD are tied together.
2. VPP must be greater than or equal to VDD at all times.
3. VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
4. VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.

8. Operating, Standby, and Refresh Currents

- 16GB XRDIMM (2 Rank 1Gx8 DDR4 SDRAMs)

Symbol	Proposed Conditions	Value		Units
		IDD Max.	IPP Max.	
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	486	72	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	522	72	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	576	72	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	612	72	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	324	54	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	324	54	mA

IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	324	54	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	252	54	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	306	54	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	306	54	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	342	54	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	198	54	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	306	54	mA
IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	486	54	mA

IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	504	54	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	342	54	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1476	54	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	1548	54	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	1530	54	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	1440	54	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	1530	54	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	1440	54	mA

IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	1278	54	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	1602	54	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	3330	324	mA
IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	2340	270	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	1944	252	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	378	72	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	612	90	mA

IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	270	90	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	378	90	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	2430	180	mA
IDD8	Maximum Power Down Current TBD	162	54	mA

9. Timing Parameters

Clock Timing				
Parameter	Symbol	MIN	MAX	Units
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns
Average Clock Period	tCK(avg)	0.833	<0.938	ns
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min_ to t	tCK(avg)max + tJIT(per)max_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)
Clock Period Jitter- total	JIT(per)_tot	-42	42	ps
Clock Period Jitter- deterministic	JIT(per)_dj	-21	21	ps
Clock Period Jitter during DLL lock-ing period	tJIT(per, lck)	-33	33	ps
Cycle to Cycle Period Jitter	tJIT(cc)_to-tal	83		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	67		ps
Cumulative error across 2 cycles	tERR(2per)	-61	61	ps
Cumulative error across 3 cycles	tERR(3per)	-73	73	ps
Cumulative error across 4 cycles	tERR(4per)	-81	81	ps
Cumulative error across 5 cycles	tERR(5per)	-87	87	ps
Cumulative error across 6 cycles	tERR(6per)	-92	92	ps
Cumulative error across 7 cycles	tERR(7per)	-97	97	ps

Cumulative error across 8 cycles	tERR(8per)	-101	101	ps
Cumulative error across 9 cycles	tERR(9per)	-104	104	ps
Cumulative error across 10 cycles	tERR(10per)	-107	107	ps
Cumulative error across 11 cycles	tERR(11per)	-110	110	ps
Cumulative error across 12 cycles	tERR(12per)	-112	112	ps
Cumulative error across 13 cycles	tERR(13per)	-114	114	ps
Cumulative error across 14 cycles	tERR(14per)	-116	116	ps
Cumulative error across 15 cycles	tERR(15per)	-118	118	ps
Cumulative error across 16 cycles	tERR(16per)	-120	120	ps
Cumulative error across 17 cycles	tERR(17per)	-122	122	ps
Cumulative error across 18 cycles	tERR(18per)	-124	124	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		ps
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	62	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	162	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	87	-	ps
Command and Address hold time to CK_t, CK_c referenced	tIH(Vref)	162	-	ps

to Vref levels				
Control and Address Input pulse width for each input	tIPW	410	-	ps
Command and Address Timing				
Parameter	Symbol	MIN	MAX	Units
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5 ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,3.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 1/ 2KB page size	tRRD_S(1/ 2K)	Max(4nCK,3.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,4.9ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nCK,4.9ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,13ns)	-	ns
Delay from start of internal write transaction to internal read com-mand for different	tWTR_S	max(2nCK,2.5ns)	-	

bank group				
Delay from start of internal write transaction to internal read com-mand for same bank group	tWTR_L	max(4nCK,7.5ns)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for different bank group with both CRC and DM enabled	tWTR_S_C RC_DM	tWTR_S+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for same bank group with both CRC and DM enabled	tWTR_L_C RC_DM	tWTR_L+max (5nCK,3.75ns)	-	ns
DLL locking time	tDLLK	768	-	nCK
Mode Register Set command cycle time	tMRD	8	-	nCK
Mode Register Set command up-date delay	tMOD	max(24nCK,15ns)	-	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
Multi Purpose Register Write Re-covery Time	tWR_MPR	tMOD (min) + AL + PL	-	-
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	UI
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing	tPDA_H	0.5	-	UI

edge				
CS_n to Command Address Latency				
CS_n to Command Address Laten-cy	tCAL	5	-	nCK
DRAM Data Timing				
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	tCK(avg) /2
DQ output hold time from DQS_t,DQS_c	tQH	0.78	-	tCK(avg) /2
Data Valid Window per device: tQH - tDQSQ for a device	tDVWd	0.64	-	UI
Data Valid Window per device, per pin: tQH - tDQSQ each device's out-put	tDVWp	0.72	-	UI
Data Strobe Timing				
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9	-	tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	-	tCK
DQS_t,DQS_c differential output high time	tQSH	0.4	-	tCK
DQS_t,DQS_c differential output low time	tQSL	0.4	-	tCK
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	-	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-1)	tLZ(DQS)	-330	175	ps
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	175	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS_t, DQS_c differential	tDQSH	0.46	0.54	tCK

input high pulse width				
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK
DQS_t, DQS_c rising edge output timing locatino from rising	tDQSCK (DLL On)	-175	175	ps
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		290	ps
MPSM Timing				
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		
Exit MPSM to commands not requiring a locked DLL	tXMP	txs(imin)		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	
Calibration Timing				
Power-up and RESET calibration time	tZQinit	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	nCK
Reset/Self Refresh Timing				

Exit Reset from CKE HIGH to a valid command	command tXPR	max (5nCK,tRFC(min)+ 10ns)	-	
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+1 0ns	-	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+ 10ns	-	
Exit Self Refresh to commands re-quiring a locked DLL	tXSDLL	tDLLK(min)	-	
Minimum CKE low width for Self re-fresh entry to exit timing	tCKESR	tCKE(min)+1 nCK	-	
Minimum CKE low width for Self re-fresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+ 1nCK+PL	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down Entry (PDE)	tCKSRE	max(5nCK,10 ns)	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down when CA Parity is enabled	tCKS-RE_PAR	max (5nCK,10ns) +PL	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10 ns)	-	
Power Down Timing				
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	(4nCK,6ns)	-	

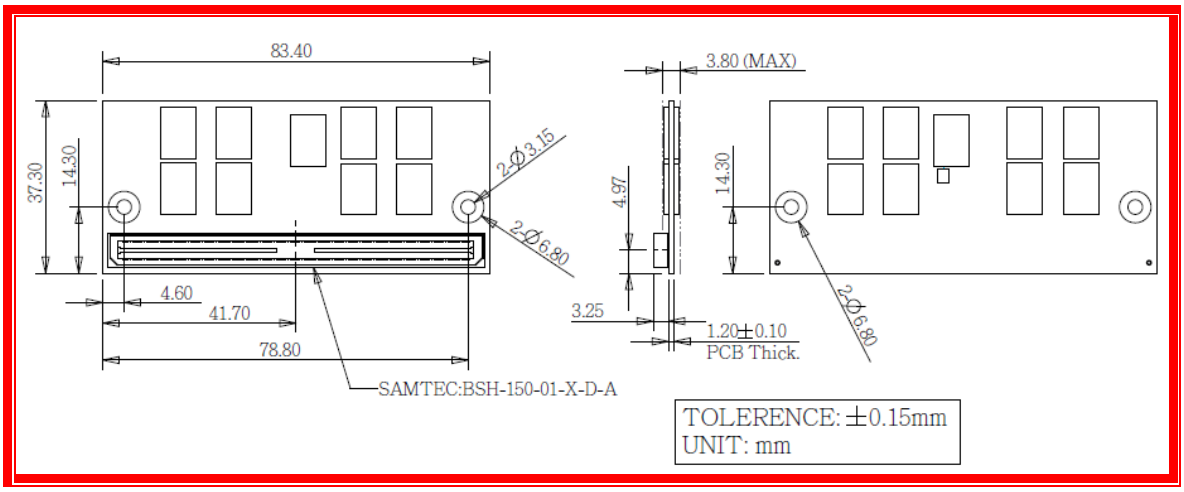
CKE minimum pulse width	tCKE	max (3nCK, 5ns)	-	
Command pass disable delay	tCPDED	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
PDA Timing				
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		
Mode Register Set command up-date delay in PDA mode	tMOD_PDA	tMOD		
ODT Timing				
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL	tAOFAS	1.0	9.0	ns

frozen)				
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS_t/DQS_n rising edge af-ter write leveling mode is pro-grammed	tWLMRD	40	-	nCK
DQS_t/DQS_n delay after write lev-eling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK_t, CK_c crossing to rising DQS_t/DQS_n crossing	tWLS	0.13	-	tCK(avg)
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE			ns
CA Parity Timing				
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	
Delay from errant command to ALERT_n assertion	tPAR_ALER T_ON	-	PL+6ns	
Pulse width of ALERT_n signal when asserted	tPAR_ALER T_PW	72	144	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER T_RSP	-	64	nCK
Parity Latency	PL	5		nCK
CRC Error Reporting				
CRC error to ALERT_n latency	tCRC_ALER T	3	13	ns
CRC ALERT_n pulse width	CRC_ALER T_PW	6	10	nCK
tREFI				
tRFC1 (min)	2Gb	160	-	ns

	4Gb	260	-	ns
	8Gb	350	-	ns
	16Gb	550	-	ns
tRFC2 (min)	2Gb	110	-	ns
	4Gb	160	-	ns
	8Gb	260	-	ns
	16Gb	350	-	ns
tRFC3 (min)	2Gb	90	-	ns
	4Gb	110	-	ns
	8Gb	160	-	ns
	16Gb	260	-	ns

10. PACKAGE DIMENSION

- (16GB, 2 Rank 1Gx8 DDR4 base XRDIMM)



Note: All dimensions are in millimeters and should be kept within a tolerance of ±0.15, unless otherwise specified.

11. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

三、 本公司聲明我們的產品符合 RoHS 指令的附件中(7a)、(7c-I)允許豁免。
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.
※ (7a) Lead in high melting temperature type solders(i.e. lead-based alloys containing 85% by weight or more lead).
※ (7C-I) Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
鉛（Pb）	< 1000 ppm
汞（Hg）	< 1000 ppm
鎘（Cd）	< 100 ppm
六價鉻（Cr 6+）	< 1000 ppm
多溴聯苯（PBBs）	< 1000 ppm
多溴二苯醚（PBDEs）	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯（DEHP）	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯（BBP）	< 1000 ppm
鄰苯二甲酸二丁酯（DBP）	< 1000 ppm
鄰苯二甲酸二異丁酯（DIBP）	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2018 / 07 / 01

12. REACH Declaration

宜鼎國際股份有限公司

Innodisk Corporation

REACH Declaration

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

We hereby confirm that the product(s) delivered to

Innodisk P/N	Description
All Innodisk DRAM Products	DDR Series

☐ contain(s) **no** hazardous substances or constituents exceeding the defined threshold 0.1 % by weight in homogenous material if not otherwise specified, as described in the candidate list table currently including 201 substances and shown on the ECHA website (http://echa.europa.eu/de/candidate-list-table).

☑ contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in homogenous material if not otherwise specified in candidate list table. Where the threshold value is exceeded, the substances in question are to be declared in accompanying Appendix A .

☑ Comply with REACH Annex XVII.

Guarantor

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2019 / 07 / 24

Revision Log

Rev	Date	Modification
0.1	14th May 2020	Preliminary Edition
1.0	14th May 2020	Official Released