innodisk

Total Solution For Industrial Flash Storage

nanoSSD

PCIe 3TE7 Series

Customer: _____

Customer Part Number: _____

Innodisk Part Number: _____

Innodisk Model Name: _____

Date: _____

Innodisk Approver	Customer Approver

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REVISION HISTORY

Revision	Description	Date
Rev. 1.0	First Released	Sep., 2020
Rev. 1.1	Update MSL Declaration	Oct., 2020
Rev. 1.2	Update 512GB	Nov., 2020
Rev. 1.3	Remove AES and TCG Opal support	Jun., 2021
Rev. 1.4	Updates: - pin layout drawing - pin assignment for Y19 - device parameters (user capacity) - mechanical dimensions 32GB-256GB, 512GB and bottom view - RoHS and REACH declaration	Jul., 2021
Rev. 1.5	Updates: -performance -feature list -storage temperature -power consumption Remove: RoHS, REACH and MSL	Jul., 2021
Rev 1.6	Update nanoSSD PCIe 3TE7 pin assignment for C10, D10, and C6 Update block diagram	Mar., 2022
Rev 1.7	Update mechanical drawing and PN rule table	Apr., 2022

Features:

- PCIe Gen.3 x 2
- Industrial 3D TLC 64-layer NAND
- Standard & Wide-temperature
- Dynamic Thermal Management
- Hybrid Write

Power Requirements:

Input Voltage	3.3V±5%
Max Operating Wattage	1.6W
Idle Wattage	0.4W

Performance:

- Sequential Read up to 1,650 MB/s
- Sequential Write up to 1,350 MB/s

Reliability:

Capacity	[Client] TBW	[Client] DWPD
32GB	19	0.81
64GB	38	0.81
128GB	76	0.81
256GB	152	0.81
512GB	304	0.81

Data Retention	Years
Warranty	2 Years*

*2years duration after 100% (3000) P/E cycles at 55℃

For warranty details, please refer to:

https://www.innodisk.com/en/support_and_service/warranty

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1. Product Overview

1.1 Introduction of Innodisk nanoSSD PCIe 3TE7

InnoDisk nanoSSD PCIe 3TE7 is an NVM Express storage device designed as the standard 11.5*13.0 mm2 ball grid array (BGA) package form factor with PCIe interface. The nanoSSD supports PCIe Gen III x2 within a tiny dimension, and it is compliant with NVM 1.3 providing excellent performance. Moreover, it adopts industrial 3D TLC NAND Flash providing high endurance and reliability, as well as low power consumption and high reliability. It offers an ideal solution for embedded, automotive, medical, gaming and most industrial applications.

CAUTION TRIM must be enabled.

TRIM enables SSD's controller to skip invalid data instead of moving. It can free up significant amount of resources, extends the lifespan of SSD by reducing erase, and write cycles on the SSD. Innodisk's handling of garbage collection along with TRIM command improves write performance on SSDs.

1.2 Product View and Models

Innodisk nanoSSD PCIe 3TE7 is available in follow capacities:

nanoSSD PCIe 3TE7 32GB nanoSSD PCIe 3TE7 64GB

nanoSSD PCIe 3TE7 128GB nanoSSD PCIe 3TE7 256GB

nanoSSD PCIe 3TE7 512GB

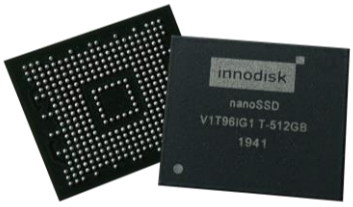


Figure 1: Innodisk nanoSSD PCIe 3TE7

2. Product Specifications

2.1 Capacity and Device Parameters

nanoSSD PCIe 3TE7 device parameters are shown in Table 1.

Table 1: Device parameters

Capacity	LBA	User Capacity (MB)
32GB	62533296	30533
64GB	125045424	61057
128GB	250069680	122104
256GB	500118192	244198
512GB	1000215216	488386

2.2 Performance

Burst Transfer Rate: 6.0Gbps

Table 2: Performance

Capacity	32GB	64GB	128GB	256GB	512GB
Sequential Read (Max)	300 MB/s	600 MB/s	1,150 MB/s	1,600 MB/s	1,650 MB/s
Sequential Write (Max)	130 MB/s	280 MB/s	550 MB/s	1,100 MB/s	1,350 MB/s
4KB Random Read (QD32)	26,000	52,000	101,700	155,000	157,000
4KB Random Write (QD32)	30,000	64,000	126,000	132,000	136,000

Note: * Performance is based on CrystalDiskMark 6.0.2 with file size 1000MB of Queue Depth 32

2.3 Electrical Specifications

2.3.1 Power Requirement

Table 3: Innodisk nanoSSD PCIe 3TE7 Power Requirement

Item	Symbol	Rating	Unit
Input voltage	V_{IN}	+3.3 DC +- 5%	V

2.3.2 Power Consumption

Table 4: Power Consumption

Voltage Rail	Rating	Power Consumption (W)
Main power supply	3.3 V ±5%	1.6
Flash IO supply	1.8 V ±5%	0.3
Controller core supply	1.2 V ±5%	0.6

* Target: nanoSSD PCIe 3TE7 512GB

2.4 Environmental Specifications

2.4.1 Temperature Ranges

Table 5: Temperature Range for nanoSSD PCIe 3TE7

Temperature	Range
Operating	Standard Grade: 0°C to +70°C Industrial Grade: -40°C to +85°C
Storage	-40°C to +85°C

Below are some recommendations for PCB design to lowest effect of thermal.

- Maximize copper thickness and trace width for all pins to thermal features such as thermal vias, thermal side rails, and thermal conduction screw holes.
- Copper ground/supply planes in the PCB can provide very effective heat dissipation for the IC package. To maximize effectiveness, thermal vias should be added to connect the package's mechanical ground balls to the ground plane. There should be at least one thermal via allocated for each MGB of the package. The plating thickness of vias should be maximized to optimize thermal conduction.

2.4.2 Humidity

Relative Humidity: 10-95%, non-condensing

2.4.3 Shock and Vibration

Table 6: Shock/Vibration Testing for nanoSSD PCIe 3TE7

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2K Hz, 20G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 0.5ms, 1500 G, 3 axes	IEC 68-2-27

2.4.4 Mean Time between Failures (MTBF)

Table 7 summarizes the MTBF prediction results for various nanoSSD PCIe 3TE7 configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 7: nanoSSD PCIe 3TE7 MTBF

Product	Condition	MTBF (Hours)
Innodisk nanoSSD PCIE 3TE7	Telcordia SR-332 GB, 25°C	>3,000,000

2.5 RoHS Compliance

nanoSSD PCIE 3TE7 is fully compliant with RoHS directive.

2.6 Reliability

Parameter	Value
Read Cycles	Unlimited Read Cycles
Flash endurance	3,000 P/E cycles
Wear-Leveling Algorithm	Support
Bad Blocks Management	Support
DIE RAID Recovery	Support
Error Correct Code	Support
TBW* (Total Bytes Written)	
Capacity	**Client workload**
32GB	18.75
64GB	37.5
128GB	75
256GB	150
512GB	300

* Note:

Client: Follow JESD218 Test method and JESD219A Workload, tested by ULINK. (The capacity lower than 64GB client workload is not specified in JEDEC219A, the values are estimated.)

2.7 Transfer Mode

nanoSSD PCIe 3TE7 supports following transfer modes:

PCIe Gen III 8Gbps

PCIe Gen II 4Gbps

PCIe Gen I 2Gbps

2.8 Ball and Signal Description

The following table provides the pin definition of nanoSSD PCIe 3TE7 345-balls.

"P" and "N" in differential signals, e.g. PTXP1 and PTXN1, mean positive-end signal and negative-end signal.

In signal names with "#", e.g. PCLKREQ#, PRESET#, RESET# and JT_TRST#, the "#" means "active low".

Table 8: Innodisk nanoSSD PCIe 3TE7 Pin Assignment

Signal Name	Ball Number	Pin Type *		Description
PCIE_REFCLKP	AA4	I	PCIe interface	PCIe Reference Clock P
PCIE_REFCLKN	AA5	I		PCIe Reference Clock N
PTXP1	AA16	O		PCIe Lane 1 Transmitter Differential Signal P
PTXN1	AA17	O		PCIe Lane 1 Transmitter Differential Signal N
PRXP1	Y13	I		PCIe Lane 1 Receiver Differential Signal P
PRXN1	Y14	I		PCIe Lane 1 Receiver Differential Signal N
PTXP0	Y10	O		PCIe Lane 0 Transmitter Differential Signal P
PTXN0	Y11	O		PCIe Lane 0 Transmitter Differential Signal N
PRXP0	Y7	I		PCIe Lane 0 Receiver Differential Signal P
PRXN0	Y8	I		PCIe Lane 0 Receiver Differential Signal N
PCLKREQ#	W3	I/O		PCIe Clock Request, Active Low
PRESET#	W4	I		PCIe Interface Hardware Reset, Active Low
XTAL_OUT	W18	O	Crystal	Crystal Output
XTAL_IN	W19	I		Crystal Input
RZQ_1	L2	N/A	ZQ	Memory or NAND calibration resistor
RZQ_2	L19	N/A		Memory or NAND calibration resistor
RESET#	B4	I	Reset	Power-on Reset, Active Low
TEST_MODE	D5	I	Test	ATE Test Mode Select
TP	B5	O		Analog Test Output

Signal Name	Ball Number	Pin Type *		Description
GP0	D4	I/O	Debug GPIO (1.8V)	General Purpose Input and Output 0
GP1	C4	I/O		General Purpose Input and Output 1
GP2	C5	I/O		General Purpose Input and Output 2
GP3	C12	I/O		General Purpose Input and Output 3
GP4/LED_1#	Y2	I/O		General Purpose Input and Output 4 / Signal output to drive an external transistor to provide status indication via LED device (Output, Active Low)
SDA/SMB_DATA	C11	I/O	I2C/SMBus (1.8V)	I2C Data / SMBus Data - Open Drain
SCL/SMB_CLK	D11	I/O		I2C Clock / SMBus Clock - Open Drain
UTX/UAO	C13	O	UART (1.8V)	UART Transmitter / UART Output
URX/UAI	D12	I		UART Receiver / UART Input
JT_TMS	C14	I	JTAG (1.8V)	JTAG Mode Select
JT_TDI	C15	I		JTAG Data Input
JT_TRST#	D13	I		JTAG Reset, Active Low
JT_TDO	D14	O		JTAG Data Output
JT_TCK	D15	I		JTAG Clock
VCC	H2, H3, H18, H19, J2, J3, J18, J19, K3, K18	Power (3.3V)		External Power Supply
VCCQ	D2, D3, D18, D19, E2, E3, E18, E19, F2, F3,F18, F19, T3, U3	Power (1.2/1.8V)		External Power Supply
VDDI	M3, M18, N2, N3, N18,N19, P2, P3, P18,	Power (1.2V)		Power Supply for internal LDO

	P19		
VDD	B6	Power (0.9V)	LDO Output - Core Power
1V8	T2, T18, T19, U2, U18,U19	Power (1.8V)	Power for PCIe/PLL/Digital Input and Output, Power Supplier Used by ATE

Signal Name	Ball Number	Pin Type *	Description
GND	A1, A2, A3, A6, A9, A12, A15, A18, A19, A20, AA1, AA2, AA3, AA6, AA9, AA12, AA15, AA18, AA19, AA20, AB1, AB2, AB3, AB6, AB9, AB12, AB15, AB18, AB19, AB20, B1, B2, B3, B9, B12, B15, B19, B20, C1, C2, C3, C18, C19, C20, E1, E4, E17, E20, F4, F17, G2, G3, G4, G18, G19, H1, H17, H20, J4, K2, K17, K19, L1, L3, L4, L18, L20, M1, M2, M17, M19, M20, N4, P17, R1, R2, R3, R4, R18, R19, R20, T17, U4, U17, V1, V2, V3, V4, V17, V18, V19, V20, W5, W6, W7, W8, W9, W10, W11, W12, W13, W14, W15, Y1, Y3, Y4, Y5, Y6, Y9, Y12, Y15, Y16, Y17, Y18, Y20	Ground	Ground
HSB	E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, E15, E16, F5, F6, F7, F8, F9, F10, F11, F12, F13, F14, F15, F16, G5, G6, G7, G8, G9, G10, G11, G12, G13, G14, G15, G16, G17, H4, H5, H6, H7, H15, H16, J5, J6, J8, J9, J10, J11, J12, J13, J15, J16, J17, K4, K5, K6, K8, K13, K15, K16, L5, L6, L8, L13, L15, L16, L17, M4, M5, M6, M8, M13, M15, M16, N5, N6, N8, N13, N15, N16, N17, P4, P5, P6, P8, P9, P10, P11, P12, P13, P15, P16, R5, R6, R15, R16, R17, T4, T5, T6, T7, T8, T9, T10, T11, T12, T13, T14, T15, T16, U5, U6, U7, U8, U9, U10, U11, U12, U13, U14, U15, U16, V5, V6, V7, V8, V9, V10, V11, V12, V13, V14, V15, V16	NC	Host specific balls
RFU	C7, C8, C9, D6, D7, D8, D9, D16, W16	NC	Reserved for future use
NC	B16, B17, B18, C6, C10, C16, C17, D10, D17, W2, W17, Y19	NC	Not Connect

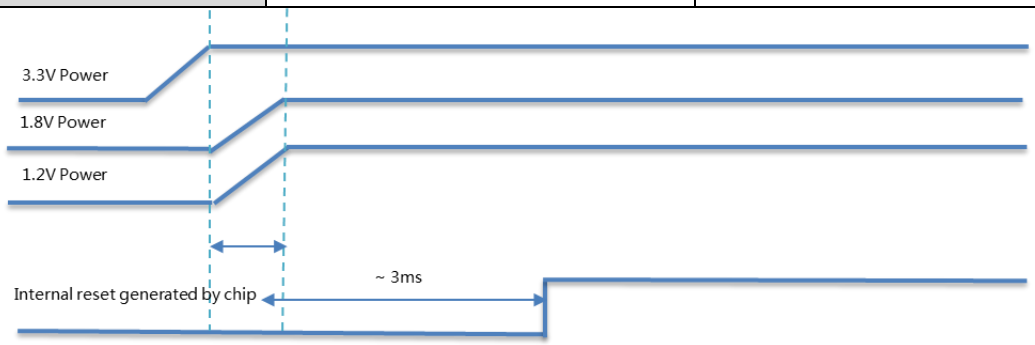
*Note: I - Input Only, O - Output Only, I/O - Input and Output

Figure 2: Innodisk nanoSSD PCIe 3TE7 Pin Layout

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	
A	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND	A
B	GND	GND	GND	RESET#	TP	VDD			GND			GND			GND	NC	NC	NC	GND	GND	B
C	GND	GND	GND	GP1	GP2	GP9	RFU	RFU	RFU	GP7/PLN#	SDA/SMB_DATA	GP3	UTX/UAO	JT_TMS	JT_TDI	NC	NC	GND	GND	GND	C
D		VCCQ	VCCQ	GP0	TEST_MODE	RFU	RFU	RFU	RFU	GP8/PLA#	SCL/SMB_CLK	URX/UAI	JT_TRST#	JT_TDO	JT_TCK	RFU	NC	VCCQ	VCCQ		D
E	GND	VCCQ	VCCQ	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	VCCQ	VCCQ	GND	E
F		VCCQ	VCCQ	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	VCCQ	VCCQ		F
G		GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND		G
H	GND	VCC	VCC	HSB	HSB	HSB	HSB								HSB	HSB	GND	VCC	VCC	GND	H
J		VCC	VCC	GND	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	HSB	VCC	VCC		J
K		GND	VCC	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	VCC	GND		K
L	GND	RZQ_1	GND	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	GND	RZQ_2	GND	L
M	GND	GND	VDDI	HSB	HSB	HSB		HSB					HSB		HSB	HSB	GND	VDDI	GND	GND	M
N		VDDI	VDDI	GND	HSB	HSB		HSB					HSB		HSB	HSB	HSB	VDDI	VDDI		N
P		VDDI	VDDI	HSB	HSB	HSB		HSB	HSB	HSB	HSB	HSB	HSB		HSB	HSB	GND	VDDI	VDDI		P
R	GND	GND	GND	GND	HSB	HSB									HSB	HSB	HSB	GND	GND	GND	R
T		1V8	VCCQ	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	1V8	1V8		T
U		1V8	VCCQ	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	1V8	1V8		U
V	GND	GND	GND	GND	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	HSB	GND	GND	GND	GND	V
W		NC	PCLKREQ#	PRESET#	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	RFU	NC	XTAL_OUT	XTAL_IN		W
Y	GND	GP4/LED_1#	GND	GND	GND	GND	PRXP0	PRXN0	GND	PTXP0	PTXN0	GND	PRXP1	PRXN1	GND	GND	GND	GND	NC	GND	Y
AA	GND	GND	GND	PCIE_REFCLKP	PCIE_REFCLKN	GND			GND			GND			GND	PTXP1	PTXN1	GND	GND	GND	AA
AB	GND	GND	GND			GND			GND			GND			GND			GND	GND	GND	AB
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	

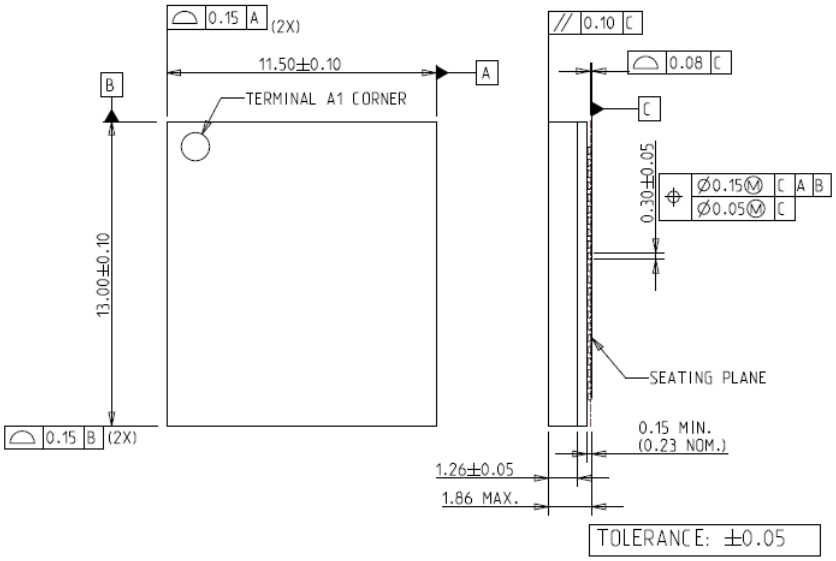
2.9 Power Supply & Sequence

	Voltage Rail	Specification
Input voltage	VCC	3.3V± 10%
	VCCQ	1.8V ± 5%
	VDDI	1.2V ± 5%

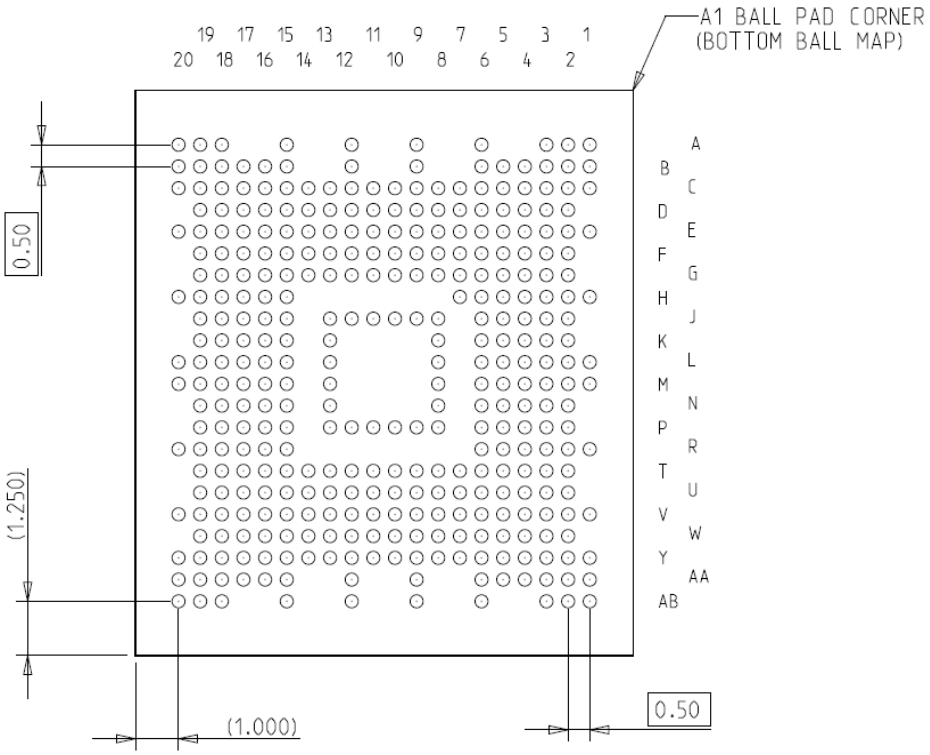


- 3.3V ramp up no later than 1.8V and 1.2V
- 1.8V needs to be ramp up no later than 1.2V
- 1.2V ram up time should be < 2ms

2.10 Mechanical Dimensions



Bottom View (345-ball)



2.11 Seek Time

Innodisk nanoSSD PCIe 3TE7 is not a magnetic rotating design. There is no seek or rotational latency required.

2.12 NAND Flash Memory

Innodisk nanoSSD PCIe 3TE7 uses 3D TLC NAND flash memory, with 3,000 program & erase cycles, which is non-volatility, high reliability and high-speed memory storage.

3. Theory of Operation

3.1 Overview

Figure 2 shows the operation of Innodisk nanoSSD PCIe 3TE7 from the system level, including the major hardware blocks.

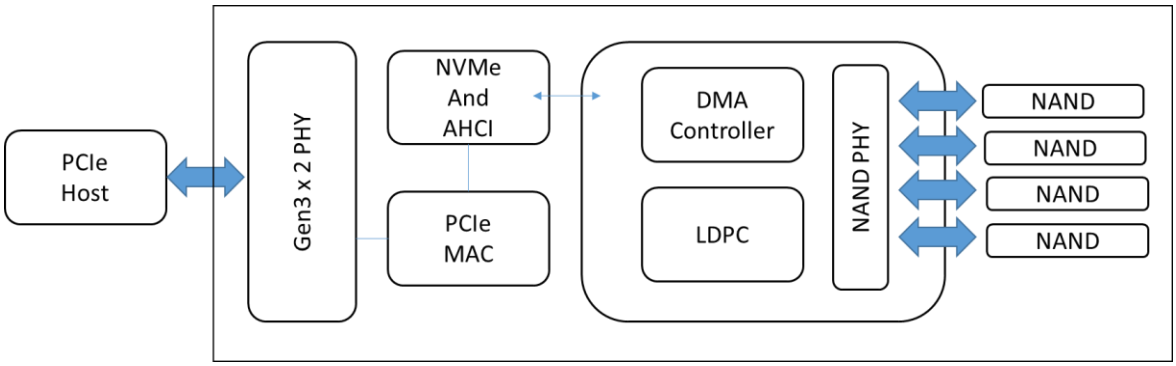


Figure 3: Innodisk nanoSSD PCIe 3TE7 Block Diagram

Innodisk nanoSSD PCIe 3TE7 integrates a PCIe Gen 3x2 controller and NAND flash memories. When connected with a host, the nanoSSD uses the integrated controller with four NAND channels x 4 native CE and PCIe Gen3 x2 interface to manage the embedded NAND flash array consisting of either 1/2/4/8/16 NAND dies

3.2 Error Detection and Correction

Innodisk nanoSSD PCIe 3TE7 is designed with hardware LDPC ECC engine with hard-decision and Soft-decision decoding. Low-density parity-check (LDPC) codes have excellent error correcting performance close to the Shannon limit when decoded with the belief-propagation (BP) algorithm using soft-decision information.

3.3 Wear-Leveling

Flash memory can be erased within a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

Innodisk nanoSSD PCIe 3TE7 uses a static wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page/block in the flash. This spreads flash media usage evenly across all pages, thereby extending flash lifetime.

3.4 Bad Blocks Management

Bad Blocks are blocks that contain one or more invalid bits whose reliability are not guaranteed. The Bad Blocks may be presented while the SSD is shipped, or may develop during the life time of the SSD. When the Bad Blocks is detected, it will be flagged, and not be used anymore. The SSD implement Bad Blocks management, Bad Blocks replacement, Error Correct Code to avoid data error occurred. The functions will be enabled automatically to transfer data from Bad Blocks to spare blocks, and correct error bit.

3.5 Power Cycling

Innodisk's power cycling management is a comprehensive data protection mechanism that functions before and after a sudden power outage to SSD. Low-power detection terminates data writing before an abnormal power-off, while table-remapping after power-on deletes corrupt data and maintains data integrity. Innodisk's power cycling provides effective power cycling management, preventing data stored in flash from degrading with use.

3.6 Garbage Collection

Garbage collection technology is used to maintain data consistency and perform continual data cleansing on SSDs. It runs as a background process, freeing up valuable controller resources while sorting good data into available blocks, and deleting bad blocks. It also significantly reduces write operations to the drive, thereby increasing the SSD's speed and lifespan.

3.7 TRIM

The TRIM command is designed to enable the operating system to notify the SSD which pages no longer contain valid data due to erases either by the user or operating system itself. During a delete operation, the OS will mark the sectors as free for new data and send a TRIM command to the SSD to mark them as not containing valid data. After that the SSD knows not to preserve the contents of the block when writing a page, resulting in less write amplification with fewer writes to the flash, higher write speed, and increased drive life.

3.8 Power Management

- Support multi-level power states: PS0, PS1, PS2, PS3, PS4
- Support thermal throttling with configurable temperature threshold.

4. Installation Requirements

4.1 Reference Design

A reference design using the nanoSSD has been provided here to help with the integration. All peripheral circuits are included in the design and meet specifications laid out in the earlier sections of this document. We recommend this circuit design to match the reference design as closely as possible. Please refer to attachments for reference design.

4.2 Production Guide

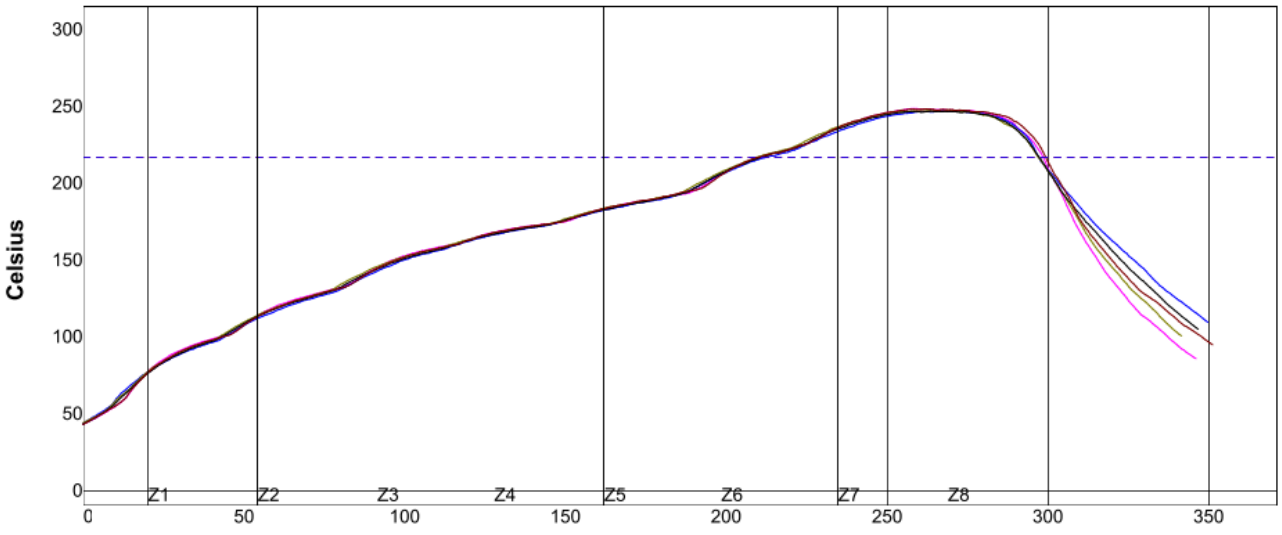
4.2.1 Preheat

Before printed circuit board assembly, a process of preheat is requested.

Preheat condition: 16 HRs with 125°C

4.2.2 Reflow Profile

Setpoints (Celsius)								
Zone	1	2	3	4	5	6	7	8
Top	100	130	165	170	180	230	255	245
Bottom	100	130	165	170	180	230	255	245
Conveyor Speed (cm/min):	65.0							



PWI= 97%	ax Rising Slo		ax Falling Slo		reheat	30-110	ak Time 110-15		flow Time /21		Peak Temp		lope1 (30-110		ope2 (217-255		Time 150-217	
2	1.84	49%	-3.85	-90%	50.97	27%	44.64	-2%	88.53	95%	248.81	38%	1.84	68%	0.91	-73%	113.84	79%
3	1.67	25%	-2.70	-13%	52.28	31%	47.50	17%	84.64	82%	247.17	22%	1.67	52%	0.85	-80%	112.70	76%
4	1.74	34%	-3.28	-52%	50.93	27%	46.26	8%	87.52	92%	247.40	24%	1.74	58%	0.87	-77%	112.90	76%
5	1.73	32%	-2.83	-22%	50.55	26%	47.44	16%	86.53	88%	246.95	20%	1.73	57%	0.86	-79%	112.13	74%
6	1.77	39%	-3.44	-63%	51.04	28%	45.85	6%	89.09	97%	248.43	34%	1.77	61%	0.91	-72%	112.75	76%
Delta	0.17		1.15		1.73		2.86		4.45		1.86		0.17		0.06		1.71	

Process Window:

Solder Paste: System Default for Reflow

Statistic Name	Low Limit	High Limit	Units
Max Rising Slope (Target=1.5)	0.7	2.2	Degrees/Second
(Calculate Slope over 20 Seconds)			
Slope1 (Target=1.1)			
Between 30.0 and 110.0	0	2.2	Degrees/Second
(Calculate Slope over 20 Seconds)			
Slope2 (Target=1.5)			
Between 217.0 and 255.0	0.7	2.2	Degrees/Second
(Calculate Slope over 20 Seconds)			
Max Falling Slope	-4	-1	Degrees/Second
(Calculate Slope over 20 Seconds)			
Preheat Time 30-110C	0	80	Seconds
Soak Time 110-150C	30	60	Seconds
Soak Time 150-217C-(2)	60	120	Seconds
Time Above Reflow - 217C	30	90	Seconds
Peak Temperature	235	255	Degrees Celsius

5. Part Number Rule

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
	D	**E**	**N**	**S**	**D**	**-**	**C**	**1**	**2**	**I**	**G**	**1**	**E**	**W**	**A**	**Q**	**H**	**-**	**X**	**X**
Description	Disk	nanoSSD PCIe 3TE7					Capacity			Category			Flash Mode	Operation Temp.	Internal Control	CH.	Flash	-	Customized Code	

Definition	
Code 1st (Disk)	**Code 13th (Flash mode)**
D : Disk	E: 64 layers 3D flash
Code 2nd	**Code 14th (Operation Temperature)**
E: Embedded	C: Standard Grade (0℃~ +70℃)
	W: Industrial Grade (-40℃~ +85℃)
Code 3rd ~ 5th (Form Factor)	**Code 15th (Internal control)**
NSD:nanoSSD	A~Z: BGA version
Code 7th ~9th (Capacity)	**Code 16th (Channel of data transfer)**
32G: 32GB	S: Single Channel
64G: 64GB	D: Dual Channels
B56: 256GB	Q: Quad Channels
C12: 512GB	
Code 10th ~12th (Series)	**Code 17th (Flash Type)**
IG1: nanoSSD PCIe 3TE7 Controller	H: Industrial 64 Layers 3D TLC
	Code 19th~20th (Customized Code)