DFI

WL9A3

COM Express Mini Module
User's Manual

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Changes after the publication's first release will be based on the product's revision. The website will always provide the most updated information.

Trademarks

Product names or trademarks appearing in this manual are for identification purpose only and are the properties of the respective owners.

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules.

These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation.

This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications.

However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

1. The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
2. Shielded interface cables must be used in order to comply with the emission limits.

Table of Contents

About this Manual

This manual can be downloaded from the website.

The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products.

Please visit our website or contact our sales representatives for the latest editions.

Warranty

1. Warranty does not cover damages or failures that arised from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
2. The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
3. Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
4. We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

1. To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
2. Wear an antistatic wrist strap.
3. Do all preparation work on a static-free surface.
4. Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
5. Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

Important:
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

- To avoid damage to the system, use the correct AC input voltage range.
- To reduce the risk of electric shock, unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- One WL9A3 board
- CPU Cooler / Heatsink (only for certain SKUs)

Optional Items

- COM100-B carrier board kit
- Heat spreader

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

When installing the system board in a new system, you will need at least the following internal components.

- Carrier Board
- Storage device such as hard disk drive, CD-ROM, etc.
- Power adaptor

External system peripherals may also be required for navigation and display, including at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

Specifications

SYSTEM	Processor	8th Gen Intel® Core™ Processor, FCBGA1528 - i7-8665UE Processor, Quad Core, 8M Cache, 1.7GHz (4.4GHz), 15W - i5-8365UE Processor, Quad Core, 6M Cache, 1.6GHz (4.1GHz), 15W - i3-8145UE Processor, Dual Core, 4M Cache, 2.1GHz (3.9GHz), 15W
	Memory	8GB/16GB Memory Down Dual Channel LPDDR3 2133MHz
	BIOS	SPI 128Mbit (default supports FTPM)
GRAPHICS	Controller	Intel® UHD Graphics 620
	Feature	OpenGL 5.0, DirectX 12, OpenCL 2.1 HW Decode: AVC/H.264, MPEG2, VC1, WMV9, JPEG/MJPEG, HEVC/H.265, VP8, VP9, MVC HW Encode: AVC/H.264, JPEG/MJPEG, HEVC/H.265, VP8, VP9, MVC
	Display	1 x DDI (HDMI/DP++) 1 x LVDS/eDP LVDS: single channel 24-bit, resolution up to 1366x768 @ 60Hz HDMI: resolution up to 4096x2160 @ 30 Hz DP++: resolution up to 4096x2304 @ 60Hz eDP: resolution up to 4096x2304 @ 60Hz
	Dual Display	DDI + LVDS DDI + eDP
EXPANSION	Interface	4 x PCIe x1 (Gen 3) 1 x SDIO 1 x LPC 2 x I2C 1 x SMBus 1 x SPI 2 x UART (TX/RX)
AUDIO	Interface	HD Audio
ETHERNET	Controller	1 x Intel® I219 (10/100/1000Mbps)
I/O	USB	2 x USB 3.0 8 x USB 2.0
	SATA	2 x SATA 3.0 (up to 6Gb/s)
	GPIO	1 x 8-bit GPIO

WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds
POWER	Type	12V~20V, 5VSB, VCC_RTC (ATX mode) 12V~20V, VCC_RTC (AT mode)
OS SUPPORT (UEFI ONLY)		Windows 10 IoT Enterprise 64-bit Linux
ENVIRONMENT	Temperature	Operating: 0 to 60°C / -30 to 85°C Storage: -40 to 85°C
	Humidity	Operating: 5 to 90% RH Storage: 5 to 90% RH
MECHANICAL	Dimensions	COM Express® Mini: 84mm (3.30") x 55mm (2.16")
	Compliance	PICMG COM Express® R3.0, Type 10

▶ Specification Comparison

The table below lists the base specifications of COM Express Module Revision 3.0, Type 10 (Single Connector), and the corresponding specifications supported by the WL9A3 module.

		COM Express Min / Max	DFI WL9A3
	System I/O		
	PCI Express Lanes 0 - 5	1 / 4	4
	LVDS Channel A	0 / 1	1
	LVDS Channel B	NA	NA
	eDP on LVDS CH A pins	0 / 1	1(option)
	VGA Port	NA	NA
	TV-Out	NA	NA
	DDI 0	0 / 1	1
Note1	Serial Ports 1 - 2	0 / 2	2
	CAN interface on SER1	0 / 1	1
	SATA / SAS Ports	1 / 2	2
	AC'97 / HDA Digital Interface	0 / 1	1
	USB 2.0 Ports	4 / 8	8
	USB Client	0 / 1	0
	USB 3.0 Ports	0 / 2	2
	LAN Port 0	1 / 1	1
	Express Card Support	NA	NA
	LPC Bus	1 / 1	1
	SPI	1 / 2	1
	System Management		
Note2	SDIO (muxed on GPIO) General Purpose I/O	0 / 1 8 / 8	1(option) 8
	SMBus	1 / 1	1
	I2C	1 / 1	1
	Watchdog Timer	0 / 1	1
	Speaker Out	1 / 1	1
	External BIOS ROM Support	0 / 2	1
	Reset Functions	1 / 1	1
	Power Management		
	Thermal Protection	0 / 1	1
	Battery Low Alarm	0 / 1	1
	Suspend/Wake Signals	0 / 3	3
	Power Button Support	1 / 1	1
	Power Good	1 / 1	1
	VCC_5V_SBY Contacts	4 / 4	4
	Sleep Input	0 / 1	1
	Lid Input	0 / 1	1
	Fan Control Signals	0 / 2	2
	Trusted Platform Modules	0 / 1	0
	Power		
	VCC_12V Contacts	12 / 12	12

Note:
1. It indicates 12V-tolerant features on former VCC_12V signals.
2. The two indicate an approximation of features sharing connector pins.

▶ Features

Watchdog Timer

The Watchdog Timer function allows your application to regularly "clear" the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

LPDDR3

Low-Power Double Data Rate (LPDDR) is a form of RAM that targets less power consumption. LPDDR3 achieves a data rate of 1600 MT/s.

Graphics

The integrated Intel® UHD 620 graphics engine delivers an excellent blend of graphics performance and features to meet business needs. It provides excellent video and 3D graphics with outstanding graphics responsiveness. These enhancements deliver the performance and compatibility needed for today's and tomorrow's business applications. Supports VGA, LVDS, eDP and DDI display outputs.

Serial ATA

The system supports multiple SATA 3.0 (up to 6Gb/s) ports and allows for different configurations of RAID levels to meet various requirements for data redundancy and performance.

Gigabit LAN

The Intel® I219 Gigabit LAN controller features up to 1Gbps data transmission with support for Intel® Active Management Technology. It provides remote maintenance and manageability for networked computing assets in an enterprise environment.

Wake-On-LAN

This feature allows the network to remotely wake up a Soft Power Down (Soft-Off) PC. It is supported via the onboard LAN port or via a PCI LAN card that uses the PCI PME (Power Management Event) signal. However, if your system is in the Suspend mode, you can power-on the system only through an IRQ or DMA interrupt.

USB

The system board supports the new USB 3.0. It is capable of running at a maximum transmission speed of up to 5 Gbit/s (625 MB/s) and is faster than USB 2.0 (480 Mbit/s, or 60 MB/s) and USB 1.1 (12Mb/s). USB 3.0 reduces the time required for data transmission, reduces power consumption, and is backward compatible with USB 2.0. It is a marked improvement in device transfer speeds between your computer and a wide range of simultaneously accessible external Plug and Play peripherals.

ACPI STR

The system board is designed to meet the ACPI (Advanced Configuration and Power Interface) specification. ACPI has energy saving features that enables PCs to implement Power Management and Plug-and-Play with operating systems that support OS Direct Power Management. ACPI when enabled in the Power Management Setup will allow you to use the Suspend to RAM function.

With the Suspend to RAM function enabled, you can power-off the system at once by pressing the power button or selecting "Standby" when you shut down Windows® without having to go through the sometimes tiresome process of closing files, applications and operating system.

This is because the system is capable of storing all programs and data files during the entire operating session into RAM (Random Access Memory) when it powers-off. The operating session will resume exactly where you left off the next time you power-on the system.

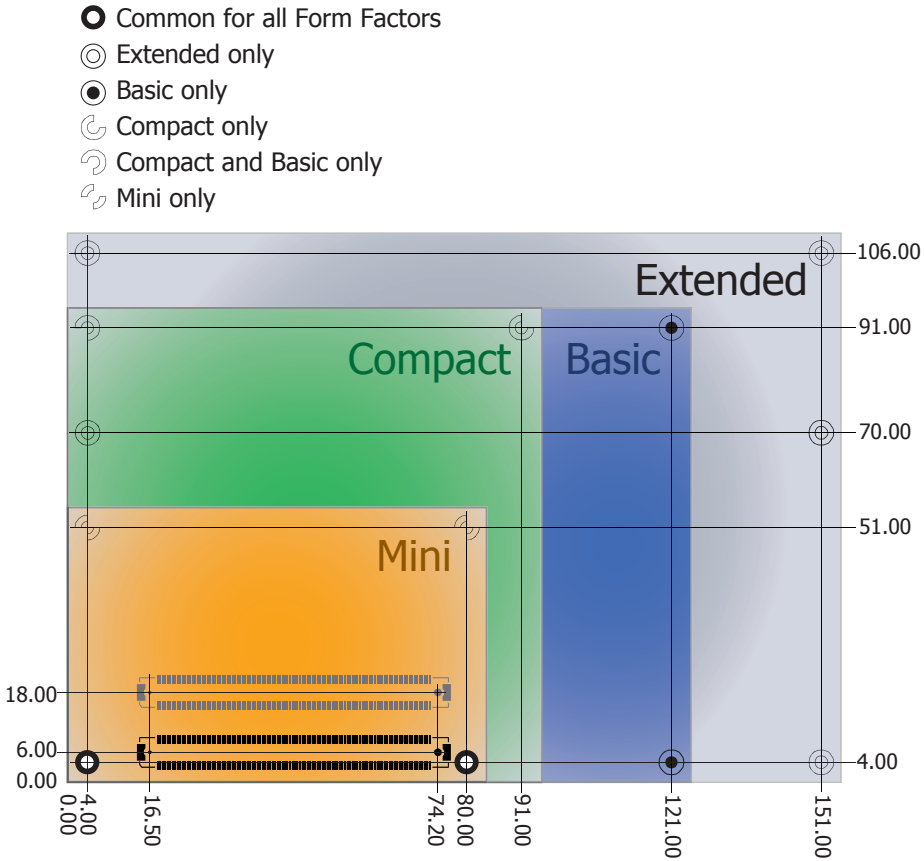
Power Failure Recovery

When power returns after an AC power failure, you may choose to either power-on the system manually or let the system power-on automatically.

▶ Concept

COM Express

Computer-on-module (COM) Express is a PC form factor designed with the core computing integrated on a fairly compact module. All the I/O signals and power supply are concentrated and mapped to the board-to-board connectors on the bottom side to interface with a carrier board that is typically customized to fit the application. When an upgrade or change of application is needed, the physical separation of the core computing and the I/O of COM Express cuts back the cost greatly, whereas canonical IPC designs would typically require an entire makeover. The COM Express module can be replaced when there is only need to upgrade for higher computing performance, while the carrier board can be redesigned when there is solely change in application. COM Express also comes in different form factors and signal Types cut out for different scales and aspects of the system's application. Detailed specifications of COM Express are available on the website of PCI Industrial Computer Manufacturers Group (PICMG).



Carrier Board

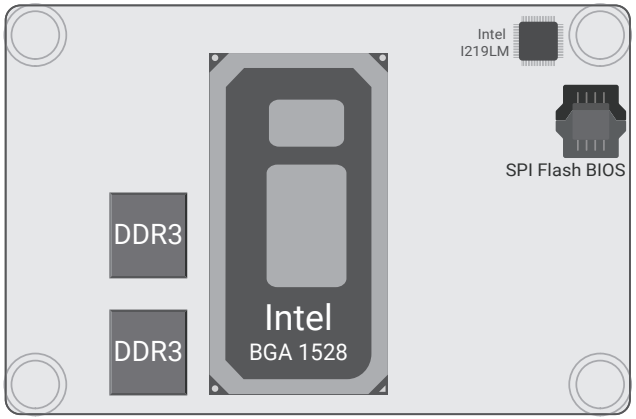
The design of a carrier board for COM Express greatly depends on the form factor and signal Type of the COM Express module. The carrier board typically handles — but not limited to — one COM Express module, and is populated with stand-offs that conform to the form factor of the module's mounting holes.

WL9A3 is a Type 10 COM Express Revision 3.0 module compatible with DFI's proprietary carrier board — COM100-B — as an optional item. If the carrier board is to be customized, the design guide for the carrier board can be attained via the Partner Zone page on our website.

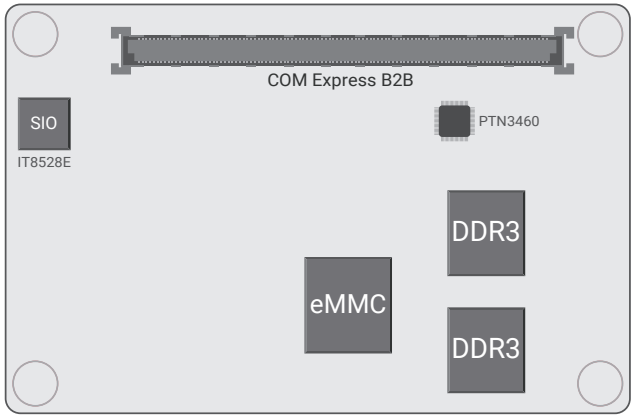
Chapter 2 - Hardware Installation

▶ Board Layout

Top View ⩛



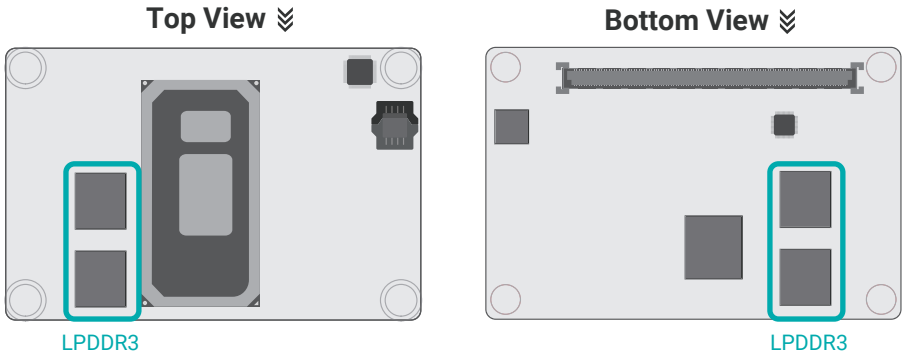
Bottom View ⩛



Important:
Electrostatic discharge (ESD) can damage your board, processor, disk drives, add-in boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Important:
When the Standby Power LED on the carrier board lights up, it indicates that there is power on the system board. Power-off the PC then unplug the power cord prior to installing any devices. Failure to do so will cause severe damage to the motherboard and components.

System Memory



The system board supports the following memory interface.

Single Channel (SC)
Data will be accessed in chunks of 64 bits from the memory channels.

Dual Channel (DC)
Data will be accessed in chunks of 128 bits from the memory channels. Dual channel provides better system performance because it doubles the data transfer rate.

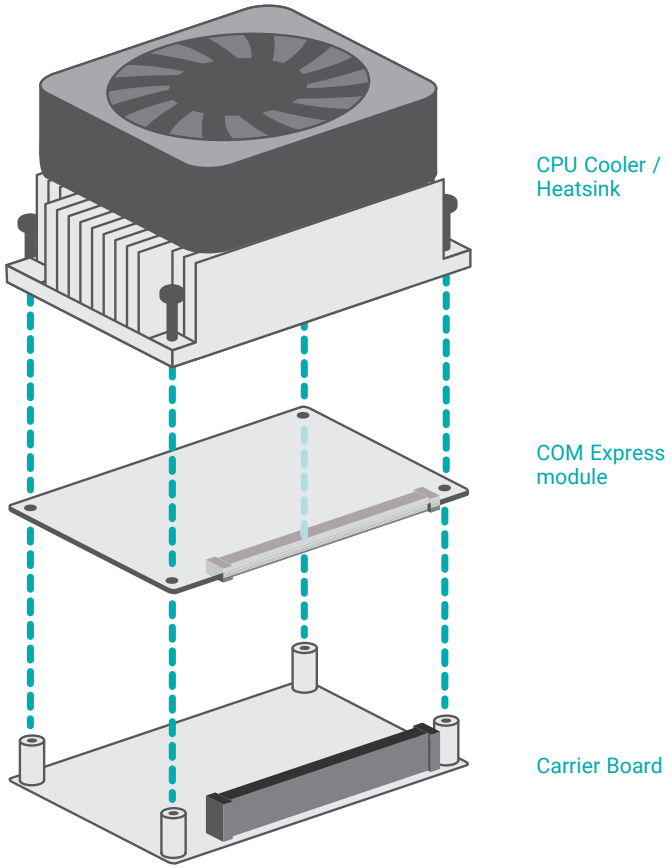
Single Channel	DIMMs are on the same channel. DIMMs in a channel can be identical or completely different. However, we highly recommend using identical DIMMs. Not all slots need to be populated.
Dual Channel	DIMMs of the same memory configuration are on different channels.

Features

- LPDDR3 2133MHz memory
- 8G or 16G memory down
- Dual channel memory interface

Assembly

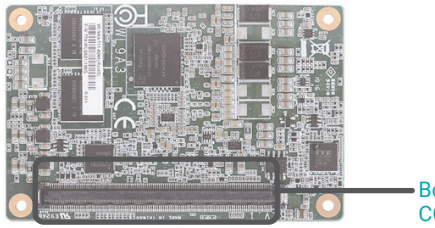
A CPU cooler / Heatsink may be included in the package. The CPU cooler / Heatsink contains four spring screws and shall be installed after the COM Express module is securely mounted onto the carrier board. Please make sure the cooler, the module, and the carrier board are oriented correctly by inspecting whether the screws, screw holes, and stand-offs all align.

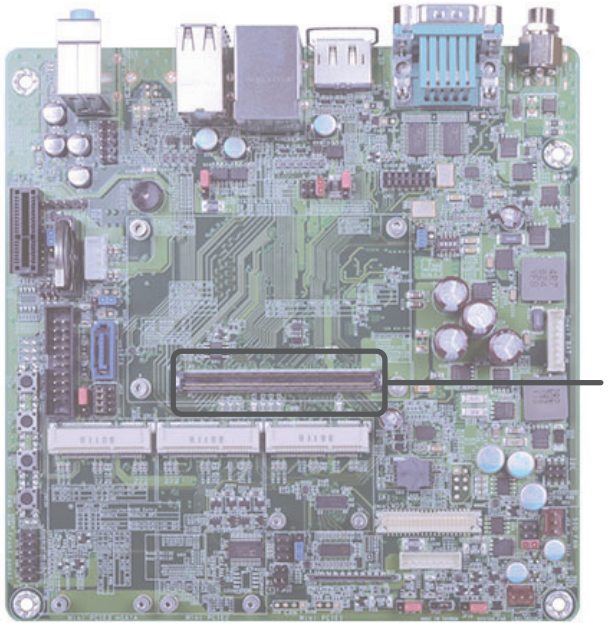


Note:
The carrier board is not included in the standard package and is typically customized.

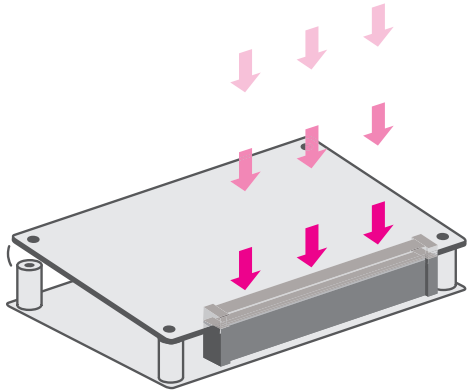
Assembly

1. Locate the COM Express board-to-board connector on the bottom side of the module and the carrier board. Locate the mounting holes on the module and the corresponding stand-offs on the carrier board.

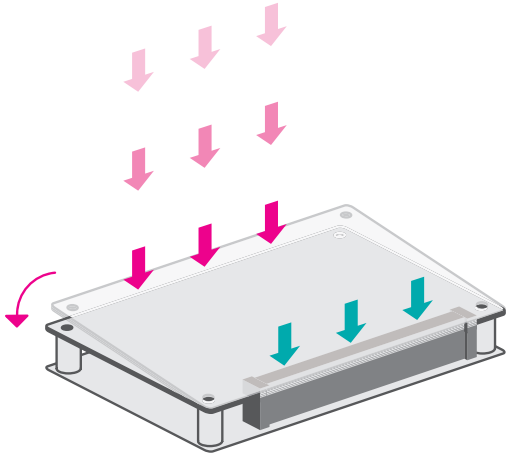




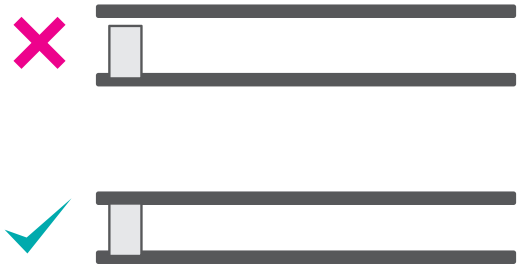
2. Place the module on the carrier board while making sure the mounting holes and connectors all align. At the long edge of the module closer to the connector, apply firm pressure onto the module and press it onto the carrier board until the two stand-offs and the edge of the module close up. The other edge of the module away from the connector may still remain slightly aloft from the stand-offs at this moment.



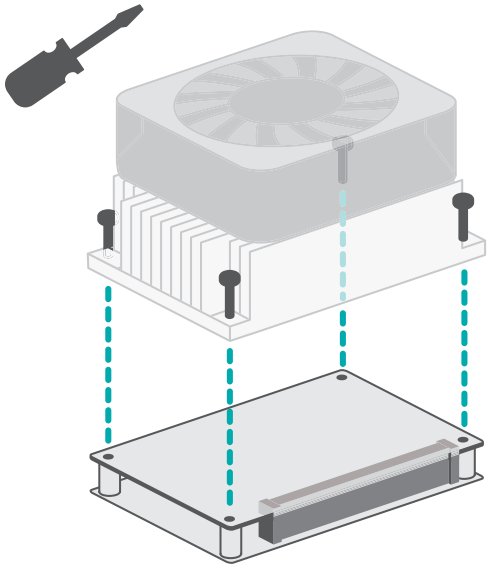
3. At the long edge away from the connector, apply firm pressure with another hand onto the module and press it onto the carrier board until the module is against the remaining two stand-offs. Please also maintain the pressure described in the previous step the whole time.



4. Inspect whether the gaps between the module and the stand-offs all close up. It is highly recommended that the module be removed and installed again following the previous steps when there is discernable gap.

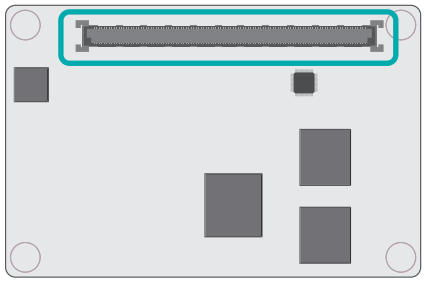


5. Place the CPU cooler / Heatsink, onto the module while making sure the screws on the cooler align with the screw holes on the module. The thermal interface metal underneath the cooler should also sit directly on top of the CPU chipset on the module. Use a screw driver to fasten the screws.



I/O Connectors

Board-to-board Connector



The board-to-board connector is located at the bottom side of the COM Express module. Two rows (row A & B) of pins and their signals are specified as listed below.

Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#
A3	GBE0_MDI3+	B3	LPC_FRAME#/ESPI_CS0#
A4		B4	LPC_AD0/ESPI_IO_0
A5	GBE0_LINK1000#	B5	LPC_AD1/ESPI_IO_1
A6	GBE0_MDI2-	B6	LPC_AD2/ESPI_IO_2
A7	GBE0_MDI2+	B7	LPC_AD3/ESPI_IO_3
A8	GBE0_LINK#	B8	LPC_DRQ0#/ESPI_ALERT0#
A9	GBE0_MDI1-	B9	LPC_DRQ1#/ESPI_ALERT1#
A10	GBE0_MDI1+	B10	LPC_CLK/ESPI_CK
A11	GND (FIXED)	B11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#
A13	GBE0_MDI0+	B13	SMB_CK
A14	GBE0_CTREF	B14	SMB_DAT
A15	SUS_S3#	B15	SMB_ALERT#
A16	SATA0_TX+	B16	SATA1_TX+
A17	SATA0_TX-	B17	SATA1_TX-
A18	SUS_S4#	B18	SUS_STAT#/ESPI_RESET#
A19	SATA0_RX+	B19	SATA1_RX+
A20	SATA0_RX-	B20	SATA1_RX-
A21	GND (FIXED)	B21	GND (FIXED)
A22	USB_SSRX0-	B22	USB_SSTX0-
A23	USB_SSRX0+	B23	USB_SSTX0+
A24	SUS_S5#	B24	PWR_OK

A25	USB_SSRX1-	B25	USB-SSTX1-
A26	USB_SSRX1+	B26	USB-SSTX1+
A27	BATLOW#	B27	WDT
A28	ATA_ACT#	B28	HDA_SDIN2
A29	AC/HDA_SYNC	B29	HDA_SDIN1
A30	AC/HAD_RST#	B30	HDA_SDIN0
A31	GND (FIXED)	B31	GND (FIXED)
A32	HDA_BITCLK	B32	SPKR
A33	HDA_SDOUT	B33	I2C_CK
A34	BIOS_DIS0#/ESPI_SAFS	B34	I2C_DAT
A35	THRMTRIP#	B35	THRM#
A36	USB6-	B36	USB7-
A37	USB6+	B37	USB7+
A38	USB_6_7_OC#	B38	USB_4_5_OC#
A39	USB4-	B39	USB5-
A40	USB4+	B40	USB5+
A41	GND (FIXED)	B41	GND (FIXED)
A42	USB2-	B42	USB3-
A43	USB2+	B43	USB3+
A44	USB_2_3_OC#	B44	USB_0_1_OC#
A45	USB0-	B45	USB1-
A46	USB0+	B46	USB1+
A47	VCC_RTC	B47	ESPI_EN#
A48	RSVD	B48	USB0_HOST_PRSNT
A49	GBE0_SDP	B49	SYS_RESET#
A50	LPC_SERIRQ/ESPI_CS1#	B50	CB_RESET#
A51	GND (FIXED)	B51	GND (FIXED)
A52	RSVD	B52	RSVD
A53	RSVD	B53	RSVD
A54	GPI0	B54	GPO1
A55	RSVD	B55	RSVD
A56	RSVD	B56	RSVD
A57	GND	B57	GPO2
A58	PCIE_TX3+	B58	PCIE_RX3+
A59	PCIE_TX3-	B59	PCIE_RX3-
A60	GND (FIXED)	B60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+
A62	PCIE_TX2-	B62	PCIE_RX2-
A63	GPI1	B63	GPO3
A64	PCIE_TX1+	B64	PCIE_RX1+
A65	PCIE_TX1-	B65	PCIE_RX1-
A66	GND	B66	WAKE0#
A67	GPI2	B67	WAKE1#
A68	PCIE_TX0+	B68	PCIE_RX0+
A69	PCIE_TX0-	B69	PCIE_RX0-
A70	GND (FIXED)	B70	GND (FIXED)
A71	LVDS_A0+/ eDP_TX2+	B71	DDI0_PAIR0+
A72	LVDS_A0-/ eDP_TX2-	B72	DDI0_PAIR0-
A73	LVDS_A1+/ eDP_TX1+	B73	DDI0_PAIR1+
A74	LVDS_A1-/ eDP_TX1-	B74	DDI0_PAIR1-
A75	LVDS_A2+/ eDP_TX0+	B75	DDI0_PAIR2+
A76	LVDS_A2-/ eDP_TX0-	B76	DDI0_PAIR2-
A77	LVDS_VDD_EN/ eDP_VDD_EN	B77	DDI0_PAIR4+
A78	LVDS_A3+	B78	DDI0_PAIR4-
A79	LVDS_A3-	B79	LVDS_BKLT_EN/ eDP_BKLT_EN
A80	GND (FIXED)	B80	GND (FIXED)
A81	LVDS_A_CK+/ eDP_TX3+	B81	DDI0_PAIR3+
A82	LVDS_A_CK-/ eDP_TX3-	B82	DDI0_PAIR3-
A83	LVDS_I2C_CK/ eDP_AUX+	B83	LVDS_BKLT_CTRL/ eDP_BKLT_CTRL
A84	LVDS_I2C_DAT/ eDP_AUX-	B84	VCC_5V_SBY
A85	GPI3	B85	VCC_5V_SBY
A86	RSVD	B86	VCC_5V_SBY
A87	eDP_HPD	B87	VCC_5V_SBY
A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A89	PCIE0_CK_REF-	B89	DDI0_HPD
A90	GND (FIXED)	B90	GND (FIXED)
A91	SPI_POWER	B91	DDI0_PAIR5+
A92	SPI_MISO	B92	DDI0_PAIR5-
A93	GPO0	B93	DDI0_PAIR6+
A94	SPI_CLK	B94	DDI0_PAIR6-
A95	SPI_MOSI	B95	DDI0_DDC_AUX_SEL
A96	TPM_PP	B96	USB7_HOST_PRSNT
A97	TYPE10#	B97	SPI_CS#
A98	SER0_TX	B98	DDI0_CTRLCLK_AUX+
A99	SER0_RX	B99	DDI0_CTRLDATA_AUX-
A100	GND (FIXED)	B100	GND (FIXED)
A101	SER1_TX	B101	FAN_PWNOUT
A102	SER1_RX	B102	FAN_TACHIN
A103	LID#	B103	SLEEP#
A104	VCC_12V	B104	VCC_12V
A105	VCC_12V	B105	VCC_12V
A106	VCC_12V	B106	VCC_12V
A107	VCC_12V	B107	VCC_12V
A108	VCC_12V	B108	VCC_12V
A109	VCC_12V	B109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)

▶ Signal Descriptions

Pin Types

I	Input to the Module
O	Output from the Module
I/O	Bi-directional input / output signal
OD	Open drain output

AC97/HDA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
HAD_RST#	A30	O CMOS	3.3V Suspend/3.3V	Serise 33 ohm	Connect to CODEC pin 11 RESET#	Reset output to CODEC, active low.
HDA_SYNC	A29	O CMOS	3.3V/3.3V	Serise 33 ohm	Connect to CODEC pin 10 SYNC	Sample-synchronization signal to the CODEC(s).
HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V	Serise 33 ohm	Connect to CODEC pin 6 BIT_CLK	Serial data clock generated by the external CODEC(s).
HDA_SDOUT	A33	O CMOS	3.3V/3.3V	Serise 33 ohm	Connect to CODEC pin 5 SDATA_OUT	Serial TDM data output to the CODEC.
HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC2 pin 8 SDATA_IN	Serial TDM data inputs from up to 3 CODECs.
HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC1 pin 8 SDATA_IN	
HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC0 pin 8 SDATA_IN	

Gigabit Ethernet Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
GBE0_MDI0+	A13	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI0+/-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following: 1000BASE-T / 100BASE-TX / 10BASE-T MDI[0]+/- B1_DA+/- TX+/- TX+/- MDI[1]+/- B1_DB+/- RX+/- RX+/- MDI[2]+/- B1_DC+/- MDI[3]+/- B1_DD+/-
GBE0_MDI0-	A12	I/O Analog	3.3V max Suspend			
GBE0_MDI1+	A10	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI1+/-	
GBE0_MDI1-	A9	I/O Analog	3.3V max Suspend			
GBE0_MDI2+	A7	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI2+/-	
GBE0_MDI2-	A6	I/O Analog	3.3V max Suspend			
GBE0_MDI3+	A3	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI3+/-	
GBE0_MDI3-	A2	I/O Analog	3.3V max Suspend			
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller 0 activity indicator, active low.
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		NC	Gigabit Ethernet Controller 0 link indicator, active low.
GBE0_ LINK100#	A4	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.
GBE0_ LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor 150Ω to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.
GBE0_SDP	A49	I/O	3.3V Suspend/3.3V	N/A		Gigabit Ethernet Controller 0 Software-Definable Pin. Can also be used for IEEE1588 support such as a 1pps signal.

SATA Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
SATA0_TX+	A16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn TX pin	Serial ATA or SAS Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA0_RX+	A19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn RX pin	Serial ATA or SAS Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_TX+	B16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn TX pin	Serial ATA or SAS Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module	AC Coupling capacitor		
SATA1_RX+	B19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn RX pin	Serial ATA or SAS Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module	AC Coupling capacitor		
ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V	PU 10K to 3.3V Suspend	Connect to LED and recommend current limit resistor 220Ω to 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.

PCI Express Lanes Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
PCIE_TX0+	A68	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 0
PCIE_TX0-	A69			AC Coupling capacitor		
PCIE_RX0+	B68	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF Slot - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 0
PCIE_RX0-	B69					
PCIE_TX1+	A64	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 1
PCIE_TX1-	A65			AC Coupling capacitor		
PCIE_RX1+	B64	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF Slot - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 1
PCIE_RX1-	B65					
PCIE_TX2+	A61	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 2
PCIE_TX2-	A62			AC Coupling capacitor		
PCIE_RX2+	B61	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF Slot - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 2
PCIE_RX2-	B62					

PCIE_TX3+	A58	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 3
PCIE_TX3-	A59			AC Coupling capacitor		
PCIE_RX3+	B58	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF Slot - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 3
PCIE_RX3-	B59					
PCIE0_CK_REF+	A88	O PCIE	PCIE		Connect to PCIE device, PCIe CLK Buffer or slot	Reference clock output for all PCI Express and PCI Express Graphics lanes.
PCIE0_CK_REF-	A89					

DDI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
DDI1_PAIR0+/ DP0_LANE0+	B71	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI1_PAIR0-/ DP0_LANE0-	B72				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR1+/ DP0_LANE1+	B73	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 1 differential pairs/Serial Digital Video B green output differential pair
DDI1_PAIR1-/ DP0_LANE1-	B74				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR2+/ DP0_LANE2+	B75	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI1_PAIR2-/ DP0_LANE2-	B76				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR3+/ DP0_LANE3+	B81	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 3 differential pairs/Serial Digital Video B clock output differential pair.
DDI1_PAIR3-/ DP0_LANE3-	B82				Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR4+	B77			NA	NA	NA for WL9A3
DDI1_PAIR4-	B78			NA	NA	
DDI1_PAIR5+	B91			NA	NA	NA for WL9A3
DDI1_PAIR5-	B92			NA	NA	
DDI1_PAIR6+	B93			NA	NA	NA for WL9A3
DDI1_PAIR6-	B94			NA	NA	
DDI1_CTRLCLK/DP0_AUX+	B98	I/O PCIE	AC coupled on Module	PD 100K to GND (S/W IC between Rpu/PCH)	Connect to DP AUX+	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V, PD 100K to GND (S/W IC between Rpu/Rpd resistor)	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high

DDI1_CTRLDA-TA/DP0_AUX-	B99	I/O PCIE	AC coupled on Module	PU 100K to 3.3V (S/W IC between Rpu/PCH)	Connect to DP AUX-	DP AUX- function if DDI1_DDC_AUX_SEL is no connect
		I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V/PU 100K to 3.3V (S/W IC between 2.2K/100K resistor)	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high
DDI1_HPD/ DP0_HPD	B89	I CMOS	3.3V / 3.3V	PD 100K to GND	PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI1_DDC_ AUX_SEL	B95	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRL-DATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals ********** DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort

USB Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
USB0+	A46	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 0
USB0-	A45					
USB1+	B46	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 1
USB1-	B45					
USB2+	A43	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 2
USB2-	A42					
USB3+	B43	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 3
USB3-	B42					
USB4+	A40	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 4
USB4-	A39					
USB5+	B40	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 5
USB5-	B39					
USB6+	A37	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 6
USB6-	A36					
USB7+	B37	I/O USB	3.3V Suspend/3.3V		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 7
USB7-	B36					
USB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.

USB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3.3VSB	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
USB_SSTX0+	B23	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX0-	B22			AC Coupling capacitor		
USB_SSRX0+	A23	I PCIE	AC coupled off Modul		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX0-	A22					
USB_SSTX1+	B26	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX1-	B25			AC Coupling capacitor		
USB_SSRX1+	A26	I PCIE	AC coupled off Modul		Connect 90Ω @100MHz Common Choke in series and ESD suppressors to GND to USB connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX1-	A25					
USB0_HOST_PRSNT	B48	I CMOS	3.3V Suspend/3.3V	PD 20k to GND, Reserved PU 10K to 3.3V		Module USB client may detect the presence of a USB host. A high value indicates that a host is present.
USB7_HOST_PRSNT	B96	I CMOS	3.3V Suspend/3.3V	PD 20k to GND, Reserved PU 10K to 3.3V		Module USB client may detect the presence of a USB host. A high value indicates that a host is present.

LVDS Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
LVDS_A0+	A71	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential pairs
LVDS_A0-	A72					
LVDS_A1+	A73	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A1-	A74					
LVDS_A2+	A75	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A2-	A76					
LVDS_A3+	A78	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A3-	A79					
LVDS_A_CK+	A81	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential clock
LVDS_A_CK-	A82					
LVDS_VDD_EN	A77	O CMOS	3.3V / 3.3V		Connect to enable control of LVDS panel power circuit	LVDS panel power enable

LVDS_BKLT_EN	B79	O CMOS	3.3V / 3.3V		Connect to enable control of LVDS panel backlight power circuit.	LVDS panel backlight enable
LVDS_BKLT_CTRL	B83	O CMOS	3.3V / 3.3V		Connect to brightness control of LVDS panel backlight power circuit.	LVDS panel backlight brightness control
LVDS_I2C_CK	A83	I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V	Connect to DDC clock of LVDS panel	I2C clock output for LVDS display use
LVDS_I2C_DAT	A84	I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V	Connect to DDC data of LVDS panel	I2C data line for LVDS display use

LPC Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
LPC_AD0/ ESPI_IO_0	B4	I/O CMOS	LPC: 3.3V / 3.3V ESPI: 1.8V Suspend / 1.8V	LPC Mode	Connect to LPC / ESPI device	LPC Mode: LPC multiplexed address, command and data bus. ESPI Mode: eSPI Master Data Input / Outputs.
LPC_AD1/ ESPI_IO_1	B5					
LPC_AD2/ ESPI_IO_2	B6					
LPC_AD3/ ESPI_IO_3	B7					
LPC_FRAME#/ ESPI_CS0#	B3	O CMOS	LPC: 3.3V / 3.3V ESPI: 1.8V Suspend / 1.8V	LPC Mode		LPC Mode: LPC frame indicates the start of an LPC cycle ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select0#.
LPC_DRQ0#/ ESPI_ALERT0#	B8	I CMOS	LPC: 3.3V / 3.3V ESPI: 1.8V Suspend / 1.8V	LPC Mode PU 10K to 3.3V		LPC Mode: LPC serial DMA request ESPI Mode: ESPI Mode: eSPI pins used by eSPI slave to request service from the eSPI master.
LPC_DRQ1#/ ESPI_ALERT1#	B9					
LPC_SERIRQ/ ESPI_CS1#	A50	LPC: I/O CMOS ESPI: O CMOS	LPC: 3.3V / 3.3V ESPI: 1.8V Suspend / 1.8V	LPC Mode PU 10K to 3.3V		LPC Mode: LPC serial interrupt ESPI Mode: eSPI Master Chip Select Outputs Driving Chip Select1#.
LPC_CLK/ ESPI_CK	B10	O CMOS	LPC: 3.3V / 3.3V ESPI: 1.8V Suspend / 1.8V	LPC Mode		LPC Mode: LPC clock output - 33MHz nominal ESPI Mode: eSPI Master Clock Output
ESPI_EN#	B47	I CMOS	NA	N/A		This signal is used by he Carrier to indicate the operating mode of the LPC/eSPI bus.

SPI Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
SPI_CS#	B97	O CMOS	3.3V Suspend/3.3V		Connect a series resistor 33Ω to Carrier Board SPI Device CS# pin	Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1
SPI_MISO	A92	I CMOS	3.3V Suspend/3.3V	Connect a series resistor 49.9Ω	Connect a series resistor 33Ω to Carrier Board SPI Device SO pin	Data in to Module from Carrier SPI
SPI_MOSI	A95	O CMOS	3.3V Suspend/3.3V	Connect a series resistor 49.9Ω	Connect a series resistor 33Ω to Carrier Board SPI Device SI pin	Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend/3.3V	Connect a series resistor 49.9Ω	Connect a series resistor 33Ω to Carrier Board SPI Device SCK pin	Clock from Module to Carrier SPI
SPI_POWER	A91	O	3.3V Suspend/3.3V	3.3V Susped Output		Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier
BIOS_DIS0#/ ESPI_SAFS	A34	I CMOS	NA	PU 10K to 3.3V		Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to COM Express Module Base Specification Revision 2.1 for strapping options of BIOS disable signals.
BIOS_DIS1#	B88					

Serial Interface Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
SER0_TX	A98	O CMOS	5V / 12V(design 3.3v~5V tolerant)		PD 4.7K	General purpose serial port 0 transmitter
SER0_RX	A99	I CMOS	5V / 12V(design 3.3v~5V tolerant)			General purpose serial port 0 receiver
SER1_TX	A101	O CMOS	5V / 12V(design 3.3v~5V tolerant)		PD 4.7K	General purpose serial port 1 transmitter
SER1_RX	A102	I CMOS	5V / 12V(design 3.3v~5V tolerant)			General purpose serial port 1 receiver

Miscellaneous Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
I2C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3SB		General purpose I2C port clock output
I2C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3SB		General purpose I2C port data I/O line
SPKR	B32	O CMOS	3.3V / 3.3V			Output for audio enunciator - the “speaker” in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes.
WDT	B27	O CMOS	3.3V / 3.3V			Output indicating that a watchdog time-out event has occurred.
FAN_PWNOUT	B101	O OD CMOS	3.3V / 12V			Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan’s RPM.
FAN_TACHIN	B102	I OD CMOS	3.3V / 12V			Fan tachometer input for a fan with a two pulse output.
TPM_PP	A96	I CMOS	3.3V / 3.3V	N/A		Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM. (NC for WL9A3)

Power and System Management Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
PWRBTN#	B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3VSB		A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.
SYS_RESET#	B49	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3VSB		Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.
CB_RESET#	B50	O CMOS	3.3V Suspend/3.3V			Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.
PWR_OK	B24	I CMOS	3.3V / 3.3V			Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
SUS_STAT#/ ESPI_RESET#	B18	O CMOS	LPC: 3.3V Suspend/3.3V ESPI: 1.8V Suspend / 1.8V	LPC Mode		LPC Mode: Indicates imminent suspend operation; used to notify LPC devices. ESPI Mode: eSPI Reset Reset the eSPI interface for both master and slaves.
SUS_S3#	A15	O CMOS	3.3V Suspend/3.3V			Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
SUS_S4#	A18	O CMOS	3.3V Suspend/3.3V			Indicates system is in Suspend to Disk state. Active low output.
SUS_S5#	A24	O CMOS	3.3V Suspend/3.3V			Indicates system is in Soft Off state.
WAKE0#	B66	I CMOS	3.3V Suspend/3.3V	PU 1K to 3.3VSB		PCI Express wake up signal.
WAKE1#	B67	I CMOS	3.3V Suspend/3.3V	PU 1K to 3.3VSB		General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity.
BATLOW#	A27	I CMOS	3.3V Suspend/ 3.3V	PU 10K to 3.3VSB		Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes.
LID#	A103	I OD CMOS	3.3V Suspend/12V	PU 47K to 3.3VSB		LID switch. Low active signal used by the ACPI operating system for a LID switch.
SLEEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 47K to 3.3VSB		Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again.
THRM#	B35	I CMOS	3.3V / 3.3V	PU 4.7K to 3.3V		Input from off-Module temp sensor indicating an over-temp situation.
THRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 10K to 3.3V		Active low output indicating that the CPU has entered thermal shutdown.
SMB_CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3VSB		System Management Bus bidirectional clock line.
SMB_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3.3VSB		System Management Bus bidirectional data line.
SMB_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 10K to 3.3VSB		System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.

GPIO Signals Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
GPO0	A93	O CMOS	3.3V / 3.3V			General purpose output pins.
GPO1	B54					
GPO2	B57					
GPO3	B63					
GPI0	A54	I CMOS	PU 100K to 3V3			General purpose input pins.
GPI1	A63					
GPI2	A67					
GPI3	A85					

Power and GND Signal Descriptions

Signal	Pin#	Pin Type	Pwr Rail /Tolerance	WL9A3	Carrier Board	Description
VCC_12V	A104~A109 B104~B109	Power	12V – 20V	12V – 20V		Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used. The module supplies a wide range of power from 12V to 20.0V.
VCC_5V_SBY	B84~B87	Power	4.75V - 5.25V	4.75V - 5.25V		Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.
VCC_RTC	A47	Power	2.0V - 3.3V	2.0V - 3.3V		Real-time clock circuit-power input. Nominally +3.0V.
GND	Pin Type: Power; Pin#: A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110					Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.

Chapter 3 - BIOS Setup

▶ Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board.

The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

Note:
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.

The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message “Press DEL to run setup” will appear on the screen. If the message disappears before you respond, restart the system or press the “Reset” button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

Legends

Keys	Function
Right / Left arrow	Move the highlight left or right to select a menu
Up / Down arrow	Move the highlight up or down between submenus or fields
<Enter>	Enter the highlighted submenu
+ (plus key)/F6	Scroll forward through the values or options of the highlighted field
- (minus key)/F5	Scroll backward through the values or options of the highlighted field
<F1>	Display general help
<F2>	Previous Values
<F9>	Optimized defaults
<F10>	Save and Exit
<Esc>	Return to previous menu

Scroll Bar

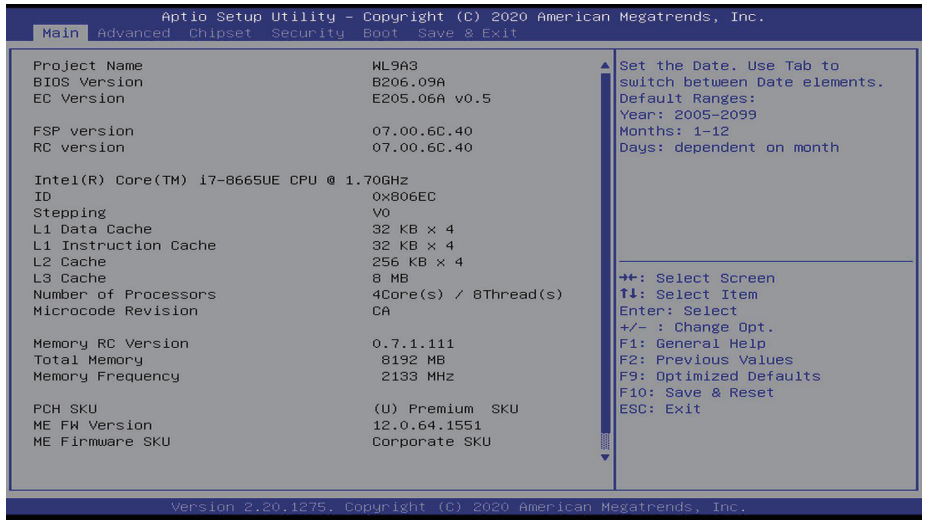
When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

Submenu

When “▶” appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

▶ Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

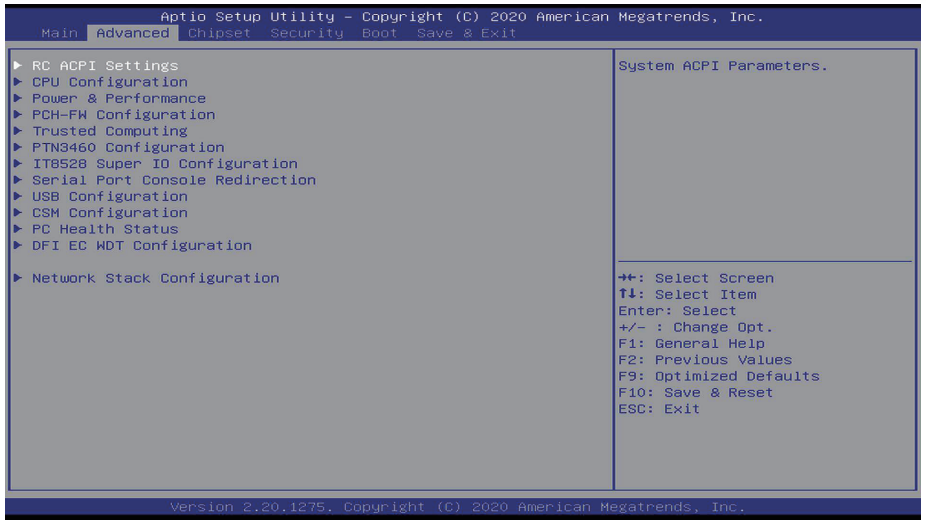
System Date

The date format is <month>, <date>, <year>. Month displays the month, from 01 to 12. Date displays the date, from 01 to 31. Year displays the year, from 2000 to 2099.

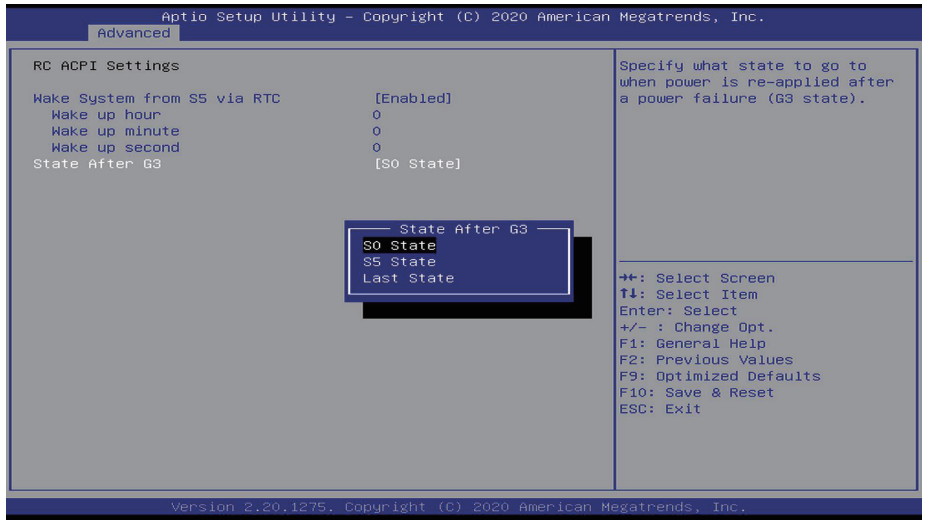
▶ Advanced

The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

Important:
Setting incorrect field values may cause the system to malfunction.



ACPI Configuration



Wake System from S5 via RTC

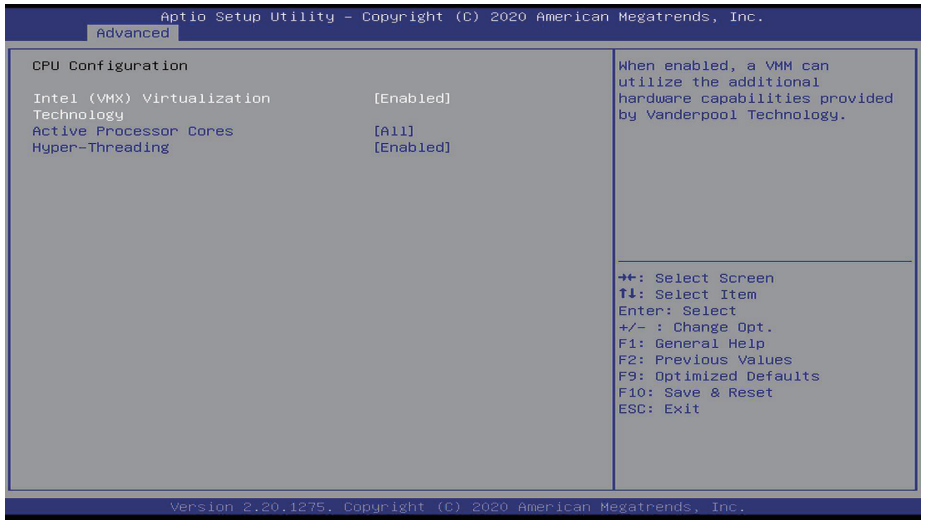
If enabled, system will wake up at specific time.

State After G3

Select between S0 State, Last State, and S5 State. This field is used to specify what state the system is set to return to when power is re-applied after a power failure (G3 state).

S0 State	The system automatically powers on after power failure.
S5 State	The system enter soft-off state after power failure. Power-on signal input is required to power up the system.
Last State	The system will return to the state before power failure.

CPU Configuration



Intel (VMX) Virtualization Technology

When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Active Processor Cores

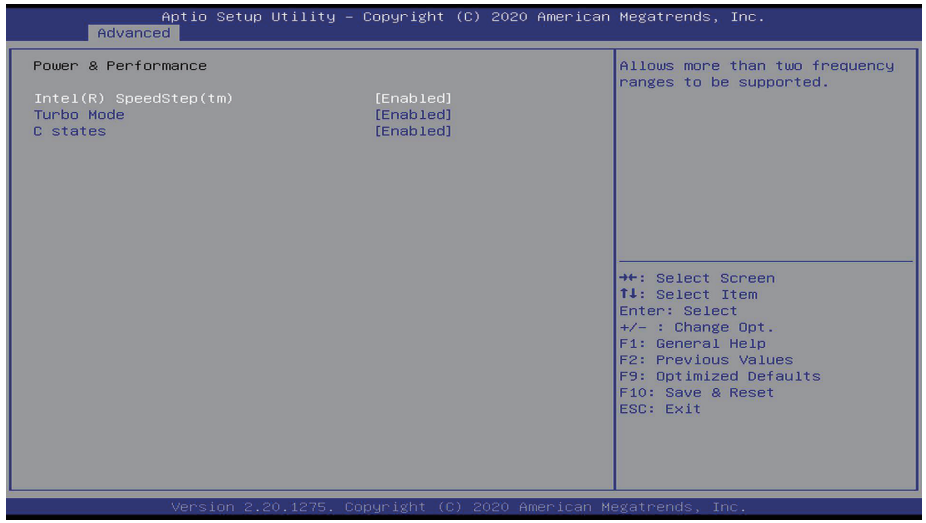
Select number of cores to enable in each processor package.

Hyper-threading

Enables this field for Windows XP and Linux which are optimized for Hyper-Threading technology. Select disabled for other OSes not optimized for Hyper-Threading technology. When disabled, only one thread per enabled core is enabled.

▶ Advanced

Power & Performance



Intel(R) SpeedStep(tm)

This field is used to enable or disable the Enhanced Intel SpeedStep® Technology (EIST), which helps optimize the balance between system's power consumption and performance. After it is enabled in the BIOS, EIST features can then be enabled via the operating system's power management.

Turbo Mode

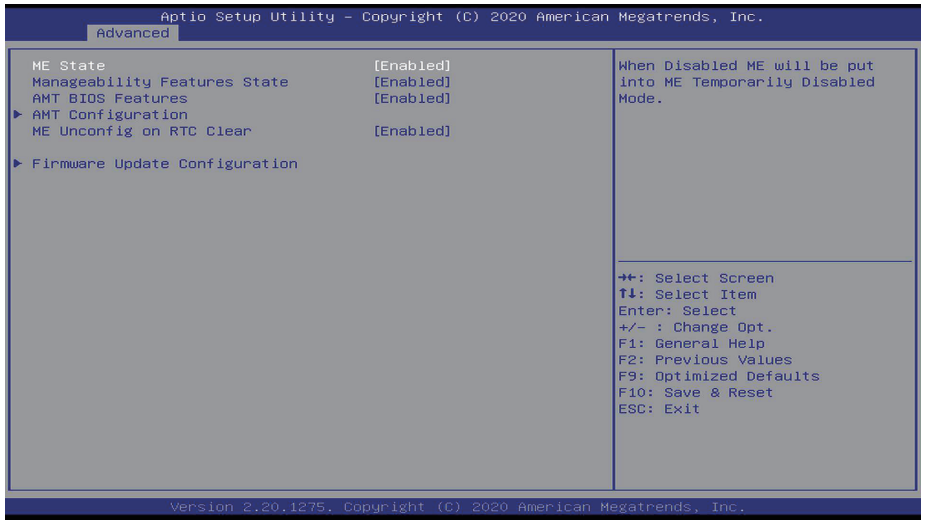
Enable or disable turbo mode of the processor. This field will only be displayed when EIST is enabled.

C-States

Enable or disable CPU Power Management. It allows CPU to go to C States when it's not 100% utilized.

▶ Advanced

PCH-FW Configuration



ME State

When this field is set to Disabled, ME will be put into ME Temporarily Disabled Mode.

Manageability Features State

Enable or disable Intel(R) Manageability features. This option disables/enables Manageability Features support in FW. To disable, support platform must be in an unprovisioned state first.

AMT BIOS Features

When disabled, AMT BIOS features are no longer supported and user is no longer able to access MEBx Setup. This option does not disable manageability features in FW.

AMT Configuration

This section is used to configure Intel(R) Active Management Technology Parameters.

ME Unconfig on RTC Clear

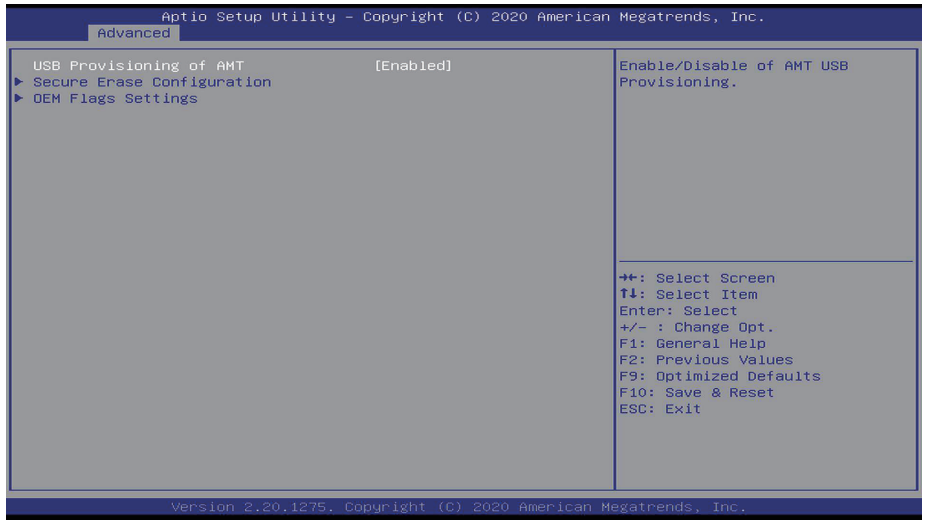
When disabled, ME will not be unconfigured on RTC Clear.

Firmware Update Configuration

This section is used to configure Management Engine Technology Parameters. Refer page 39 for more information.

▶ Advanced

PCH-FW Configuration > AMT Configuration



USB Provisioning of AMT

Enable or disable AMT USB Provisioning.

Secure Erase Configuration

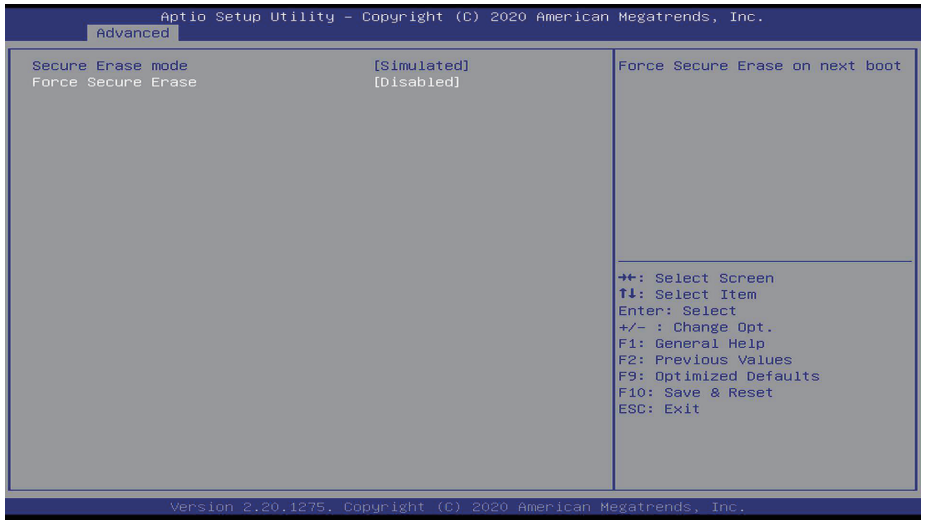
This section is used to configure Secure Erase.

OEM Flags Settings

Configure OEM flags.

▶ Advanced

PCH-FW Configuration > AMT Configuration > Secure Erase Configuration



Secure Erase Mode

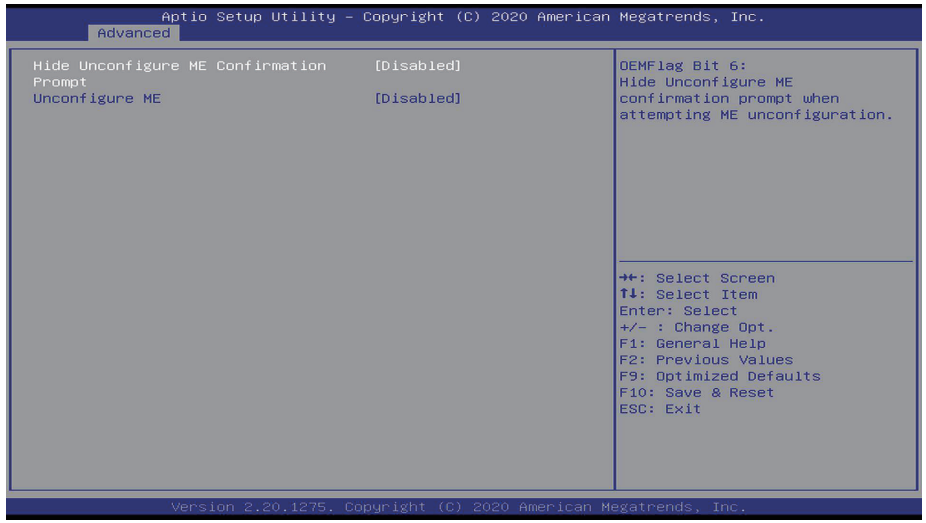
Select Secure Erase module behavior: Simulated or Real.

Force Secure Erase

Enable or disable Force Secure Erase on next boot.

▶ Advanced

PCH-FW Configuration > AMT Configuration > OEM Flags Settings



Hide Unconfigure ME Confirmation Prompt

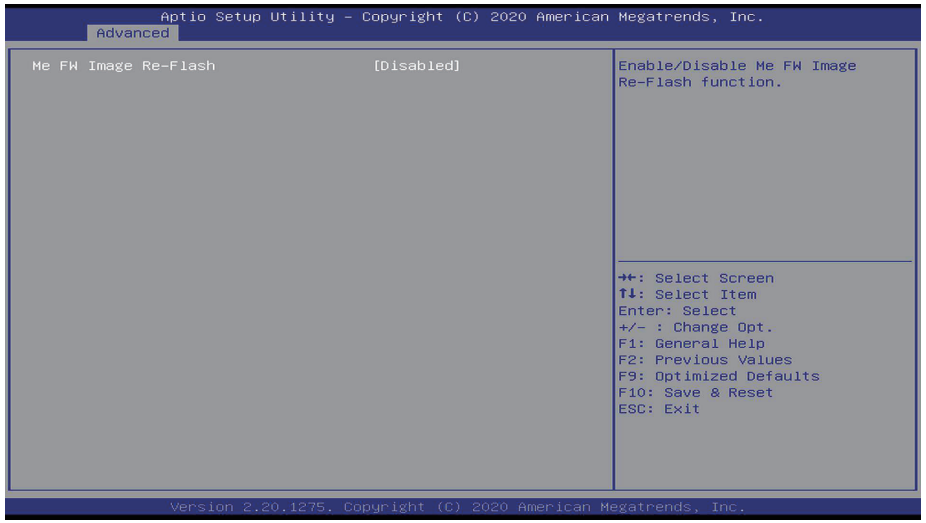
Enable or disable to hide unconfigure ME confirmation prompt when attempting ME unconfiguration.

Unconfigure ME

Enable or disable to unconfigure ME with resetting MEBx password to default

▶ Advanced

PCH-FW Configuration > Firmware Update Configuration

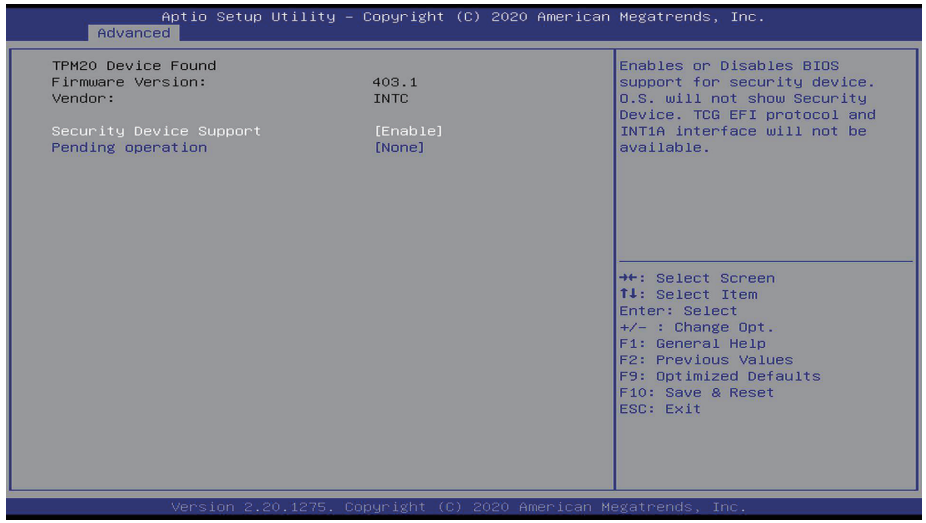


Me FW Image Re-Flash

This field is used to enable or disable the Me FW Image Re-Flash function.

▶ Advanced

Trusted Computing



Security Device Support

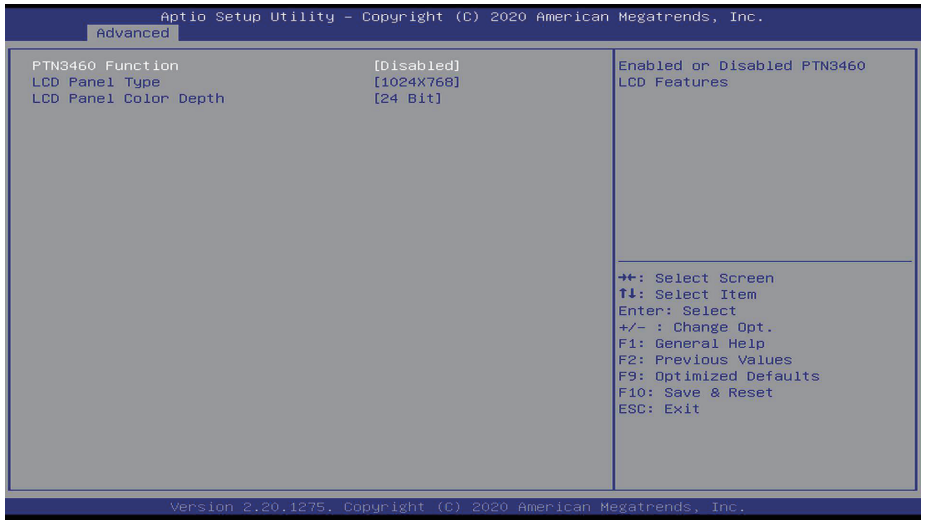
This field is used to enable or disable BIOS support for the security device. O.S will not show the security device. TCG EFI protocol and INT1A interface will not be available.

Pending operation

Schedule an operation for the security device.

▶ Advanced

PTN3460 Configuration



PTN3460 Function

Enable or disable PTN3460 LCD Features.

LCD Panel Type

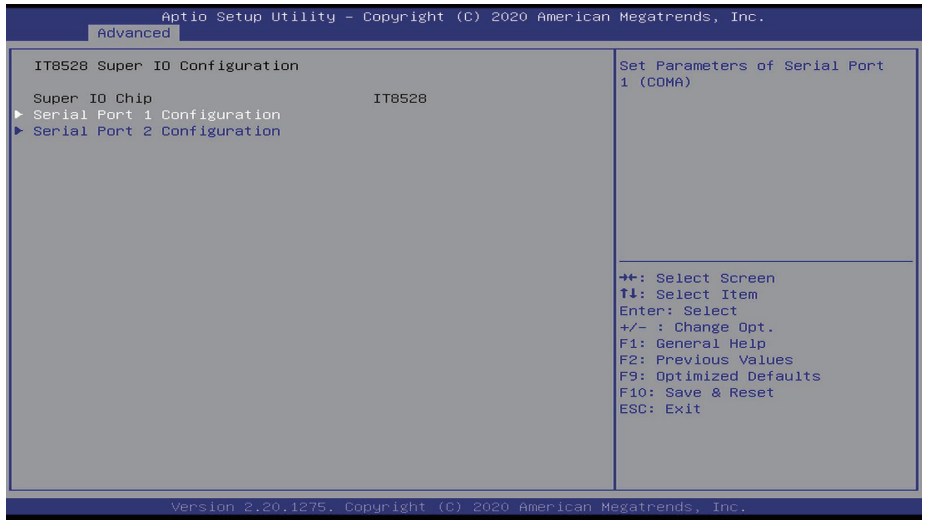
Choose a resolution of LCD panel.

LCD Panel Color Depth

Select the LCD panel color depth: 18 bit, 24 bit, 36 bit or 48 bit.

▶ Advanced

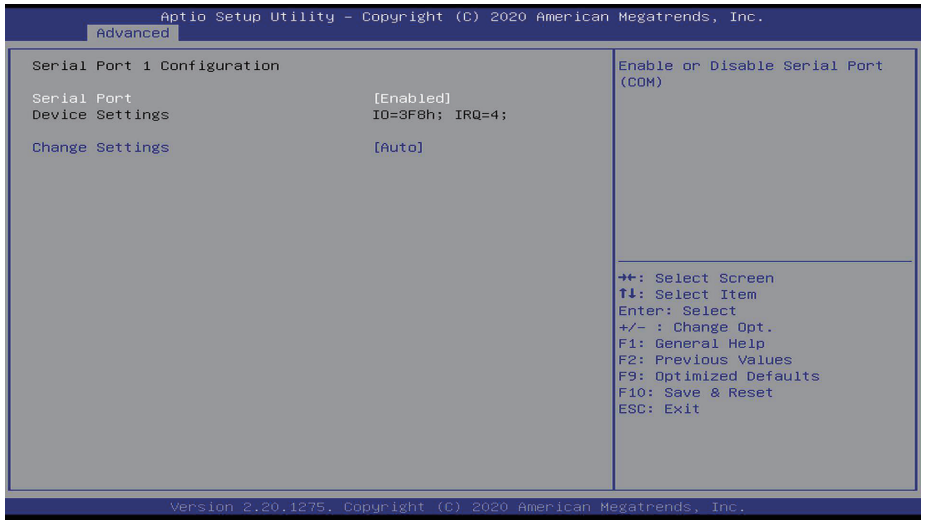
IT8528 Super IO Configuration



To configure serial port 1(COMA) and serial port 2(COMB).

▶ Advanced

IT8528 Super IO Configuration > Serial Port Configuration



Serial Port

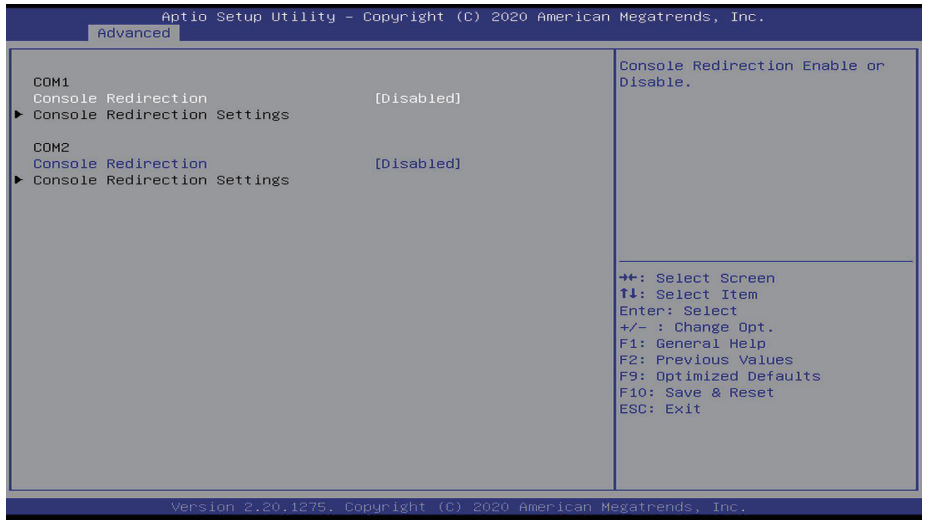
Enable or disable the serial port.

Change Settings

Select an optimal setting for Super IO Device.

▶ Advanced

Serial Port Console Redirection

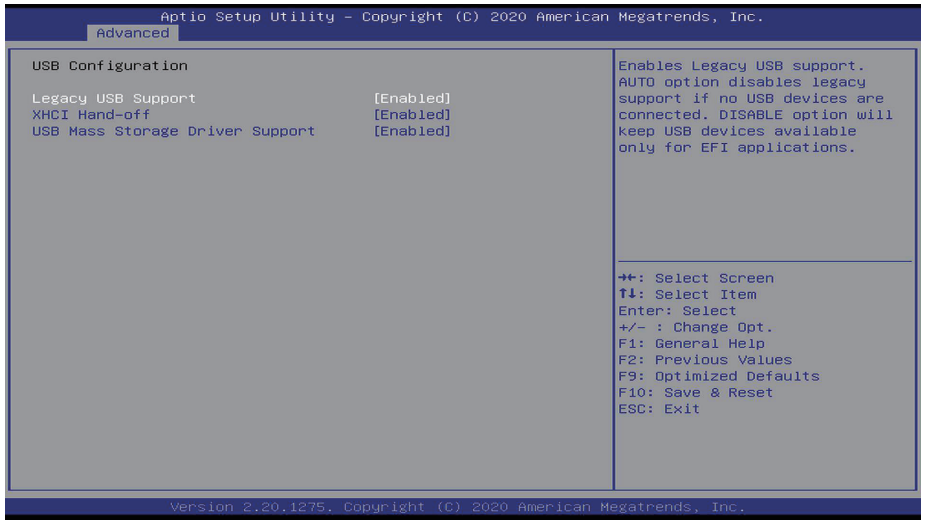


Console Redirection

Enable or disable console redirection.

▶ Advanced

USB Configuration



Legacy USB Support

Enabled

Enable Legacy USB support.

Disabled

Keep USB devices available only for EFI applications.

Auto

Disable Legacy support if no USB devices are connected.

XHCI Hand-off

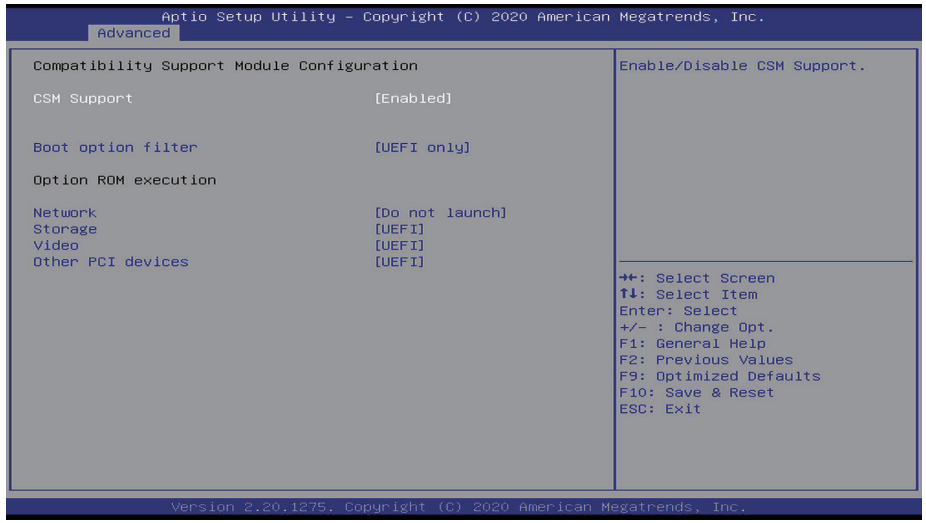
Enable or disable XHCI Hand-off.

USB Mass Storage Driver Support

Enable or disable USB Mass Storage Driver Support.

▶ Advanced

CSM Configuration



CSM Support

This section is used to enable or disable CSM Support. When CSM Support is set to enabled, several options will appear for configuration.

Boot option filter

This field controls Legacy/UEFI ROMs priority.

Network

This field controls the execution of UEFI and Legacy Network OpROM.

Storage

This field controls the execution of UEFI and Legacy Storage OpROM.

Video

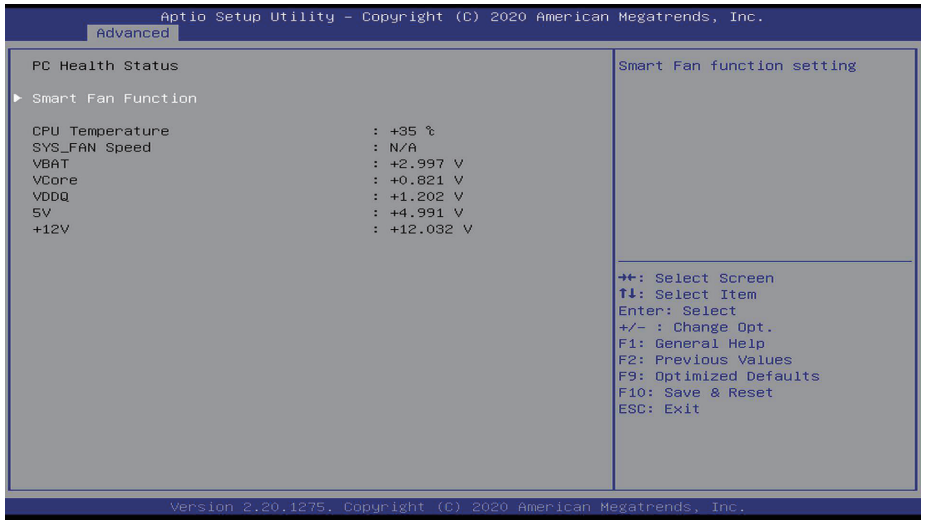
This field controls the execution of UEFI and Legacy Video OpROM.

Other PCI devices

This field determines OpROM execution policy for devices other than Network, Storage or Video.

▶ Advanced

PC Health Status

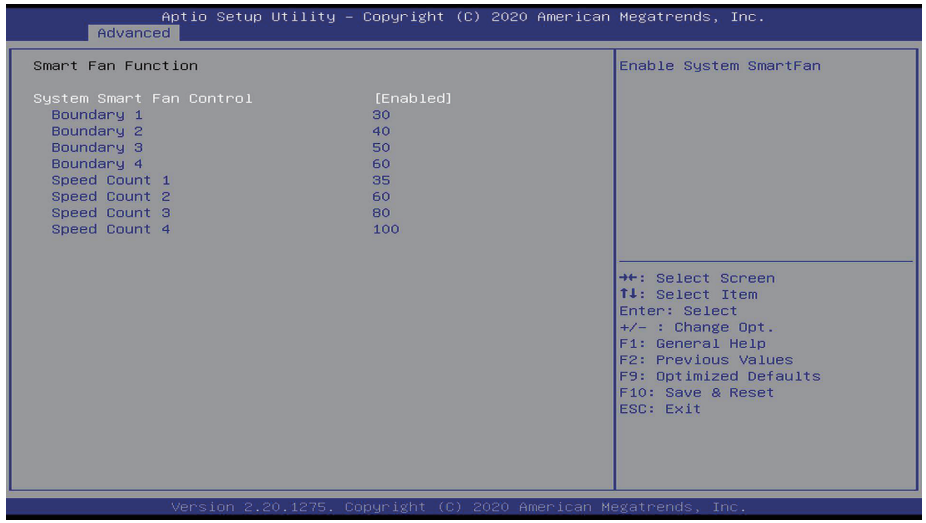


Smart Fan Function

This section is for smart fan function setting. Refer next page for more information.

▶ Advanced

PC Health Status > Smart Fan Function



CPU Smart Fan and System Smart Fan Control

Enable or disable the CPU smart fan and system smart fan, if disabled a value of fan speed should be assigned.

Boundary 1 to Boundary 4

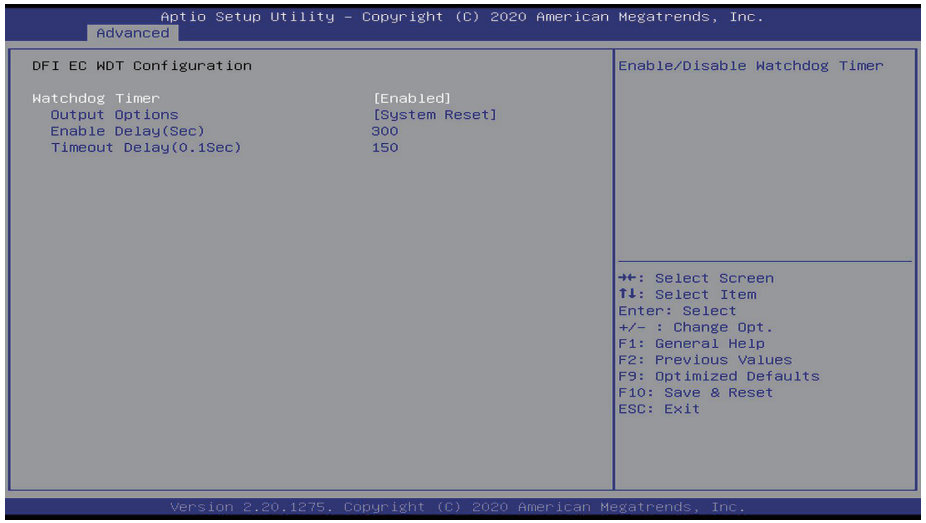
Set the boundary temperatures that determine the operation of the fan with different fan speeds accordingly. For example, when the system or the CPU temperature reaches boundary temperature 1, the system or CPU fan should be turned on and operate at the designated speed. The range is from 0-127oC.

Speed Count 1 to Speed Count 4

Set the fan speed. The range is from 1-100% (full speed).

▶ Advanced

DFI EC WDT Configuration



Watchdog Timer

Enable or disable watchdog timer.

Output Options

System Reset

A watchdog timeout triggers the system to reset.

Output Only

WDT pin goes high upon timeout of the watchdog timer.

Generate NMI

Generate NMI upon timeout of the watchdog timer.

Enable Delay(Sec)

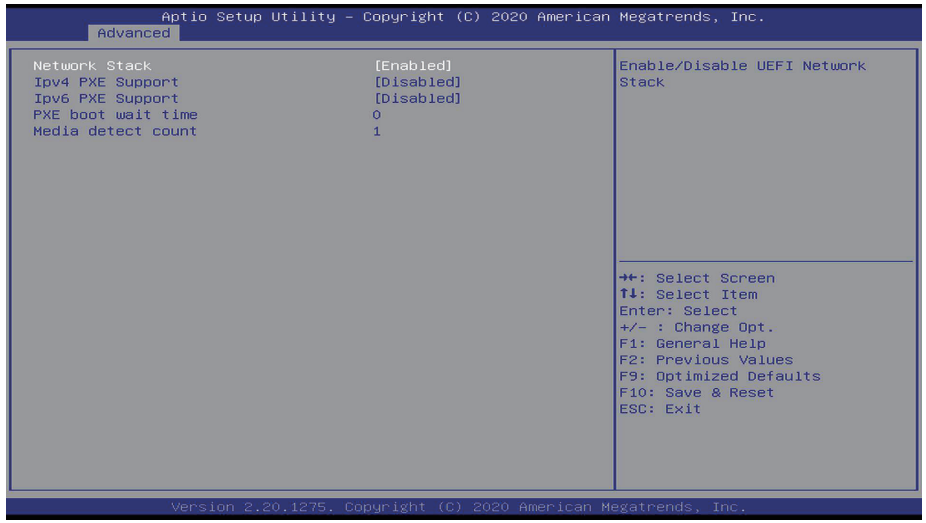
Enter a value of seconds to wait for OS to boot and follow-up operations.

Timeout Delay(0.1Sec)

Enter a value to delay the timeout period of watchdog timer.

▶ Advanced

Network Stack Configuration



Network Stack

This section is used to enable or disable UEFI network stack. When Network Stack is enabled, the following fields will appear.

Ipv4 PXE Support

Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

PXE boot wait time

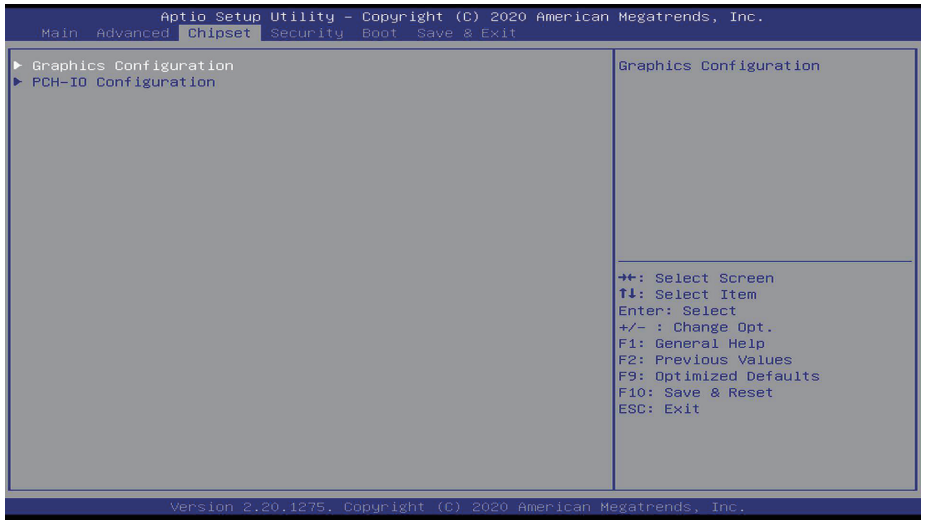
Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

Media detect count

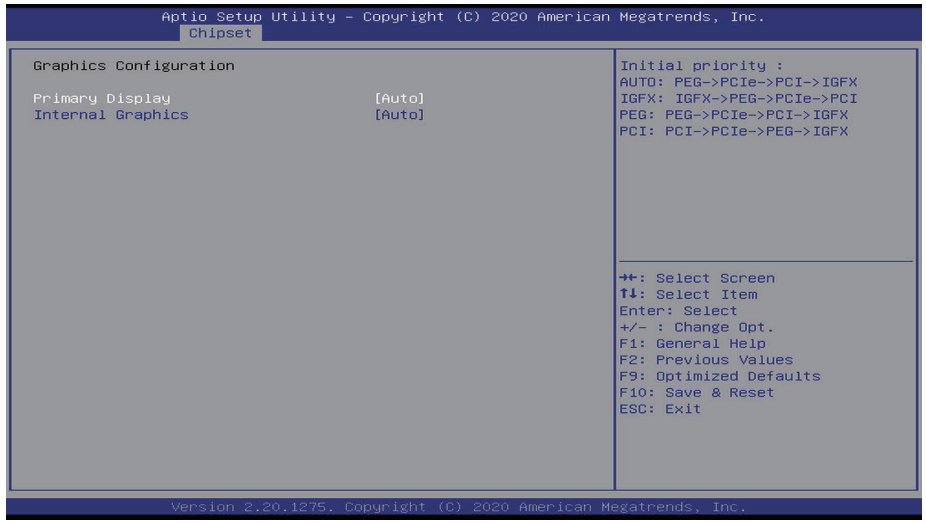
Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

▶ Chipset

To configure parameters of graphics and PCH-IO.



Graphics Configuration



Primary Display

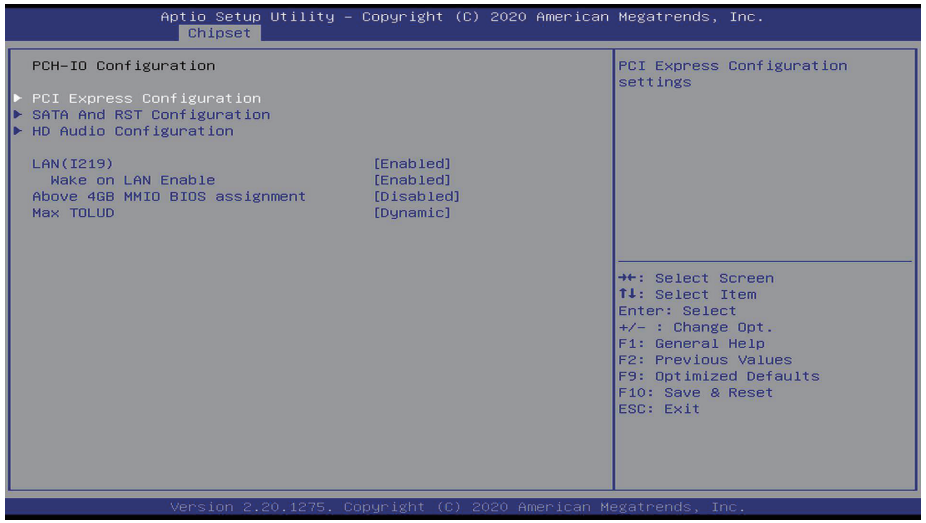
Select which of IGFX/PEG/PCI Graphics device to be the primary display.

Internal Graphics

Keep IGFX enabled based on the setup options.

▶ Chipset

PCH-IO Configuration



Above 4GB MMIO BIOS assignment

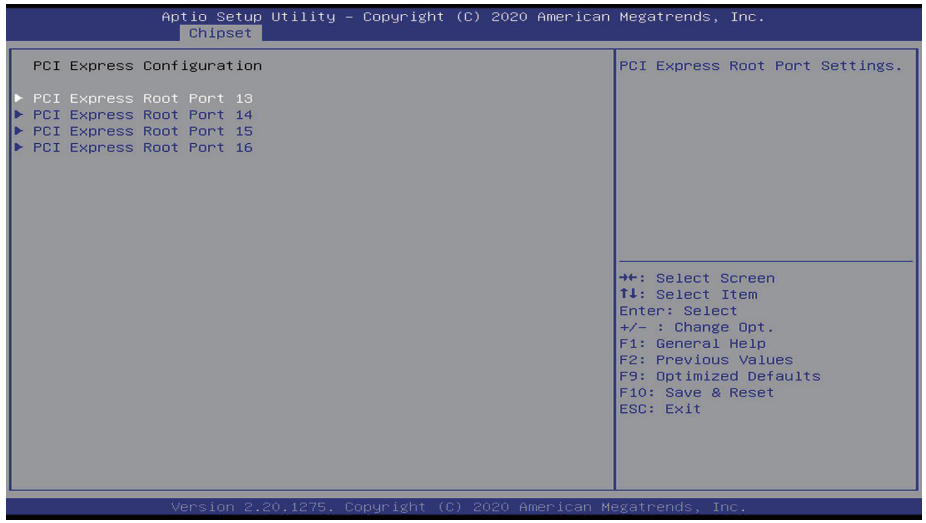
Enable/Disable above 4GB MemoryMappedIO BIOS assignment. This is enabled automatically when Aperture Size is set to 2048MB.

Max TOLUD

Assign the maximum value of Top Of Lower Usable DRAM (TOLUD). Select to specify a fixed value, or select "Dynamic" so that the assignment would adjust TOLUD automatically based on largest MMIO length of installed graphic controller.

▶ Chipset

PCH-IO Configuration > PCI Express Configuration

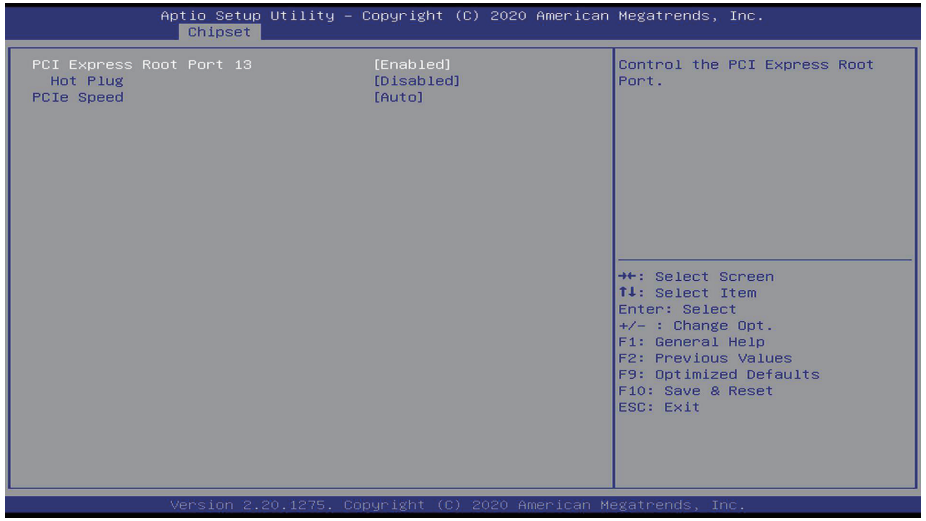


PCI Express Configuration

This section configures settings relevant to PCI Express root ports.

▶ Chipset

PCH-IO Configuration > PCI Express Configuration



PCI Express Root Port

Enable or disable PCI Express root port.

Hot Plug

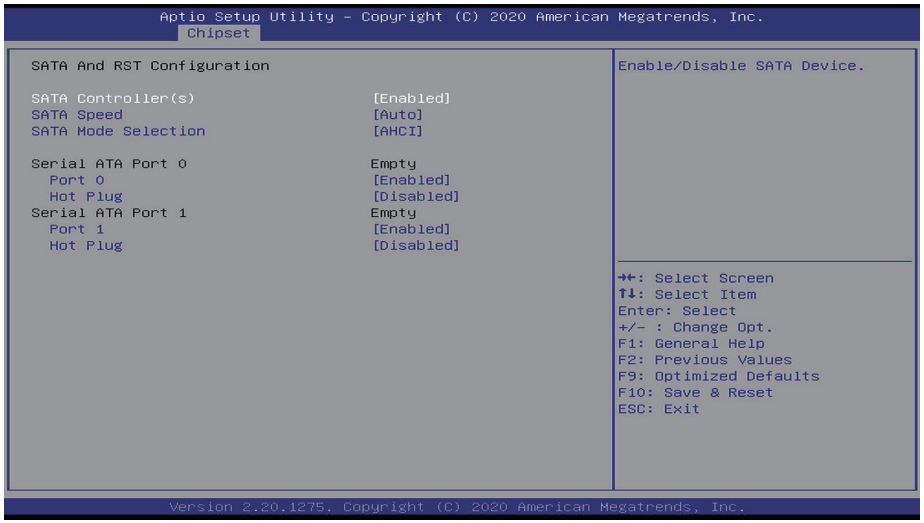
Enable or disable PCI Express root port hot plug.

PCIe Speed

Set it Auto or Gen1/Gen2/Gen3.

▶ Chipset

PCH-IO Configuration > SATA And RST Configuration



SATA Controller(s)

This field is used to enable or disable the Serial ATA controller.

SATA Speed

This field is used to select SATA speed generation limit: Auto, Gen1, Gen2 or Gen3.

SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.
AHCI This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

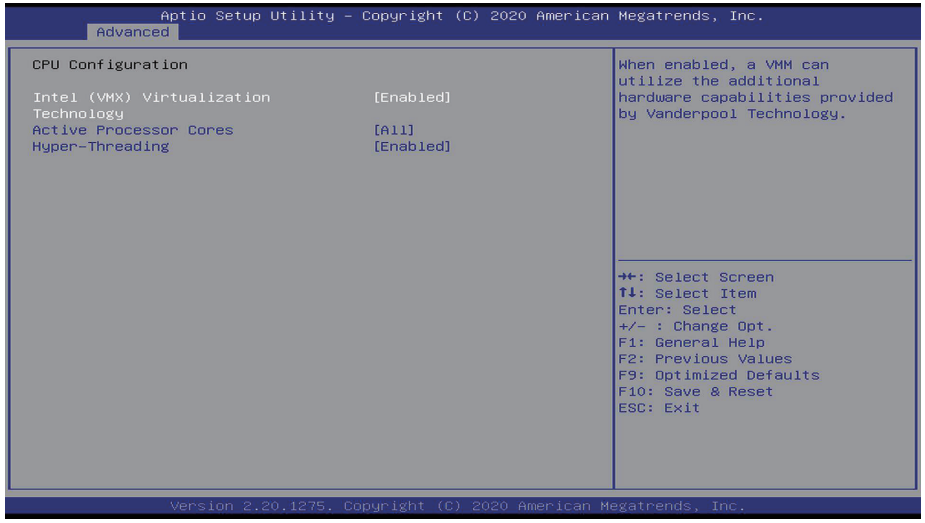
Intel RST Premium With Intel Optane System Acceleration allows you to create RAID or Intel Rapid Storage configuration with Intel® Optane™ system acceleration on Serial ATA devices.

Hot Plug

Enable or disable the Serial ATA port and its hot plug function.

▶ Chipset

PCH-IO Configuration > HD Audio Configuration

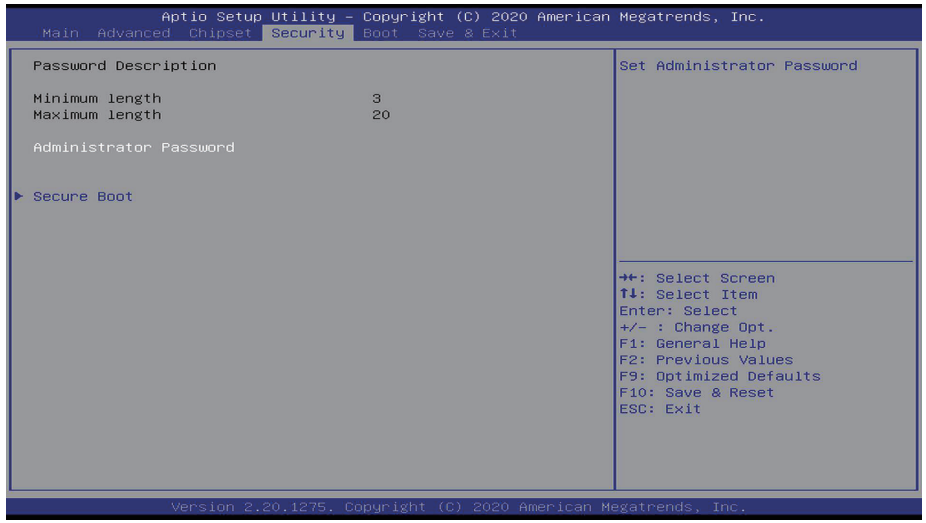


HD Audio

Unconditionally disable or enable HD audio.

▶ Security

To configure relevant settings of security.

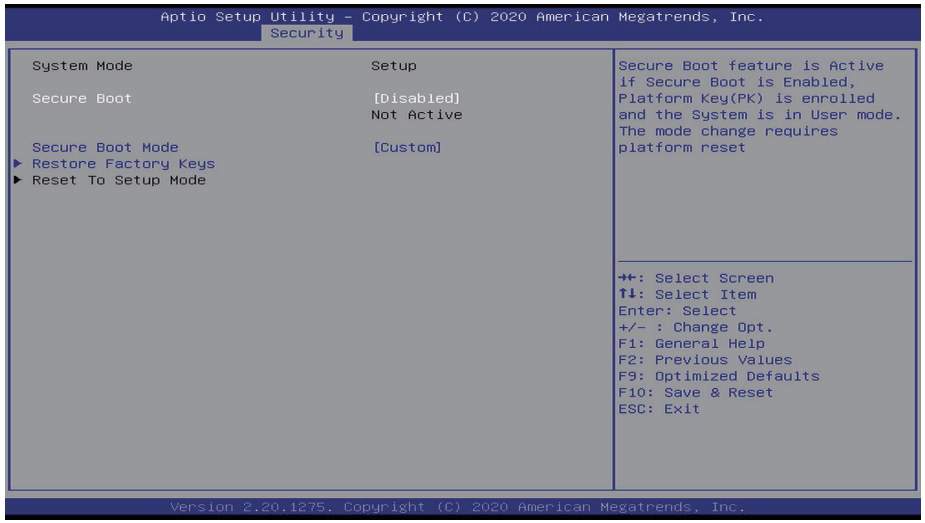


Administrator Password

Set the administrator password. To clear the password, input nothing and press enter when a new password is asked. Administrator Password will be required when entering the BIOS.

▶ Chipset

Security > Secure Boot



Secure Boot

The Secure Boot store a database of certificates in the firmware and only allows the OSes with authorized signatures to boot on the system. To activate Secure Boot, please make sure that “Secure Boot” is “[Enabled]”, Platform Key (PK) is enrolled, “System Mode” is “User”, and CSM is disabled. After enabling/disabling Secure Boot, please save the configuration and restart the system. When configured and activated correctly, the Secure Boot status will be “Active”.

Secure Boot Customization

Select the secure boot mode — Standard or Custom. When set to Custom, the following fields will be configurable for the user to manually modify the key database.

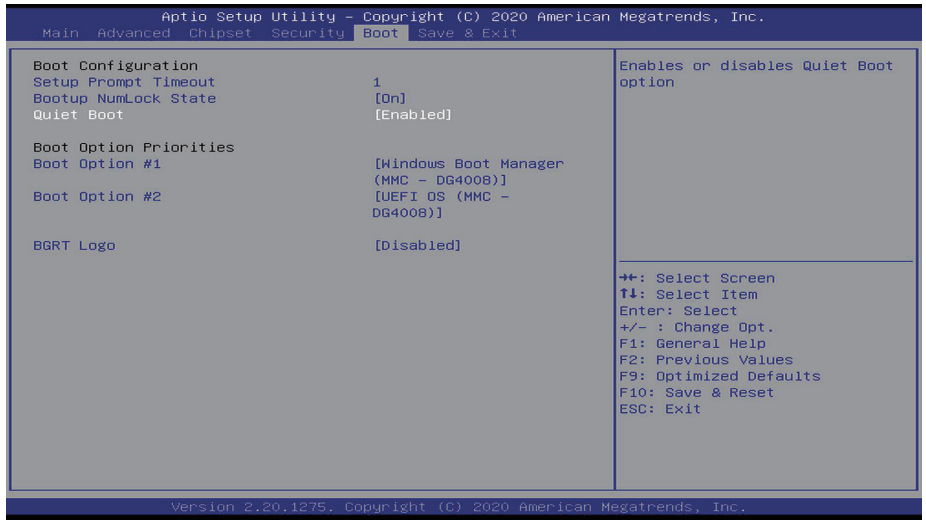
Restore Factory Keys

Force system to User Mode. Load OEM-defined factory defaults of keys and databases onto the Secure Boot. Press Enter and a prompt will show up for you to confirm.

Reset To Setup Mode

Clear the database from the NVRAM, including all the keys and signatures installed in the Key Management menu. Press Enter and a prompt will show up for you to confirm.

▶ Boot



Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state: On or Off.

Quiet Boot

This section is used to enable or disable quiet boot option.

Boot Option Priorities

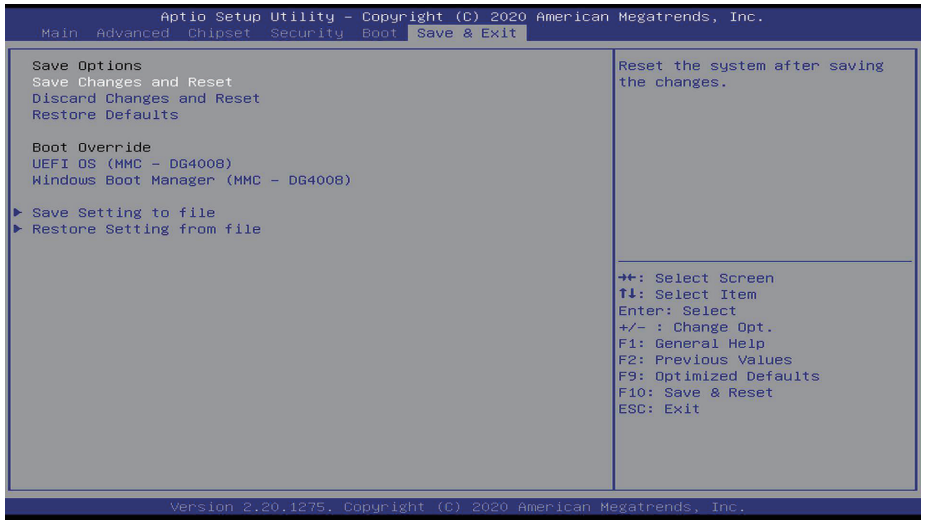
Rearrange the system boot order of available boot devices.

BGRT Logo

It is used to enable or disable to support display logo with ACPI BGRT table.

Note:
If “Boot option filter” of “CSM Configuration” is set to “UEFI and Legacy” or “UEFI only” and “Quiet Boot” is set to enabled, “BGRT Logo” will show up for configuration. Refer to the Advanced > CSM Configuration for more information.

▶ Save & Exit



Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

Boot Override

Move the cursor to an available boot device and press Enter, and then the system will immediately boot from the selected boot device. The Boot Override function will only be effective for the current boot. The “Boot Option Priorities” configured in the Boot menu will not be changed.

Save Setting to file

Select this option to save BIOS configuration settings to a USB flash device.

Restore Setting from file

This field will appear only when a USB flash device is detected. Select this field to restore setting from the USB flash device.

▶ Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility. For updating Insyde BIOS in UEFI mode, you may refer to the how-to video at https://www.dfi.com/tw/knowledge/video/5.

▶ Notice: BIOS SPI ROM

1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.

2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.

3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

Note:
a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.
b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.