

Approval Sheet

| | |
|-----------------------------|----------------------------------|
| Customer | |
| Product Number | M4US-2GSV1C0J-E |
| Module speed | PC4-2400 |
| Pin | 288 pin |
| CI-tRCD-tRP | 17-17-17 |
| SDRAM Operating Temp | 0°C~95°C |
| Date | 23rd June 2017 |

**The Total Solution For
Industrial Flash Storage**

Rev 1.0

1. Features

Key Parameter

| Industry Nomenclature | Speed Grade | Data Rate MT/s | | | tRCD (ns) | tRP (ns) | tRC (ns) |
|-----------------------|-------------|----------------|-------|-------|-----------|----------|----------|
| | | CL=13 | CL=15 | CL=17 | | | |
| PC4-2400 | S | 1866 | 2133 | 2400 | 14.16 | 14.16 | 46.16 |

- JEDEC Standard 288-pin Dual In-Line Memory Module
- Intend for PC4-2400 applications
- Inputs and Outputs are SSTL-12 compatible
- VDD=VDDQ= 1.2 Volt (TYP)
- VPP=2.5 Volt (TYP)
- VDDSPD=2.2-3.6V
- Low-Power auto self-refresh (LPASR)
- SDRAMs have 16 internal banks for concurrent operation (4 Bank Group of 4 banks each)
- Normal and Dynamic On-Die Termination for data, strobe and mask signals.
- Data bus inversion (DBI) for data bus
- Fixed burst chop (BC) of 4 and burst length (BL) of 8 via the MRS
- Selectable BC4 or BL8 on-the fly (OTF)
- Golden Connector
- Fly-By topology
- Terminated control, command and address bus
- Programmable /CAS Latency: 10,11,12,13,14,15,16,17,18
- Operation temperature – Tc (0°C ~95°C)
- On-die VREFDQ generation and Calibration
- On-Board EEPROM
- RoHS and Halogen free (*Section 13*)

2. Environmental Requirements

DDR4 UDIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning. (Followed JEDEC)

| Symbol | Parameter | Rating | Units | Notes |
|--------|---|-------------|----------|-------|
| TOPR | Operating Temperature (ambient) | 0 to +55 | °C | 1 |
| TSTG | Storage Temperature | -50 to +100 | °C | |
| HOPR | Operating Humidity (relative) | 10 to 90 | % | |
| HSTG | Storage Humidity (without condensation) | 5 to 95 | % | |
| PBAR | Barometric Pressure (operating & storage) | 105 to 69 | K Pascal | 1,2 |

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR4 DRAM component specification.
 2. Up to 9850 ft.

3. SDRAM Parameters by device density

| RTT_Nom Setting | Parameter | 4Gb | Units |
|-----------------|-----------------------------------|---------------------|--------|
| tREFI | Average periodic refresh interval | 0°C ≤ TCASE ≤ 85°C | 7.8 μs |
| | | 85°C < TCASE ≤ 95°C | 3.9 μs |

4. Ordering Information

| DDR4 UDIMM | | | | | | |
|------------------------|---------|----------|-------------------|----------------|----------------|-----|
| Part Number | Density | Speed | DIMM Organization | Number of DRAM | Number of rank | ECC |
| M4US-2GSV1C0J-E | 2GB | PC4-2400 | 256Mx64 | 4 | 1 | N |

5. Pin Configurations (Front side/Back side)

DDR4 UDIMM

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|-----|---------------------|-----|--------|-----|---------------------|-----|---------|-----|---------------------|-----|--------------|-----|---------------------|-----|--------|
| 1 | NC | 145 | NC | 37 | VSS | 181 | DQ29 | 73 | VDD | 217 | VDD | 109 | VSS | 253 | DQ41 |
| 2 | VSS | 146 | VREFCA | 38 | DQ24 | 182 | VSS | 74 | CK0_t | 218 | CK1_t | 110 | DM5_n/ DBI5_n,NC | 254 | VSS |
| 3 | DQ4 | 147 | VSS | 39 | VSS | 183 | DQ25 | 75 | CK0_c | 219 | CK1_c | 111 | NC | 255 | DQS5_c |
| 4 | VSS | 148 | DQ5 | 40 | DM3_n/ DBI3_n,NC | 184 | VSS | 76 | VDD | 220 | VDD | 112 | VSS | 256 | DQS5_t |
| 5 | DQ0 | 149 | VSS | 41 | NC | 185 | DQS3_c | 77 | VTT | 221 | VTT | 113 | DQ46 | 257 | VSS |
| 6 | VSS | 150 | DQ1 | 42 | VSS | 186 | DQS3_t | 78 | EVENT_n,NF | 222 | PARITY | 114 | VSS | 258 | DQ47 |
| 7 | DM0_n/ DBI0_n | 151 | VSS | 43 | DQ30 | 187 | VSS | 79 | A0 | 223 | VDD | 115 | DQ42 | 259 | VSS |
| 8 | NC | 152 | DQS0_c | 44 | VSS | 188 | DQ31 | 80 | VDD | 224 | BA1 | 116 | VSS | 260 | DQ43 |
| 9 | VSS | 153 | DQS0_t | 45 | DQ26 | 189 | VSS | 81 | BA0 | 225 | A10/AP | 117 | DQ52 | 261 | VSS |
| 10 | DQ6 | 154 | VSS | 46 | VSS | 190 | DQ27 | 82 | RAS_n /A16 | 226 | VDD | 118 | VSS | 262 | DQ53 |
| 11 | VSS | 155 | DQ7 | 47 | CB4/NC | 191 | VSS | 83 | VDD | 227 | NC | 119 | DQ48 | 263 | VSS |
| 12 | DQ2 | 156 | VSS | 48 | VSS | 192 | CB5,NC | 84 | CS0_n | 228 | WE_n/ A14 | 120 | VSS | 264 | DQ49 |
| 13 | VSS | 157 | DQ3 | 49 | CB0/NC | 193 | VSS | 85 | VDD | 229 | VDD | 121 | DM6_n/ DBI6_n | 265 | VSS |
| 14 | DQ12 | 158 | VSS | 50 | VSS | 194 | CB1,NC | 86 | CAS_n/ A15 | 230 | NC | 122 | NC | 266 | DQS6_c |
| 15 | VSS | 159 | DQ13 | 51 | DM8_n/ DBI8_n,NC | 195 | VSS | 87 | ODT0 | 231 | VDD | 123 | VSS | 267 | DQS6_t |
| 16 | DQ8 | 160 | VSS | 52 | NC | 196 | DQS8_c | 88 | VDD | 232 | A13 | 124 | DQ54 | 268 | VSS |
| 17 | VSS | 161 | DQ9 | 53 | VSS | 197 | DQS8_t | 89 | CS1_n | 233 | VDD | 125 | VSS | 269 | DQ55 |
| 18 | DMI_n/ DBI1_n,NC | 162 | VSS | 54 | CB6 DBI8_n,NC | 198 | VSS | 90 | VDD | 234 | NC | 126 | DQ50 | 270 | VSS |
| 19 | NC | 163 | DQS1_c | 55 | VSS | 199 | CB7,NC | 91 | ODT1 | 235 | NC | 127 | VSS | 271 | DQ51 |
| 20 | VSS | 164 | DQS1_t | 56 | CB2/NC | 200 | VSS | 92 | VDD | 236 | VDD | 128 | DQ60 | 272 | VSS |
| 21 | DQ14 | 165 | VSS | 57 | VSS | 201 | CB3,NC | 93 | NC | 237 | NC | 129 | VSS | 273 | DQ61 |
| 22 | VSS | 166 | DQ15 | 58 | RESET_n | 202 | VSS | 94 | VSS | 238 | SA2 | 130 | DQ56 | 274 | VSS |
| 23 | DQ10 | 167 | VSS | 59 | VDD | 203 | CKE1 | 95 | DQ36 | 239 | VSS | 131 | VSS | 275 | DQ57 |
| 24 | VSS | 168 | DQ11 | 60 | CKE0 | 204 | VDD | 96 | VSS | 240 | DQ37 | 132 | DM7_n/ DBI7_n,NC | 276 | VSS |
| 25 | DQ20 | 169 | VSS | 61 | VDD | 205 | NC | 97 | DQ32 | 241 | VSS | 133 | NC | 277 | DQS7_c |
| 26 | VSS | 170 | DQ21 | 62 | ACT_n | 206 | VDD | 98 | VSS | 242 | DQ33 | 134 | VSS | 278 | DQS7_t |
| 27 | DQ16 | 171 | VSS | 63 | BG0 | 207 | BG1 | 99 | DM4_n/ DBI4_n,NC | 243 | VSS | 135 | DQ62 | 279 | VSS |
| 28 | VSS | 172 | DQ17 | 64 | VDD | 208 | ALERT_n | 100 | NC | 244 | DQS4_c | 136 | VSS | 280 | DQ63 |
| 29 | DM2_n/ DBI2_n,NC | 173 | VSS | 65 | A12/BC_n | 209 | VDD | 101 | VSS | 245 | DQS4_t | 137 | DQ58 | 281 | VSS |
| 30 | NC | 174 | DQS2_c | 66 | A9 | 210 | A11 | 102 | DQ38 | 246 | VSS | 138 | VSS | 282 | DQ59 |
| 31 | VSS | 175 | DQS2_t | 67 | VDD | 211 | A7 | 103 | VSS | 247 | DQ39 | 139 | SA0 | 283 | VSS |
| 32 | DQ22 | 176 | VSS | 68 | A8 | 212 | VDD | 104 | DQ34 | 248 | VSS | 140 | SA1 | 284 | VSSSPD |
| 33 | VSS | 177 | DQ23 | 69 | A6 | 213 | A5 | 105 | VSS | 249 | DQ35 | 141 | SCL | 285 | SDA |
| 34 | DQ18 | 178 | VSS | 70 | VDD | 214 | A4 | 106 | DQ44 | 250 | VSS | 142 | VPP | 286 | VPP |
| 35 | VSS | 179 | DQ19 | 71 | A3 | 215 | VDD | 107 | VSS | 251 | DQ45 | 143 | VPP | 287 | VPP |
| 36 | DQ28 | 180 | VSS | 72 | A1 | 216 | A2 | 108 | DQ40 | 252 | VSS | 144 | NC | 288 | VPP |

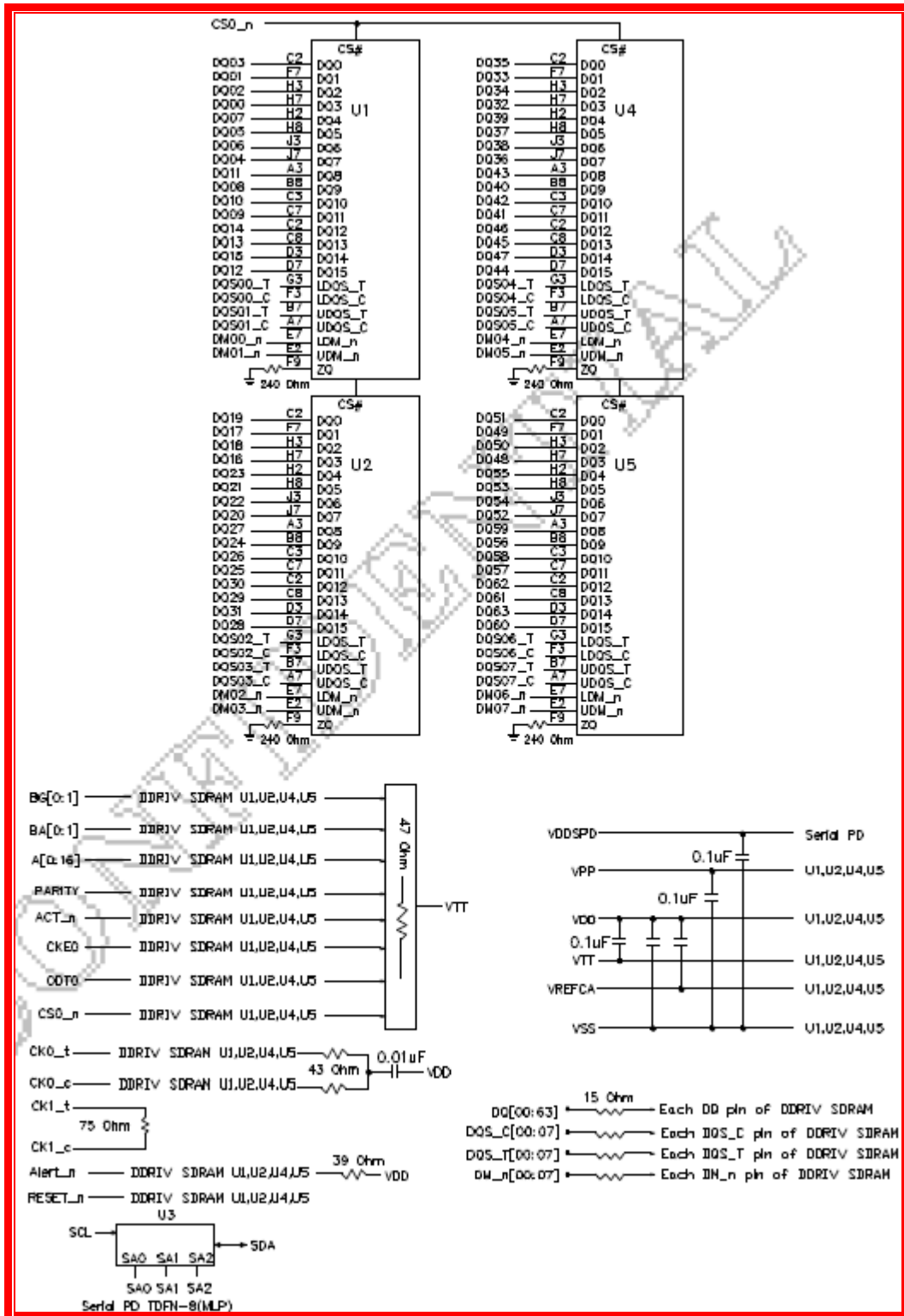
Notes:
1. NC = No Connect, RFU = Reserved for Future Use
2. Address A17 is only valid for 16 Gb x4 based SDRAMs.
3. RAS_n is a multiplexed function with A16.
4. CAS_n is a multiplexed function with A15.
5. WE_n is a multiplexed function with A14.
6. CBx is for ECC UDIMM only

6. Architecture

Pin Definition

| Pin Name | Description | Pin Name | Description |
|--|-------------------------------|---|--|
| Ax | SDRAM address bus | SCL | Serial Clock for temperature sensor/SPD EEPROM |
| A10/AP | Auto-Precharge | DQx, CBx | Data input/output and check bit input/output: |
| A12/BC _n | Burst Chop | DM _n / DBI _n /TDQS _t (DMU _n , DBIU _n), (DML _n /DBII _n) | Input data mask and data bus inversion: |
| ACT _n | Command Input | SDA | Serial Data |
| BAx | Bank Address Inputs | DQS _t DQS _c DQSU _t DQSU _c DQSL _t DQSL _c | Data strobe: |
| BGx | Bank Group Address Inputs | ALERT _n | Alert output |
| C0, C1, C2 (RDIMM or LRDIMM only) | Chip ID | EVENT _n | Temperature event |
| CK _{x_t} CK _{x_c} | Clock | TDQS _t , TDQS _c (x8 DRAM-based RDIMM only) | Termination data strobe: |
| CKEx | Clock enable | VDD | Module power supply: 1.20V (TYP) |
| CS _{x_n} | Chip Select | VPP | DRAM activating power supply: 2.5V – 0.125V / +0.250V |
| ODTx | On-Die Termination | VREFCA | Reference voltage for control, command, and address pins |
| Parity | Parity of Command and Address | VSS | Ground |
| RAS _n /A16 CAS _n /A15 WE _n /A14 | Command Input | VTT | Power supply for termination of address, command, and control VDD/2. |
| RESET _n | Active LOW asynchronous reset | VDDSPD | Power supply used to power the I2C bus for SPD. |
| SAx | Serial address Input | RFU | Reserved for future use. |
| NF | No function | NC | No Connect |

7. Function Block Diagram:
 - (2GB, 1 Rank 256Mx16 DDR4 SDRAMs)



Note: 1. The ZQ ball on each DDR4 component is connected to an external 240Ω ±1% resistor that is tied to ground. It is used for the calibration of the component's ODT and output driver.

8. SDRAM Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units | Note | |
|------------------------------------|--|--------------------------|----------|------|-----|
| T _{OPER} | Operation Temperature | Normal Operating Temp. | 0 to 85 | °C | 1,2 |
| | | Extended Temp.(optional) | 85 to 95 | °C | 1,3 |
| T _{STG} | Storage Temperature | -55 to 100 | °C | 4,5 | |
| V _{IN} , V _{OUT} | Voltage on any pins relative to V _{SS} | -0.3 to +1.5 | V | 4 | |
| V _{DD} | Voltage on VDD supply relative to V _{SS} | -0.3 to +1.5 | V | 4,6 | |
| V _{DDQ} | Voltage on VDDQ supply relative to V _{SS} | -0.3 to +1.5 | V | 4,6 | |

Note:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM.

For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stressing only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. Module Absolute Maximum Ratings

| Symbol | Parameter | Rating | Units | Notes |
|-------------------|--|--------------|-------|-------|
| V_{IN}, V_{OUT} | Voltage on I/O pins relative to Vss | -0.3 to +1.5 | V | |
| V_{DD} | Voltage on VDD supply relative to Vss | -0.3 to +1.5 | V | 1 |
| V_{DDQ} | Voltage on VDDQ supply relative to Vss | -0.3 to +1.5 | V | 1 |
| V_{PP} | Voltage on VPP supply relative to Vss | -0.3 to +3.0 | V | 2 |

Note:

- VDDQ tracks with VDD; VDDQ and VDD are tied together.
- VPP must be greater than or equal to VDD at all times.

10. Operating Condition

| Symbol | Parameter | Min | Nom | Max | Units | Notes |
|------------|--|--------------|-----------|------------|-------|-------|
| VDD | Supply Voltage | 1.14 | 1.2 | 1.26 | V | 1 |
| VPP | DRAM activating power supply | 2.375 | 2.5 | 2.75 | V | 2 |
| VREFCA(DC) | Input reference voltage command/ address bus | 0.49 x VDD | 0.5 x VDD | 0.51 x VDD | V | 3 |
| IVTT | Termination reference voltage (DC) – command/address bus | -750 | - | 750 | mA | |
| VTT | Termination Voltage | 0.49 x VDD | 0.5 x VDD | 0.51 x VDD | V | 4 |
| II | Input leakage current; any input excluding ZQ; 0V < VIN < 1.1V | -2.0 | - | 2.0 | μA | 5 |
| II/O | DQ leakage; 0V < Vin < VDD | -4.0 | - | 4.0 | μA | 5 |
| Iozpd | Output leakage current; VOUT = VDD; DQ is disabled | - | - | 5.0 | μA | 5,6 |
| Iozpu | Output leakage current; VOUT =VSS; DQ and ODT are disabled; ODT is disabled with ODT input HIGH | VREF + 0.125 | - | VDDQ + 0.3 | μA | 1 |
| Iozpd | VREFCA leakage; VREFCA = VDD/2 (after DRAM is initialized) | -2.0 | - | 2.0 | μA | 5 |

Note:

- VDDQ tracks with VDD; VDDQ and VDD are tied together.
- VPP must be greater than or equal to VDD at all times.
- VREFCA must not be greater than 0.6 x VDD. When VDD is less than 500mV, VREF may be less than or equal to 300mV.
- VTT termination voltages in excess of the specification limit adversely affect the voltage margins of command and address signals and reduce timing margins.
- Multiply by the number of DRAM die on the module.
- Tied to ground. Not connected to edge connector.

11. Operating, Standby, and Refresh Currents

- 2GB UDIMM (1 Rank 265Mx16 DDR4 SDRAMs)

| Symbol | Proposed Conditions | Value | | Units |
|--------|---|----------|----------|-------|
| | | IDD Max. | IPP Max. | |
| IDD0 | Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern | 140 | 16 | mA |
| IDD0A | Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0 | 148 | 16 | mA |
| IDD1 | Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern | 212 | 16 | mA |
| IDD1A | Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1 | 224 | 16 | mA |
| IDD2N | Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern | 60 | 12 | mA |
| IDD2NA | Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N | 72 | 12 | mA |

| | | | | |
|-----------|---|-----|----|----|
| IDD2NT | Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern | 64 | 12 | mA |
| IDD2NL | Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3 | 44 | 12 | mA |
| IDD2NG | Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3 | 60 | 12 | mA |
| IDD2ND | Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3 | 48 | 12 | mA |
| IDD2N_par | Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3 | 60 | 12 | mA |
| IDD2P | Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0 | 40 | 12 | mA |
| IDD2Q | Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0 | 52 | 12 | mA |
| IDD3N | Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern | 108 | 12 | mA |

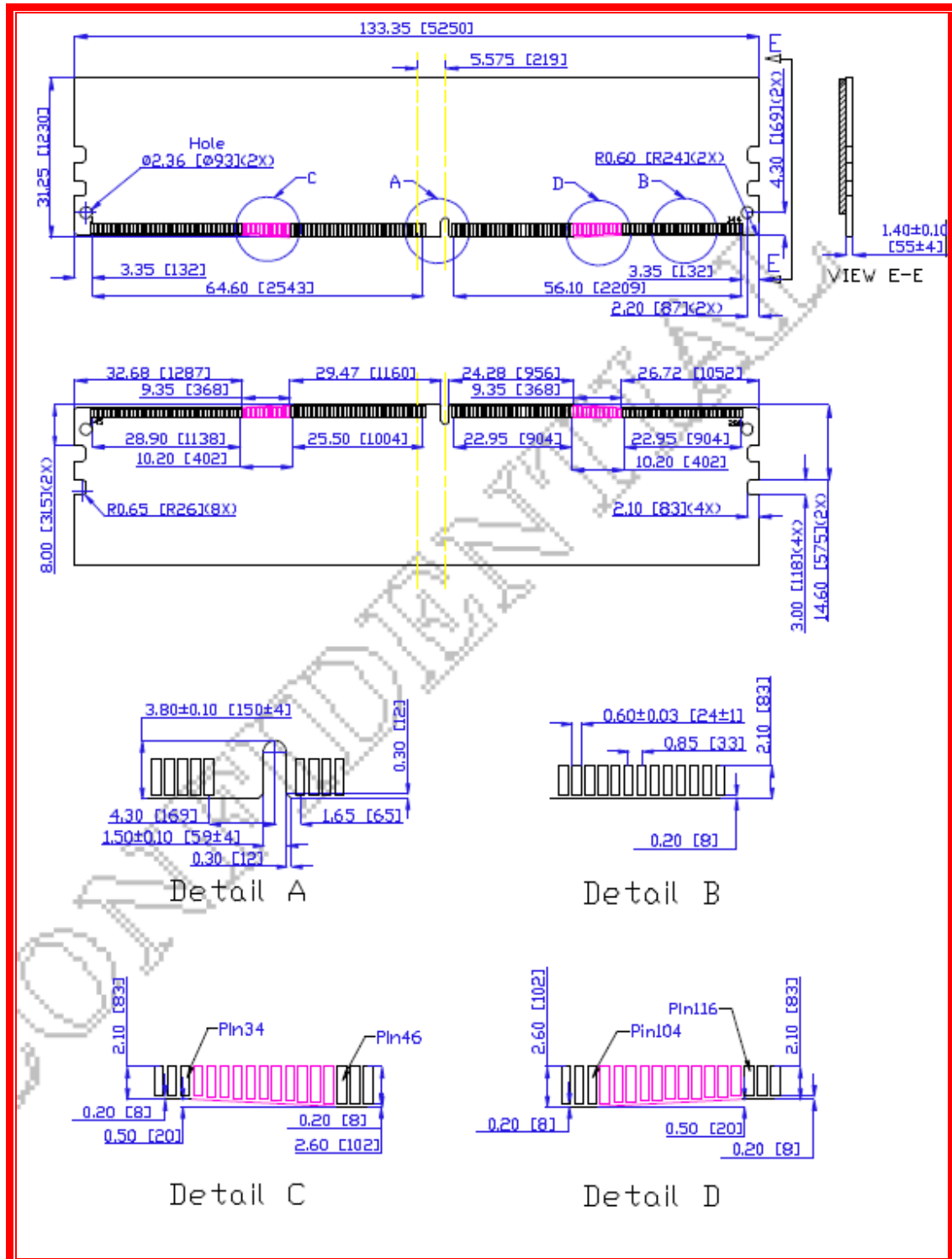
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|--------|---|-----|----|----|
| IDD3NA | Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N | 112 | 12 | mA |
| IDD3P | Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0 | 52 | 12 | mA |
| IDD4R | Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern | 516 | 12 | mA |
| IDD4RA | Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R | 532 | 12 | mA |
| IDD4RB | Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R | 532 | 12 | mA |
| IDD4W | Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern | 344 | 12 | mA |
| IDD4WA | Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W | 400 | 12 | mA |
| IDD4WB | Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W | 384 | 12 | mA |

| | | | | |
|-----------|---|-----|----|----|
| IDD4WC | Operating Burst Write Current with Write CRC Write CRC enabled ³ , Other conditions: see IDD4W | 332 | 12 | mA |
| IDD4W_par | Operating Burst Write Current with CA Parity CA Parity enabled ³ , Other conditions: see IDD4W | 412 | 12 | mA |
| IDD5B | Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern | 780 | 76 | mA |
| IDD5F2 | Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B | 640 | 64 | mA |
| IDD5F4 | Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B | 480 | 48 | mA |
| IDD6N | Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MIDDLELEVEL | 52 | 16 | mA |
| IDD6E | Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended ⁴ ; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers ² ; ODT Signal: MID-LEVEL | 80 | 16 | mA |

| | | | | |
|--------------|---|------------|-----------|-----------|
| <p>IDD6R</p> | <p>Self-Refresh Current: Reduced Temperature Range TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL</p> | <p>40</p> | <p>16</p> | <p>mA</p> |
| <p>IDD6A</p> | <p>Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL</p> | <p>52</p> | <p>16</p> | <p>mA</p> |
| <p>IDD7</p> | <p>Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern</p> | <p>744</p> | <p>48</p> | <p>mA</p> |
| <p>IDD8</p> | <p>Maximum Power Down Current TBD</p> | <p>26</p> | <p>8</p> | <p>mA</p> |

12. PACKAGE DIMENSION

- (2GB, 1 Rank 256x16 DDR4 base UDIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ± 0.15 (6), unless otherwise specified.

13. RoHS Declaration

| | | |
|--|------------------------------------|----------|
| innodisk | 宜鼎國際股份有限公司 Innodisk Corporation | Page 1/1 |
| Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/ | | |
| RoHS 自我宣告書 (RoHS Declaration of Conformity) | | |
| Manufacturer Product: All Innodisk EM Flash and Dram products | | |
| 一、宜鼎國際股份有限公司 (以下稱本公司) 特此保證售予貴公司之所有產品, 皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。 | | |
| Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement. | | |
| 二、本公司同意因本保證書或與本保證書相關事宜有所爭議時, 雙方宜友好協商, 達成協議。 | | |
| Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations. | | |
| Name of hazardous substance | Limited of RoHS ppm (mg/kg) | |
| 鉛 (Pb) | < 1000 ppm | |
| 汞 (Hg) | < 1000 ppm | |
| 鎘 (Cd) | < 100 ppm | |
| 六價鉻 (Cr 6+) | < 1000 ppm | |
| 多溴聯苯 (PBBs) | < 1000 ppm | |
| 多溴二苯醚 (PBDEs) | < 1000 ppm | |
| 立 保 證 書 人 (Guarantor) | | |
| Company name 公司名稱: <u>Innodisk Corporation 宜鼎國際股份有限公司</u> | | |
| Company Representative 公司代表人: <u>Randy Chien 顏川騰</u> | | |
| Company Representative Title 公司代表人職稱: <u>Chairman 董事長</u> | | |
| Date 日期: <u>2016 / 08 / 04</u> | | |
|  | | |

Revision Log

| Rev | Date | Modification |
|-----|----------------------------|---------------------|
| 0.1 | 23 rd June 2017 | Preliminary Edition |
| 1.0 | 23 rd June 2017 | Official Released |