Approval Sheet

Customer	
Product Number	**M1SF-56MB3CDB-J**
Module speed	**PC-2700**
Pin	**200 pin**
CAS Latency	**CL-2.5**
SDRAM Operating Temp	**0 ℃ ~ 70 ℃**
Date	**14 June 2016**

Approval by Customer

P/N:

Signature:

Date:

Sales:_____ **Sr. Mkt. Manager: John Hsieh**

Rev 1.1

The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=2	CL=2.5	CL=3			
PC-2700	D	266	333	333	15	15	55

- JEDEC Standard 200-pin Dual In-Line Memory Module
- Intend for 333 MHz applications
- Inputs and Outputs are SSTL-2 compatible
- VDD=VDDQ= 2.5 Volt ± 0.2 (PC-2700)
- Differential clock input
- DLL aligns DQ and DQS transition with CK transition
- Bi-Directional data strobe with one clock cycle
- Auto Refresh (CBR) and Self-Refresh Modes support.
- Serial Presence Detect with EEPROM
- Auto & self-refresh 7.8µs ($T_C \leq +70°C$)
- SDRAM Operation Temperature
  - $0°C \leq T_C \leq +70°C$
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 2, 2.5, 3
  - Burst Length: 2, 4 or 8
- RoHS Compliant *(section 13)*

2. SDRAM Environmental Requirements

iDIMM's SDRAM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (case)	0 to +70	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	1

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.

3. Ordering Information

DDR SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M1SF-56MB3CDB-J	256MB	PC-2700	32M x64	4	1	N/A

4. Pin Configurations (Front side/Back side)

Pin	Front	Pin	Front	Pin	Front	Pin	Back	Pin	Back	Pin	Back
1	VREF	67	DQ27	135	DQ34	2	VREF	68	DQ31	136	DQ38
3	VSS	69	VDD	137	VSS	4	VSS	70	VDD	138	VSS
5	DQ0	71	*CB0	139	DQ35	6	DQ4	72	*CB4	140	DQ39
7	DQ1	73	*CB1	141	DQ40	8	DQ5	74	*CB5	142	DQ44
9	VDD	75	VSS	143	VDD	10	VDD	76	VSS	144	VDD
11	DQS0	77	*DQS8	145	DQ41	12	DM0	78	*DM8	146	DQ45
13	DQ2	79	*CB2	147	DQS5	14	DQ6	80	*CB6	148	DM5
15	VSS	81	VDD	149	VSS	16	VSS	82	VDD	150	VSS
17	DQ3	83	*CB3	151	DQ42	18	DQ7	84	*CB7	152	DQ46
19	DQ8	85	DU	153	DQ43	20	DQ12	86	DU	154	DQ47
21	VDD	87	VSS	155	VDD	22	VDD	88	VSS	156	VDD
23	DQ9	89	*CK2	157	VDD	24	DQ13	90	VSS	158	/CK1
25	DQS1	91	*/CK2	159	VSS	26	DM1	92	VDD	160	CK1
27	VSS	93	VDD	161	VSS	28	VSS	94	VDD	162	VSS
29	DQ10	95	*CKE1	163	DQ48	30	DQ14	96	CKE0	164	DQ52
31	DQ11	97	DU	165	DQ49	32	DQ15	98	DU	166	DQ53
33	VDD	99	A12	167	VDD	34	VDD	100	A11	168	VDD
35	CK0	101	A9	169	DQS6	36	VDD	102	A8	170	DM6
37	/CK0	103	VSS	171	DQ50	38	VSS	104	VSS	172	DQ54
39	VSS	105	A7	173	VSS	40	VSS	106	A6	174	VSS
KEY		107	A5	175	DQ51	KEY		108	A4	176	DQ55
41	DQ16	109	A3	177	DQ56	42	DQ20	110	A2	178	DQ60
43	DQ17	111	A1	179	VDD	44	DQ21	112	A0	180	VDD
45	VDD	113	VDD	181	DQ57	46	VDD	114	VDD	182	DQ61
47	DQS2	115	A10/AP	183	DQS7	48	DM2	116	BA1	184	DM7
49	DQ18	117	BA0	185	VSS	50	DQ22	118	/RAS	186	VSS
51	VSS	119	/WE	187	DQ58	52	VSS	120	/CAS	188	DQ62
53	DQ19	121	/S0	189	DQ59	54	DQ23	122	*/S1	190	DQ63
55	DQ24	123	DU	191	VDD	56	DQ28	124	DU	192	VDD
57	VDD	125	VSS	193	SDA	58	VDD	126	VSS	194	SA0
59	DQ25	127	DQ32	195	SCL	60	DQ29	128	DQ36	196	SA1
61	DQS3	129	DQ33	197	VDDSPD	62	DM3	130	DQ37	198	SA2
63	VSS	131	VDD	199	*VDDID	64	VSS	132	VDD	200	DU
65	DQ26	133	DQS4			66	DQ30	134	DM4		

Note: *=Not Use ; DU=Don't Use

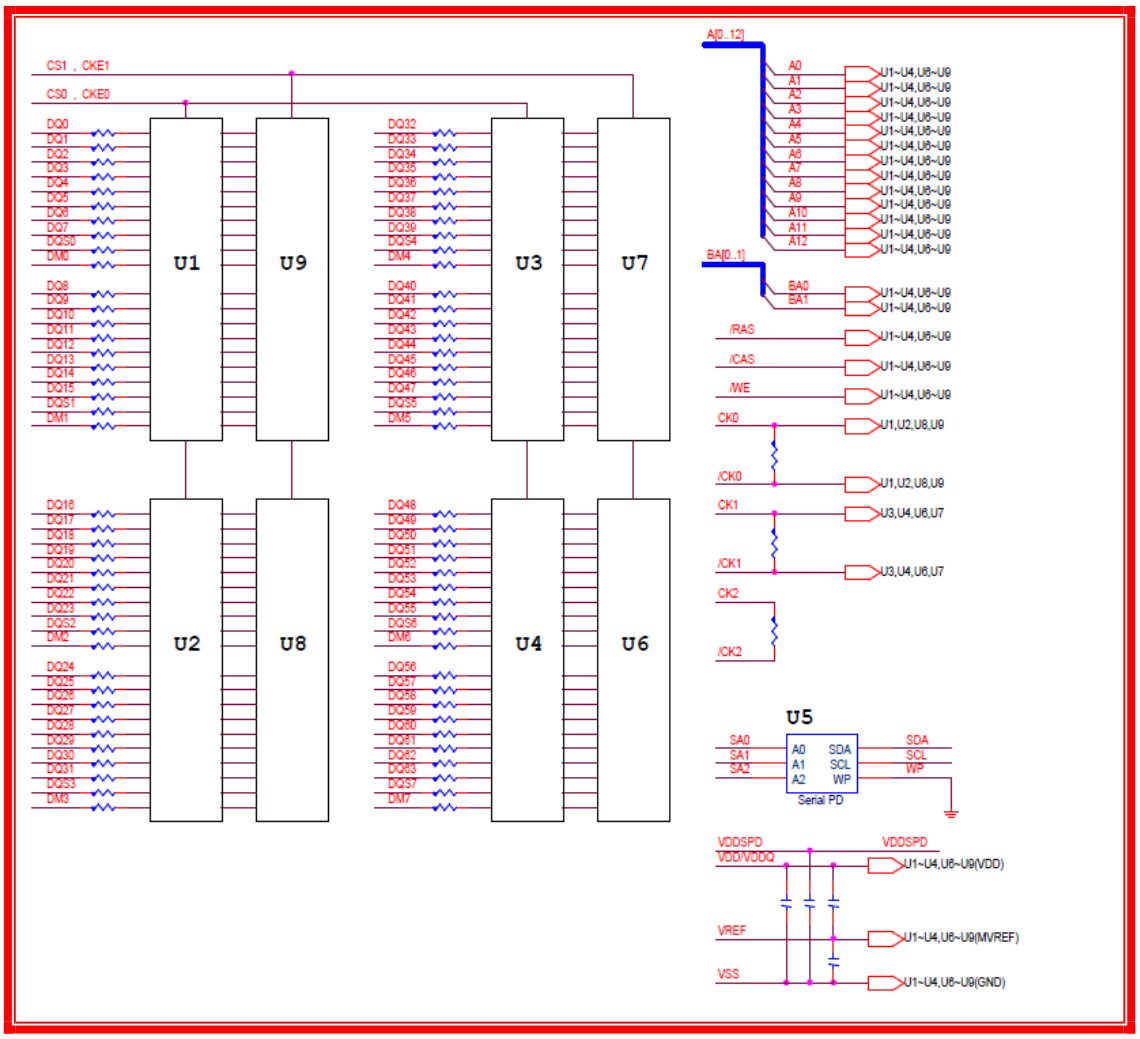
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	CK0 – CK1 CK0# - CK1#	Differential SDRAM Clocks
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS#	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS#	SDRAM column address strobe	SA0 – SA1	Serial Presence Detect Address Inputs
WE#	SDRAM write enable	V_{DD}	Power Supply
S0# - S1#	DIMM Rank Select Lines	V_{DDID}	V_{DD} Identification Flag
CK0 – CKE1	SDRAM clock enable lines	V_{DDQ}	SDRAM I/O Driver power supply
DQ0 – DQ63	DIMM memory data bus	V_{REF}	SDRAM I/O Reference supply
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS17	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM7	SDRAM data masks	Reset	Reset enable
NC	Spare Pin		

6. Function Block Diagram:

- (256MB, 1 Rank 32Mx16 DDR Unbuffered DIMM)



Note:U6~U9 is for 2Rank 32M16 base DDR module

7. SDRAM Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
T_A	Operation Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 100	°C
V_{INPUT}	Voltage input pins relative to Vss	-1.0 to +3.6	V
V_{IO}	Voltage on I/O pins relative to Vss	-0.5 to +3.6	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-1.0 to +3.6	V
I_{OS}	Output short Circuit Current	50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. AC & DC Operating Conditions

- AC Operating Conditions

(T_{CASE} = 0 °C ~ 70 °C; V_{SS}=0V)

Symbol	Parameter	Value		Units	Notes
		Min	Max		
V_{IH} (AC)	Input High (Logic1) Voltage	V_{REF} + 0.31	-	V	
V_{IL} (AC)	Input Low (Logic0) Voltage	-	V_{REF} + 0.31	V	
V_{ID} (AC)	Input differential Voltage: CK, /CK	0.7	V_{DDQ} + 0.6	V	1
V_{IX} (AC)	Input crossing point Voltage: CK, /CK	0.5* V_{DDQ} + 0.2	0.5* V_{DDQ} - 0.2	V	2

Note:

1. VID is the magnitude of the difference between the input level on CK and the input on/CK.

2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

- DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 70 °C; V_{SS} = 0V)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
V_{DD}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
V_{DDQ}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
$V_{IH\ (DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	1
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage	-0.3	-	V_{REF} - 0.15	V	1
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
V_{REF}	I/O Reference Voltage	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	2
$V_{IN(DC)}$	Input Voltage Level: CK, /CK	-0.3	-	V_{DDQ} + 0.3	V	
$V_{ID(DC)}$	Input Differential Voltage: CK, /CK	0.36	-	V_{DDQ} + 0.6	V	
$V_{I(RATIO)}$	V-I Matching	0.71	-	1.4	V	

Note:

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} of transmitting device must track V_{REF} of receiving device.

9. Operating, Standby, and Refresh Currents

- 256MB SODIMM (1 Rank, 32Mx16 DDR SDRAMs T_{CASE} = 0 °C ~ 70 °C)

Symbol	Parameter/Condition	PC-2700	Unit
I_{DD0}	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	300	mA
I_{DD1}	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	340	mA
I_{DD2P}	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	20	mA
I_{DD2F}	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle.VIN=VREF for DQ, DQS and DM	92	mA
I_{DD3P}	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	72	mA
I_{DD3N}	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge;tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	160	mA
I_{DD4R}	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	480	mA
I_{DD4W}	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	480	mA
I_{DD5}	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	480	mA
I_{DD6}	CKE=<0.2V; External clock on; tCK=tCK(min)	20	mA
I_{DD7}	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	920	mA

10. AC Timing Specifications

(T_{CASE} = 0 °C ~ 70 °C; V_{DDQ} = V_{DD}, See AC Characteristics)

Symbol	Parameter	PC2-2700		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.7	0.7	ns
tDQSCK	DQS output access time from CK/CK#	-0.60	0.60	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	Min (tCL,tCH)	-	ns
tCK	Clock Cycle Time	6	12	ns
tDS	DQ and DM input setup time(differential data strobe)	0.45	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.45	-	ns
tIPW	Input pulse width	2.2	-	ns
tDIPW	DQ and DM input pulse width (each input)	1.75	-	ns
tHZ	Data-out high-impedance time from CK/CK	-	0.7	ns
tLZ(DQS)	DQS low-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQ)	DQ low-impedance time from CK/CK	-0.7	0.7	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.45	ns
tQHS	Data hold Skew Factor	-	0.55	ns
tQH	Data output hold time from DQS	tHP -tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	0.75	1.25	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.35	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.4	-	tCK
tMRD	Mode register set command cycle time	2	-	tCK
tWPST	Write postamble	0.4	0.6	tCK
tWPRE	Write preamble	0.25	0.25	tCK
tIH	Address and control input hold time	0.75	-	ns

tIS	Address and control input setup time	0.75	-	ns
tRPRE	Read preamble	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	tCK
tRRD	Active bank A to Active bank B command	12	-	ns
tREFI	Average Periodic Refresh Interval ($85^oC < T_{CASE} \leq 95^oC$)	-	3.9	µs
	Average Periodic Refresh Interval ($0^oC \leq T_{CASE} \leq 85^oC$)	-	7.8	µs
tWR	Write recovery time without Auto-Precharge	15		ns
tDAL	Auto precharge write recovery + precharge time	-	-	tCK
tWTR	Internal write to read command delay	1	-	ns
tXSNR	Exit self refresh to a Non-read command	75	-	ns
tXSRD	Exit self refresh to a Read command	200	-	tCK

11. SPD

Serial Presence Detect – (256MB)

32Mx64 1 RANK UNBUFFERED DDR SDRAM DIMM based on 32Mx16, 4Banks, 8K Refresh, 2.6V DDR SDRAMs with SPD

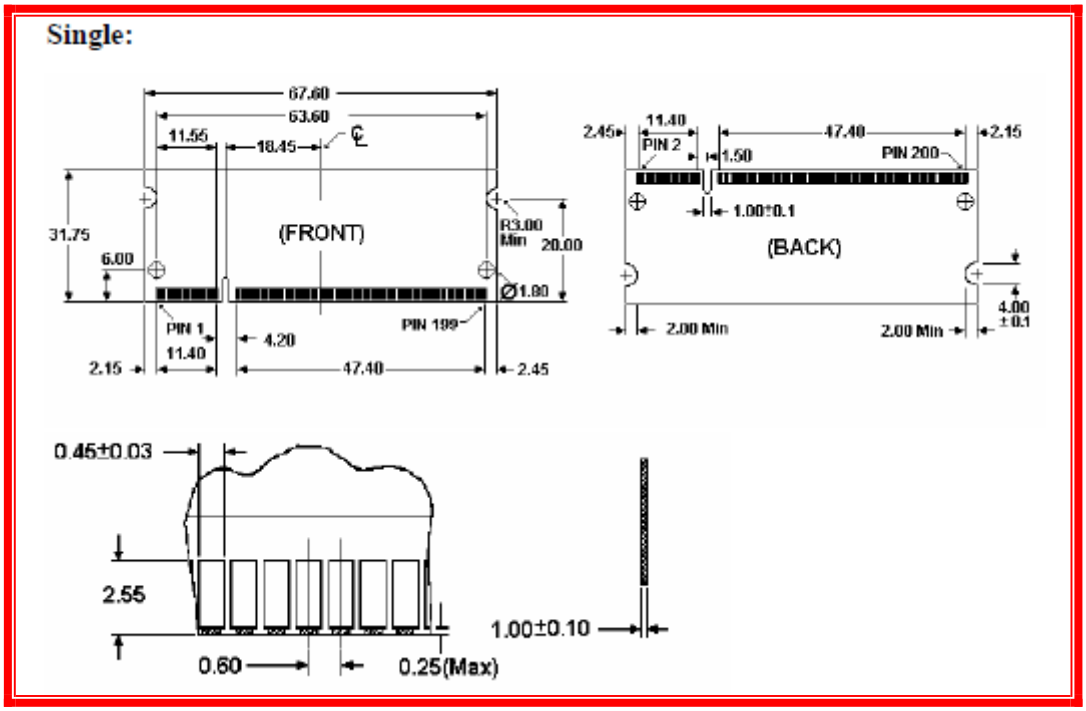
Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
		M1SF-56MB3CDB-J	
0	Number of Serial PD Bytes Written during Production	80	
1	Total Number of Bytes in Serial PD device	08	
2	Fundamental Memory Type	07	
3	Number of Row Addresses on Assembly	0D	
4	Number of Column Addresses on Assembly	0A	
5	Number of module ranks	01	
6	Module data width	40	
7	Module data width (continued)	00	
8	Voltage Interface Level of this Assembly	04	
9	DDR SDRAM Cycle Time	60	
10	DDR2 SDRAM Access Time from Clock	70	
11	Module error correction configuration type	00	
12	Refresh Rate/Type	82	
13	DDR SDRAM Width	10	
14	Error Checking Width	00	
15	Minimum clock delay for back to back random colun Addreses	01	
16	Burst Length Supported	0E	
17	Number of banks internal to discrete SDRAM Device	04	
18	CAS latencies supported	0C	
19	CS latency	01	
20	WE latency	02	
21	DDR SDRAM Module Attributes:	20	
22	DDR2 SDRAM Device Attributes: General	C0	
23	DDR SDRAM cycle time(tCK)	75	
24	DDR SDRAM access from tAC	70	

25	DDR SDRAM cycle time (tCK)	00	
26	DDR ADRAM access from clock (tAC)	00	
27	Minimum Row Precharge Time	48	
28	Minimum Row Active to Row Active delay	30	
29	Minimum RAS to CAS delay	48	
30	Minimum RAS Pulse Width	2A	
31	Module Bank Density	40	
32	Address and Command \Setup time before clock	75	
33	Address and Command Hold Time After Clock	75	
34	Data signal input setup	45	
35	Data signal input setup	45	
36-40	Reserved	00	
41	Device minimum active/auto-refresh time	3C	
42	Device minimum active/auto-refresh to active/auto refresh command period	48	
43	Device maximum device cycle time	30	
44	Device DQS-DQ skew for DQS and associated DQ signals	2D	
45	Device read data hold skew factor	55	
46	Reserved	00	
47	DIMM height	00	
48-61	Reserved	00	
62	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	00	

63	Checksum for byte 0-62	19	
64-71	Manufacture's JEDEC ID Code	7F 7F 7F 7F 7F 7F F1 FF	
72	Module Manufacturing Location	02	
73-90	Module Part number	69 2D 44 49 4D 4D	
91	PCB IDENTIFICATION CODE	00	
92	PCB IDENTIFICAION CODE(CONTINUED)	00	
93	YEAR OF MANUFACTURE		
94	WEEK OF MANUFACTURE		
95-98	MODULE SERIAL NUMBER		
92-127	MNAUFACTURER SPECIFIC DATA		
128-255	UNUSED		

12. PACKAGE DIMENSION

- (256MB, 1 Rank, 32Mx16 DDR SDRAMs)



Note: Device position is only for reference.

13. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI (Cr+6)	< 1000 ppm
Polybromodiphenyl ether (PBDE)	< 1000 ppm
Polybrominated Biphenyls (PBB)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Richard Lee 李鐘亮

Company Representative Title 公司代表人職稱： CEO 執行長

Date 日期： 2014 / 07 / 29

(Company Stamp/公司大小章)

Revision Log

Re	Date	Modificatio
0.1	27 May 2011	Preliminary Edition
1.0	25 August 2011	Official Released.
1.1	14 June 2016	Added RoHS declaration and SPD table.