ASB200-919

Fanless System with 3.5” Disk-Size SBC System

User’s Manual

Version 1.0a
(February 2022)

iBASE

Compliance

CE

This product has passed CE tests for environmental specifications and limits. This product is in accordance with the directives of the Union European (EU). If users modify and/or install other devices in this equipment, the CE conformity declaration may no longer apply.

FC

This product has been tested and found to comply with the limits for a Class B device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer's instructions, may cause harmful interference to radio communications.

WEEE

This product must not be disposed of as normal household waste, in accordance with the EU directive of for waste electrical and electronic equipment (WEEE - 2012/19/EU). Instead, it should be disposed of by returning it to a municipal recycling collection point. Check local regulations for disposal of electronic products.

Green IBASE

This product is compliant with the current RoHS restrictions and prohibits use of the following substances in concentrations exceeding 0.1% by weight (1000 ppm) except for cadmium, limited to 0.01% by weight (100 ppm).

- Lead (Pb)
- Mercury (Hg)
- Cadmium (Cd)
- Hexavalent chromium (Cr6+)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ether (PBDE)

Important Safety Information

Carefully read the precautions before using the device.

Environmental conditions:

- Lay the device horizontally on a stable and solid surface in case the device may fall, causing serious damage.
- Leave plenty of space around the device and do not block the openings for ventilation. NEVER DROP OR INSERT ANY OBJECTS OF ANY KIND INTO THE VENTIILATION OPENINGS.
- Slots and openings on the chassis are for ventilation. Do not block or cover these openings. Make sure you leave plenty of space around the device for ventilation. NEVER INSERT OBJECTS OF ANY KIND INTO THE VENTILATION OPENINGS.
- Use this product in environments with ambient temperatures -20˚C ~ 60˚C for SSD, and 0˚C ~ 45˚C for HDD.
- DO NOT LEAVE THIS DEVICE IN AN ENVIRONMENT WHERE THE STORAGE TEMPERATURE MAY GO BELOW -20˚C OR ABOVE 80˚C. This could damage the device. The device must be used in a controlled environment.

Care for your IBASE products:

- Before cleaning the device, turn it off and unplug all cables such as power in case a small amount of electrical current may still flow.
- Use neutral cleaning agents or diluted alcohol to clean the device chassis with a cloth. Then wipe the chassis with a dry cloth.
- Vacuum the dust with a computer vacuum cleaner to prevent the air vent or slots from being clogged.

WARNING

Attention during use:

- Do not place heavy objects on the top of the device.
- Operate this device from the type of power indicated on the marking label. If you are not sure of the type of power available, consult your distributor or local power company.
- Do not walk on the power cord or allow anything to rest on it.
- If you use an extension cord, make sure that the total ampere rating of the product plugged into the extension cord does not exceed its limits.

Avoid Disassembly

Do not disassemble, repair or make any modification to the device. Disassembly, modification, or any attempt at repair could generate hazards and cause damage to the device, even bodily injury or property damage, and will void any warranty.

CAUTION

Danger of explosion if internal lithium-ion battery is replaced by an incorrect type. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions.

Warranty Policy

- **IBASE standard products:**

  IBASE offers a 24-month (2-year) warranty from the date of shipment. If the date of shipment cannot be ascertained, the product serial numbers can be used to determine the approximate shipping date.

- **3rd-party parts:**

  12-month (1-year) warranty from delivery for the 3rd-party parts that are not manufactured by IBASE, such as CPU, memory, HDD, power adapter, panel and touchscreen.

* PRODUCTS, HOWEVER, THAT FAILS DUE TO MISUSE, ACCIDENT, IMPROPER INSTALLATION OR UNAUTHORIZED REPAIR SHALL BE TREATED AS OUT OF WARRANTY AND CUSTOMERS SHALL BE BILLED FOR REPAIR AND SHIPPING CHARGES.

Technical Support & Services

1. Visit the IBASE website at www.ibase.com.tw to find the latest information about the product.
2. If you need any further assistance from your distributor or sales representative, prepare the following information of your product and elaborate upon the problem.
   - Product model name
   - Product serial number
   - Detailed description of the problem
   - The error messages in text or in screenshots if there is any
   - The arrangement of the peripherals
   - Software in use (such as OS and application software, including the version numbers)
3. If repair service is required, you can download the RMA form at http://www.ibase.com.tw/english/Supports/RMAService/. Fill out the form and contact your distributor or sales representative.

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Chapter 1
General Information

The information provided in this chapter includes:

- Features
- Packing List
- Optional Accessories
- Specifications
- Product View
- Dimensions

1.1 Introduction

The ASB200-919 is mini embedded system based on the Intel® 8th Gen. Core™ and Celeron processors and the IBASE IB919 series 3.5” disk-size SBC that supports two DDR4 memory slots with a capacity of 32GB. The compact and fanless design makes it suitable for smart retail, transportation, healthcare, and smart factory applications even in large field deployments. It is equipped with two DisplayPort (DP & Type C), two Gigabit LAN ports, and two M.2 slots (M2280 & E2230) for NVMe drives and CNVi wireless connectivity.

1.2 Features

- Fanless system with IBASE 3.5” disk-size SBC
- Onboard Intel® 8th Gen. Core™ i7/i5/i3 U-series processor
- 2 x DisplayPort (1 x USB Type C (USB 3.1) / DP)
- 2 x RJ-45 GbE
- 4 x USB 3.1 ports
- 1 x DB9 (COM #1 for RS232/422/485 jumperless select)
- Input DC Voltage: +12~ +24V

1.3 Packing List

Your product package should include the items listed below. If any of the items below is missing, contact the distributor or the dealer from whom you purchased the product.

- ASB200-919 x 1
- 3-pin Terminal Block (for power) x 1
- 10-pin Terminal Block (for GPIO connector) x 1
- Side Brackets x 1
- Screws for Side Brackets x 4
- Screws for M key and E key M.2 x 2
- Power Adaptor and Power Cord x 1

1.4 Optional Accessories

- WiFi / Bluetooth Module Kit

1.5 Specifications

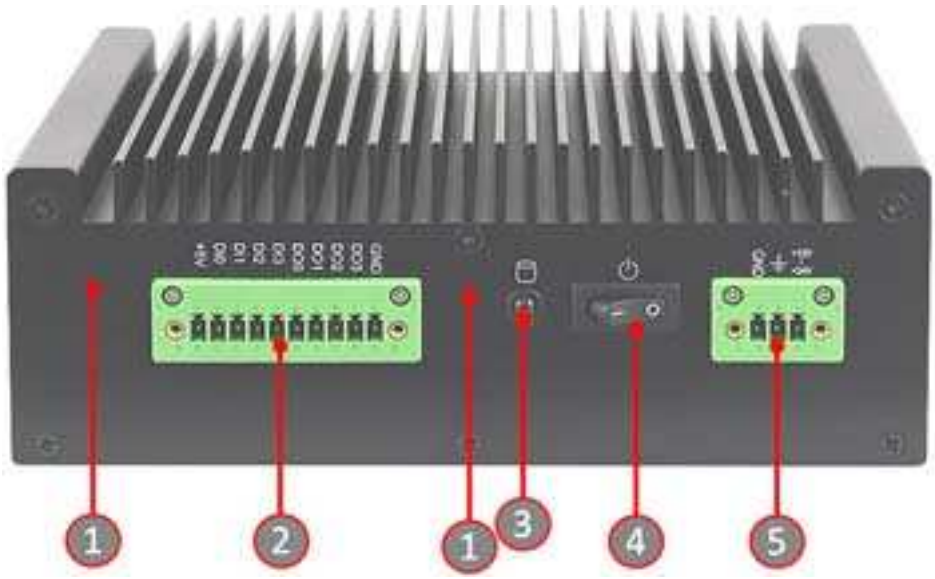
Product Name	ASB200-919-i7	ASB200-919-i5	ASB200-919-i3	ASB200-919-CEL
Motherboard	IB919AF-8665	IB919AF-8365	IB919F-8145	IB919F-4305
System				
Operating System	• Windows 10 • Linux Ubuntu / Fedora			
CPU	Intel® 8th Gen. Core™ i7-8665U	Intel® 8th Gen. Core™ i5-8365U	Intel® 8th Gen. Core™ i3-8145U	Intel® 8th Gen. Celeron 4305U
CPU Frequency	1.7GHz /4.4GHz	1.6GHz / 4.1GHz	2.2 GHz / 3.9 GHz	2.0 GHz
Memory	2 x DDR4-2666 SO-DIMM 8GB, expandable to 32 GB			
Storage	1 x SSD;2.5" SATA3 64G TLC (default)			
Super I/O	Fintek F81846AD-I			
Audio Codec	Realtek ALC269Q			
LAN	• Intel® I219LM & I211AT		• Intel® I219V & I211AT	
Power Supply	90W power adaptor			
BIOS	AMI BIOS			
Watchdog	Watchdog Timer 256 segments, 0, 1, 2…255 sec/min			
Chassis	Aluminum & steel, black			
Mounting	• Desktop mount • Wall mount • VESA mount (Optional)			
Dimensions (W x H x D)	180 x 66 x 150 mm (7.09” x 2.6” x 5.9”)			
Weight	1.8 kg (3.97 lb)			
Certificate	CE / LVD / FCC Class B			
I/O Ports				
Front I/O	1 x 3-pin terminal block connector for external digital I/O			
Rear I/O	• 2 x Antenna holes for WiFi • 1 x DB9 for COM#1 (RS232/422/485) • 2 x DisplayPort (1 x USB Type C x 1 for USB 3.1 / DP) • 2 x RJ-45 GbE • 4 x USB 3.1 ports			
TPM 2.0	Infineon SLB9670VQ			
Expansion	• M.2 @ 2230 (E-key) x 1 for CNVi • M.2 @ 2280 (M-key) x 1 for NVMe			

Environment	
Temperature	• **Operating:** 0 ~ 45 °C (32 ~ 113 °F) • **Storage:** -20~ 80 °C (-4 ~ 176 °F)
Relative Humidity	5 ~ 90% at 45 °C (non-condensing)
Vibration Protection	• **Operating:** 0.25 Grms / 5 ~ 500 Hz • **Non-operating:** 1 Grms / 5 ~ 500Hz
Shock Protection	• **Operating:** 20 g / 11 ms • **Non-operating:** 40 g / 11 ms

All specifications are subject to change without prior notice.

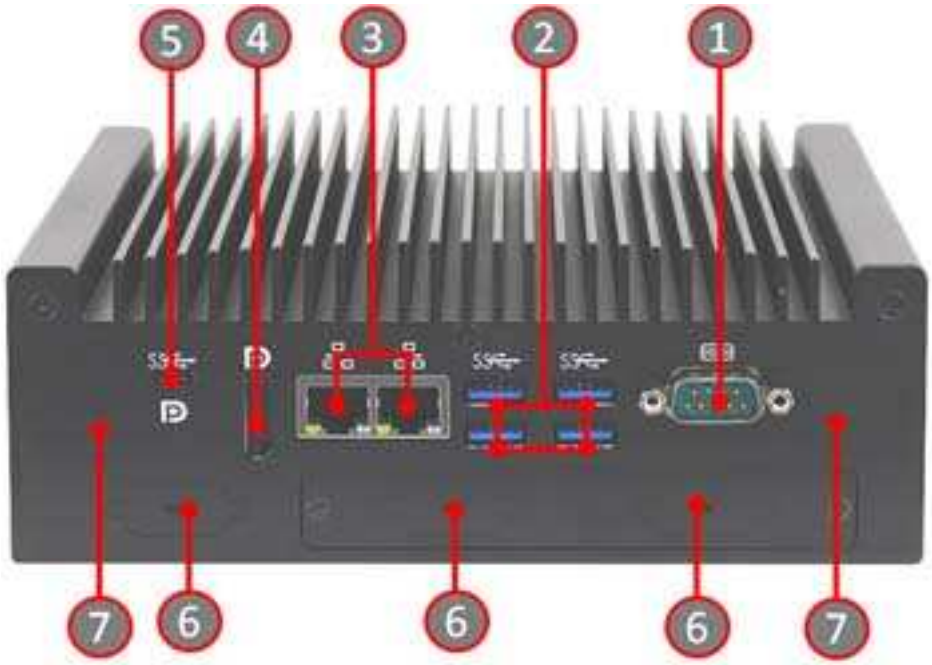
1.6 Product View

Front View



No.	Name	No.	Name
1	Antenna Holes	4	Power Switch
2	Digital I/O (4-In / 4-Out)	5	DC +12V~ +24V Power Input
3	HDD LED		

Rear View

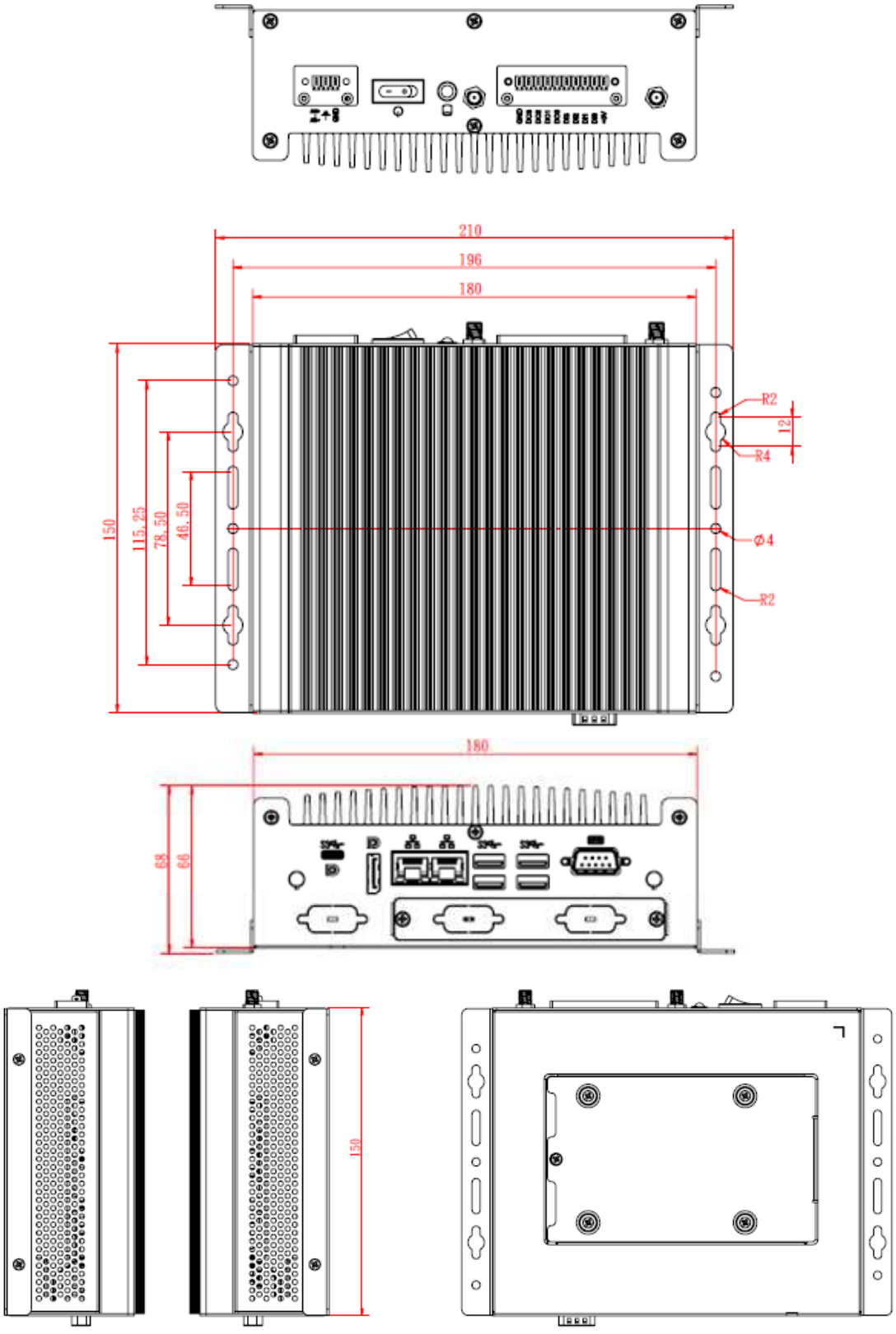


No.	Name	No.	Name
1	COM1 RS-232/422/485	5	Display Port / USB Type-C
2	USB 3.0 Ports	6	COM Port Holes
3	LAN Port	7	Antenna Holes
4	Display Port		

Oblique View

1.7 Dimensions

Unit: mm



Chapter 2
Hardware Configuration

The information provided in this chapter includes:

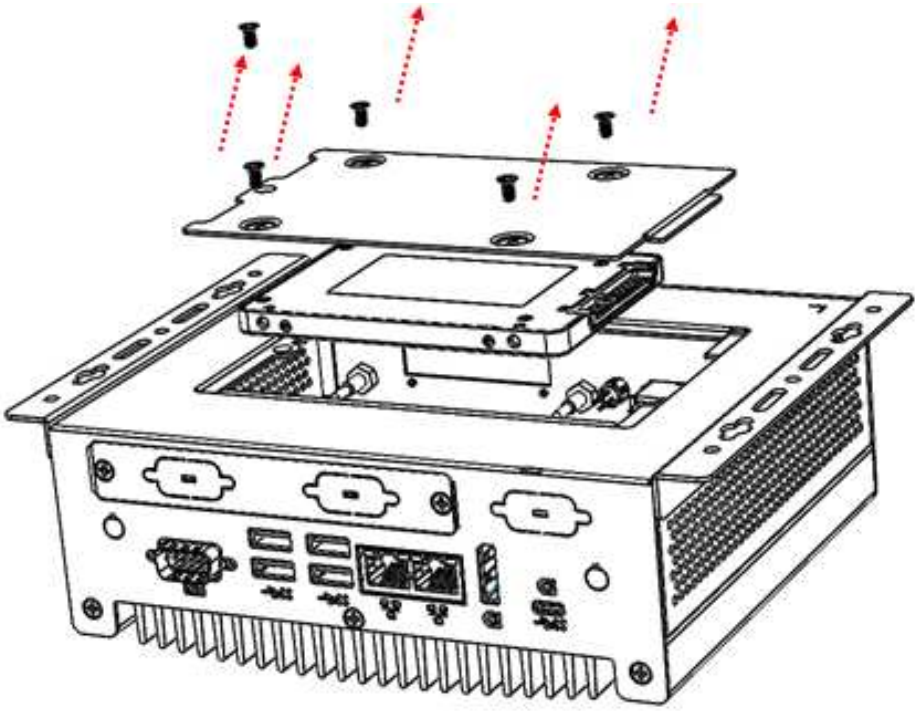
- Installations
- Descriptions and locations of connectors

2.1 Installations

2.1.1 HDD Installation

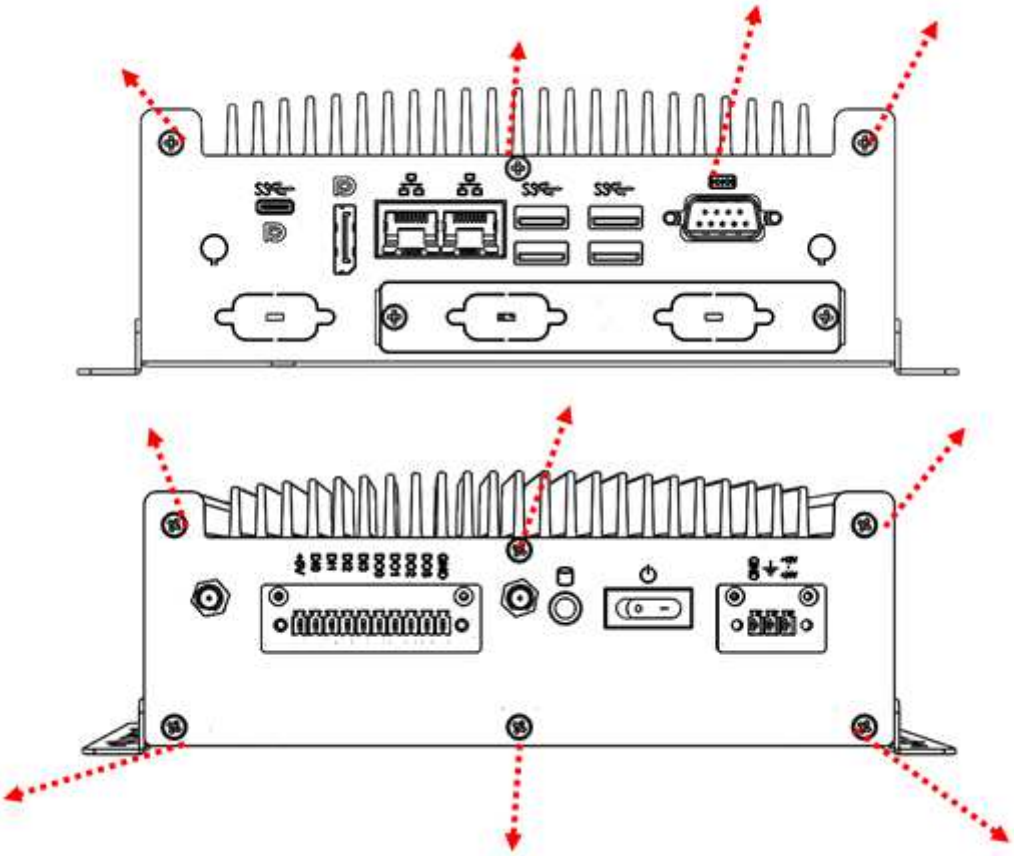
If you need to install or replace an SSD or a HDD, follow the instructions below.

1. Remove the five screw shown below. Lift the hard drive cover and proceed to remove or install the SSD/HDD drive.

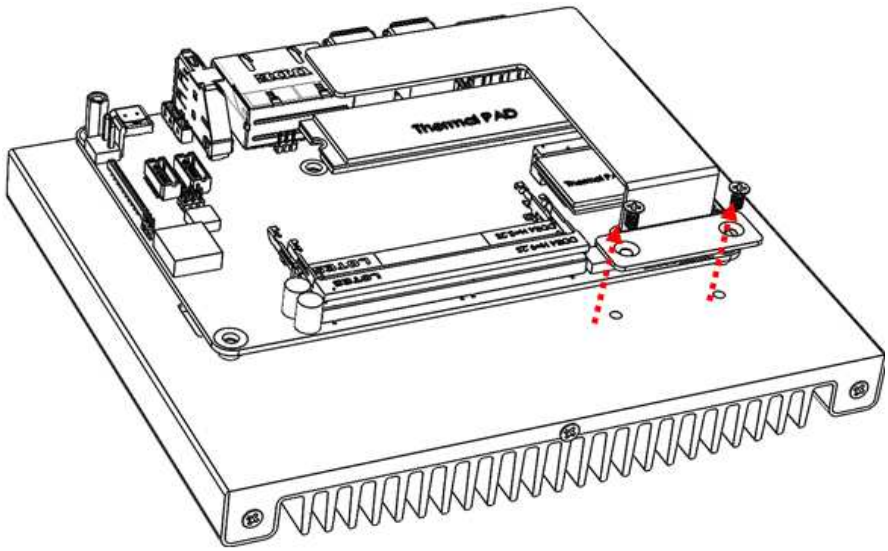


2.1.2 M.2 Card Installation

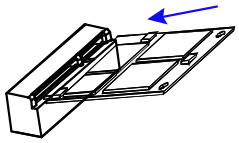
1. Remove the bottom chassis cover by loosening the 9 screws and the COM port standoff as indicated below.



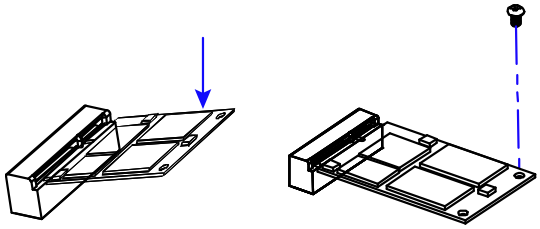
2. Remove the 2 screws shown below and proceed to install the M.2 card.



3. Align the key of the m.2 card to the m.2 interface, and insert the card slantwise.

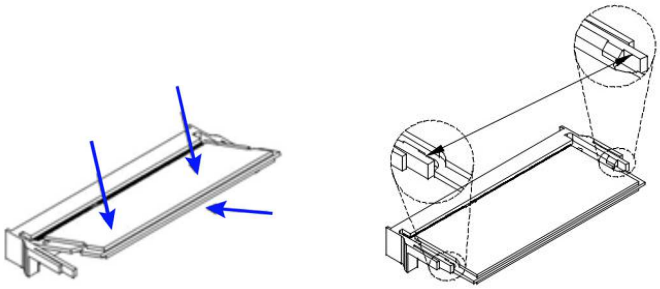


4. Push the m.2 card down, fix it onto the standoff with a screw.



2.1.3 Memory Installation

If you need to install or replace a memory module, perform the following steps:

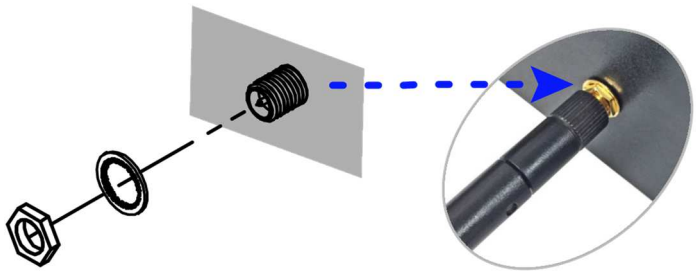


1. Locate the memory slot on the board.
2. Align the key of the memory module with that on the memory slot and insert the module slantwise.
3. Gently push the module down in an upright position until the clips of the slot close to hold the module in place when the module touches the bottom of the slot.

To remove the module, press the clips outwards with both hands, and the module will pop-up.

2.1.4 WiFi / 3G / 4G Antenna Installation

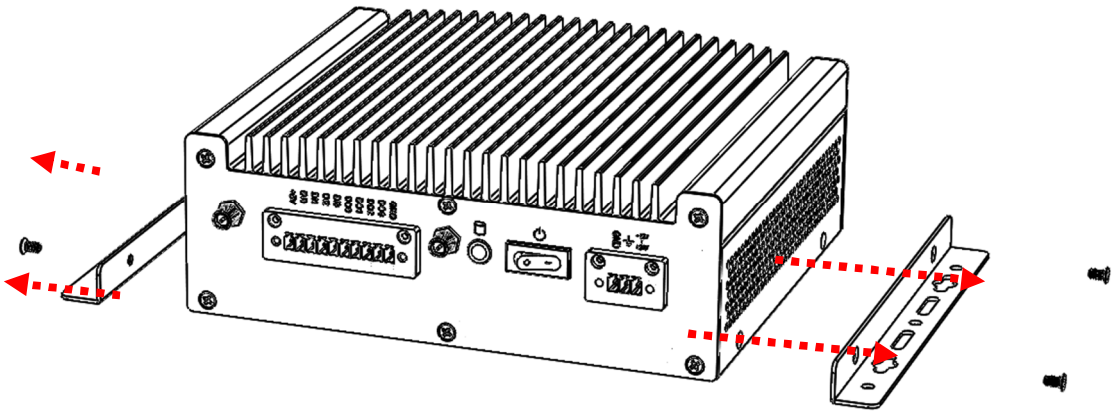
Thread the WiFi / 3G / 4G antenna cable through an antenna hole. Then fasten the antenna as shown below.



Info: The diameter of the nut is around 6.35 mm (0.25”-36UNC).

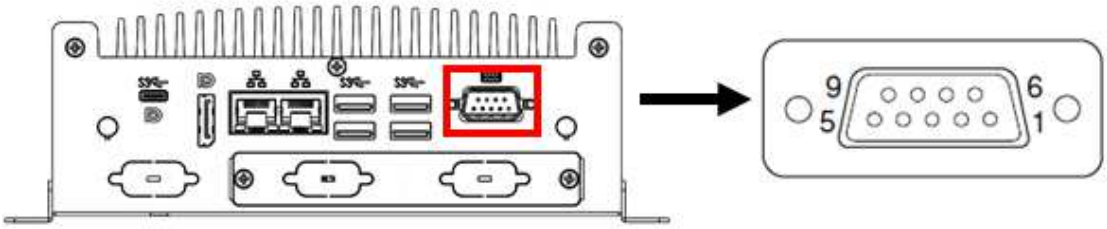
2.1.5 Side Bracket Installation

Use the screws provided in the accessory kit to lock the case together with the bracket



2.1.6 Pinout for COM Ports, DC Power & Digital I/O Connectors

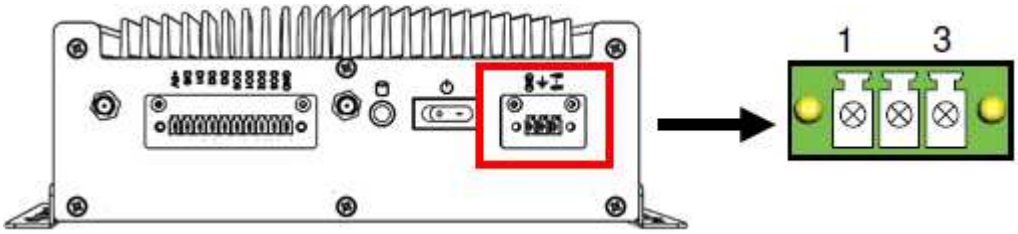
- **COM1 RS232/422/485 Port**



Pin	Assignment	Pin	Assignment
1	DCD, Data carrier detect	6	DSR, Data set ready
2	RXD, Receive data	7	RTS, Request to send
3	TXD, Transmit data	8	CTS, Clear to send
4	DTR, Data terminal ready	9	RI, Ring indicator
5	Ground		

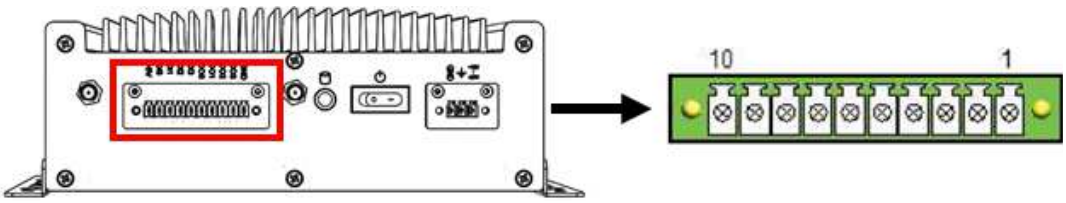
Pin	Assignment		
	RS-232	RS-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

- **DC Power Input Connector (terminal block)**



Pin	Assignment	Pin	Assignment
1	Ground	3	+12V ~ +24V
2	Chassis Ground		

- **Digital I/O Connector (terminal block)**



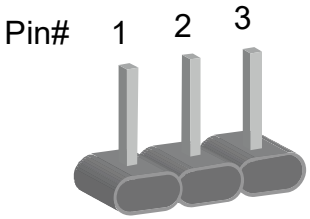
Pin	Assignment	Pin	Assignment
1	Ground	6	DI3
2	DO3	7	DI2
3	DO2	8	DI1
4	DO1	9	DI0
5	DO0	10	+5V

2.2 Setting the Jumpers

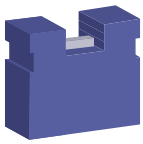
Set up and configure your product by using jumpers for various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your use.

2.2.1 How to Set Jumpers

Jumpers are short-length conductors consisting of several metal pins with a non-conductive base mounted on the circuit board. Jumper caps are used to have the functions and features enabled or disabled. If a jumper has 3 pins, you can connect either PIN1 to PIN2 or PIN2 to PIN3 by shorting.

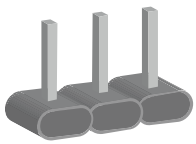
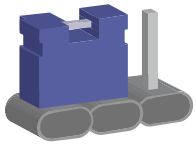
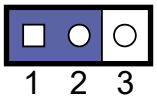
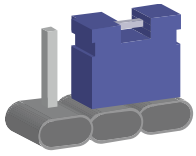
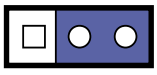


A 3-pin jumper



A jumper cap

Refer to the illustration below to set jumpers.

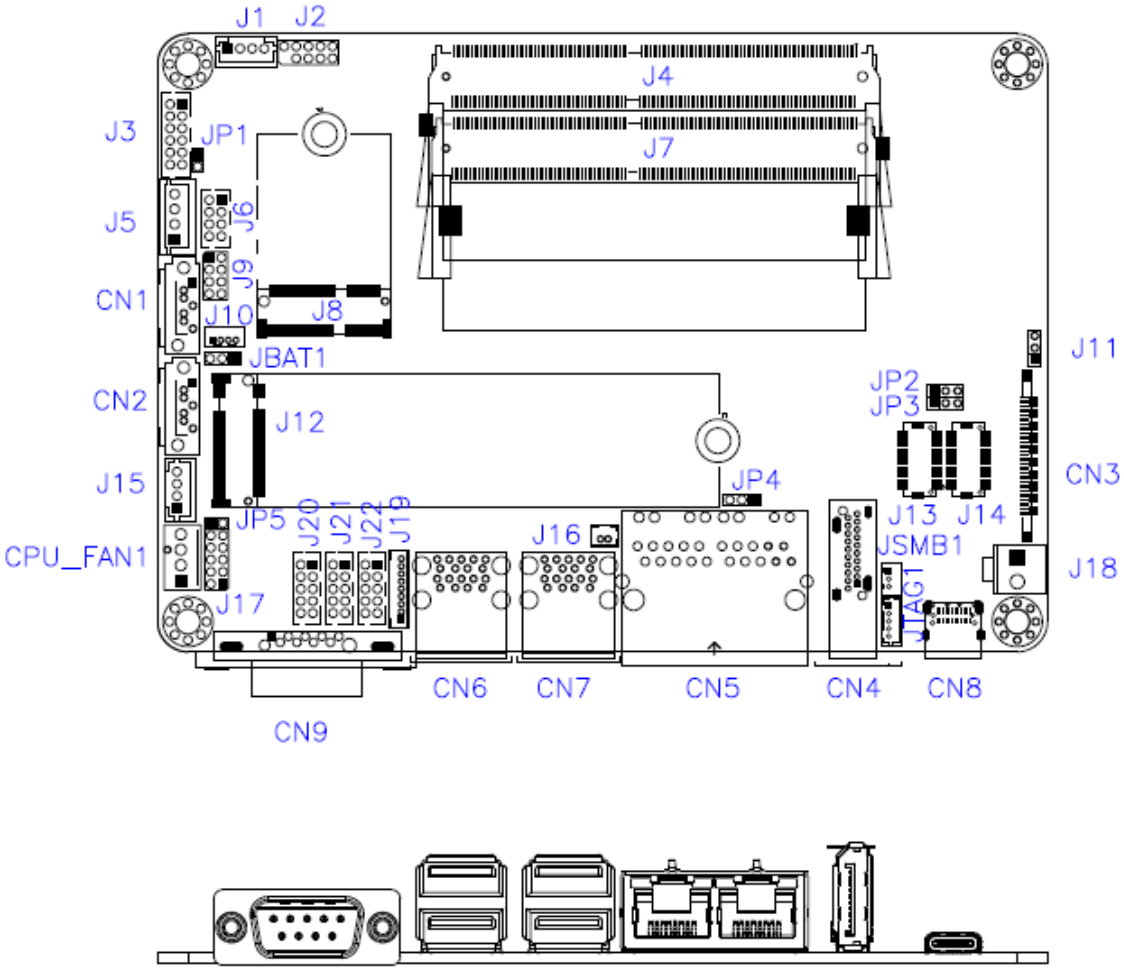
Pin closed	Oblique view	illustration
Open		
1-2		
2-3		

When two pins of a jumper are encased in a jumper cap, this jumper is **closed**, i.e. turned **On**.

When a jumper cap is removed from two jumper pins, this jumper is **open**, i.e. turned **Off**.

2.3 Jumper & Connector Locations on the Motherboard

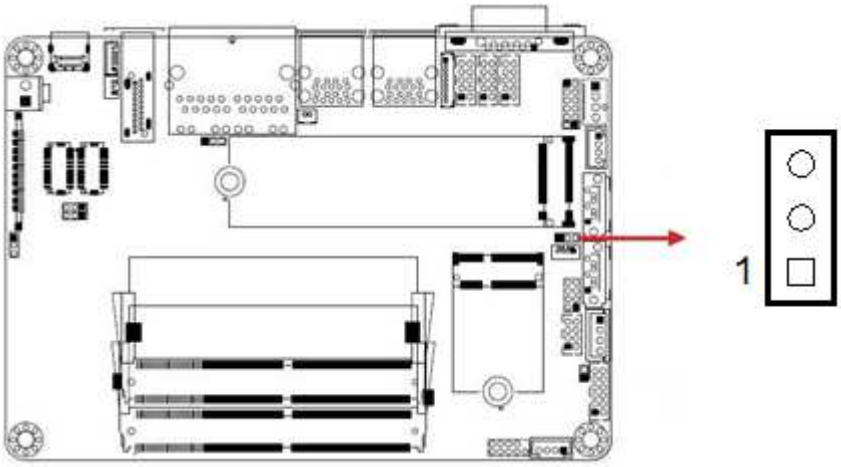
Motherboard: IB919

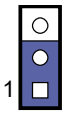
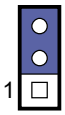


2.4 Jumpers Quick Reference

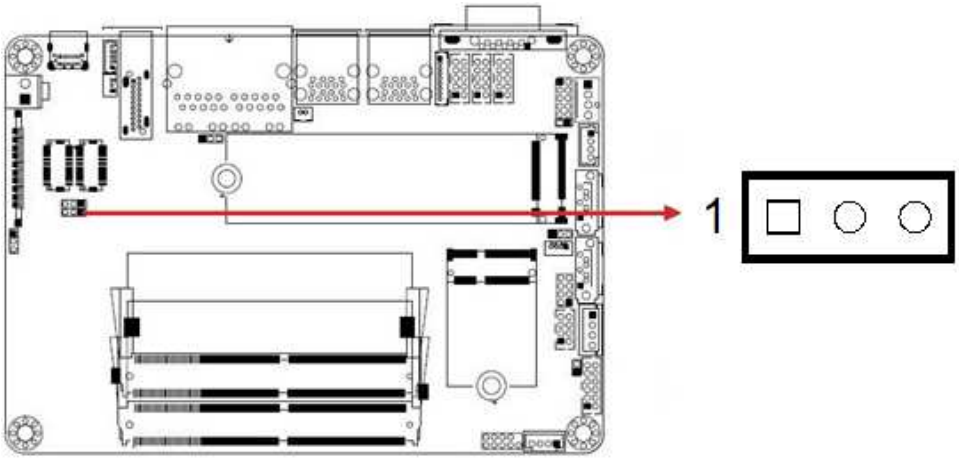
Function	Jumper
Clear CMOS Data	JBAT1
EDP Panel Power Selection	JP2
LVDS Panel Power / Brightness Selections	JP3(For power) / JP5 (For brightness)
EDP / LVDS Selection	JP4
Factory Use Only	JP1

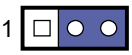
2.4.1 Clear CMOS Data (JP2)



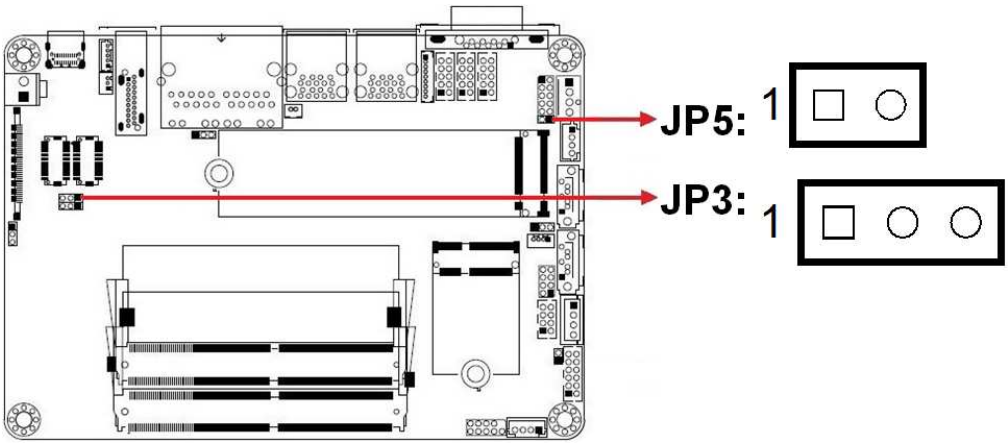
Function	Pin closed	Illustration
Normal (default)	1-2	
Clear CMOS	2-3	

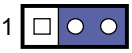
2.4.2 EDP Panel Power Selection (JP2)



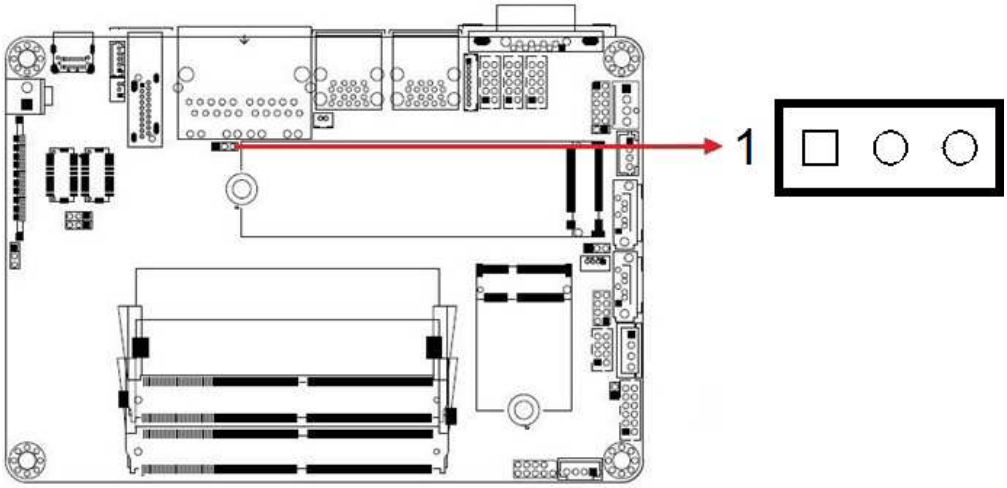
Jumper	Function	Pin closed	Illustration
JP2	3.3V (default)	1-2	
	5V	2-3	

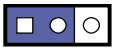
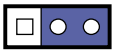
2.4.3 LVDS Panel Power / Brightness Selections (JP3 / JP5)



Jumper	Function	Pin closed	Illustration
JP3	3.3V (default)	1-2	
	5V	2-3	
JP5	3.3V (default)	Open	
	5V	Close	

2.4.4 EDP / LVDS Selection (JP4)

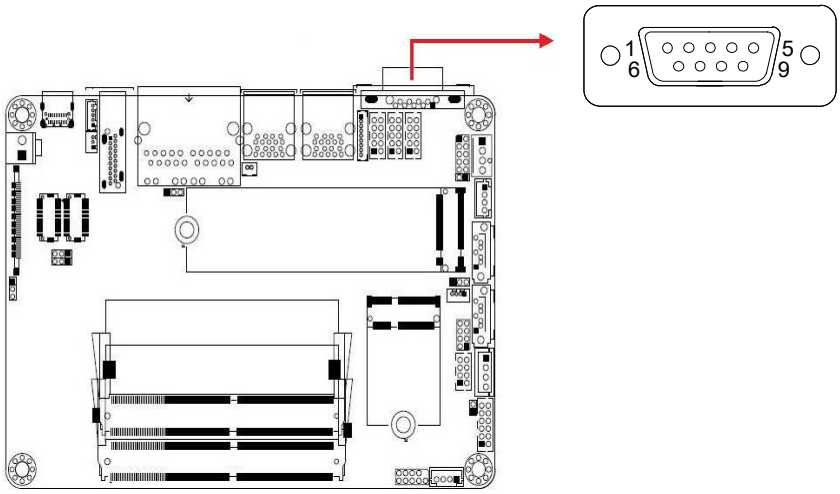


Jumper	Function	Pin closed	Illustration
JP4	EDP (default)	1-2	
	LVDS	2-3	

2.5 Connectors Quick Reference

Function	Connector
COM1 RS-232/422/485 Port	CN9
Amplifier Connector	J1
Audio Connector	J3
SATA HDD Power Connector	J5
SMBUS Connector	J10
Front Panel Setting Connector	J9
USB 2.0 Connector	J6
Battery Connector	J16
COM 2, COM3, COM4 RS-232 Ports	J20, J21, J22
DC Power Input Connector	J18
Digital I/O Connector	J17
LCD Backlight Connector	J15
LVDS Connectors	J14 (1st channel), J13 (2nd channel)
CPU Fan Connector	CPU_FAN1
EDP Connector	CN3
SATA III Port	CN1, CN2
Display Port	CN4
GbE LAN Ports	CN5
USB 3.0 Port	CN6, CN7
USB Type-C	CN8
DDR4 SO-DIMM Slot	J4, J7
M.2 E-Key / M.2 M-Key	J8, J12
Factory Use Only	J2, J19, J11

2.5.1 COM1 RS-232/422/485 Port (CN9)

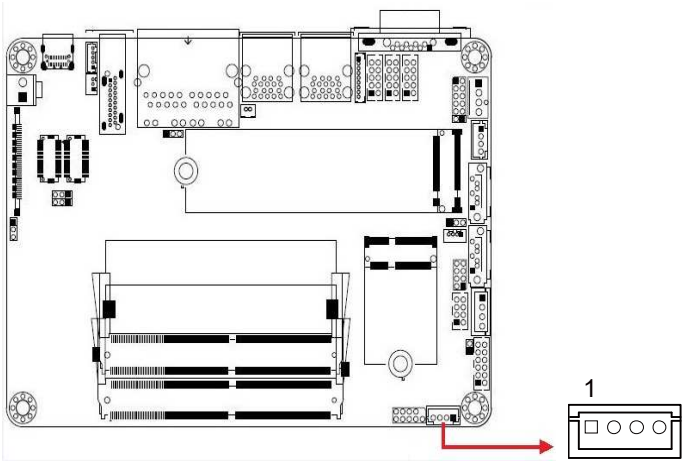


COM1 port is jumper-less and configurable in BIOS.

Pin	Assignment	Pin	Assignment
1	DCD, Data carrier detect	6	DSR, Data set ready
2	RXD, Receive data	7	RTS, Request to send
3	TXD, Transmit data	8	CTS, Clear to send
4	DTR, Data terminal ready	9	RI, Ring indicator
5	Ground		

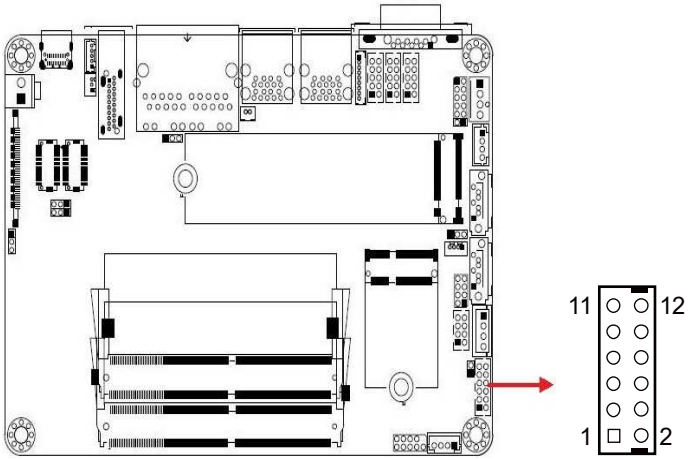
Pin	Assignment		
	RS-232	RS-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

2.5.2 Amplifier Connector (J1)



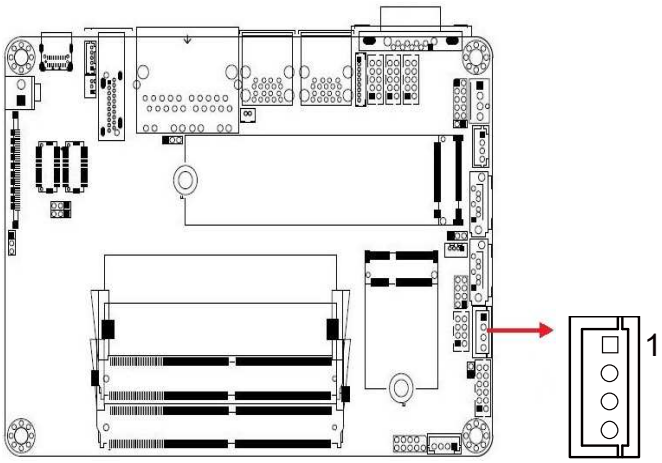
Pin	Assignment	Pin	Assignment
1	SPK_L+	3	SPK_R-
2	SPK_L-	4	SPK_R+

2.5.3 Audio Connector (J3)



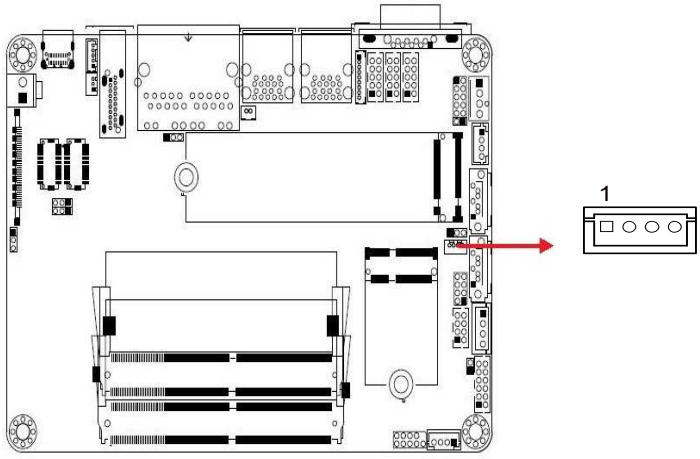
Pin	Assignment	Pin	Assignment
1	LINEOUT_L	2	LINEOUT_R
3	JD_FRONT	4	Ground
5	LINEIN_L	6	LINEIN_R
7	JD_LINEIN	8	Ground
9	MIC_L	10	MIC-R
11	JD_MIC1	12	Ground

2.5.4 SATA HDD Power Connector (J5)



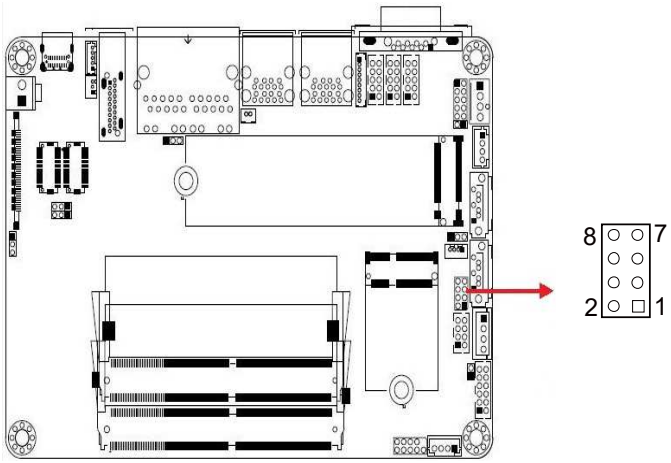
Pin	Assignment	Pin	Assignment
1	+5V	3	Ground
2	Ground	4	+12V

2.5.5 SMBUS Connector (J10)



Pin	Assignment	Pin	Assignment
1	+3.3V	3	SMB_DATA
2	SMB_CLK-	4	Ground

2.5.6 Front Panel Connector (J9)

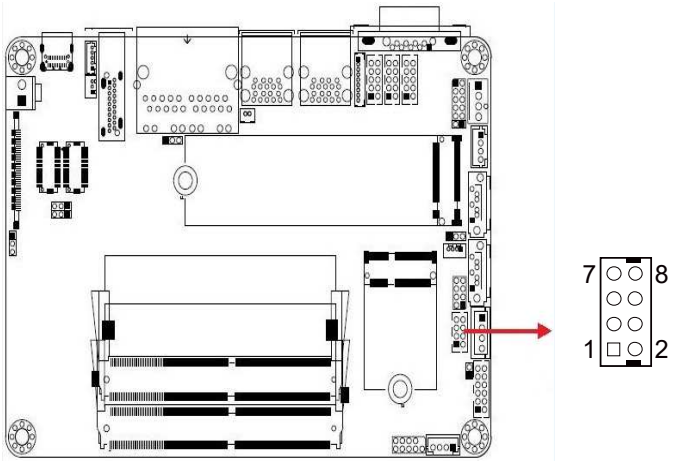


Pin	Assignment	Pin	Assignment
1	Ground	2	PWR_BTN
3	3.3V	4	HDD Active
5	Ground	6	Reset
7	+5V	8	Ground

J9 is utilized for system indicators to provide light indication of the computer activities and switches to change the computer status. It provides interfaces for the following functions.

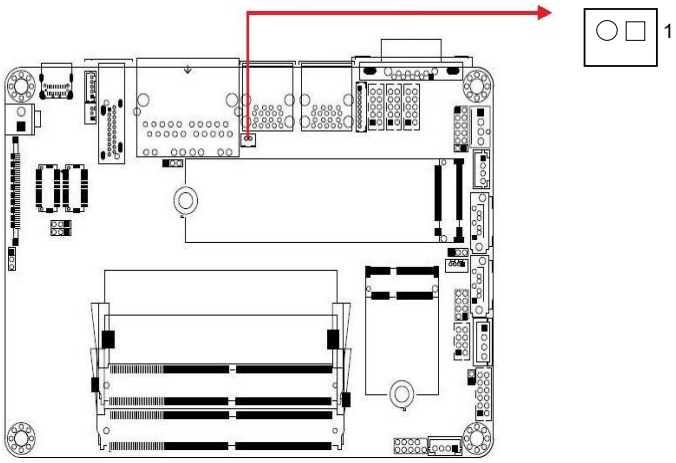
- **ATX Power ON Switch (Pins 1 and 2)**
  The 2-pin makes an “ATX Power Supply On/Off Switch” for the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will power off the system.
- **Hard Disk Drive LED Connector (Pins 3 and 4)**
  This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.
- **Reset Switch (Pins 5 and 6)**
  The reset switch allows you to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.
- **Power LED: Pins 7 and 8**
  This connector connects to the system power LED on control panel. This LED will light when the system turns on.

2.5.7 USB 2.0 Connector (J6)



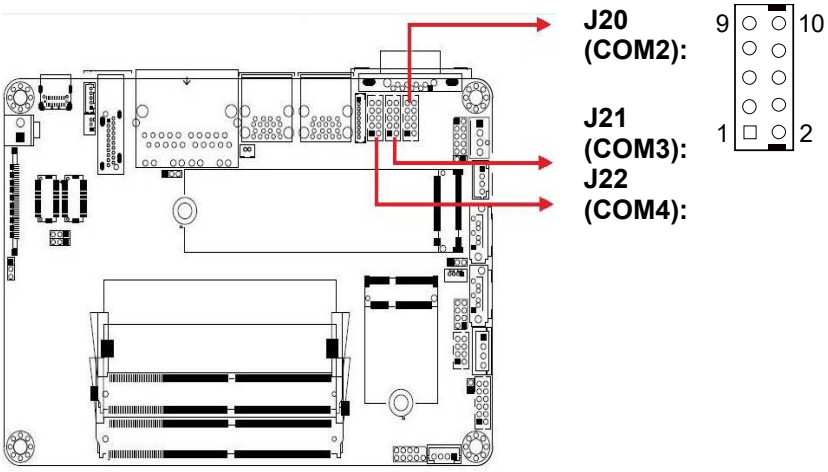
Pin	Assignment	Pin	Assignment
1	VCC	2	Ground
3	D0-	4	D1+
5	D0+	6	D1-
7	Ground	8	VCC

2.5.8 Battery Connector (J16)



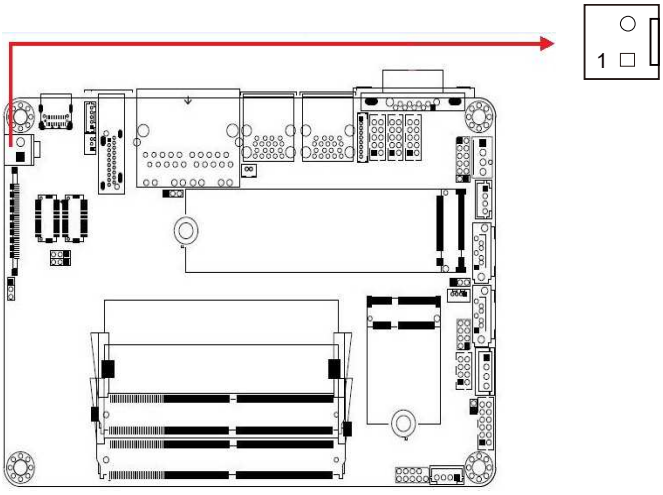
Pin	Assignment
1	Battery+
2	Ground

2.5.9 COM2, COM3, COM4 RS-232 Ports (J20, J21, J22)



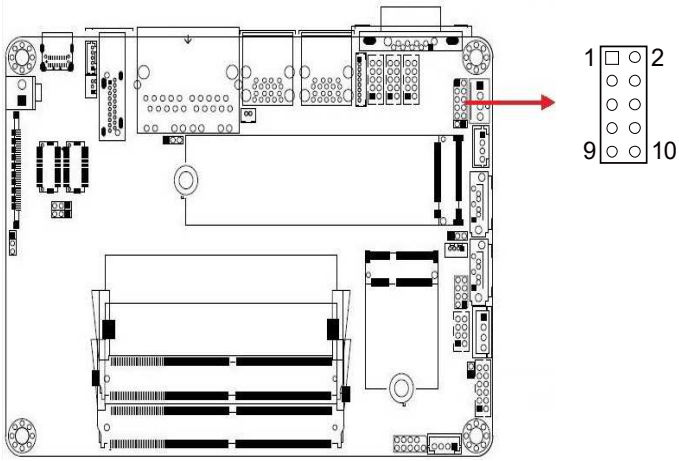
Pin	Assignment	Pin	Assignment
1	DCD, Data carrier detect	2	RXD, Receive data
3	TXD, Transmit data	4	DTR, Data terminal ready
5	Ground	6	DSR, Data set ready
7	RTS, Request to send	8	CTS, Clear to send
9	RI, Ring indicator	10	Not Used

2.5.10 DC Power Input Connector (J18)



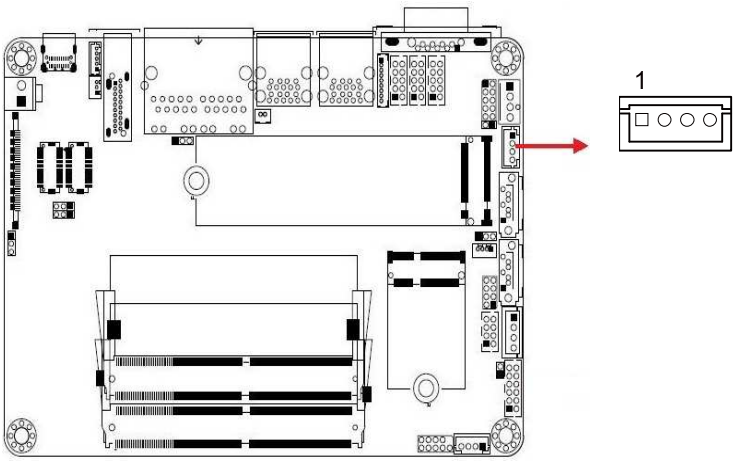
Pin	Assignment
1	+12V ~ +24V
2	Ground

2.5.11 Digital I/O Connector (J17)



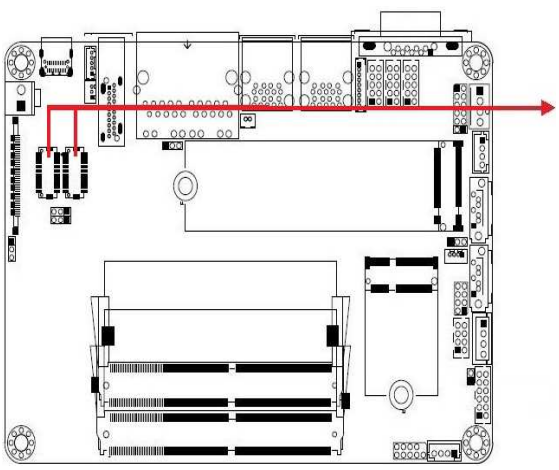
Pin	Assignment	Pin	Assignment
1	Ground	2	VCC
3	OUT3	4	OUT1
5	OUT2	6	OUT0
7	IN3	8	IN1
9	IN2	10	IN0

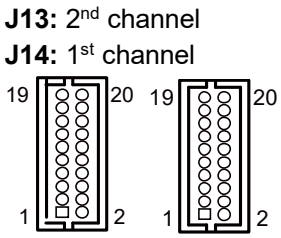
2.5.12 LCD Backlight Connector (J15)



Pin	Assignment	Pin	Assignment
1	+12V	3	Brightness Control
2	Backlight Enable	4	Ground

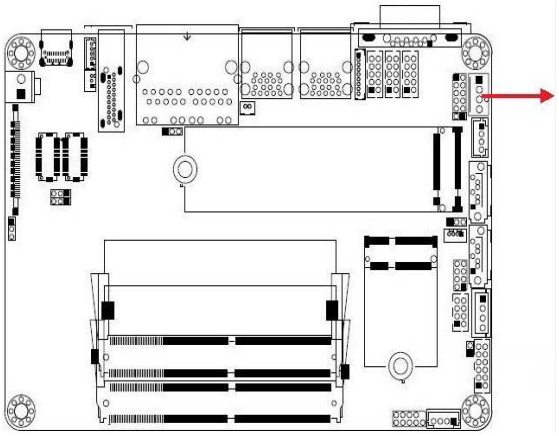
2.5.13 LVDS Connector (J14, J13)

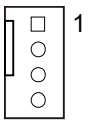




Pin	Assignment	Pin	Assignment
1	TX0P	2	TX0N
3	Ground	4	Ground
5	TX1P	6	TX1N
7	Ground	8	Ground
9	TX2P	10	TX2N
11	Ground	12	Ground
13	CLKP	14	CLKN
15	Ground	16	Ground
17	TX3P	18	TX3N
19	Power	20	Power

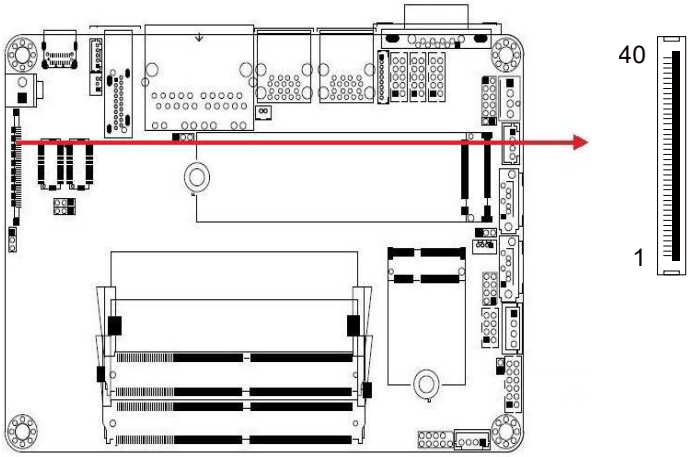
2.5.14 CPU Fan Connector (CPU_FAN1)





Pin	Assignment	Pin	Assignment
1	Ground	3	CPU Fan In
2	+12V	4	CPU Fan Out

2.5.15 EDP Connector (CN3)



Pin	Signal Name	Pin	Signal Name
1	eDP VCC	21	TXN0
2	eDP VCC	22	TXP0
3	eDP VCC	23	Ground
4	eDP VCC	24	AUXP
5	eDP VCC	25	AUXN
6	Ground	26	X
7	Ground	27	+3.3V
8	Ground	28	+12V
9	Ground	29	X
10	Hot Plug detect	30	Ground
11	Ground	31	+5V
12	TXN3	32	X
13	TXP3	33	Back Light Control
14	Ground	34	Back Lignt Enable
15	TXN2	35	+12V
16	TXP2	36	+3.3V
17	Ground	37	Ground
18	TXN1	38	X
19	TXP1	39	X
20	Ground	40	X

Chapter 3
Driver Installation

The information provided in this chapter includes:

- Intel® Chipset Software Installation Utility
- Graphics Driver Installation
- HD Audio Driver Installation
- LAN Driver Installation
- Intel® Management Engine Driver Installation

3.1 Introduction

This section describes the installation procedures for software drivers. The software drivers are in a disk enclosed with the product package. If you find anything missing, please contact the distributor where you made the purchase.

Note: After installing your Windows OS, you must install the Intel® Chipset Software Installation Utility first before proceeding with the drivers installation.

3.2 Intel® Chipset Software Installation Utility

The Intel® Chipset drivers should be installed first before the software drivers to install INF files for Plug & Play function for the chipset components. Follow the instructions below to complete the installation.

1. Insert the disk enclosed in the package. Click **Intel** on the left pane and then **Intel(R) Kabylake-U Chipset Drivers** on the right pane.

2. Click **Intel(R) Chipset Software Installation Utility**.

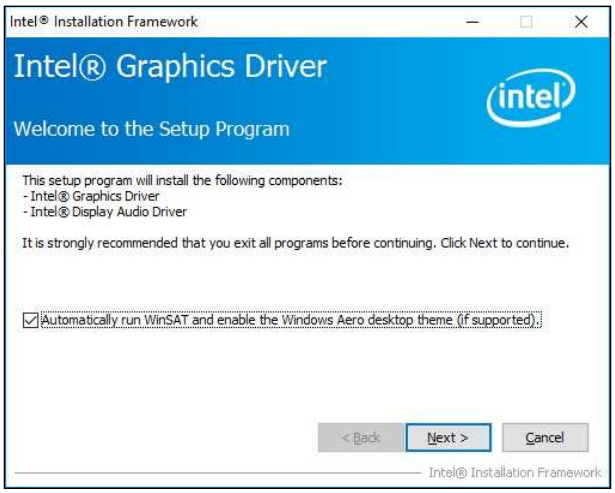
3. When the *Welcome* screen appears, click **Next** to continue.
4. Accept the software license agreement to proceed with the process.
5. On the *Readme File Information* screen, click **Next** for installation.
6. When the driver is completely installed, restart the computer for changes to take effect.

3.3 Graphics Driver Installation

1. Insert the disk enclosed in the package. Click **Intel** on the left pane and then **Intel(R) Kabylake-U Chipset Drivers**.

2. Click **Intel(R) HD Graphics Driver**.

3. When the *Welcome* screen appears, click **Next**.



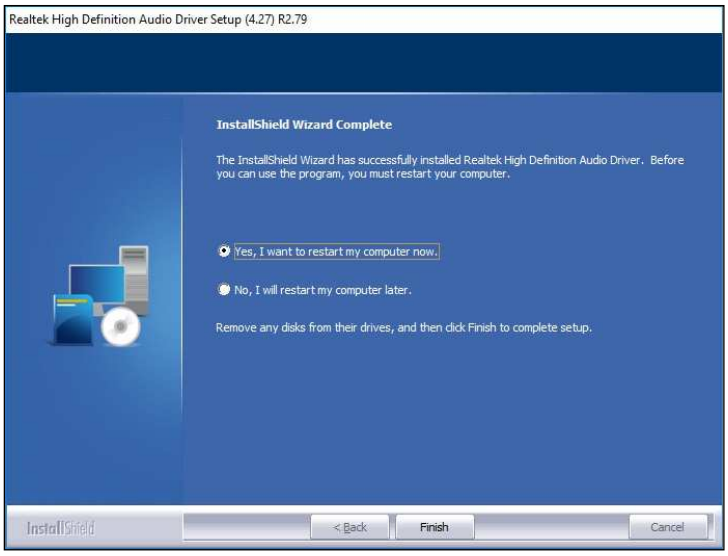
4. Click **Yes** to accept the license agreement and click **Next**.
5. On the *Readme File Information* screen, click **Next** until installation starts.
6. When the driver is completely installed, restart the computer

3.4 HD Audio Driver Installation

1. Insert the disk enclosed in the package. Click **Intel** and then **Intel(R) Kabylake-U Chipset Drivers**.

2. Click **Realtek High Definition Audio Driver**.

3. On the *Welcome* screen of the InstallShield Wizard, click **Next** until the installation starts.



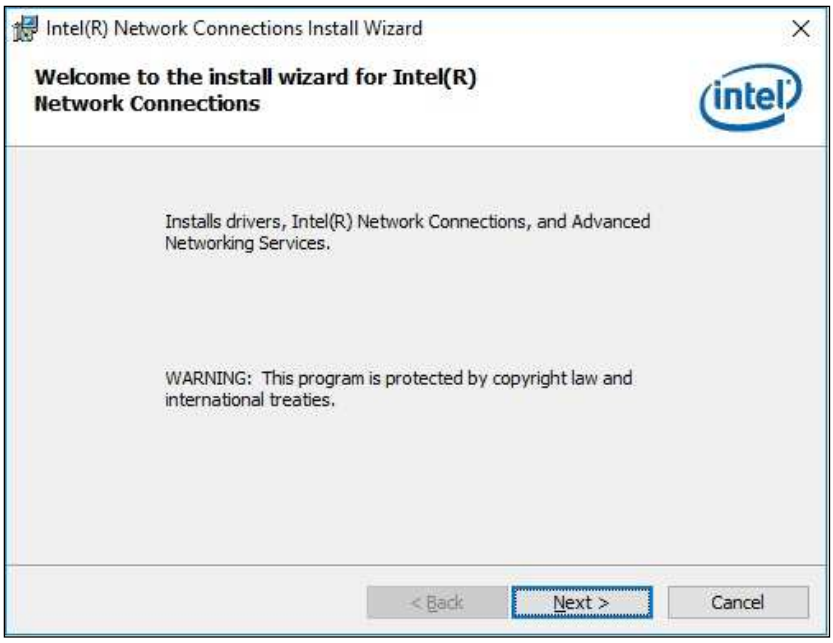
4. When the driver is completely installed, restart the computer for changes to take effect.

3.5 LAN Driver Installation

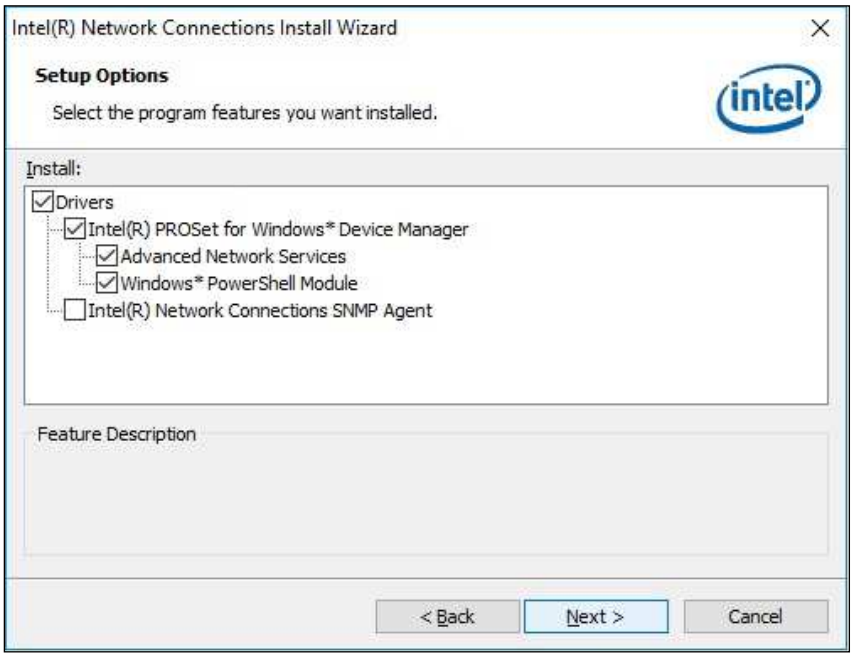
1. Insert the disk enclosed in the package with the product. Click **LAN Card** and then **Intel(R) Kabylake-U Chipset Drivers**

2. Click **Intel(R) PRO LAN Network Drivers.**.

3. When the *Welcome* screen appears, click **Next** to continue.



4. Accept the license agreement and click **Next**.
5. Tick the checkbox for **Drivers** to select the related drivers and click **Next**.



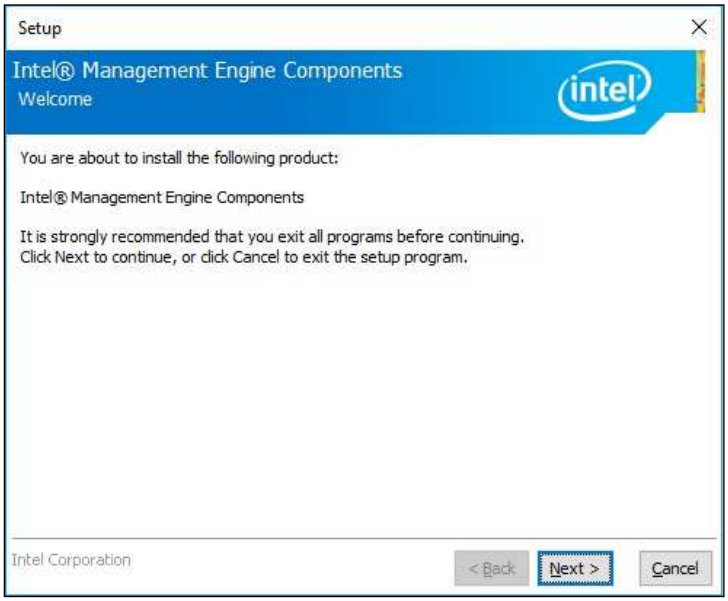
6. When the wizard is ready for installation, click **Install**.
7. As the installation is complete, restart the computer for changes to take effect.

3.6 Intel® Management Engine Driver Installation

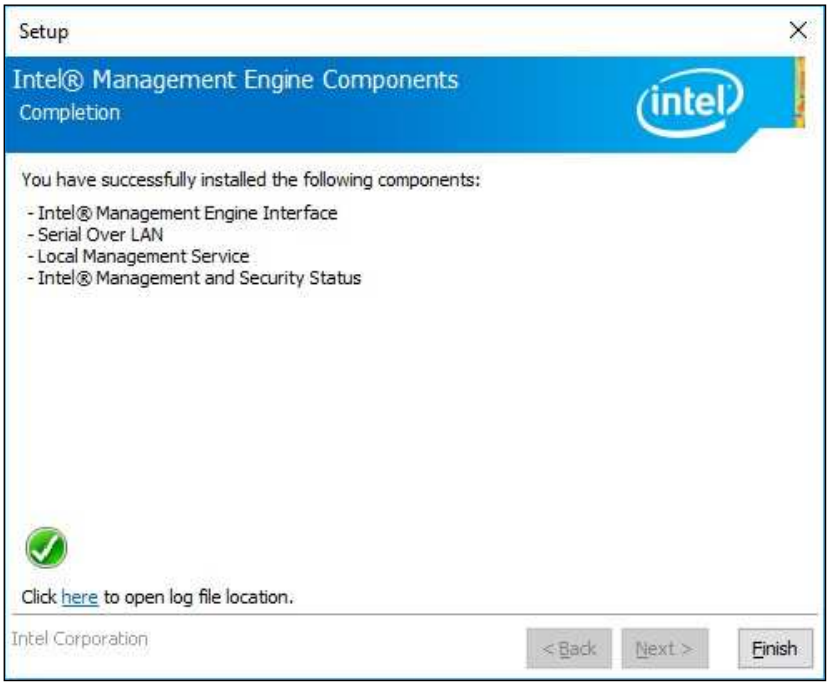
1. Insert the disk enclosed in the package. Click **Intel** and then **Intel(R) Kabylake-U Chipset Drivers**.

2. Click **Intel(R) ME 11.x Drivers**.

3. When the *Welcome* screen appears, click **Next** to continue.



4. Accept the licence agreement and click **Next** until the installation starts.
5. As the driver is completely installed, restart the computer for changes to take effect.



Chapter 4
BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

- Main Settings
- Advanced Settings
- Chipset Settings
- Security Settings
- Boot Settings
- Save & Exit

4.1 Introduction

The BIOS (Basic Input/Output System) installed in the ROM of your computer system supports Intel® processors. The BIOS provides critical low-level support for standard devices such as disk drives, serial ports and parallel ports. It also provides password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

4.2 BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Press the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup.

If you still need to enter Setup, restart the system by pressing the ”Reset” button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again.

The following message will appear on the screen:

```
Press <DEL> to Enter Setup
```

In general, press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help, and <Esc> to quit.

When you enter the BIOS Setup utility, the *Main Menu* screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: It is strongly recommended that you avoid making any changes to the chipset defaults.

These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could make the system unstable and crash in some cases.

4.3 Main Settings

BIOS Setting	Description
System Date	Sets the date. Use the <Tab> key to switch between the data elements.
System Time	Set the time. Use the <Tab> key to switch between the data elements.

NOTE: Below is the corresponding screen for the IB919EF BIOS

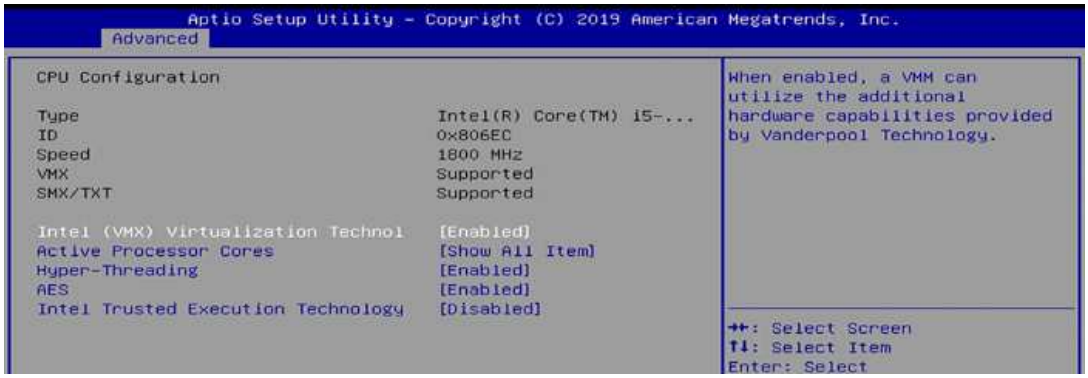
4.4 Advanced Settings

This section allows you to configure, improve your system and allows you to set up some system features according to your preference.

4.4.1 Connectivity Configuration

BIOS Setting	Description
CNVI Mode	This option configures Connectivity. ***Auto Detection*** – means that if Discrete solution is discovered it will be enabled by default. Otherwise Integrated solution (CNVi) will be enabled; ***Disable Integrated*** – disables Integrated Solution.
MfUart1 type	This is a test option which allows configuration of UART type for WiFI side band communication. Options are ISH Uart0 / SerialIO Uart2 / Uart over external pads / Not connected.
Discrete Bluetooth Module	Seiral IO UART0 needs to be enabled to select BT Module. Default: Disabled
Advanced Settings	Configure ACPI objects for wireless devices Default: Disabled
WWAN Configuration	Configure WWAN related options. WWAN Device: enable or disable M.2 WWAN device
WWAN Reset Workaround	Default: Enabled

4.4.2 CPU Configuration



This section displays the type, ID and speed of the CPU.

BIOS Setting	Description
Intel (VMX) Virtualization Technology	When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
Active Processor Cores	Number of cores to enable in each processor package
Hyper-Threading	Options; Enables or Disabled
AES	Enable/Disable AES (Advanced Encryption Standard)
Intel Trusted Execution Technology	Enables utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology. Changes require a full power cycle to take effect.

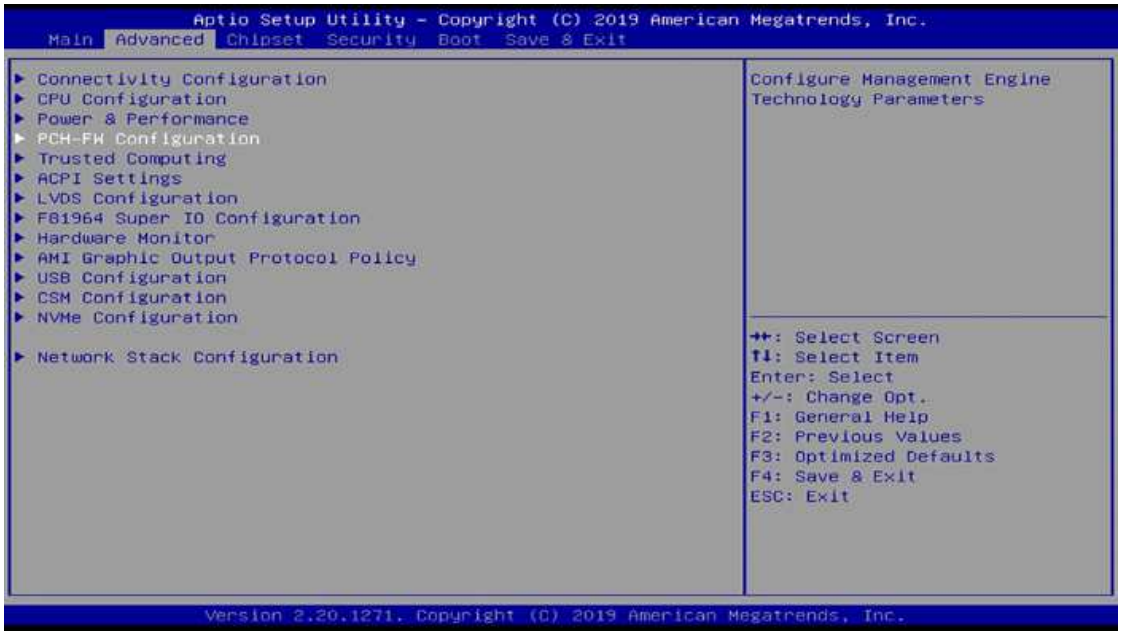
NOTE: The selections for Hyper-Threading Intel Trusted Execution Technology are not available on the IB919EF BIOS as shown below.

4.4.3 Power & Performance

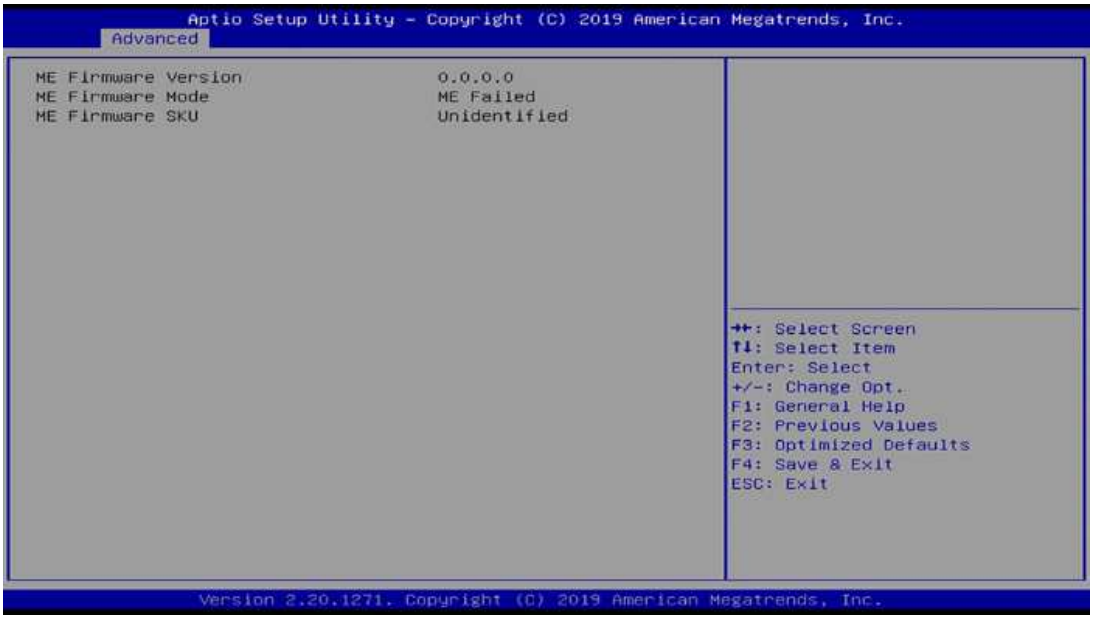
BIOS Setting	Description
Intel Speedstep	Allows more than two frequency ranges to be supported
Intel Speed Shift Technology	Enable/Disable Intel Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.
Turbo Mode	Enable/Disable processor Turbo Mode (requires Intel Speed Steop or Intel Speed Dhift to be available and enabled.)

NOTE: The selection for Turbo Mode is not available on the IB919EF BIOS as shown below.

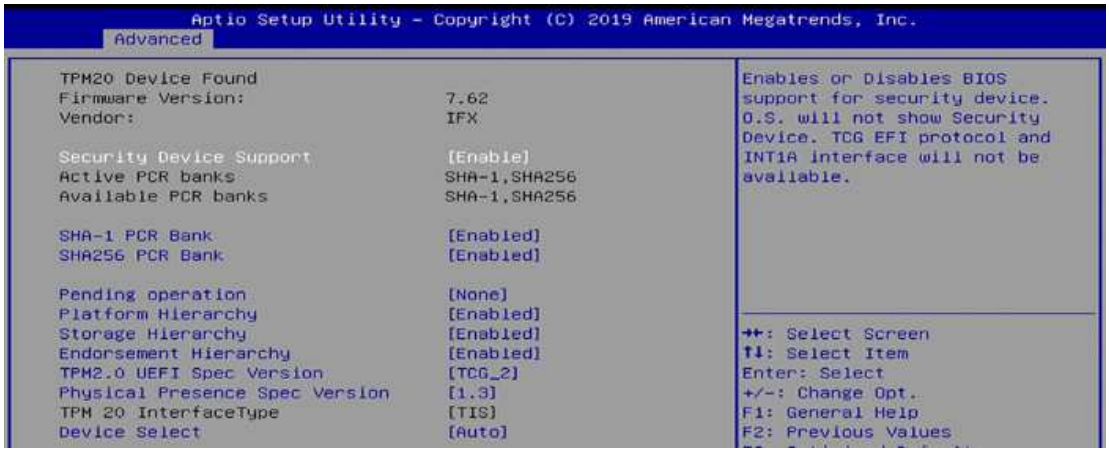
4.4.4 PCH-FW Configuration



Configure Management Engine Technology Parameters

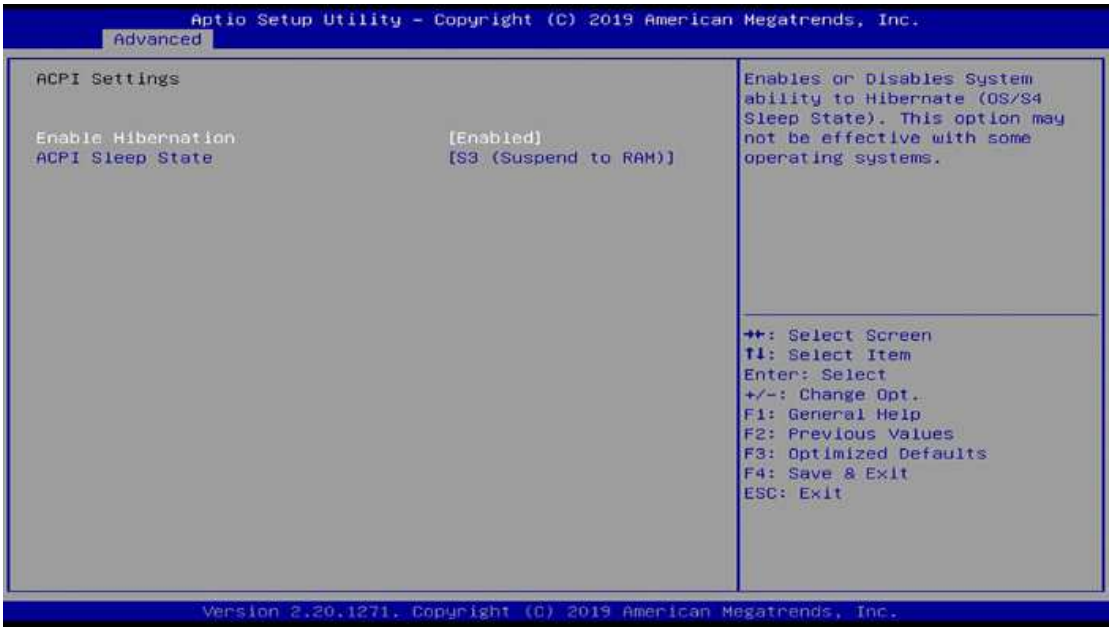


4.4.5 Trusted Computing



BIOS Setting	Description
Security Device Support	Enables / Disables BIOS support for security device. OS will not show security device. TCG EFI protocol and INT1A interface will not be available.
SHA-1 PCR Bank	Enables / Disables SHA-1 PCR Bank.
SHA256 PCR Bank	Enables / Disables SHA256 PCR Bank.
Pending operation	Schedule an operation for the security device. Note: Your computer will reboot during restart in order to change state of security device.
Platform Hierarchy	Enables / Disables platform hierarchy.
Storage Hierarchy	Enables / Disables storage hierarchy.
Endorsement Hierarchy	Enables / Disables endorsement hierarchy.
TPM2.0 UEFI Spec Version	Selects the supported TCG version based o your OS. • **TCG_1_2:** supports Win8/Win10. • **TCG_2:** supports new TCG2 protocol and event format for Windows 10 or later.
Physical Presence Spec Version	Select to tell O.S. to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
Device Select	TPM 1.2 will restrict support to TPM 1.2 devices. TPM 2.0 will restrict support to TPM 2.0 devices. Auto will support both with the default set to TPM 2.0 devices if not found, TPM 1.2 devices will be enumerated.

4.4.6 ACPI Settings

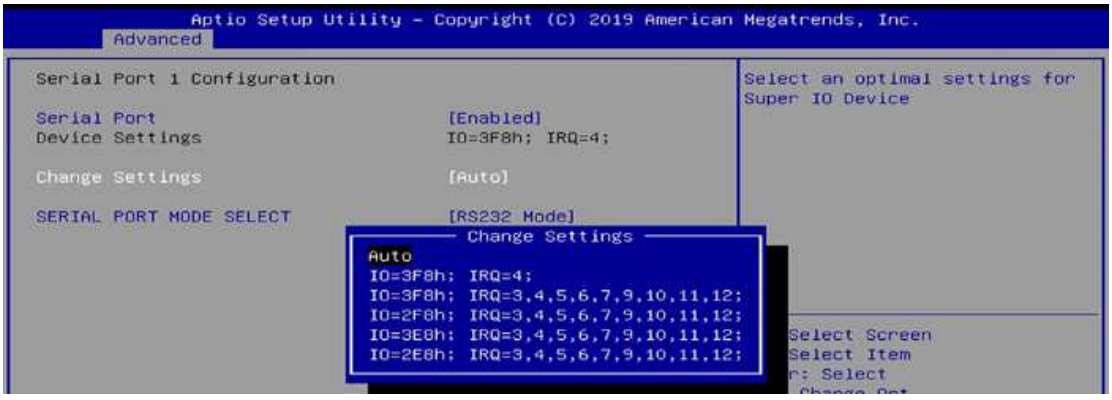


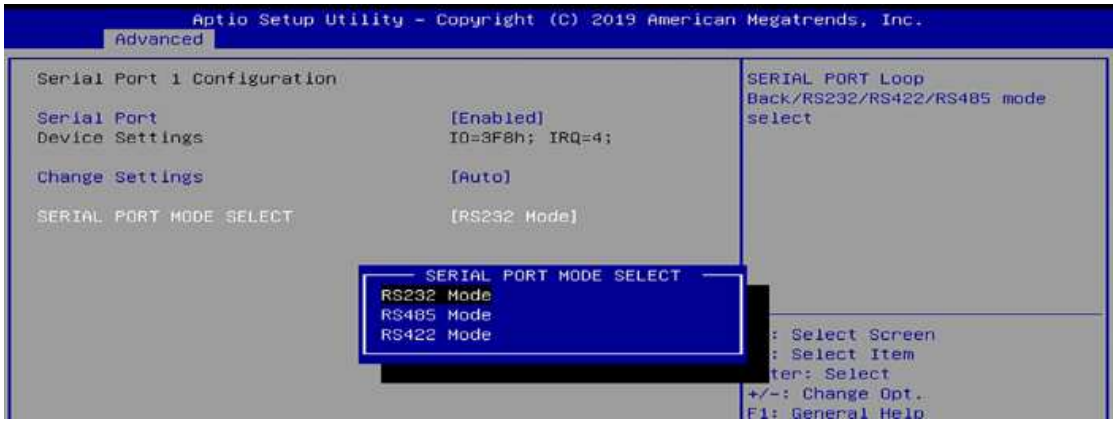
BIOS Setting	Description
Enable Hibernation	Enables / Disables the system ability to hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Selects an ACPI sleep state (Suspend Disabled or S3) where the system will enter when the Suspend button is pressed.

4.4.7 LVDS Configuration

BIOS Setting	Description
LVDS Control	Default: Enabled
Panel Color Depth	Selects the panel color depth. Options: 18 bit, 24 bit
LVDS Channel Type	Chooses the LVDS as single or dual channel.
LCD Panel Type	Panel Type (Resolution) Options: 640 x 480, 800 x 600, 1024 x 768, 1280 x 768, 1280 x 800, 1280 x 960, 1280 x 1024, 1366 x 768, 1440 x 900, 1600 x 900, 1600 x 1200, 1680 x 1050, 1920 x 1080, 1920 x 1200
LVDS Brightness Control	Options: 0(Min), 1, 2, 3, 4, 5, 6, 7(Max)

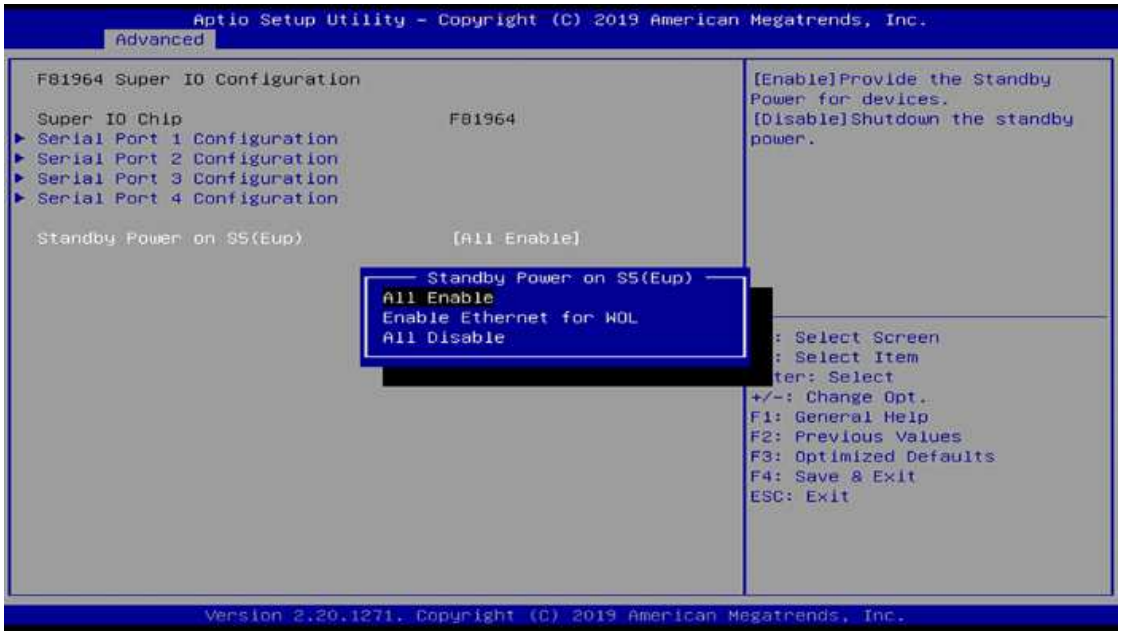
4.4.8 F81964 Super IO Configuration





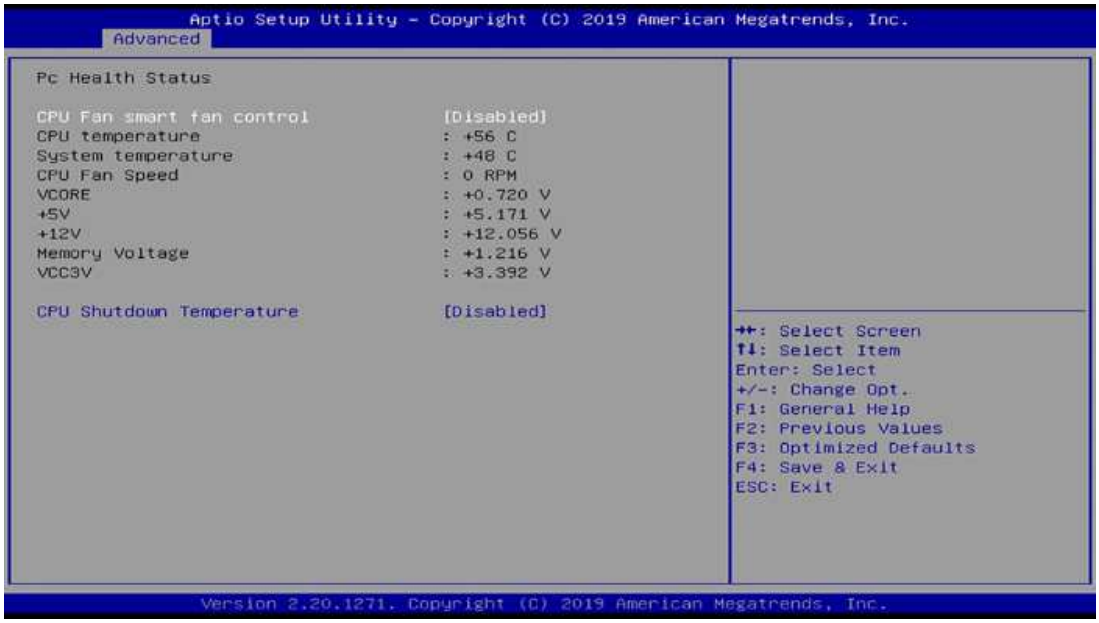
BIOS Setting	Description
Serial Ports Configuration	Sets parameters of serial ports. Enables / Disables the serial port and select an optimal setting for the Super IO device.

4.4.9 F81964 Super IO Configuration for IB919EF



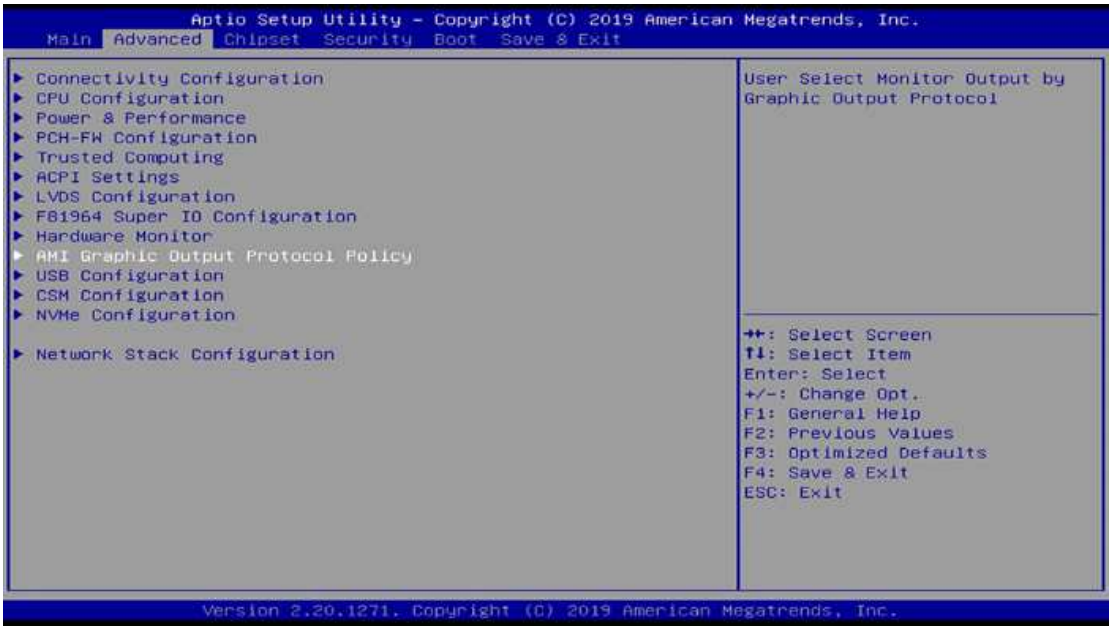
BIOS Setting	Description
Serial Ports Configuration	Sets parameters of serial ports. Enables / Disables the serial port and select an optimal setting for the Super IO device.
Standby Power on S5(Eup)	Enable: Provide the Standby Power for devices Disable: Shutdown the standby power

4.4.10 Hardware Monitor



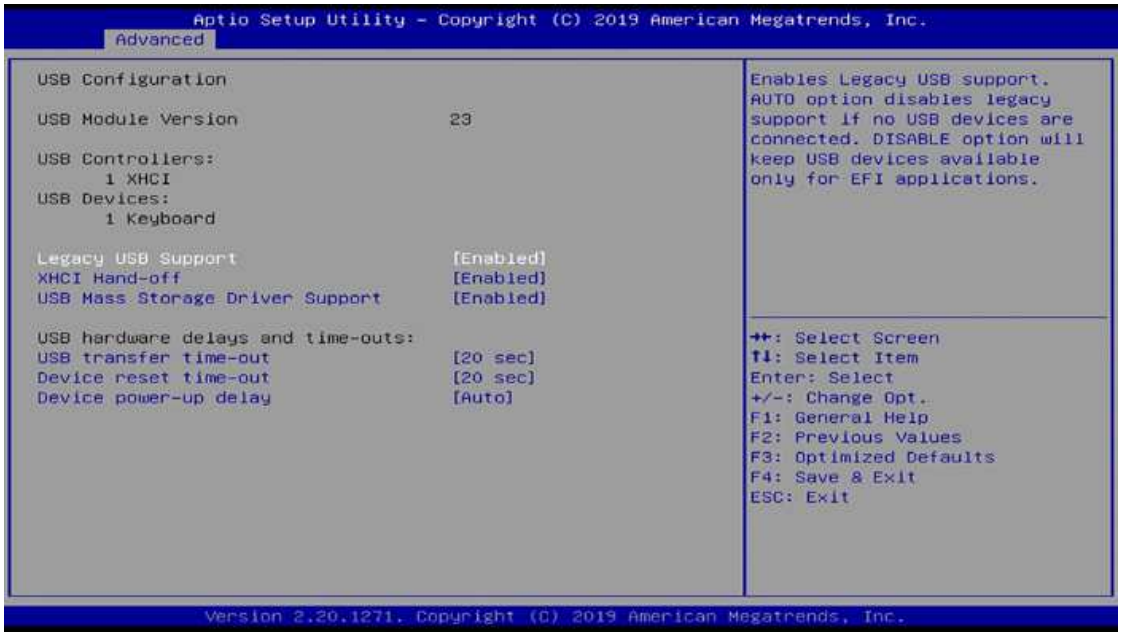
BIOS Setting	Description
CPU Fan smart fan control	Enables / Disables smart fan control.
Temperatures / Voltages	These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.
CPU Shutdown Temperature	Sets a threshold of temperature to shut down if CPU goes overheated. Options: Disabled / 70 °C / 75 °C / 80 °C / 85 °C / 90 °C / 95 °C

4.4.11 AMI Graphic Output Protocol Policy



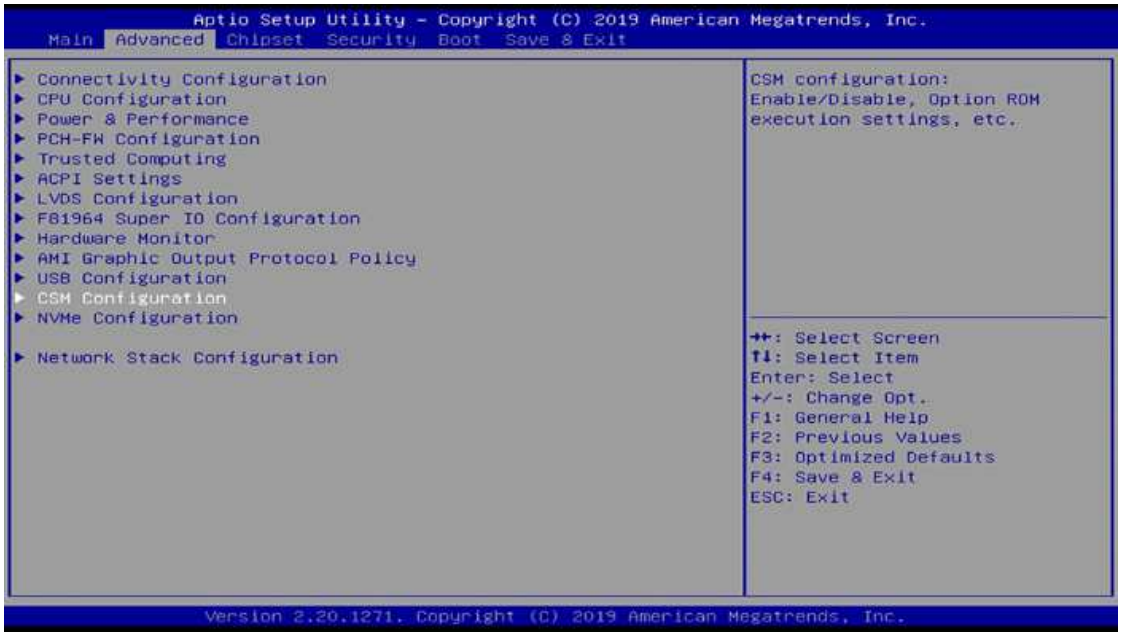
Configure Management Engine Technology Parameters

4.4.12 USB Configuration



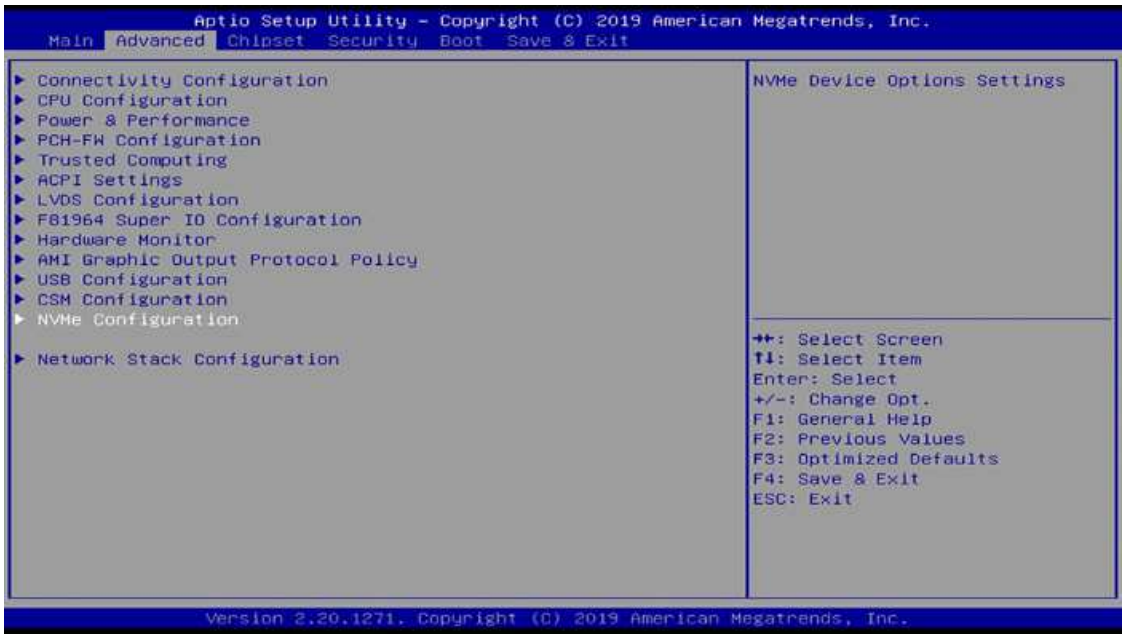
BIOS Setting	Description
Legacy USB Support	• **Enabled** enables Legacy USB support. • **Auto** disables legacy support if there is no USB device connected. • **Disabled** keeps USB devices available only for EFI applications.
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enables / Disables the support for USB mass storage driver.
Port 60/64 Emulation	Enables / Disables the support for I/O port 60h / 64h emulation. This should be enabled for the complete USB keyboard legacy support for non-USB aware OSes.
USB Transfer time-out	The time-out value (1 / 5 10 / 20 secs) for Control, Bulk, and Interrupt transfers.
Device reset time-out	Gives seconds (10 / 20 / 30 / 40 secs) to delay execution of Start Unit command to USB mass storage device.
Device power-up delay	Max.time the device will take before it properly reports itself to the Host Controller. '**Auto**' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

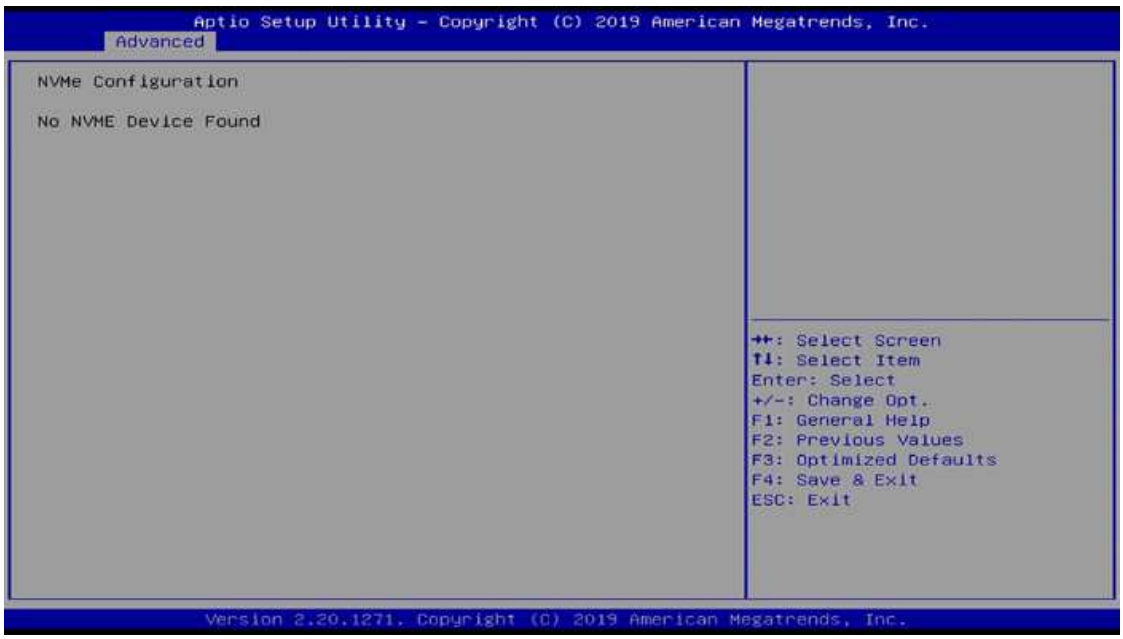
4.4.13 CSM Configuration



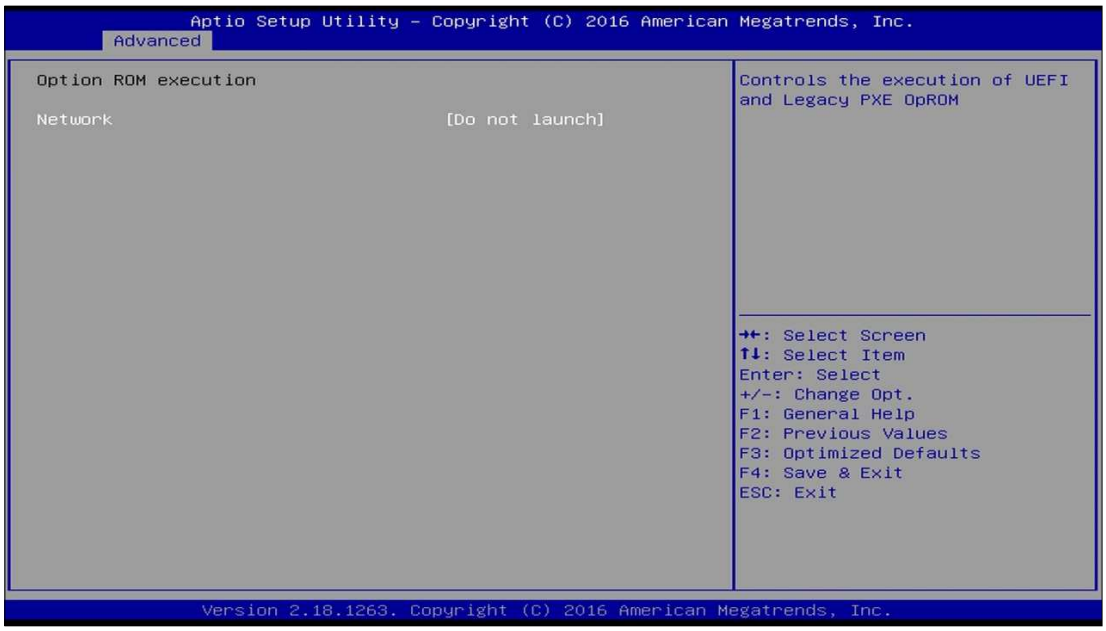
BIOS Setting	Description
Network	Controls the execution of UEFI and Legacy PXE OpROM.

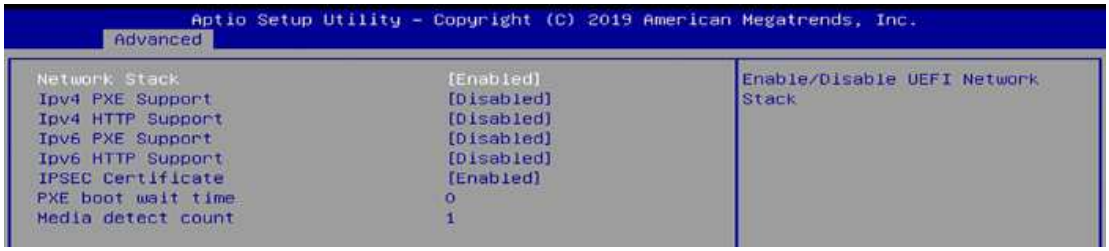
4.4.14 NVMe Configuration





4.4.15 Network Stack Configuration



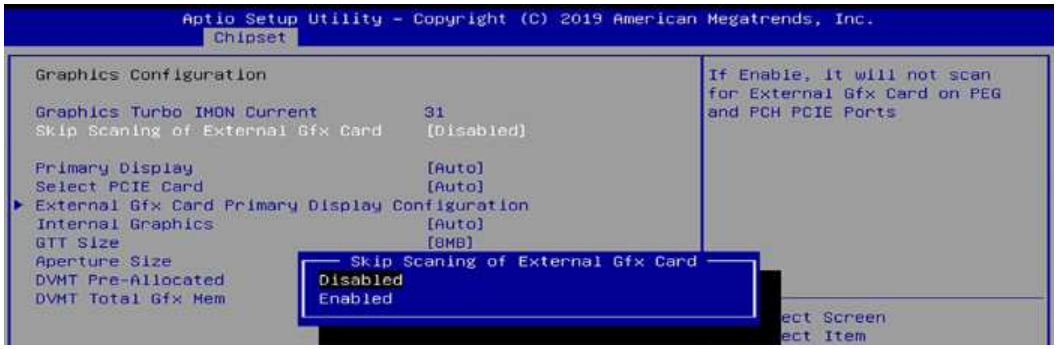


BIOS Setting	Description
Network Stack	Enable/Disable UEFI Network Stack
Ipv4 PXE Support	If disabled, IPv4 PXE boot support will not be available.
Ipv4 HTTP Support	If disabled, IPv4 HTTP boot support will not be available.
Ipv6 PXE Support	If disabled, IPv6 PXE boot support will not be available.
Ipv6 HTTP Support	If disabled, IPv6 HTTP boot support will not be available.
IPSEC Certificate	Support to Enable/Disable IPEC certificate.
PXE boot wait time	Wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value
Media detect count	Number of times the presence of media will be checked. Use either +/- nurmeric keys to set the value.

4.5 Chipset Settings

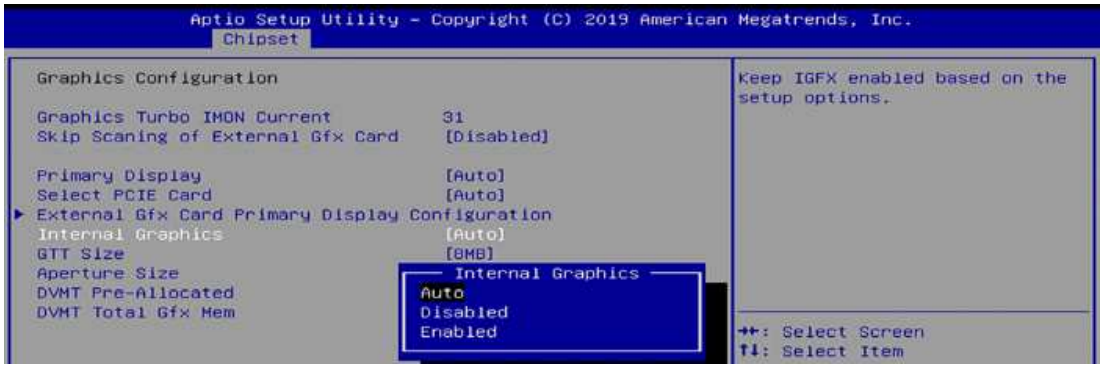
4.5.1 System Agent (SA) Configuration

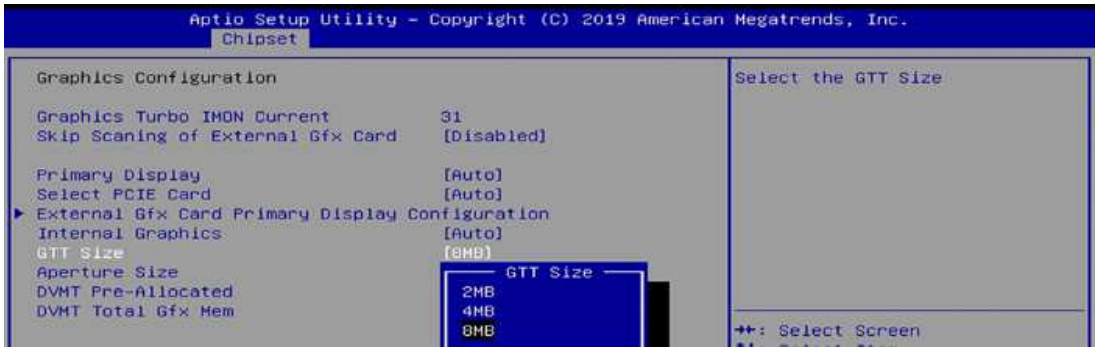
Graphics Configuration:



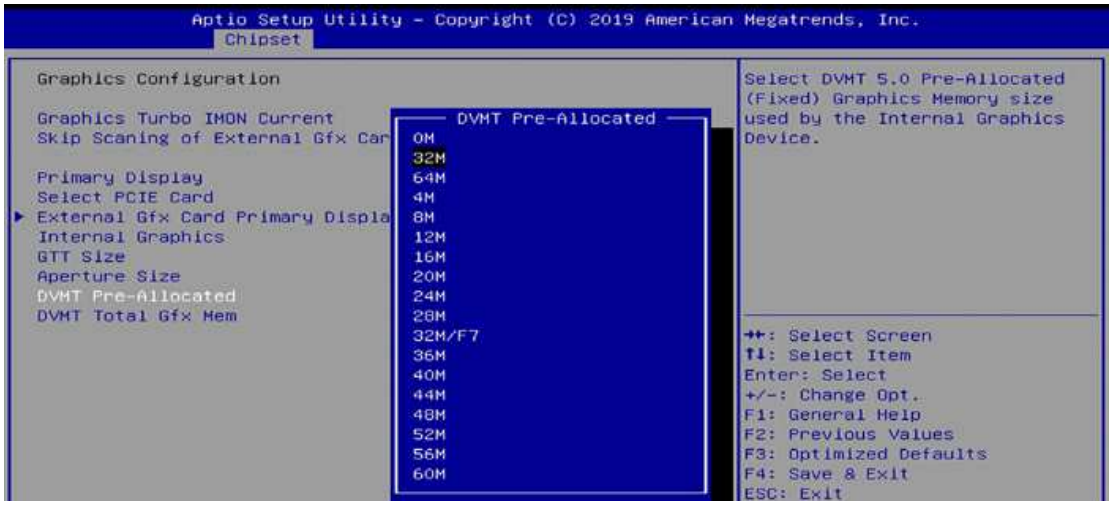

Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Chipset
Graphics Configuration
Graphics Turbo IMON Current 31
Skip Scaning of External Gfx Card [Disabled]
Primary Display [Auto]
Select PCIE Card [Auto]
External Gfx Card Primary Display Configuration
Internal Graphics [Auto]
GTT Size [8MB]
Aperture Size
DVMT Pre-Allocated
DVMT Total Gfx Mem
Select PCIE Card
Auto
Elk Creek 4
PEG Eval
Select the card used on the platform
Auto : Skip GPIO based Power Enable to dGPU
Elk Creek 4: DGPU Power Enable = ActiveLow
PEG Eval : DGPU Power Enable = ActiveHigh
→←: Select Screen
↑↓: Select Item


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Chipset
Graphics Configuration
Graphics Turbo IMON Current 31
Skip Scaning of External Gfx Card [Disabled]
Primary Display [Auto]
Select PCIE Card [Auto]
External Gfx Card Primary Display Configuration
Internal Graphics [Auto]
GTT Size [8MB]
Aperture Size [256MB]
DVMT Pre-Allocated [32M]
DVMT Total Gfx Mem [256M]
External Gfx Card Primary Display Configuration


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Chipset
Graphics Configuration
Graphics Turbo IMON Current 31
Skip Scaning of External Gfx Card [Disabled]
Primary Display [Auto]
Select PCIE Card [Auto]
External Gfx Card Primary Display Configuration
Internal Graphics [Auto]
GTT Size [8MB]
Aperture Size
DVMT Pre-Allocated
DVMT Total Gfx Mem
Internal Graphics
Auto
Disabled
Enabled
Keep IGFX enabled based on the setup options.
→←: Select Screen
↑↓: Select Item


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Chipset
Graphics Configuration
Graphics Turbo IMON Current 31
Skip Scaning of External Gfx Card [Disabled]
Primary Display [Auto]
Select PCIE Card [Auto]
External Gfx Card Primary Display Configuration
Internal Graphics [Auto]
GTT Size [8MB]
Aperture Size
DVMT Pre-Allocated
DVMT Total Gfx Mem
GTT Size
2MB
4MB
8MB
Select the GTT Size
→←: Select Screen


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Chipset
Graphics Configuration
Graphics Turbo IMON Current 31
Skip Scaning of External Gfx Card [Disabled]
Primary Display [Auto]
Select PCIE Card [Auto]
External Gfx Card Primary Display Configuration
Internal Graphics [Auto]
GTT Size
Aperture Size
DVMT Pre-Allocated
DVMT Total Gfx Mem
Aperture Size
128MB
256MB
512MB
1024MB
2048MB
Select the Aperture Size
Note : Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.
→←: Select Screen
↑↓: Select Item

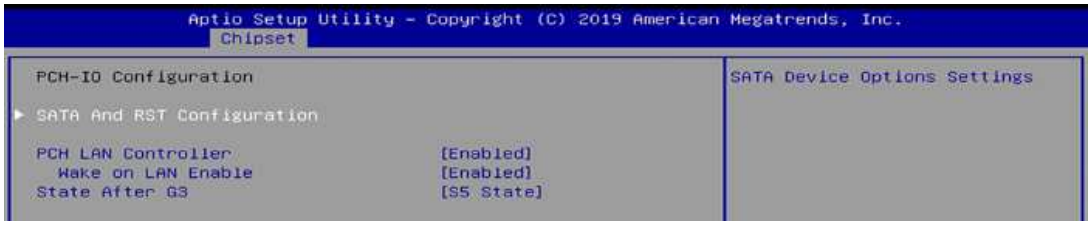

Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Chipset
Graphics Configuration
Graphics Turbo IMON Current
Skip Scaning of External Gfx Car
Primary Display
Select PCIE Card
External Gfx Card Primary Displa
Internal Graphics
GTT Size
Aperture Size
DVMT Pre-Allocated
DVMT Total Gfx Mem
DVMT Pre-Allocated
0M
32M
64M
4M
8M
12M
16M
20M
24M
28M
32M/F7
36M
40M
44M
48M
52M
56M
60M
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Chipset
Graphics Configuration
Graphics Turbo IMON Current 31
Skip Scaning of External Gfx Card [Disabled]
Primary Display [Auto]
Select PCIE Card [Auto]
External Gfx Card Primary Display Configuration
Internal Graphics [Auto]
GTT Size [8MB]
Aperture Size
DVMT Pre-Allocated
DVMT Total Gfx Mem
DVMT Total Gfx Mem
128M
256M
MAX
Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
→←: Select Screen

VT-d

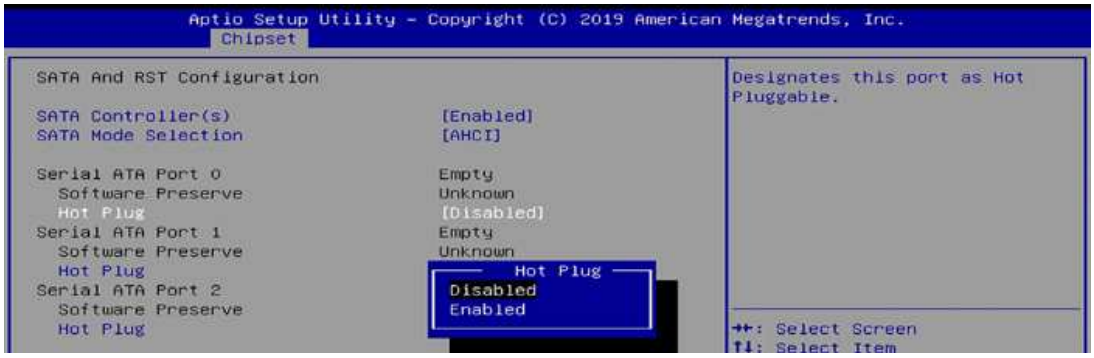

Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Chipset
System Agent (SA) Configuration
SA PCIe Code Version 7.0.96.32
VT-d Supported
Graphics Configuration
VT-d [Enabled]
VT-d
Disabled
Enabled
VT-d capability
→←: Select Screen

4.5.2 PCH-IO Configuration



SATA and RST Configuration:

BIOS Setting	Description
SATA and RST Configuration	SATA device options and settings
SATA Controller(s)	Enables / Disables the Serial ATA.
SATA Mode Selection	Selects IDE or AHCI Mode.
Serial ATA Port 0~2	Enables / Disables Serial Port 0 ~ 2.
SATA Ports Hot Plug	Enables / Disables SATA Ports HotPlug.



BIOS Setting	Description
PCH LAN Controller	Enables / Disables onboard NIC.
Wake on LAN Enable	Enables / Disables integrated LAN to wake the system.
State After G3	Specify what state to go when power is re-applied afater a power failure (G3 state).

4.6 Security Settings

BIOS Setting	Description
Setup Administrator Password	Sets an administrator password for the setup utility.
User Password	Sets a user password.
Secure Boot	Secure Boot feature is Active if Secure Boot is enabled. Platform Key(PK) is enrolled and the system is in user mode. The mode change requires platform reset.

4.7 Boot Settings

BIOS Setting	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	Selects the keyboard NumLock state.
Quiet Boot	Enables / Disables Quiet Boot option.
Boot Mode Select	Selects boot mode LEGACY/UEFI
FIXED BOOT ORDER Priorities	Configures the boot order priorities. Up to 9 boot options can be configured.

4.8 Save & Exit Settings

BIOS Setting	Description
Save Changes and Exit	Exits system setup after saving the changes.
Discard Changes and Exit	Exits system setup without saving any changes.
Save Changes and Reset	Resets the system after saving the changes.
Discard Changes and Reset	Resets system setup without saving any changes.
Save Changes	Saves changes done so far to any of the setup options.
Discard Changes	Discards changes done so far to any of the setup options.
Restore Defaults	Restores / Loads defaults values for all the setup options.
Save as User Defaults	Saves the changes done so far as User Defaults.
Restore User Defaults	Restores the user defaults to all the setup options.

Appendix

This section provides the mapping addresses of peripheral devices and the sample code of watchdog timer configuration.

- I/O Port Address Map
- Interrupt Request Lines (IRQ)
- Digital I/O Sample Code
- Watchdog Timer Configuration

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x00000000-0x00000CF7	PCI Express Root Complex
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x0000002E-0x0000002F	Motherboard resources
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x00000040-0x00000043	System timer
0x0000004E-0x0000004F	Motherboard resources
0x00000050-0x00000053	System timer
0x00000060-0x00000060	Standard PS/2 Keyboard
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000064-0x00000064	Standard PS/2 Keyboard
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000080-0x00000080	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B2-0x000000B3	Motherboard resources
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller

Address	Device Description
0x000002E8-0x000002EF	Communications Port (COM4)
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003E8-0x000003EF	Communications Port (COM3)
0x000003F8-0x000003FF	Communications Port (COM1)
0x000004D0-0x000004D1	Programmable interrupt controller
0x00000680-0x0000069F	Motherboard resources
0x00000A00-0x00000A0F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x0000164E-0x0000164F	Motherboard resources
0x00001800-0x000018FE	Motherboard resources
0x00001854-0x00001857	Motherboard resources
0x00002000-0x000020FE	Motherboard resources
0x00003000-0x00003FFF	Intel(R) PCI Express Root Port #8 – 9D8F
0x00004000-0x0000403F	Intel(R) UHD Graphics 620
0x00004060-0x0000407F	Standard SATA AHCI Controller
0x00004080-0x00004083	Standard SATA AHCI Controller
0x00004090-0x00004097	Standard SATA AHCI Controller
0x0000EFA0-0x0000EFBF	Intel(R) SMBus – 9DA3

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System timer
IRQ 1	Standard PS/2 Keyboard
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 5	Communications Port (COM3)
IRQ 7	Communications Port (COM4)
IRQ 11	PCI Standard RAM Controller
IRQ 11	Intel(R) Thermal Subsystem - A379
IRQ 11	Intel(R) SMBus – 9DA3
IRQ 12	Microsoft PS/2 Mouse
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3450
IRQ 16	High Definition Audio Controller
IRQ 16	Intel(R) SD Controller
IRQ 55~ IRQ 511	Microsoft ACPI-Compliant System
IRQ 4294967281	Intel(R) Management Engine Interface
IRQ 4294967282	Intel(R) Dual Band Wireless-AC 7265
IRQ 4294967283-88	Intel(R) I210 Gigabit Network Connection #3
IRQ 4294967289	Intel(R) USB 3.1 eXtensible Host Controller - 1.10 (Microsoft)
IRQ 4294967290	Intel(R) UHD Graphics 620
IRQ 4294967291	Intel(R) Ethernet Connection (6) I219-LM
IRQ 4294967292	Standard SATA AHCI Controller
IRQ 4294967293	Intel(R) PCI Express Root Port #9 – 9DB0
IRQ 4294967294	Intel(R) PCI Express Root Port #8 – 9DBF

C. Digital I/O Sample Code

1. DIO Sample Code: The file F81846.cpp

```
//=====================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====================================================================
#include "F81846.H"
#include <dos.h>
//=====================================================================
unsigned int F81846_BASE;
void Unlock_F81846 (void);
void Lock_F81846 (void);
//=====================================================================
unsigned int Init_F81846(void)
{
	unsigned int result;	//
	unsigned char ucDid;

	F81846_BASE = 0x4E;
	result = F81846_BASE;

	ucDid = Get_F81846_Reg(0x20);
	if ((ucDid == 0x07) || (ucDid == 0x10) || (ucDid == 0x15)) //Fintek
81865/81846/81846/81946/81846
	{	goto Init_Finish;}

	F81846_BASE = 0x2E;
	result = F81846_BASE;

	ucDid = Get_F81846_Reg(0x20);
	if ((ucDid == 0x07) || (ucDid == 0x10) || (ucDid == 0x15))	//Fintek
81865/81846/81846/81946/81846
	{	goto Init_Finish;}

	F81846_BASE = 0x00;
	result = F81846_BASE;

Init_Finish:
	return (result);
}
//=====================================================================
void Unlock_F81846 (void)
{
	outportb(F81846_INDEX_PORT, F81846_UNLOCK);
	outportb(F81846_INDEX_PORT, F81846_UNLOCK);
}
//=====================================================================
```

```
void Lock_F81846 (void)
{
	outportb(F81846_INDEX_PORT, F81846_LOCK);
}
//=====================================================================
void Set_F81846_LD( unsigned char LD)
{
	Unlock_F81846();
	outportb(F81846_INDEX_PORT, F81846_REG_LD);
	outportb(F81846_DATA_PORT, LD);
	Lock_F81846();
}
//=====================================================================
void Set_F81846_Reg( unsigned char REG, unsigned char DATA)
{
	Unlock_F81846();
	outportb(F81846_INDEX_PORT, REG);
	outportb(F81846_DATA_PORT, DATA);
	Lock_F81846();
}
//=====================================================================
unsigned char Get_F81846_Reg(unsigned char REG)
{
	unsigned char Result;
	Unlock_F81846();
	outportb(F81846_INDEX_PORT, REG);
	Result = inportb(F81846_DATA_PORT);
	Lock_F81846();
	return Result;
}
//=====================================================================
```

2. DIO Sample Code: The file F81846.h

```
//=====================================================================
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//=====================================================================
#ifndef __F81846_H
#define __F81846_H              1
//=====================================================================
#define     F81846_INDEX_PORT           (F81846_BASE)
#define     F81846_DATA_PORT            (F81846_BASE+1)
//=====================================================================
#define     F81846_REG_LD               0x07
//=====================================================================
#define F81846_UNLOCK               0x87
#define     F81846_LOCK                 0xAA
//=====================================================================
unsigned int Init_F81846(void);
void Set_F81846_LD( unsigned char);
void Set_F81846_Reg( unsigned char, unsigned char);
unsigned char Get_F81846_Reg( unsigned char);
//=====================================================================
#endif      //__F81846_H
```

3. DIO Sample Code: The file MAIN.CPP

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81846.H"
//---------------------------------------------------------------------------
void ClrKbBuf(void);
int main (int argc, char *argv[]);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char result;
        char SIO;

        SIO = Init_F81846();
        if (SIO == 0)
        {
                printf("Can not detect Fintek F81846, program abort.\n");
                return(1);
        }

           Set_F81846_LD(0x06);
//switch to logic device 6

           result = ((Get_F81846_Reg(0xE2)) & 0x04) ? 0x01 : 0x00;          //result = 0x00 GPI is
Low / result = 0x01 GPI is High

        return (result);
}
```

D. Watchdog Timer Configuration

The Watchdog Timer (WDT) is used to generate a variety of output signals after a user programmable count. The WDT is suitable for the use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven.

Under normal circumstance, you will need to restart the WDT at regular intervals before the timer counts to zero.

Sample Code

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81846.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]); void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;
        printf("Fintek 81846 watch dog program\n");
        SIO = Init_F81846();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81846, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
```

```
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime); }
        else
        {       DisableWDT();  }
        return 0;
}
//-------------------------------------------------------------------------
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_F81846_Reg(0x2B);
        bBuf &= (~0x20);
        Set_F81846_Reg(0x2B, bBuf);             //Enable WDTO

        Set_F81846_LD(0x07);                    //switch to logic device 7
        Set_F81846_Reg(0x30, 0x01);             //enable timer

        bBuf = Get_F81846_Reg(0xF5);
        bBuf &= (~0x0F);
        bBuf |= 0x52;
        Set_F81846_Reg(0xF5, bBuf);             //count mode is second
        Set_F81846_Reg(0xF6, interval);         //set timer
        bBuf = Get_F81846_Reg(0xFA);
        bBuf |= 0x01;
        Set_F81846_Reg(0xFA, bBuf);             //enable WDTO output

        bBuf = Get_F81846_Reg(0xF5);
        bBuf |= 0x20;
        Set_F81846_Reg(0xF5, bBuf);             //start counting
}
//-------------------------------------------------------------------------
void DisableWDT(void)
{
        unsigned char bBuf;
        Set_F81846_LD(0x07);                    //switch to logic device 7
        bBuf = Get_F81846_Reg(0xFA);
        bBuf &= ~0x01;
        Set_F81846_Reg(0xFA, bBuf);             //disable WDTO output

        bBuf = Get_F81846_Reg(0xF5);
        bBuf &= ~0x20;
        bBuf |= 0x40;
        Set_F81846_Reg(0xF5, bBuf);             //disable WDT
}
//-------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81846.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81846_BASE; void Unlock_F81846 (void); void Lock_F81846 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81846(void)
{
	unsigned int result;
	unsigned char ucDid;

	F81846_BASE = 0x4E;
	result = F81846_BASE;

	ucDid = Get_F81846_Reg(0x20);
	if (ucDid == 0x07)			//Fintek 81846
	{	goto Init_Finish;}

	F81846_BASE = 0x2E;
	result = F81846_BASE;

	ucDid = Get_F81846_Reg(0x20);
	if (ucDid == 0x07)			//Fintek 81846
	{	goto Init_Finish;}

	F81846_BASE = 0x00;
	result = F81846_BASE;

Init_Finish:
	return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81846 (void)
{
	outportb(F81846_INDEX_PORT, F81846_UNLOCK);
	outportb(F81846_INDEX_PORT, F81846_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81846 (void)
{
	outportb(F81846_INDEX_PORT, F81846_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81846_LD( unsigned char LD)
{
	Unlock_F81846();
	outportb(F81846_INDEX_PORT, F81846_REG_LD);
```

```
        outportb(F81846_DATA_PORT, LD); Lock_F81846();
}
//-----------------------------------------------------------------------------
void Set_F81846_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_F81846();
        outportb(F81846_INDEX_PORT, REG);
        outportb(F81846_DATA_PORT, DATA);
        Lock_F81846();
}
//-----------------------------------------------------------------------------
unsigned char Get_F81846_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81846();
        outportb(F81846_INDEX_PORT, REG);
        Result = inportb(F81846_DATA_PORT);
        Lock_F81846();
        return Result;
}
//-----------------------------------------------------------------------------
```

```
//-----------------------------------------------------------------------------
//
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// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
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// PURPOSE.
//
//-----------------------------------------------------------------------------
#ifndef         F81846_H
#define         F81846_H     1
//-----------------------------------------------------------------------------
#define     F81846_INDEX_PORT      (F81846_BASE)
#define     F81846_DATA_PORT       (F81846_BASE+1)
//-----------------------------------------------------------------------------
#define     F81846_REG_LD      0x07
//-----------------------------------------------------------------------------
#define F81846_UNLOCK 0x87
#define     F81846_LOCK  0xAA
//-----------------------------------------------------------------------------
unsigned int Init_F81846(void);
void Set_F81846_LD( unsigned char);
void Set_F81846_Reg( unsigned char, unsigned char); unsigned char
Get_F81846_Reg( unsigned char);
//-----------------------------------------------------------------------------
#endif //     F81846_H
```