IBQ800 Series

Qseven CPU Module

With Intel® Atom™ x7/x5

User's Manual

Version 1.0
(Oct. 2018)

Compliance

CE

This product has passed CE tests for environmental specifications and limits. This product is in accordance with the directives of the European Union (EU). In a domestic environment, this product may cause radio interference in which case users may be required to take adequate measures.

FC

This product has been tested and found to comply with the limits for a Class B device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer's instructions, may cause harmful interference to radio communications.

WEEE

This product must not be disposed of as normal household waste, in accordance with the EU directive of for waste electrical and electronic equipment (WEEE - 2012/19/EU). Instead, it should be disposed of by returning it to a municipal recycling collection point. Check local regulations for disposal of electronic products.

Green IBASE

This product is compliant with the current RoHS restrictions and prohibits use of the following substances in concentrations exceeding 0.1% by weight (1000 ppm) except for cadmium, limited to 0.01% by weight (100 ppm).

- Lead (Pb)
- Mercury (Hg)
- Cadmium (Cd)
- Hexavalent chromium (Cr6+)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ether (PBDE)

Important Safety Information

Carefully read the precautions before using the board.

Environmental conditions:

- Use this product in environments with ambient temperatures between -40˚C and 85˚C.
- Do not leave this product in an environment where the storage temperature may be below 40° C or above 90° C. To prevent from damages, the product must be used in a controlled environment.

Care for your IBASE products:

- Before cleaning the PCB, unplug all cables and remove the battery.
- Clean the PCB with a circuit board cleaner, degreaser or use cotton swabs and alcohol.
- Vacuum the dust with a computer vacuum cleaner to prevent the fan from being clogged.

WARNING

Attention during use:

- Do not use this product near water.
- Do not spill water or any other liquids on this product.
- Do not place heavy objects on the top of this product.

Anti-static precautions

- Wear an anti-static wrist strap to avoid electrostatic discharge.
- Place the PCB on an anti-static kit or mat.
- Hold the edges of PCB when handling.
- Touch the edges of non-metallic components of the product instead of the surface of the PCB.
- Ground yourself by touching a grounded conductor or a grounded bit of metal frequently to discharge any static.

CAUTION

Danger of explosion if the internal lithium-ion battery is replaced by an incorrect type. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions or recycle them at a local recycling facility or battery collection point.

Warranty Policy

- **IBASE standard products:**

  24-month (2-year) warranty from the date of shipment. If the date of shipment cannot be ascertained, the product serial numbers can be used to determine the approximate shipping date.

- **3rd-party parts:**

  12-month (1-year) warranty from delivery for the 3rd-party parts that are not manufactured by IBASE, such as CPU, CPU cooler, memory, storage devices, power adapter, panel and touchscreen.

* PRODUCTS, HOWEVER, THAT FAIL DUE TO MISUSE, ACCIDENT, IMPROPER INSTALLATION OR UNAUTHORIZED REPAIR SHALL BE TREATED AS OUT OF WARRANTY AND CUSTOMERS SHALL BE BILLED FOR REPAIR AND SHIPPING CHARGES.

Technical Support & Services

1. Visit the IBASE website at www.ibase.com.tw to find the latest information about the product.
2. If you need any further assistance from your distributor or sales representative, prepare the following information of your product and elaborate upon the problem.
   - Product model name
   - Product serial number
   - Detailed description of the problem
   - The error messages in text or in screenshots if there is any
   - The arrangement of the peripherals
   - Software in use (such as OS and application software, including the version numbers)
3. If repair service is required, you can download the RMA form at http://www.ibase.com.tw/english/Supports/RMAService/. Fill out the form and contact your distributor or sales representative.

Table of Contents

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Chapter 1
General Information

The information provided in this chapter includes:

- Features
- Packing List
- Optional Accessories
- Specifications
- Block Diagram
- Board Overview
- Board Dimensions

1.1 Introduction

IBQ800 is a CPU module in Qseven form factor with the Intel® Atom™ x7/x5 processor, and its size is smaller than other computer-on-module standards like COMe or ETX. It comes with a 230-pin MXM2 SMT edge connector for the power and signal lanes connection to a carrier board. It also features the LPDDR4 onboard memory, TPM 2.0, SDIO, and optional eMMC 5.0.

Photo of IBQ800

1.2 Features

- Onboard Intel® Atom™ x7-E3950 / x5-E3930 processor
- Onboard LPDDR4 memory
- Intel® I210IT PCIe GbE LAN
- Wide-range operating temperature
- Configurable watchdog timer and TPM 2.0
- eMMC 5.0 (Optional)

1.3 Packing List

Your product package should include the items listed below. If any of the items below is missing, contact the distributor or dealer from whom you purchased the product.

- IBQ800 Qseven CPU Module
- Disk (including drivers and flash memory utility)
- This User's Manual

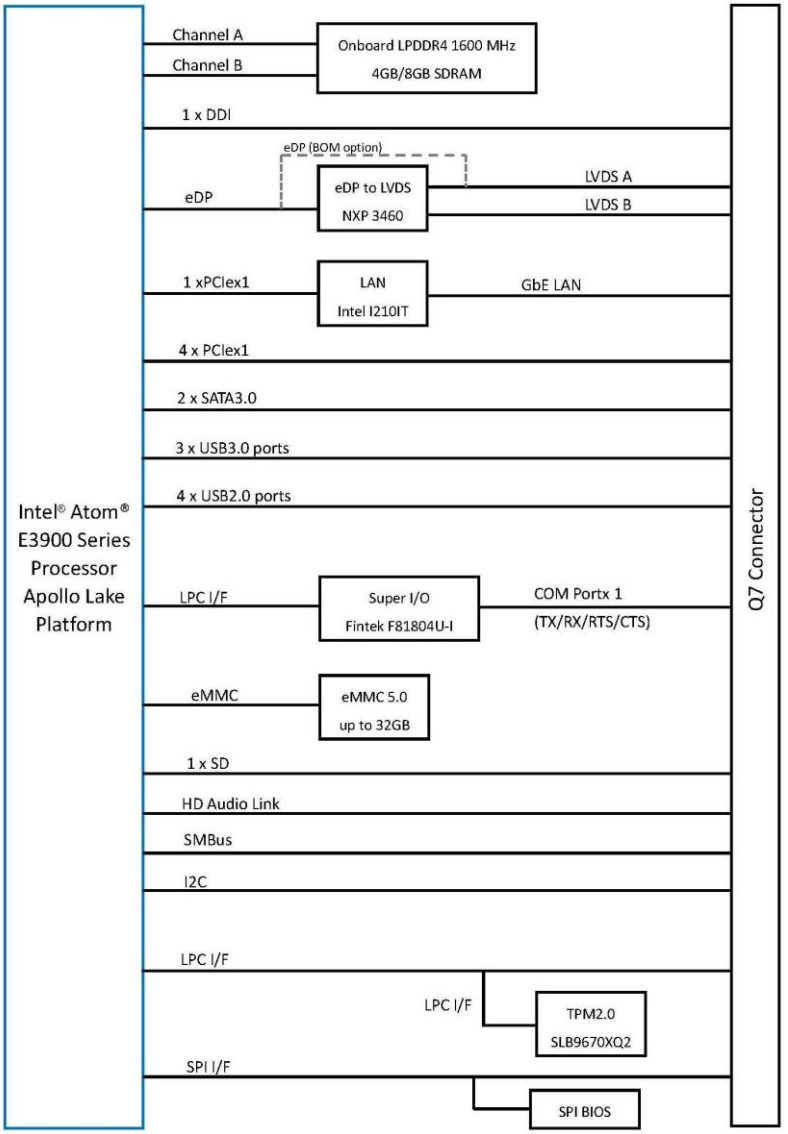
1.4 Specifications

Product Name	• IBQ800-x7LVe8G: E3950 + LVDS + eMMC + 8 GB memory • IBQ800-x5LVe8G: E3930 + LVDS + eMMC + 8 GB memory • IBQ800-x5LVe: E3930 + LVDS + eMMC + 4 GB memory • IBQ800-x5: E3930 + eDP + 4 GB memory "IBQ800" will be the model name printed on PCB surface
Form Factor	Qseven R2.1
CPU Type / Speed	• Intel® Atom™ QC x7 E3950, 2GHz, 2MB cache, 12W TDP (IBQ800-I50) • Intel® Atom™ DC x5 E3930, 1.8GHz, 2MB cache, 6W TDP (IBQ800-I30) Package = FCBGA1296,Type-3, 31 x 24 x 1.318 mm,14 nm, Tj= -0˚ C to +105˚ C
BIOS	AMI BIOS
Memory	Intel® Atom™ SoC integrated memory controller - Onboard LPDDR4 1600MHz 8GB or 4GB
Graphics	Intel® SoC integrated Gen9-LP
Display	1 x DDI port, thru NXP PTN3460 for eDP to LVDS, or 1 x eDP
LAN	Intel® I210IT GbE x 1, thru an RJ45 on carrier board
USB	Derived from Qseven CPU module: • 3 x USB 3.0 • 4 x USB 2.0
Expansion	4 x PCIe (x1)
SATA	2 x SATA 3.0 (6Gb/sec.) thru interface on carrier board
Audio	Intel® Atom™ SoC built-in HD Audio controller

eMMC	Onboard eMMC 5.0, 32GB (Optional), supports Windows & Linux O.S boot only)
TPM 2.0	Yes
SD	1 x SD 3.0
Super I/O	Fintek F81804U-I, supports 1 x UART ports (RX/ TX/ RTS/ CTS only) and 4-second delay to power off
Watchdog Timer	Yes (256 segments, 0= disable ,1, 2…255. sec/min)
H/W Monitor	Yes
Connector to Carrier Board	One 230-pin golden finger (Qseven 2.1 standard)
Power	+5V, 5VSB
Certification	CE (EN55032:2012), FCC Class B
OS support	• Windows 10 (64-bit) • Linux (Ubuntu)
Board Size	70 x 70 mm (2.76” x 2.76”)
RoHS	Yes
Temperature	• **Operating:** -40 ~ 85 °C (-40 ~ 185 °F) • **Storage:** -40 ~ 90 °C (-40 ~ 194 °F)
Relative Humidity	90%, non-condensing at 60°C
Others	Heat spreader IP416 will be the carrier board for testing

All specifications are subject to change without prior notice.

1.5 Block Diagram



1.6 Overview

Top View

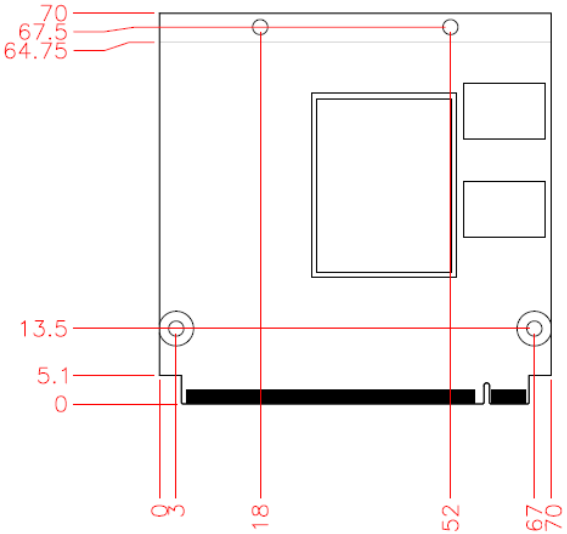
Bottom View

Photos of IBQ800

* The photos above are for reference only. Some minor components may differ.

1.7 Dimensions

Unit: mm



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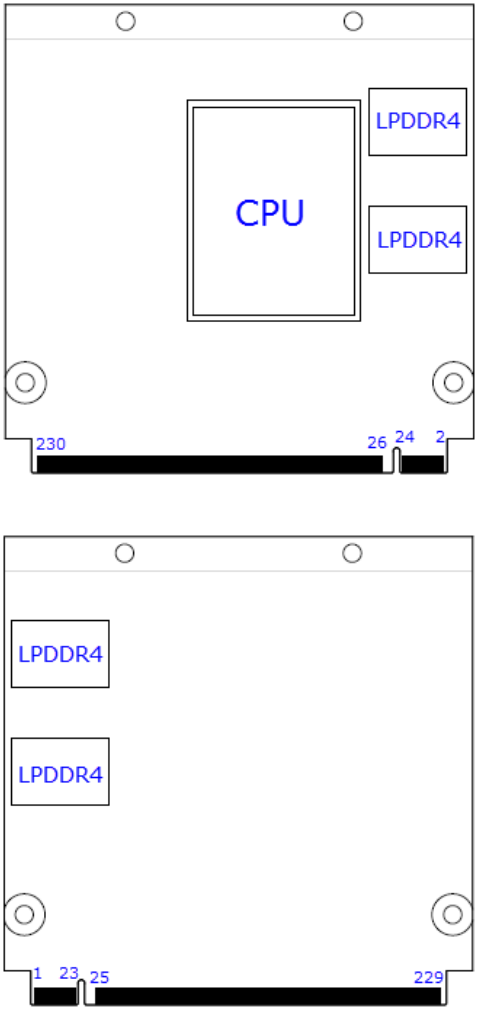
Chapter 2
Pin Definition

This section provides the pin definition of the 230-pin MXM2 SMT edge connector.

2.1 Connector Location



Board diagram of IBQ800

2.1.1 Edge Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Ground
3	GBE_MDI3-	4	GBE_MDI2-
5	GBE_MDI3+	6	GBE_MDI2+
7	GBE_LINK100#	8	GBE_LINK1000#
9	GBE_MDI1-	10	GBE_MDI0-
11	GBE_MDI1+	12	GBE_MDI0+
13	GBE_LINK#	14	GBE_ACT#
15	GBE_CTREF	16	SUS_S5#
17	WAKE#	18	SUS_S3#
19	Reserved	20	PWRBTN#
21	Reserved	22	Reserved
23	Ground	24	Ground
KEY		KEY	
25	Ground	26	PWGIN
27	BATLOW#	28	RSTBTN#
29	SATA0_TX+	30	SATA1_TX+
31	SATA0_TX-	32	SATA1_TX-
33	SATA_ACT#	34	Ground
35	SATA0_RX+	36	SATA1_RX+
37	SATA0_RX-	38	SATA1_RX-
39	Ground	40	Ground
41	BIOS_DISABLE#	42	SDIO_CLK#
43	SDIO_CD#	44	Reserved
45	SDIO_CMD	46	SDIO_WP
47	SDIO_PWR#	48	SDIO_DATA1
49	SDIO_DATA0	50	SDIO_DATA3
51	SDIO_DATA2	52	Reserved
53	Reserved	54	Reserved
55	Reserved	56	Reserved
57	Ground	58	Ground
59	HAD_SYNC	60	SMB_CLK
61	HAD_RST#	62	SMB_DAT
63	HAD_BITCLK	64	SMB_ALERT#
65	HAD_SDI	66	GP0_I2C_CLK
67	HAD_SDO	68	GP0_I2C_DAT
69	THRM#	70	WDTRIG#
71	THRMTRIP#	72	WDOUT
73	Ground	74	Ground

Pin	Signal Name	Pin	Signal Name
75	U3_USB0_TX_N	76	U3_USB0_RX_N
77	U3_USB0_TX_P	78	U3_USB0_RX_P
79	USB_OC1#	80	USB_OC1#
81	U3_USB2_TX_N	82	U3_USB2_RX_N
83	U3_USB2_TX_P	84	U3_USB2_RX_P
85	USB_OC1#	86	USB_OC0#
87	U2_USB3_N	88	U2_USB2_N
89	U2_USB3_P	90	U2_USB2_P
91	Reserved	92	Reserved
93	U2_USB0_N	94	U2_USB1_N
95	U2_USB0_P	96	U2_USB1_P
97	Ground	98	Ground
99	eDP0_TX0+/LVDS_A0+	100	LVDS_B0+
101	eDP0_TX0-/LVDS_A0-	102	LVDS_B0-
103	eDP0_TX1+/LVDS_A1+	104	LVDS_B1+
105	eDP0_TX1-/LVDS_A1-	106	LVDS_B1-
107	eDP0_TX2+/LVDS_A2+	108	LVDS_B2+
109	eDP0_TX2-/LVDS_A2-	110	LVDS_B2-
111	LVDS_VDD_EN	112	LVDS_BKLT_EN
113	eDP0_TX3+/LVDS_A3+	114	LVDS_B3+
115	eDP0_TX3-/LVDS_A3-	116	LVDS_B3-
117	Ground	118	Ground
119	eDP0_AUX+/LVDS_A_CLK+	120	LVDS_B_CLK+
121	eDP0_AUX-/LVDS_A_CLK-	122	LVDS_B_CLK-
123	LVDS_BKLT_CTRL	124	Reserved
125	LVDS_DDC_DAT	126	eDP0_HPD#
127	LVDS_DDC_CLK	128	Reserved
129	Reserved	130	Reserved
131	DP_LANE3+/TMDS_CLK+	132	U3_USB1_TX_N
133	DP_LANE3-/TMDS_CLK-	134	U3_USB1_TX_P
135	Ground	136	Ground
137	DP_LANE1+/TMDS_LANE1+	138	DP_AUX+
139	DP_LANE1-/TMDS_LANE1-	140	DP_AUX-
141	Ground	142	Ground
143	DP_LANE2+/TMDS_LANE0+	144	U3_USB1_RX_N
145	DP_LANE2-/TMDS_LANE0-	146	U3_USB1_RX_P
147	Ground	148	Ground
149	DP_LANE0+/TMDS_LANE2+	150	HDMI_CTRL_DAT
151	DP_LANE0-/TMDS_LANE2-	152	HDMI_CTRL_CLK
153	DP_HDMI_HPD#	154	DP_HPD#

Pin	Signal Name	Pin	Signal Name
155	PCIE_REF_CLK+	156	PCIE_WAKE#
157	PCIE_REF_CLK-	158	PCIE_RST#
159	Ground	160	Ground
161	PCIE3_TX+	162	PCIE3_RX+
163	PCIE3_TX-	164	PCIE3_RX-
165	Ground	166	Ground
167	PCIE2_TX+	168	PCIE2_RX+
169	PCIE2_TX-	170	PCIE2_RX-
171	UART0_TX	172	UART0_RTS#
173	PCIE1_TX+	174	PCIE1_RX+
175	PCIE1_TX-	176	PCIE1_RX-
177	UART0_RX	178	UART0_CTS#
179	PCIE0_TX+	180	PCIE0_RX+
181	PCIE0_TX-	182	PCIE0_RX-
183	Ground	184	Ground
185	LPC_AD0	186	LPC_AD1
187	LPC_AD2	188	LPC_AD3
189	LPC_CLK	190	LPC_FRAME#
191	LPC_SERIRQ	192	LPC_LDRQ#
193	VCC_RTC	194	SPKR
195	FAN_TACHOIN	196	FAN_PWMOUT
197	Ground	198	Ground
199	SPI_MOSI	200	SPI_CS0#
201	SPI_MISO	202	SPI_CS1#
203	SPI_SCK	204	NC
205	VCC_5V_SB	206	VCC_5V_SB
207	NC	208	NC
209	NC	210	NC
211	NC	212	NC
213	NC	214	NC
215	NC	216	NC
217	NC	218	NC
219	VCC	220	VCC
221	VCC	222	VCC
223	VCC	224	VCC
225	VCC	226	VCC
227	VCC	228	VCC
229	VCC	230	VCC

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Chapter 3
Drivers Installation

This chapter introduces installation of the following drivers:

- Intel® Chipset Software Installation Utility
- Graphics Driver
- HD Audio Driver
- Intel® Trusted Execution Engine Drivers
- Intel® Serial I/O Drivers
- LAN Driver

3.1 Introduction

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find anything missing, please contact the distributor where you made the purchase. The contents of this section include the following:

Note: After installing your Windows operating system, you must install the Intel® Chipset Software Installation Utility first before proceeding with the drivers installation.

3.2 Intel® Chipset Software Installation Utility

The Intel® Chipset drivers should be installed first before the software drivers to install INF files for Plug & Play function for Intel chipset components. Follow the instructions below to complete the installation.

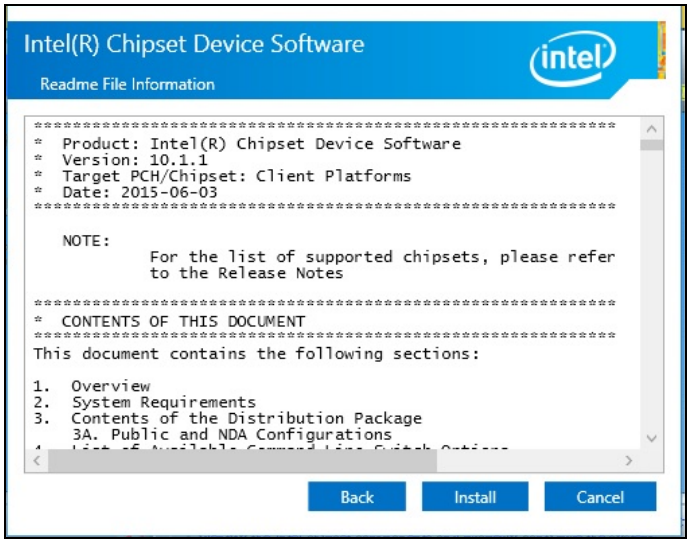
1. Insert the disk enclosed in the package with the board. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.

2. Click **Intel(R) Chipset Software Installation Utility**.

3. When the *Welcome* screen to the Intel® Chipset Device Software appears, click **Next** to continue.

4. Click **Yes** to accept the software license agreement and proceed with the installation process.

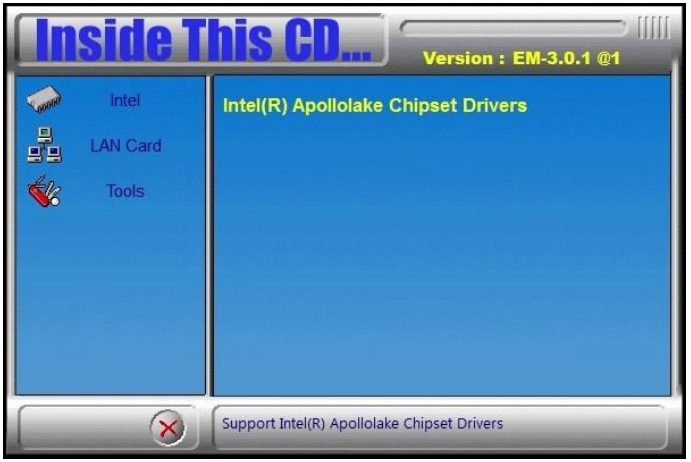
5. On the *Readme File Information* screen, click **Install** for installation.



6. As the driver is completely installed, restart the computer for changes to take effect.

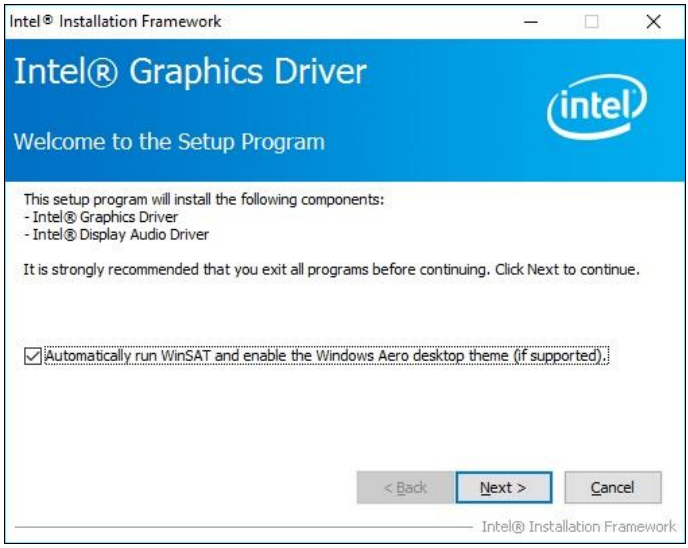
3.3 Graphics Driver Installation

1. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.



2. Click **Intel(R) Apollolake Graphics Driver**.

3. When the *Welcome* screen appears, click **Next** to continue.

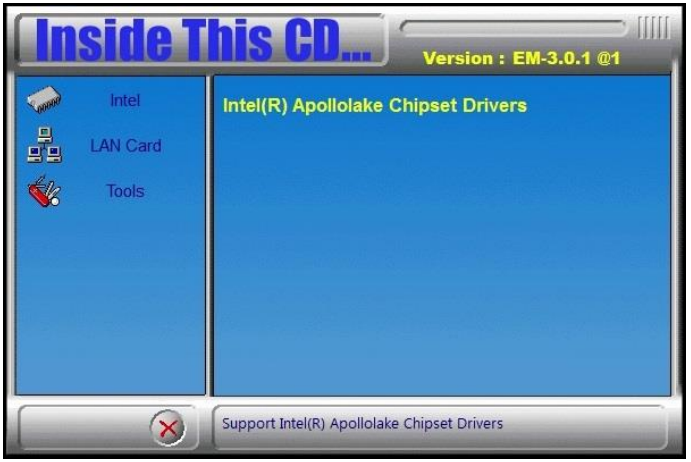


4. Click **Yes** to accept the license agreement and click **Next** until the installation starts.

5. As the driver is completely installed, restart the computer for changes to take effect.

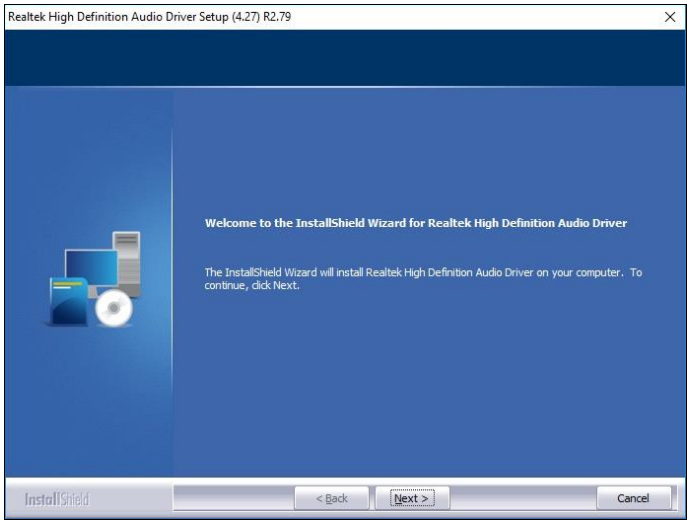
3.4 HD Audio Driver Installation

1. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.



2. Click **Realtek High Definition Audio Driver**.

3. On the *Welcome* screen of the InstallShield Wizard, click **Next**.



4. Click **Next** until the installation starts.

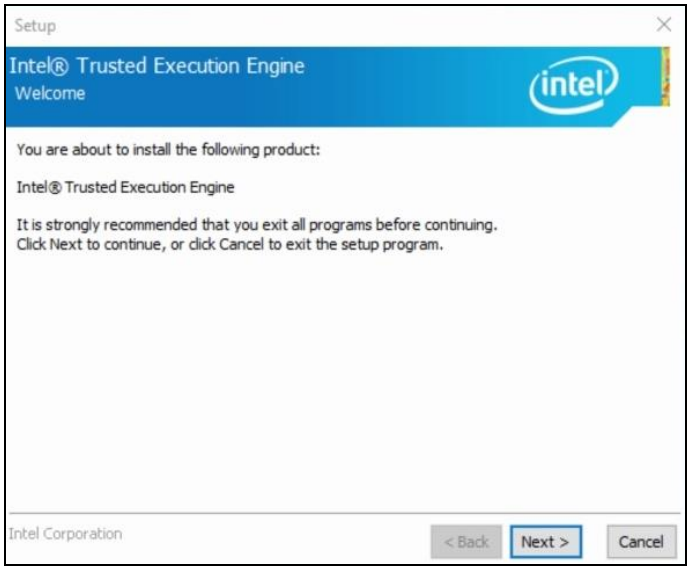
5. As the driver is completely installed, restart the computer for changes to take effect.

3.5 Intel® Trusted Execution Engine Drivers

1. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.

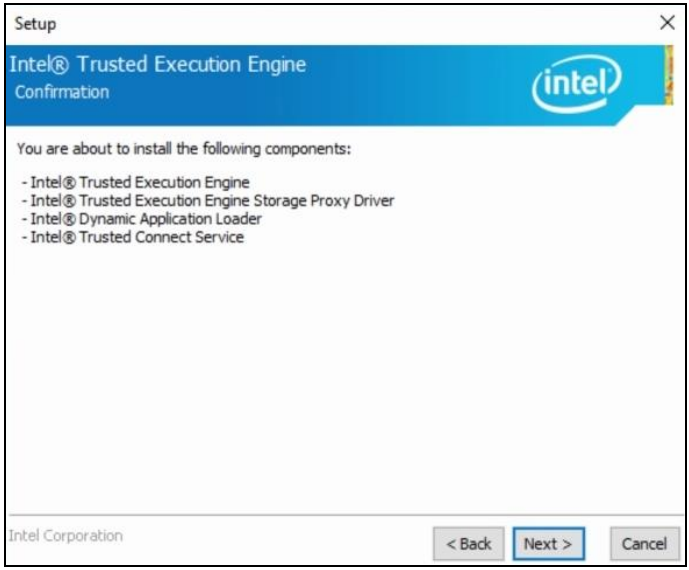
1. Click **Intel(R) TXE Drivers**.

2. When the *Welcome* screen appears, click **Next**.



3. Accept the license agreement and click **Next**.

4. Click **Next** for installation.



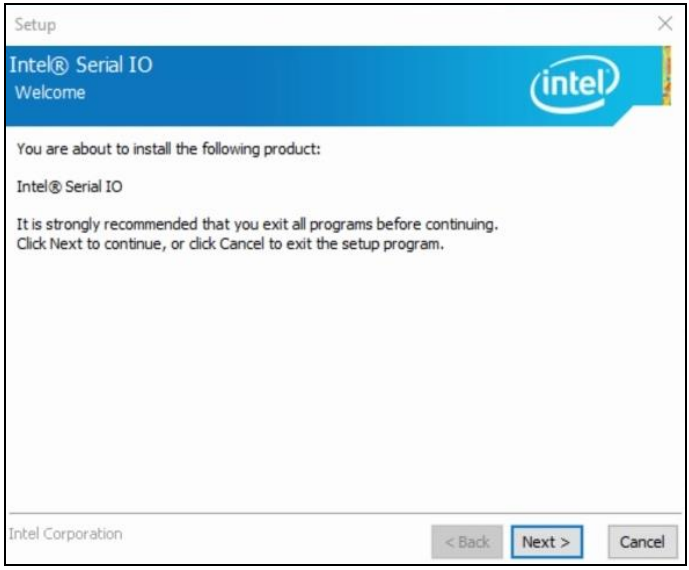
5. As the driver is sccessfully installed, restart the computer for changes to take effect.

3.6 Intel® Serial IO Drivers

1. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.

2. Click **Intel(R) Serial IO Drivers**.

3. When the *Welcome* screen to the InstallShield Wizard appears, click **Next**.

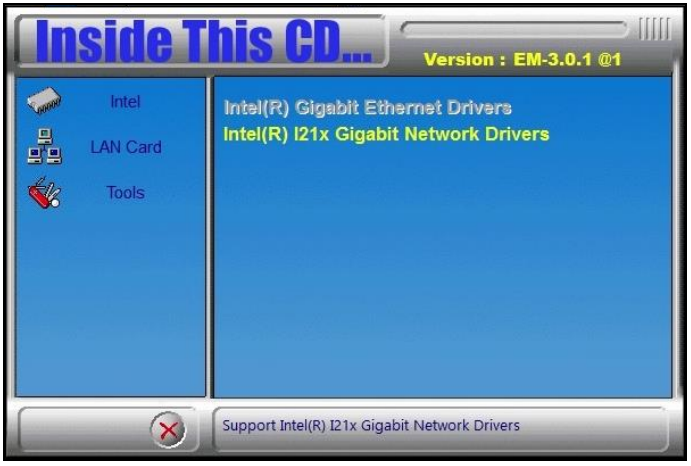


4. Accept the license agreement and click **Next**.
5. After reading the *Readme File Information*, click **Next** for installation.
6. As the driver is sccessfully installed, restart the computer for changes to take effect.

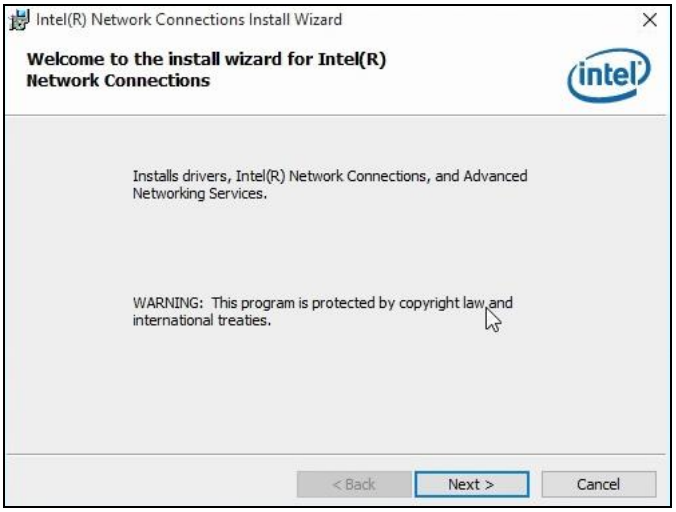
3.7 LAN Driver Installation

1. Click **LAN Card** on the left pane and then **Intel LAN Controller Drivers** on the right pane.

2. Click **Intel(R) I21x Gigabit Network Drivers.**.

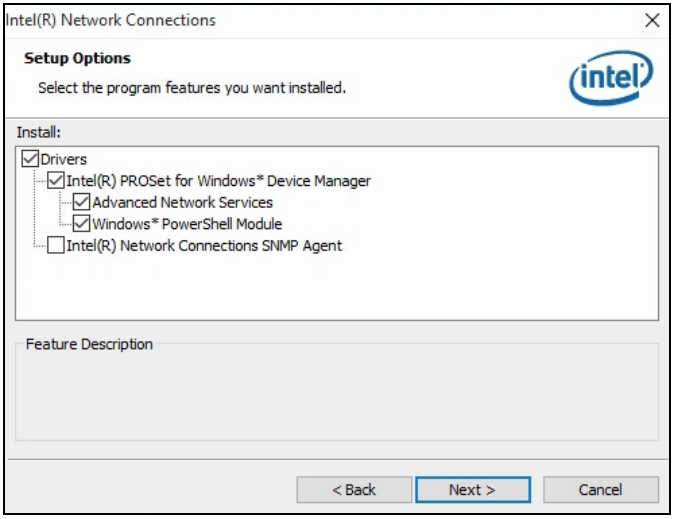


3. When the *Welcome* screen appears, click **Next**.



4. Accept the license agreement and click **Next**.

5. On the *Setup Options* screen, click the checkbox to select the desired driver(s) for installation. Then click **Next** to continue.



6. The wizard is ready for installation. Click **Install**.

7. As the installation is complete, restart the computer for changes to take effect.

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Chapter 4
BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

- Main Settings
- Advanced Settings
- Chipset Settings
- Security Settings
- Boot Settings
- Save & Exit

4.1 Introduction

The BIOS (Basic Input/Output System) installed in the ROM of your computer system supports Intel® processors. The BIOS provides critical low-level support for standard devices such as disk drives, serial ports and parallel ports. It also provides password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

4.2 BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Press the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup.

If you still need to enter Setup, restart the system by pressing the ”Reset” button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again.

The following message will appear on the screen:

```
Press  <DEL>  to  Enter  Setup
```

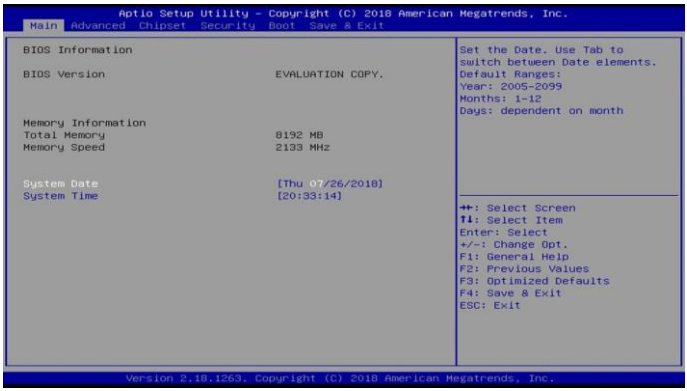
In general, press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help, and <Esc> to quit.

When you enter the BIOS Setup utility, the *Main Menu* screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: It is strongly recommended that you avoid making any changes to the chipset defaults.

These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could make the system unstable and crash in some cases.

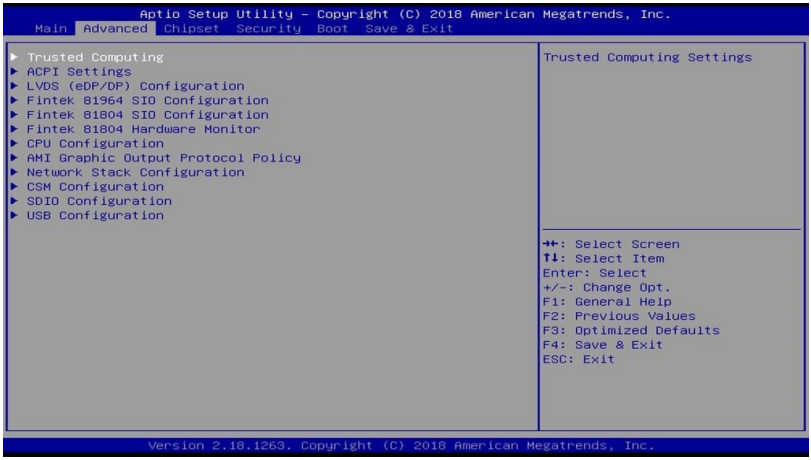
4.3 Main Settings



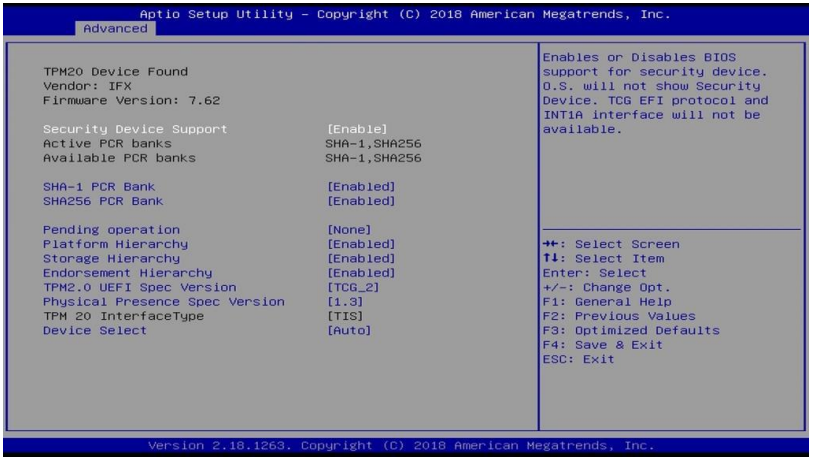
BIOS Setting	Description
System Date	Sets the date. Use the <Tab> key to switch between the data elements.
System Time	Set the time. Use the <Tab> key to switch between the data elements.

4.4 Advanced Settings

This section allows you to configure, improve your system and allows you to set up some system features according to your preference.



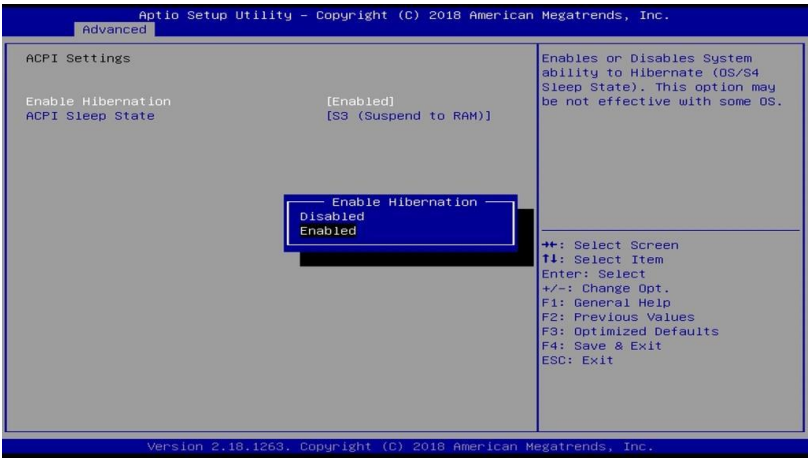
4.4.1 Trusted Computing



BIOS Setting	Description
Security Device Support	Enables / Disables BIOS support for security device. OS will not show security device. TCG EFI protocol and INTIA interface will not be available.
SHA-1 PCR Bank	Enables / Disables SHA-1 PCR Bank.
SHA256 PCR Bank	Enables / Disables SHA256 PCR Bank.
Pending operation	Schedule an operation for the security device. Note: Your computer will reboot during restart in order to change state of security device.
Platform Hierarchy	Enables / Disables platform hierarchy.
Storage Hierarchy	Enables / Disables storage hierarchy.
Endorsement Hierarchy	Enables / Disables endorsement hierarchy.
TPM2.0 UEFI Spec Version	Selects the supported TCG version based o your OS. • **TCG_1_2:** supports Windows 8 /10. • **TCG_2:** supports new TCG2 protocol and event format for Windows 10 or later.
Physical Presence Spec Version	Selects to show the PPI Spec Version (1.2 or 1.3) that the OS supports. **Note:** Some HCK tests might not support 1.3.

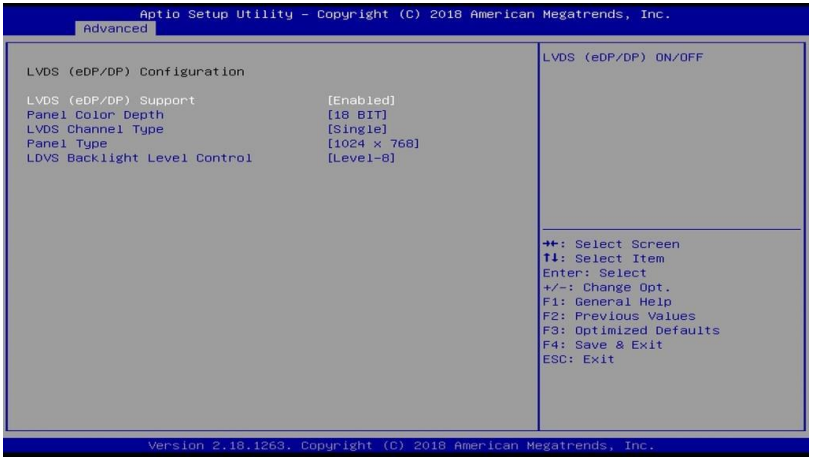
BIOS Setting	Description
Device Select	• **TPM 1.2** will restrict support to TPM 1.2 devices only. • **TPM 2.0** will restrict support to TPM 2.0 devices only. • **Auto** will support both with the default being set to TPM 2.0 deices if not found, and TPM 1.2 device will be enumerated.

4.4.2 ACPI Settings



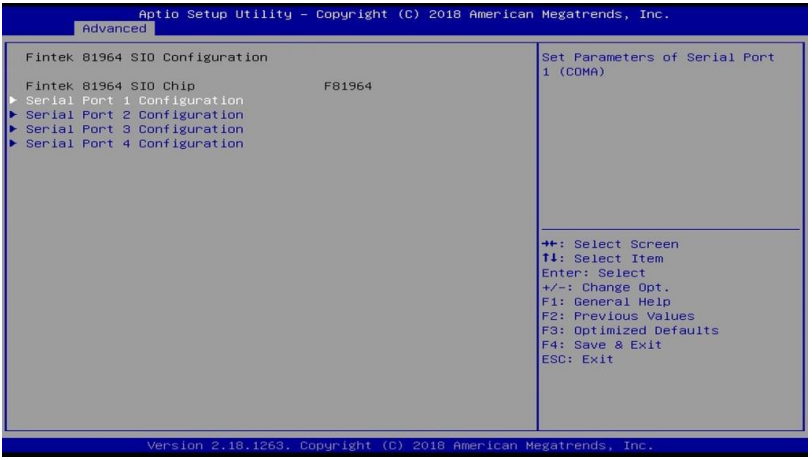
BIOS Setting	Description
Enable Hibernation	Enables / Disables the system ability to hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
ACPI Sleep State	Selects an ACPI sleep state (Suspend Disabled or S3) where the system will enter when the Suspend button is pressed.

4.4.3 LVDS (eDP/DP) Configuration



BIOS Setting	Description
LVDS (eDP/DP) Support	Enables / Disables LVDS (eDP/DP).
Panel Color Depth	Controls the panel color depth. Options: 18 bit, 24 bit (VESA), 24 bit (JEIDA)
LVDS Channel Type	Selects a LVDS protocol type. Options: Single. Dual
Panel Type	Selects the resolution of your panle. Options: 800 x 480 / 800 x 600 / 1024 x 768 / 1280 x 768 / 1280 x 800 / 1280 x 960 / 1280 x 1024 / 1366 x 768 / 1440 x 900 / 1600 x 900 / 1600 x 1200 / 1680 x 1050 / 1920 x 1080 / 1920 x 1200
LVDS Backlight Level Control	Selects a level of backlight. Options: Level-1 ~ Level-8

4.4.4 Fintek 81964 SIO Configuration



BIOS Setting	Description
Serial Ports Configuration	Set parameters of Serial Ports.

4.4.4.1. Serial Port 1 Configuration

BIOS Setting	Description
Serial Port	Enables / Disables the serial port.
Change Settings	Selects an optimal settings for Super IO device. Options: • Auto • IO = 3F8h; IRQ = 4 • IO = 3F8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2F8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 3E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12

4.4.4.2. Serial Port 2 Configuration

BIOS Setting	Description
Serial Port	Enables / Disables the serial port.
Change Settings	Selects an optimal settings for Super IO device. Options: • Auto • IO = 2F8h; IRQ = 3 • IO = 3F8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2F8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 3E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12

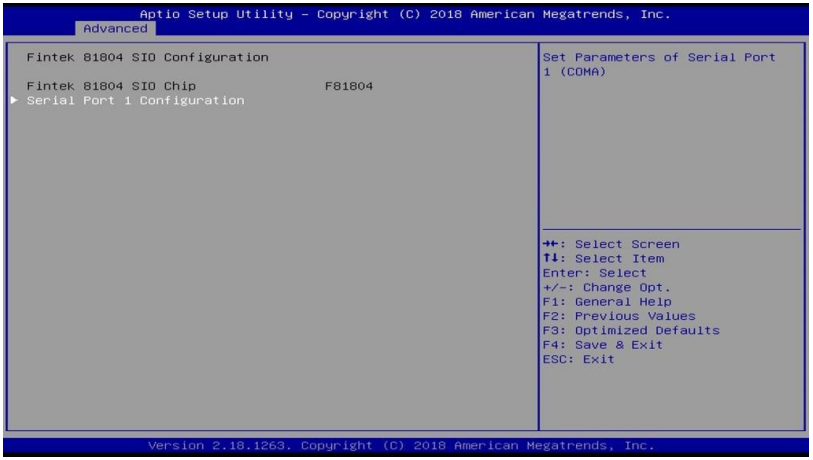
4.4.4.3. Serial Port 3 Configuration

BIOS Setting	Description
Serial Port	Enables / Disables the serial port.
Change Settings	Selects an optimal settings for Super IO device. Options: • Auto • IO = 3E8h; IRQ = 7 • IO = 3E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2F0h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2E0h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12

4.4.4.4. Serial Port 4 Configuration

BIOS Setting	Description
Serial Port	Enables / Disables the serial port.
Change Settings	Selects an optimal settings for Super IO device. Options: • Auto • IO = 2E8h; IRQ = 7 • IO = 3E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2E8h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2F0h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12 • IO = 2E0h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12

4.4.5 Fintek 81804 SIO Configuration

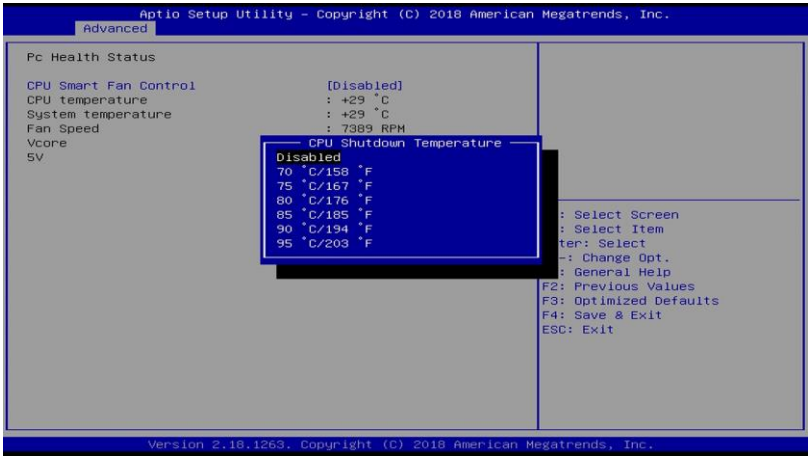


BIOS Setting	Description
Serial Port 1 Configuration	Set parameters of Serial Port 1 (COMA).

4.4.5.1. Serial Port 1 Configuration

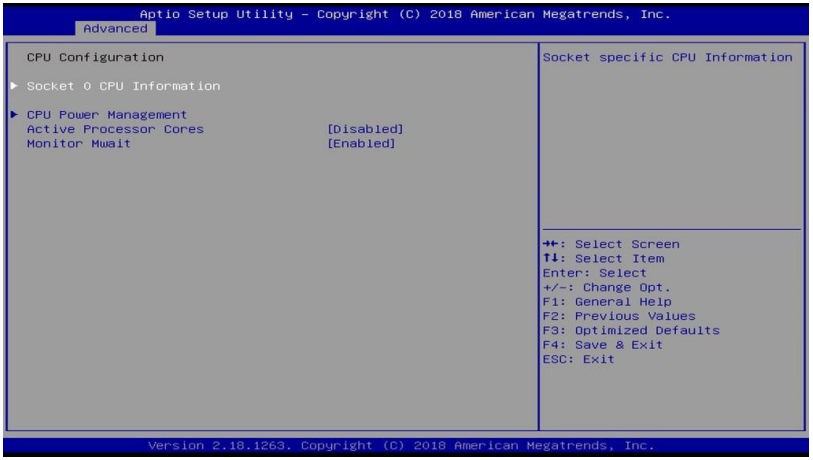
BIOS Setting	Description
Serial Port	Enables / Disables the serial port.
Change Settings	Selects an optimal settings for Super IO device. Options: • Auto • IO = 240h; IRQ = 10 • IO = 240h; IRQ = 3, 4, 5, 6, 7, 10, 11, 12 • IO = 248h; IRQ = 3, 4, 5, 6, 7, 9, 10, 11, 12

4.4.6 Fintek 81804 Hardware Monitor



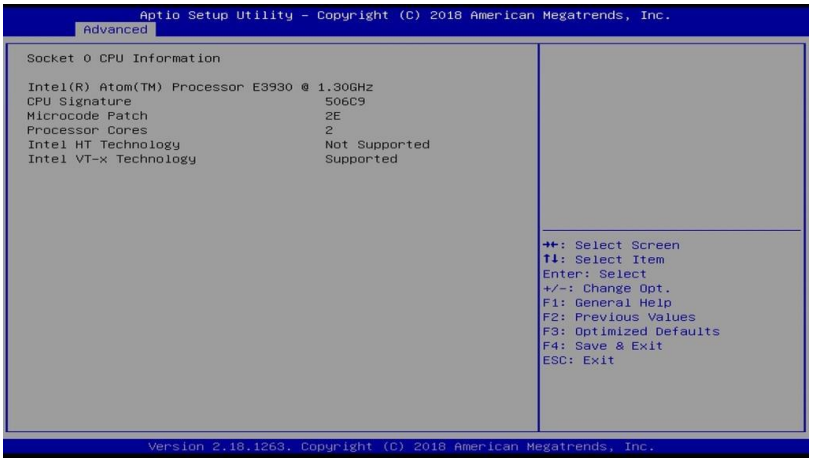
BIOS Setting	Description
CPU Smart Fan Control	Enables / Disables the smart fan feature. Options: Disabled, 50°C, 60°C, 70°C, 80°C
Temperatures / Voltages	These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

4.4.7 CPU Configuration



BIOS Setting	Description
Socket 0 CPU Information	Displays the socket specific CPU information.
CPU Power Management	Show the CPU power management options.

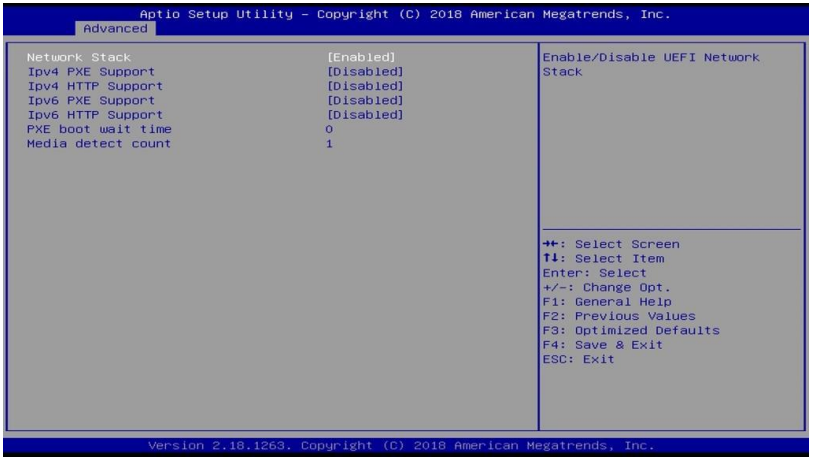
4.4.7.1. Socket 0 CPU Information



4.4.8 AMI Graphic Output Protocol Policy

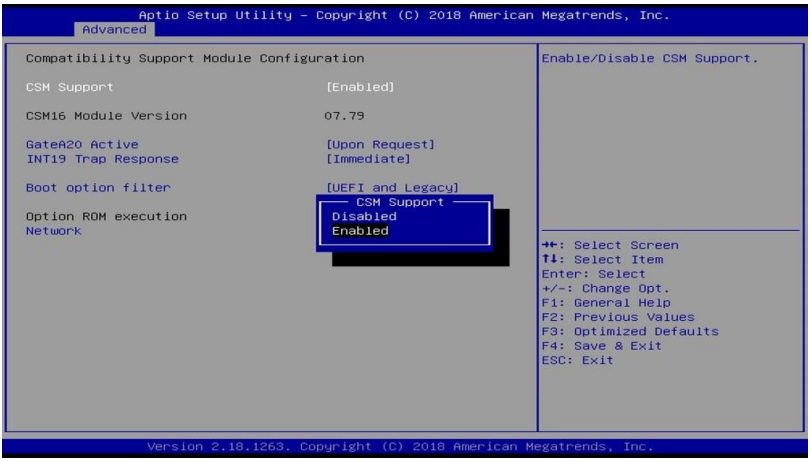
BIOS Setting	Description
Output Select	Outputs interface

4.4.9 Network Stack Configuration



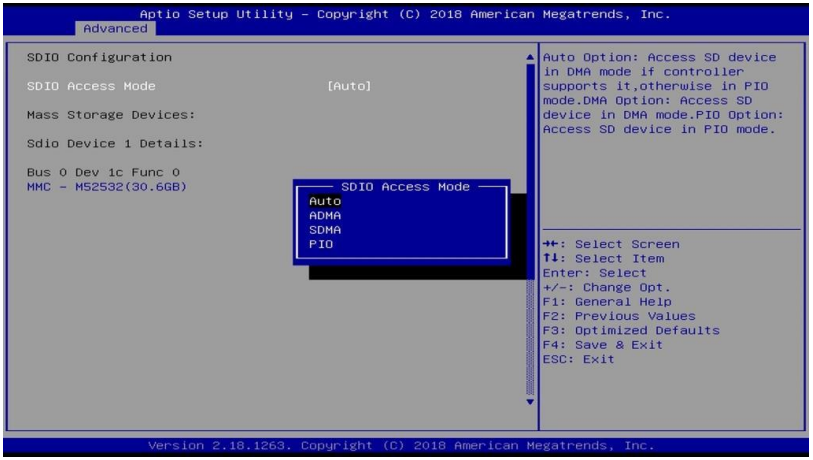
BIOS Setting	Description
Network Stack	Enables / Disables UEFI network stack.
IPv4 PXE Support	Enables / Disables IPv4 PXE Boot Support. If disabled, Ipv4 PXE boot option will not be created.
IPv4 HTTP Support	Enables / Disables IPv4 HTTP Boot Support. If disabled, Ipv4 HTTP boot option will not be created.
IPv6 PXE Support	Enables / Disables IPv6 PXE Boot Support. If disabled, Ipv4 PXE boot option will not be created.
IPv6 HTTP Support	Enables / Disables IPv6 HTTP Boot Support. If disabled, Ipv4 HTTP boot option will not be created.
PXE boot wait time	Assigns a period of time to press ESC key to abort the PXE boot.
Media detect count	Assigns a number of times to check the presence of media.

4.4.10 CSM Configuration



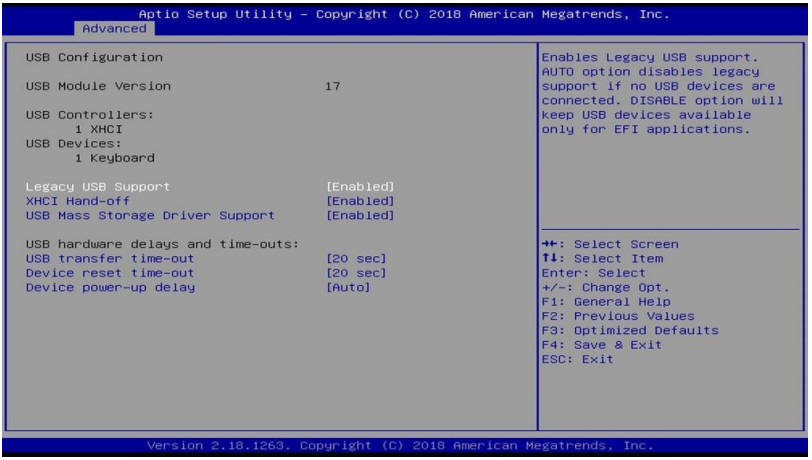
BIOS Setting	Description
CSM Support	Enables / Disables CSM support.
GateA20 Active	• The option Upon Request disables GA20 when using BIOS services. • The option Always cannot disable GA20, but is useful when any RT code is executed above 1 MB.
INT19 Trap Response	Selects the way that BIOS reacts on INT19 trapping by Option ROM. • Immediate executes the trap right away • Postponed executes the trap during legacy boot.
Boot option filter	Controls the priority of Legacy and UEFI.
Network	Controls the execution of UEFI and Legacy PXE OpROM.

4.4.11 SDIO Configuration



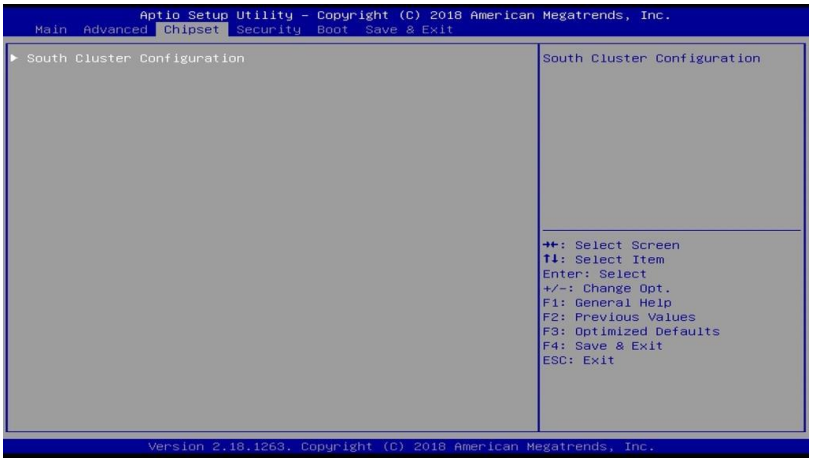
BIOS Setting	Description
SDIO Access Mode	Auto Option: Access SD device in DMA mode if controller support it. Otherwise in PIO mode. DMA Option: Access SD device in DMA mode. PIO Option: Access SD device in PIO mode. Options: Auto, ADMA, SDMA, PIO
MMC – M52532 (30.6 GB)	Mass storage device emulation type. “Auto” enumerates devices less than 530 MB as floppies. Forced FDD option can be used to force HDD formatted drive to boot as FDD. Options: Auto, Floppy, Forced FDD, Hard Disk

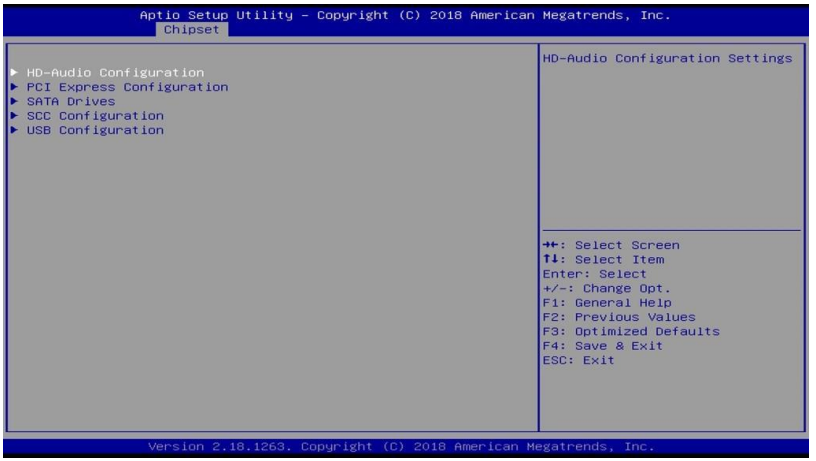
4.4.12 USB Configuration



BIOS Setting	Description
Legacy USB Support	• **Enabled** enables Legacy USB support. • **Auto** disables legacy support if there is no USB device connected. • **Disabled** keeps USB devices available only for EFI applications.
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enables / Disables the support for USB mass storage driver.
USB Transfer time-out	The time-out value (1 / 5 10 / 20 secs) for Control, Bulk, and Interrupt transfers.
Device reset time-out	Gives seconds (10 / 20 / 30 / 40 secs) to delay execution of Start Unit command to USB mass storage device.
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. “Auto” uses default value: for a root port it is 100 ms, for a hub port, the delay is taken from hub descriptor.

4.5 Chipset Settings

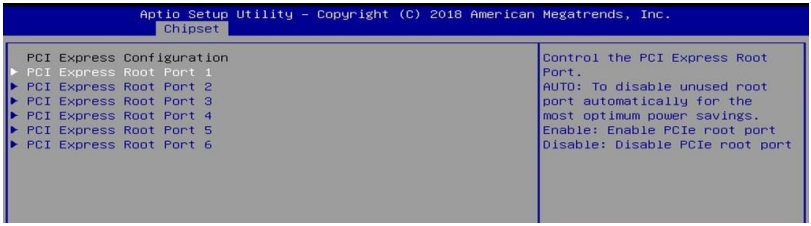




4.5.1 HD-Audio Configuration

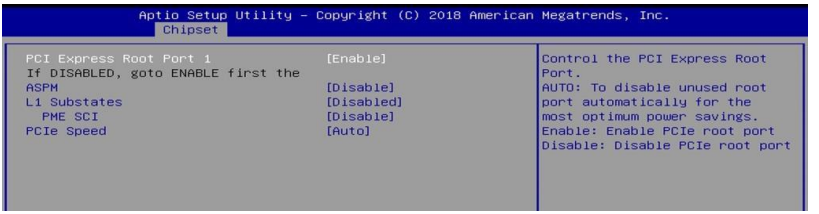
BIOS Setting	Description
HD-Audio Support	Enables / Disables HD audio support,

4.5.2 PCI Express Configuration



BIOS Setting	Description
PCI Express Root Ports 1 ~ 6	Control the PCI Express Root Port. Enables / Disables PCIe root port. Auto is to disable unused root port automatically for the most optimum power savings.

4.5.2.1. PCIe Root Ports 1~6

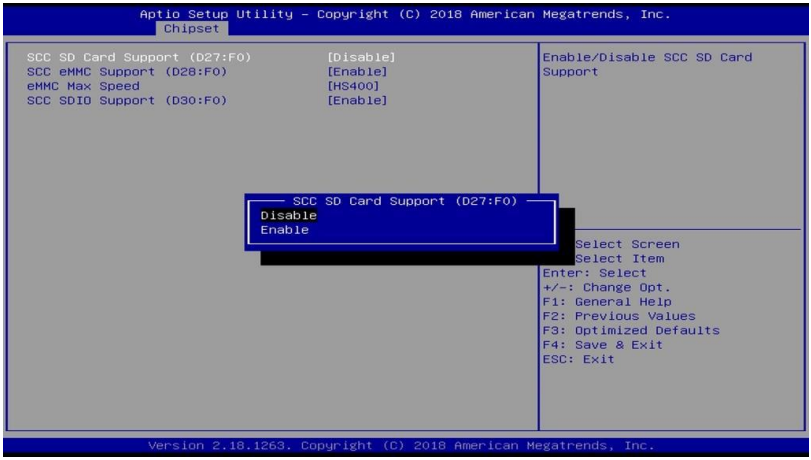


BIOS Setting	Description
PCI Express Root Port	Enables/ Disables the PCIe root port. **Auto:** To disable unused root port automatically for the most optimum power savings.
ASPM	Sets the PCIe active state power management. Options: Disable, L0s, L1, L0SL1, Auto
L1 Substates	Sets PCIe L1 substates. Options: Disabled, L1.1, L1.2, L1.1 & L1.2
PME SCI	Enables / Disables PME SCI.
PCIe Speed	Configures the PCIe speed. Options: Auto, Gen1, Gen2

4.5.3 SATA Drives

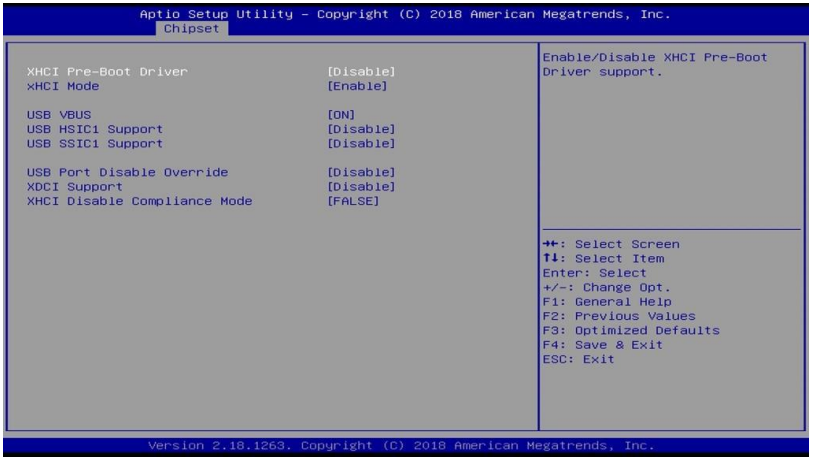
BIOS Setting	Description
Chipset SATA	Enables / Disables the chipset SATA controller. The chipsest SATA Controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).
SATA Mode Selection	Selects AHCI for SATA Controller(s) operation.

4.5.4 SCC Configuration



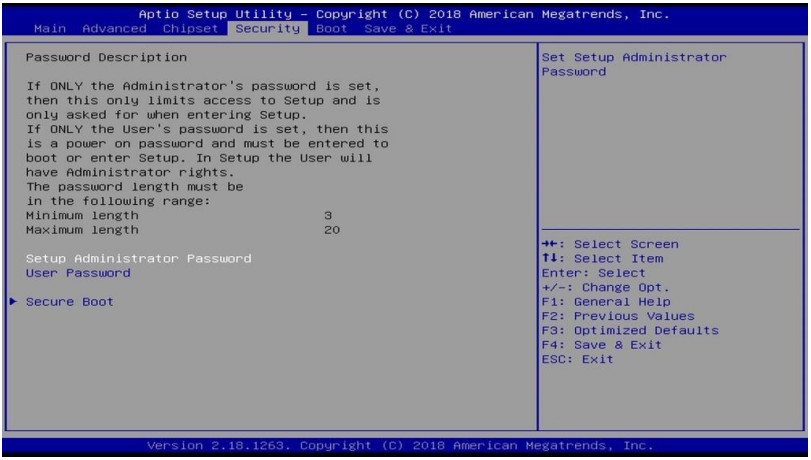
BIOS Setting	Description
SCC SD Card Support (D27:F0)	Enables / Disables SCC SD card support.
SCC eMMC Support (D28:F0)	Enables / Disables SCC eMMC support.
eMMC Max Speed	Selects the eMMC max. speed allowed.
SCC SDIO Support (D30:F0)	Enables / Disables SCC SDIO support.

4.5.5 USB Configuration



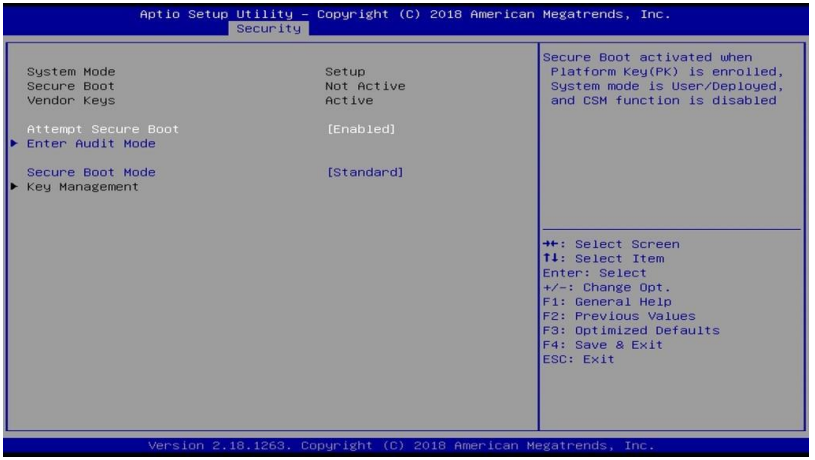
BIOS Setting	Description
XHCI Pre-Boot Driver	Enables / Disables the XHCI Pre-Boot driver.
XHCI Mode	Enables / Disables XHCI mode. If disabled, XHCI controller would be disabled, and none of the USB devices are detectable or usable when systen is booted up in OS. Do NOT disable it unless for debug purpose.
USB VBUS	VBUS should be ON in HOST mode. It should be OFF in OTG device mode.
USB HSIC1 Support	Enables / Disables USB HSIC1.
USB SSIC1 Support	Enables / Disables USB SSIC1.
USB Port Disable Override	Selectively enables / disables the corresponding USB port from reporting a device connection to the controller.
XDCI Support	Enables / Disables XDCI.
XHCI Disable Compliance Mode	FALSE makes the XHCI Link Compliance Mode not disabled. TRUE disables the XHCI Link Compliance Mode.

4.6 Security Settings



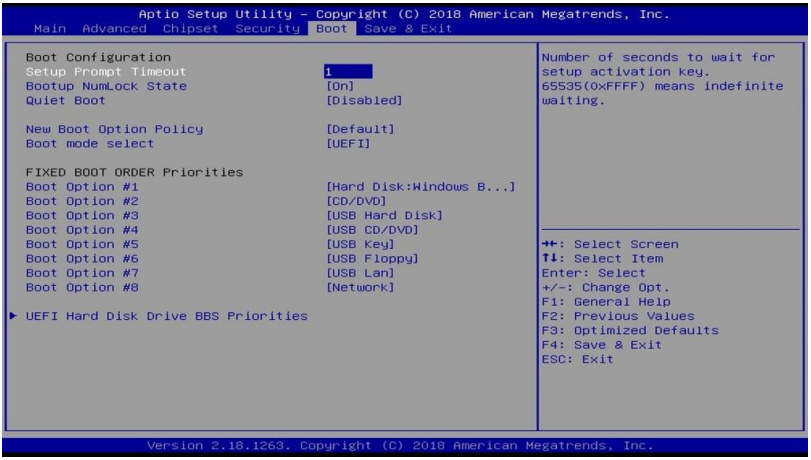
BIOS Setting	Description
Setup Administrator Password	Sets an administrator password for the setup utility.
User Password	Sets a user password.
Secure Boot	Customizable secure boot settings.

4.6.1 Secure Boot



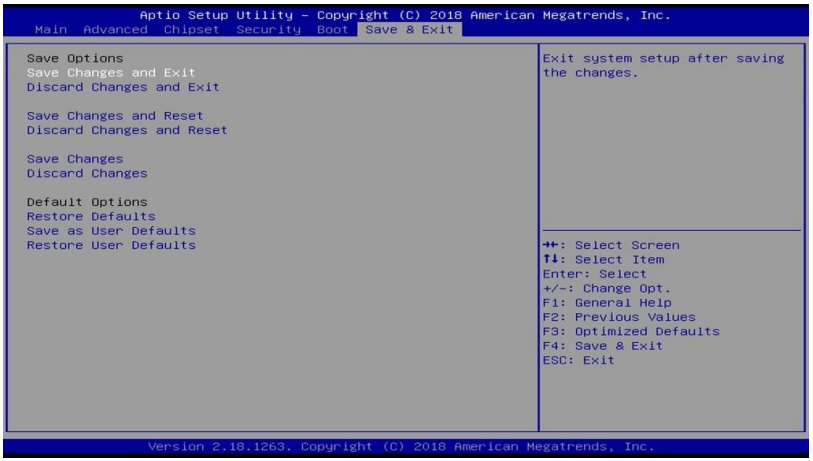
BIOS Setting	Description
Attempt Secure Boot	Secure Boot activated when platform key (PK) is enrolled, system mode is user/deployed, and CSM function is disabled.
Secure Boot Mode	Custom & standard modes for UEFI secure boot mode. This change will be effective after being saved. After reset, the mode will return to standard mode.

4.7 Boot Settings



BIOS Setting	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	Selects the keyboard NumLock state.
Quiet Boot	Enables / Disables Quiet Boot option.
New Boot Option Policy	Controls the placement of newly detected UEFI boot options.
Boot mode select	Selects a Boot mode, Legacy / UEFI.
Boot Option Priorities	Sets the system boot order priorities for hard disk, CD/DVD, USB, Network.
UEFI Hard Disk Drive BBS Priorities	Specificies the Boot device priority sequence from available UEFI USB Key drivers.

4.8 Save & Exit Settings



BIOS Setting	Description
Save Changes and Exit	Exits system setup after saving the changes.
Discard Changes and Exit	Exits system setup without saving any changes.
Save Changes and Reset	Resets the system after saving the changes.
Discard Changes and Reset	Resets system setup without saving any changes.
Save Changes	Saves changes done so far to any of the setup options.
Discard Changes	Discards changes done so far to any of the setup options.
Restore Defaults	Restores / Loads defaults values for all the setup options.
Save as User Defaults	Saves the changes done so far as User Defaults.
Restore User Defaults	Restores the user defaults to all the setup options.

Appendix

This section provides the mapping addresses of peripheral devices and the sample code of watchdog timer configuration.

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000070-0x00000070	System CMOS/real time clock
0x00000080-0x0000008F	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x00000400-0x0000047F	Motherboard resources
0x00000500-0x000005FE	Motherboard resources
0x00000600-0x0000061F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x0000F040-0x0000F05F	Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
0x00000A00-0x00000A0F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000A20-0x00000A2F	Motherboard resources
0x0000E000-0x0000EFFF	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD6
0x000003F8-0x000003FF	Communications Port (COM1)
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003E8-0x000003EF	Communications Port (COM3)
0x000002E8-0x000002EF	Communications Port (COM4)
0x000002F0-0x000002F7	Communications Port (COM5)
0x0000F000-0x0000F03F	Intel(R) HD Graphics

Address	Device Description
0x00000000-0x0000006F	PCI Express Root Complex
0x00000078-0x00000CF7	PCI Express Root Complex
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x0000F090-0x0000F097	Standard SATA AHCI Controller
0x0000F080-0x0000F083	Standard SATA AHCI Controller
0x0000F060-0x0000F07F	Standard SATA AHCI Controller
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 25	High Definition Audio Controller
IRQ 39	Intel SD Host Controller
IRQ 8	High precision event timer
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 5	Communications Port (COM3)
IRQ 10	Communications Port (COM4)
IRQ 7	Communications Port (COM5)
IRQ 4294967285	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
IRQ 4294967293	Intel(R) HD Graphics
IRQ 42	Intel SD Host Controller
IRQ 54 ~ IRQ 204	Microsoft ACPI-Compliant System
IRQ 256 ~ IRQ 511	Microsoft ACPI-Compliant System
IRQ 4294967291	Intel(R) I210 Gigabit Network Connection
IRQ 4294967290	Intel(R) I210 Gigabit Network Connection
IRQ 4294967289	Intel(R) I210 Gigabit Network Connection
IRQ 4294967288	Intel(R) I210 Gigabit Network Connection
IRQ 4294967287	Intel(R) I210 Gigabit Network Connection
IRQ 4294967286	Intel(R) I210 Gigabit Network Connection
IRQ 4294967292	Intel(R) Trusted Execution Engine Interface
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3452
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3452
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3452
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3452
IRQ 4294967294	Standard SATA AHCI Controller
IRQ 0	System timer

C. Watchdog Timer Configuration

The Watchdog Timer (WDT) is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven.

Under normal circumstance, you will need to restart the WDT at regular intervals before the timer counts to zero.

Sample Code:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81804.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81804 watch dog program\n");
        SIO = Init_F81804();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81804, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }
```

```
        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime); }
        else
        {       DisableWDT();       }
        return 0;
}
//-------------------------------------------------------------------------
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_F81804_Reg(0x2B);
        bBuf &= (~0x20);
        Set_F81804_Reg(0x2B,   bBuf);       //Enable WDTO

        Set_F81804_LD(0x07);                //switch to logic device  7
        Set_F81804_Reg(0x30,   0x01);       //enable timer

        bBuf = Get_F81804_Reg(0xF5);
        bBuf &= (~0x0F);
        bBuf |= 0x52;
        Set_F81804_Reg(0xF5,   bBuf);       //count mode is second

        Set_F81804_Reg(0xF6,   interval);   //set timer

        bBuf = Get_F81804_Reg(0xFA);
        bBuf |= 0x01;
        Set_F81804_Reg(0xFA,   bBuf);       //enable WDTO output

        bBuf = Get_F81804_Reg(0xF5);
        bBuf |= 0x20;
        Set_F81804_Reg(0xF5,   bBuf);       //start counting
}
//-------------------------------------------------------------------------
void DisableWDT(void)
{
        unsigned char bBuf;

        Set_F81804_LD(0x07);                //switch to logic device 7

        bBuf = Get_F81804_Reg(0xFA);
        bBuf &= ~0x01;
        Set_F81804_Reg(0xFA,   bBuf);       //disable WDTO output

        bBuf = Get_F81804_Reg(0xF5);
        bBuf &= ~0x20;
        bBuf |= 0x40;
        Set_F81804_Reg(0xF5,   bBuf);       //disable WDT
}
//-------------------------------------------------------------------------


//-------------------------------------------------------------------------
```

```
//
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// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81804.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81804_BASE;
void Unlock_F81804 (void);
void Lock_F81804 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81804(void)
{
        unsigned int result;
        unsigned char ucDid;

        F81804_BASE = 0x4E;
        result = F81804_BASE;

        ucDid = Get_F81804_Reg(0x20);
        if (ucDid == 0x07)                      //Fintek 81804
        {       goto Init_Finish;               }

        F81804_BASE = 0x2E;
        result = F81804_BASE;

        ucDid = Get_F81804_Reg(0x20);
        if (ucDid == 0x07)                      //Fintek 81804
        {       goto Init_Finish;               }

        F81804_BASE = 0x00;
        result = F81804_BASE;

Init_Finish:
        return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81804 (void)
{
        outportb(F81804_INDEX_PORT, F81804_UNLOCK);
        outportb(F81804_INDEX_PORT, F81804_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81804 (void)
{
        outportb(F81804_INDEX_PORT, F81804_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81804_LD( unsigned char LD)
{
        Unlock_F81804();
        outportb(F81804_INDEX_PORT, F81804_REG_LD);
        outportb(F81804_DATA_PORT, LD);
        Lock_F81804();
```

```
}
//---------------------------------------------------------------------------
void Set_F81804_Reg( unsigned char REG, unsigned char DATA)
{
        Unlock_F81804();
        outportb(F81804_INDEX_PORT, REG);
        outportb(F81804_DATA_PORT, DATA);
        Lock_F81804();
}
//---------------------------------------------------------------------------
unsigned char Get_F81804_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81804();
        outportb(F81804_INDEX_PORT, REG);
        Result = inportb(F81804_DATA_PORT);
        Lock_F81804();
        return Result;
}
//---------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
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// PURPOSE.
//
//---------------------------------------------------------------------------
#ifndef   F81804_H
#define   F81804_H                      1
//---------------------------------------------------------------------------
#define         F81804_INDEX_PORT       (F81804_BASE)
#define         F81804_DATA_PORT        (F81804_BASE+1)
//---------------------------------------------------------------------------
#define         F81804_REG_LD           0x07
//---------------------------------------------------------------------------
#define         F81804_UNLOCK           0x87
#define         F81804_LOCK             0xAA
//---------------------------------------------------------------------------
unsigned int Init_F81804(void);
void Set_F81804_LD( unsigned char);
void Set_F81804_Reg( unsigned char,
unsigned char); unsigned char
Get_F81804_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif  //   F81804_H
```