MBN500

4-port (AMD G-Series SoC)

USER'S MANUAL

Version: 1.1

Acknowledgments

Table of Content

Introduction

Product Description

The MBN500 networking motherboard is based on the latest AMD G-Series SoC. It is ideally suited for rugged and compact design as entry level networking appliance.

The motherboard is configured with the AMD GX-412HC or GX-412TC SoC. It supports one DDR3L SO-DIMM, tour GbE ports with one bypass segment, one mini PCIe half-size socket, one Cfast socket, one STAT 3.0 and two USB 3.0 connectors. Moreover, it has more extensions I/O through pin-deader such as two USB 2.0 and COM2 (LCM).

MBN500-4CG Features

- AMD GX-412HC Quad Care 1.2GHz SoC
- Four Intel® i211-AT Gigabit LAN ports
- One DDR3L SO-DIMM, up to 8GB
- Mini Display Port
- Mini PCI-E half size slot x1
- Cfast socket
- One Bypass Segment on Eth3/4 and configurable by BIOS

MBN500-4C Features

- AMD GX-412TC Quad Care 1.0GHz SoC
- Four Intel® i211-AT Gigabit LAN ports
- One DDR3L SO-DIMM, up to 8GB
- Mini PCI-E half size slot x1
- Cfast socket
- One Bypass Segment on Eth3/4 and configurable by BIOS

Checklist

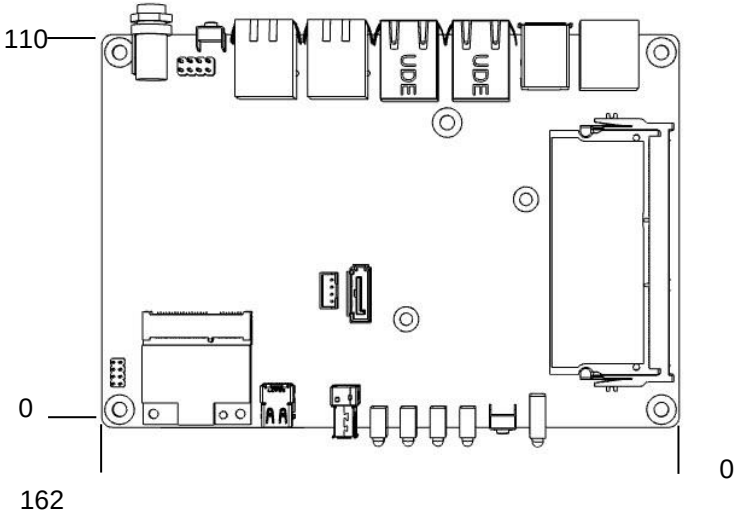
Your MBN500 package should include the items listed below.

- The MBN500-4CG or MBN500-4C embedded board
- Windows Drivers are able to download from iBase, please contact your sales representative.
- Cables are optional.

MBN500 Specifications

Product Name	MBN500-4CG or MBN500-4C
Form Factor	Proprietary Size
CPU Type Operating Frequency	AMD G-Series Crowned Eagle SoC, 28nm process technology MBN500-4CG: AMD GX-412HC Quad Core 1.2GHz [TPD = 7W] MBN500-4C: AMD GX-412TC Quad Core 1.0GHz [TPD = 6W]
BIOS	AMI BIOS 64Mb
Memory	One DDR3L SO-DIMM socket, Non-ECC, unbuffered
Display	N/A
Ethernet controller	Intel I211-AT PCI Express Gigabit ethernet controller x4
LAN	Eth1, 2, 3 & 4: Intel I211-AT @ RJ45 with LED
Network Bypass	One Bypass segment (Eth3/4) Control by GPIO / Watchdog
Front Edge	• System LED: Power (Green) / Bypass (Green/Red) / Status (Yellow/Red) • LAN LED: Link/Active (Green) x 4; LAN Speed (Yellow/Green) x 4 • 1 x Mini DP (MBN500-4CG only) • Factory Mode Restore Reset Switch (GPIO control) • 1 x USB 2.0 receptacle
Rear Edge	• 1 x RJ45 Console • 2 x USB 3.0 receptacle • RJ45 GbE port x 4 with status LED • 1 x Power on/off switch • 2 x USB 2.0 • Cylindrical (Tip) Connector DC +12V inlet with screw lock
Internal I/O Headers	• 1 x DC Fan 3-pin Connector • 1 x DC-in 2-pin header (12V) • 2 USB 2.0 DF11 8-pin connector • 1 x COM2 DF11 8-pin connector • 1 x SATA 3.0 data 7-pin connector • 1 x SATA power (5V) 4-pin JST connector • 1 x Cfast socket • 1 x Mini PCIe half-size socket • 4 x GPIO header 6-pin pitch 2.0mm
LPC I/O	Nuvoton NCT5523D: • 1 x RJ45 Console • 1 x COM2 DF11 8-pin connector; RS232 4-pin
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
Expansion Slot	Mini PCIe half-size socket x 1
Power Requirement	• Full range 40W Adapter / 12V (Optional) • Minimum 12V @ 2A without Cfast & mini PCIe module
Dimensions	162 (W) x 110 (D) mm
Operation Temperature	0 ~ 60 ˚C (32 ~ 140 ˚F)
Storage Temperature	-20 ~ 80 ˚C (-4 ~ 176 ˚F)

Board Dimensions



unit: mm

Installations

This section provides information on how to use the jumpers and connectors on the MBN500 in order to set up a workable system. The topics covered are:

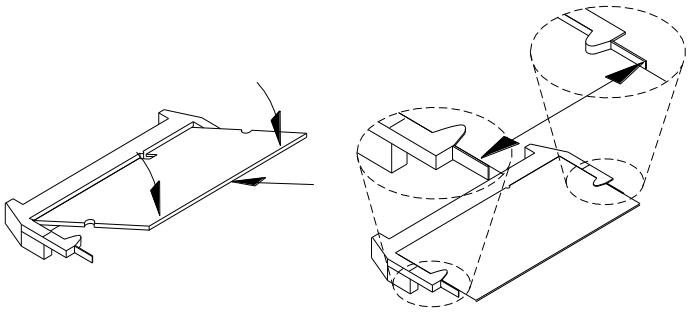
Installing the Memory

The MBN500 board supports one DDR3 memory socket that can support up to 8GB memory, DDR3L (w/o ECC function).

Installing and Removing Memory Modules

To install the DDR3L module, locate the memory slot on the board and perform the following steps:

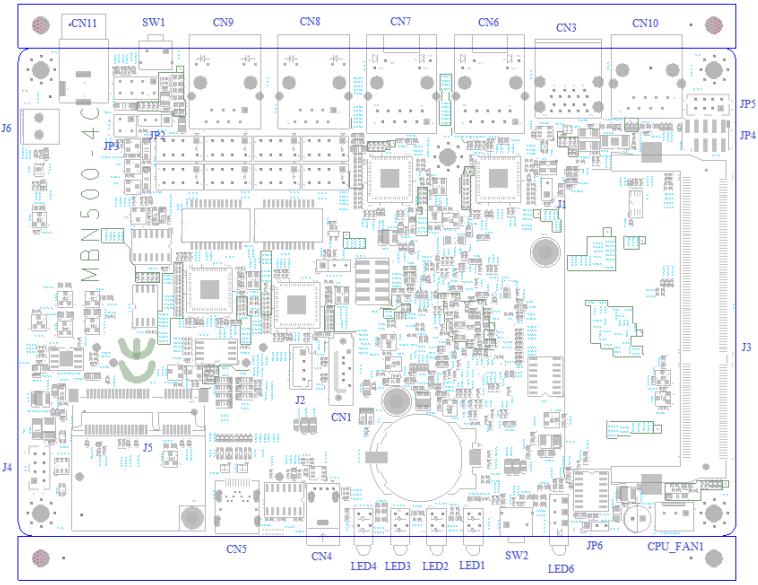
1. Hold the DDR3L module so that the key of the DDR3L module aligns with that on the memory slot. Insert the module into the socket at a slight angle (approximately 30 degrees). Note that the socket and module are both keyed, which means that the module can be installed only in one direction.
2. To seat the memory module into the socket, apply firm and even pressure to each end of the module until you feel it slip down into the socket.
3. With the module properly seated in the socket, rotate the module downward. Continue pressing downward until the clips at each end lock into position.
4. To remove the DDR3L module, press the clips with both hands.



Setting the Jumpers and Connectors

Jumpers are used on MBN500 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs.

Jumper & Connector Location on MBN500-4CG / MBN500-4C



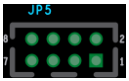
J1:SPEKER (Reserved)

Pin #	Signal Name
1	VCC5
2	SPKR#

JBAT1: Clear CMOS Setting

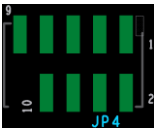
JP2	Setting
	Normal
	Clear CMOS

JP5: LCM COM2



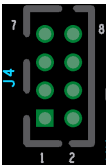
Signal Name	Pin #	Pin #	Signal Name
VCC5	1	2	VCC5
SOUT2	3	4	RTS#2
SIN2	5	6	CTS#2
GND	7	8	GND

JP4: LPC Debug Port



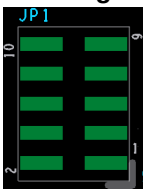
Signal Name	Pin #	Pin #	Signal Name
LPC_AD0	1	2	SIO_PLTRST#
LPC_AD1	3	4	LPC_FRAME#
LPC_AD2	5	6	+3.3V
LPC_AD3	7	8	Ground
LPC_CLK	9		

J4 : USB2.0 Ports



Signal Name	Pin #	Pin #	Signal Name
+5V	1	2	GND
P4-	3	4	P5+
P4+	5	6	P5-
GND	7	8	+5V

JP1: SPI Debug Port

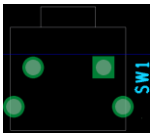


Signal Name	Pin #	Pin #	Signal Name
NC	1	2	NC
SPI_CS#0	3	4	3VDUAL
SPI_SO	5	6	SPI0_HOLD#
SPI0_WP#	7	8	SPI_CLK
GND	9	10	SPI_SI

J2: External SATA Power Connector (only for 2.5” SATA)

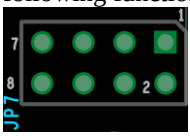
Pin #	Signal Name
1	+5V
2	Ground
3	Ground
4	NA

SW1:ATX On/Off



JP7: System Function Connector

JP7 provides connectors for system indicators that provide light indication of the computer activities and switches to change the computer status. JP7 is a 8-pin header that provides interfaces for the following functions



Power LED: Pins 1,2

The power LED indicates the status of the main power switch.

Pin #	Signal Name
1	+5V
2	GND

ATX Power ON Switch: Pins 3, 4

This 2-pin connector is an "ATX Power Supply On/Off Switch" on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.

Pin #	Signal Name
3	Power_ON
4	GND

Hard Disk Drive LED Connector: Pins 5, 6

This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.

Pin #	Signal Name
5	+3.3V
6	-HDD_LED

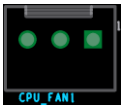
Reset Switch: Pins 7, 8

The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.

Pin #	Signal Name
7	PM_SYSRST#
8	GND

CPU_FAN1: System Fan Power Connector

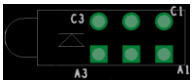
FAN1 is a 3-pin header for system fans. (Max. 1A).



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation control

LED6: Status LED

A1 & C1 : Status LED
A2 & C2 : Bypass LED
A3 & C3 : Power LED



Signal Name	Pin #	Pin #	Signal Name
SIO_GP27	A1	C1	SIO_GP26
ALARM_R	A2	C2	SIO_GP25
PWR_R	A3	C3	GND

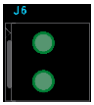
Remark: It is controlled by Logical Device 7, Index port is 0x2E, Data port is 0x2F, GPIO24-27 Data Register: 0xE9 BIT4-7

CN11 : DC Power Jack (+12V only)

Remarks: CN11 and J6 cannot be connected at the same time.

J6: AT_12V Connector

J6 is a DC-in internal connector supporting +12V.
Remarks: CN11 and J6 cannot be connected at the same time.



Pin #	Signal Name
1	+12V
2	Ground

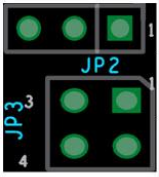
SW2: Software reset button

Signal Name	Pin #	Pin #	Signal Name
GND	1	2	GPIO_S5_7

JP6:SODIMM Power select

Pin #	Signal Name
1	MEM_1V5
2	GND
3	MEM_1V35

JP2 & JP3: Watchdog (WDT) Bypass Control

JP2,JP3	Setting	Function	Power OFF	Power ON,OS run software
	JP2 Pin 2-3 Closed JP3Pin 1-2 Open & 3-4 Closed < Default >	System LAN bypass function is controlled by Super I/O GP23	LAN Bypass	GP23 Active: Low: Bypass High: Normal
		System will reboot upon the time out of watchdog timer.		WDT Reboot System
	JP2 Pin 1-2 Closed JP3 Pin 1-2 & 3-4 Open	System will Normal LAN upon the time out of watchdog timer.		Relay Mode Change
	JP2 Pin 2-3 Closed JP3 Pin 1-2 & 3-4 Open	System LAN bypass function is controlled by Super I/O GP23.		GP23 Active: Low: Bypass High: Normal
	JP2 Pin 1-2 Closed JP3 Pin 1-2 & 3-4 Closed	System LAN is at normal		LAN Always Normal
		System will reboot upon the time out of watchdog timer.		WDT Reboot System

CN10:Console Port

CN1: SATA3.0 Port

CN3:USB3.0 Port(x2)

CN4: USB2.0 Port(x1)

CN2: CFAST Connector

J5: Mini PCI- E(x1) W/USB Connector

CN6,CN7,CN8,CN9: Intel I211 LAN

J3:SODIMM Socket

CN5: MINI DP (only MBN500-4CG)

LED1, LED2, LED3, LED4: LAN Port Link, Active LED

BIOS Setup

This chapter describes the different settings available in the BIOS that comes with the board.

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also adds virus and password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

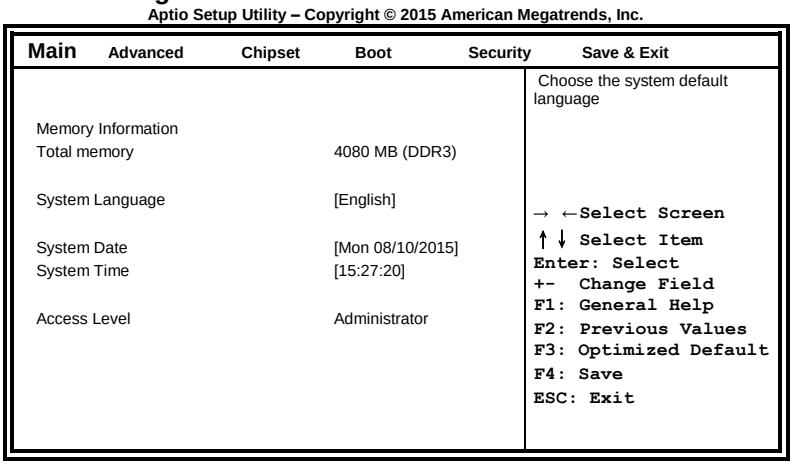
The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

```
Press  <DEL> or <F2>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Main Settings



System Date

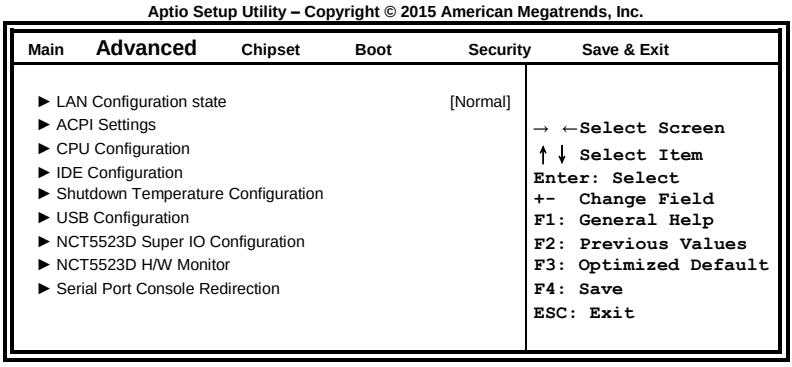
Set the Date. Use Tab to switch between Data elements.

System Time

Set the Time. Use Tab to switch between Time elements.

Advanced Settings

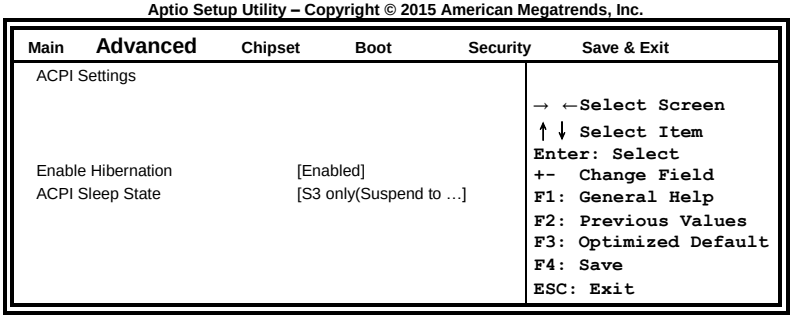
This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



LAN Configuration state

LAN Bypass Function Setting [Bypass] or [Normal]

ACPI Settings



Enable Hibernation

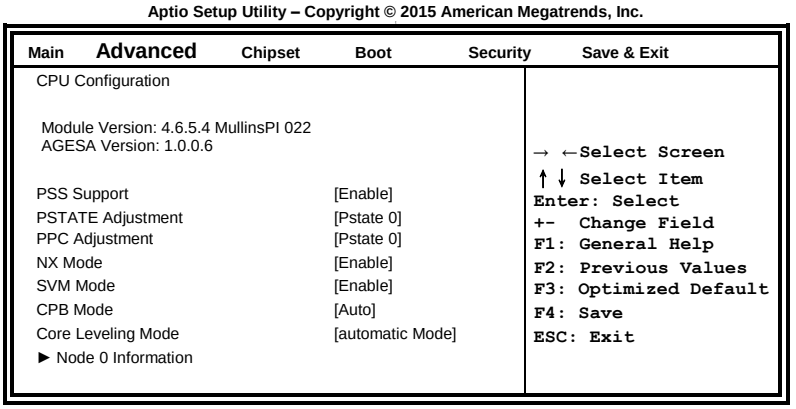
Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State

Select ACPI sleep state the system will enter, when the SUSPEND button is pressed.

CPU Configuration

This section shows the CPU configuration parameters.



PSS Support

Enable/disable the generation of ACPI _PPC, _PPC, _PSS, and _PCT objects.

PSTATE Adjustment

Provide to adjust startup P-state level.

PPC Adjustment

Provide to adjust _PPC object.

NX Mode

Enable/disable No-execute page protection function.

SVM Mode

Enable/disable CPU Virtualization.

CPB Mode

Enable/disable CPB.

Core Leveling Mode

Change the number of cores in the system.

Node 0 Information

View memory information related to Node 0.

IDE Configuration

Aptio Setup Utility – Copyright © 2015 American Megatrends, Inc.

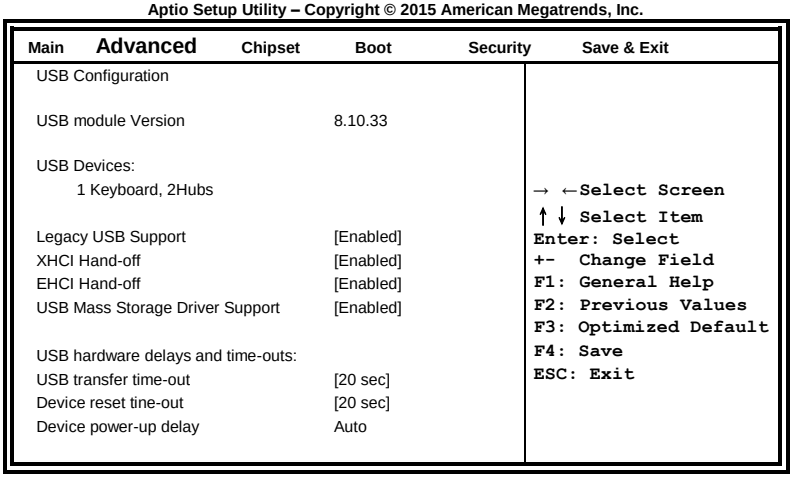
Main	Advanced	Chipset	Boot	Security	Save & Exit
IDE Configuration					
SATA Port0			Not Present		→ ←Select Screen
SATA Port1			Not Present		↑ ↓ Select Item
					Enter: Select
					+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save
					ESC: Exit

Shutdown Temperature Configuration

Aptio Setup Utility – Copyright © 2015 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
ACPI Shutdown Temperature			[Disabled]		
					→ ←Select Screen
					↑ ↓ Select Item
					Enter: Select
					+- Change Field
					F1: General Help
					F2: Previous Values
					F3: Optimized Default
					F4: Save
					ESC: Exit

USB Configuration



Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected.
DISABLE option will keep USB devices available only for EFI applications.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off

This is a workaround for OSes without EHCI hand-off support. The EHCI ownership change should be claimed by EHCI driver.

USB MASS Storage Driver Support

Enable/Disable USB Mass Storage Driver Support.

USB Transfer time-out

The time-out value for Control, Bulk, and Interrupt transfers.

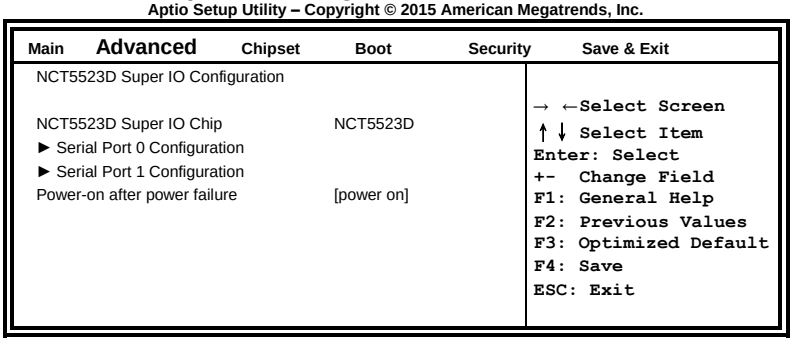
Device reset time-out

USB mass storage device start unit command time-out.

Device power-up delays

Maximum time the device will take before it properly
Reports itself to the host controller.
'Auto' uses default value: for a Root port it is 100 ms,
For a Hub port the delay is taken form Hub descriptor.

NCT5523D Super IO Configuration



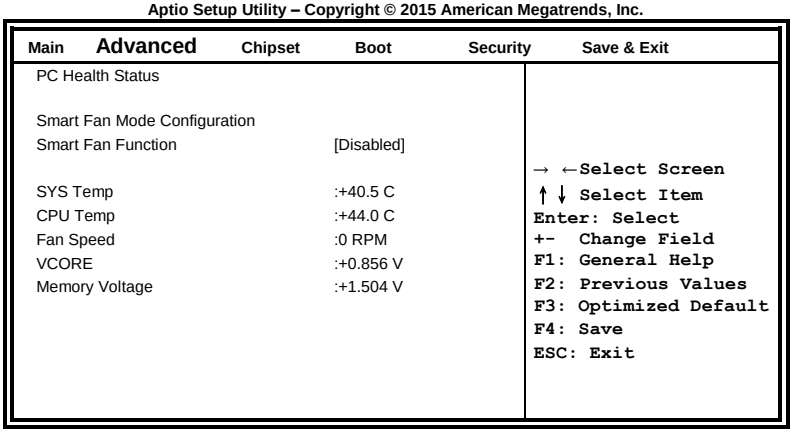
Serial Port 0 Configuration

Set parameters of Serial Port 0 (COMA)

Serial Port 1 Configuration

Set parameters of Serial Port 1 (COMB)

NCT5523D H/W Monitor



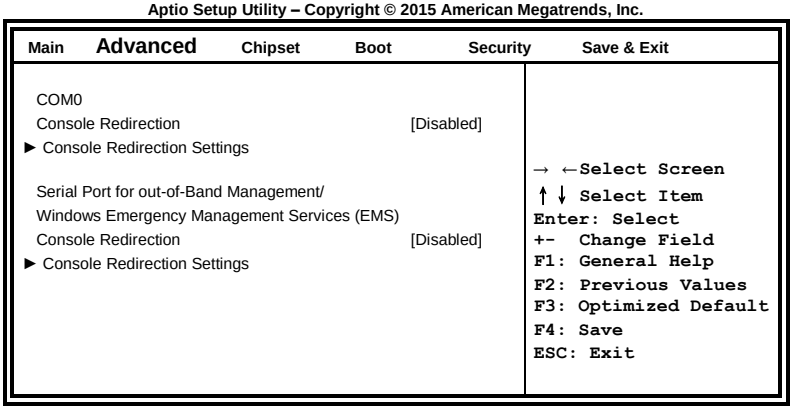
Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the board. The values are read-only values as monitored by the system and show the PC health status.

Smart Fan Function

This field enables or disables the smart fan feature. At a certain temperature, the fan starts turning. Once the temperature drops to a certain level, it stops turning again.

Serial Port Console Redirection

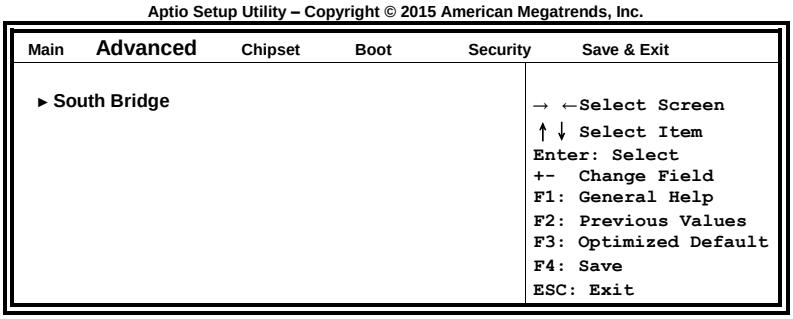


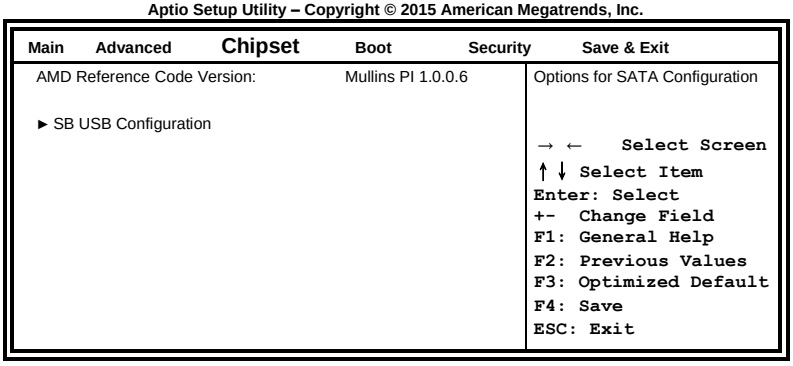
Console Redirection

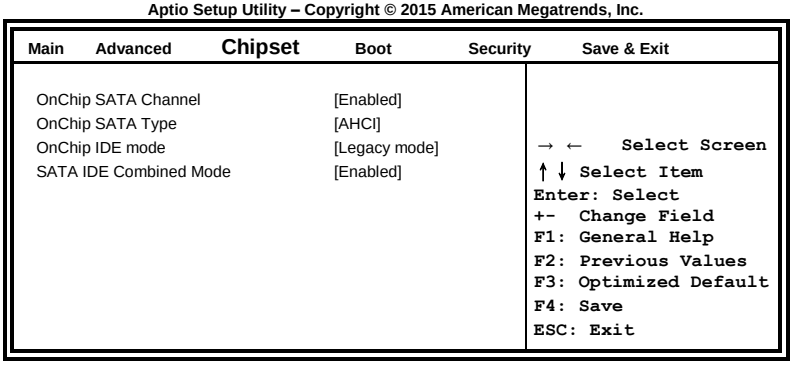
Console Redirection Enable or Disable

Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.







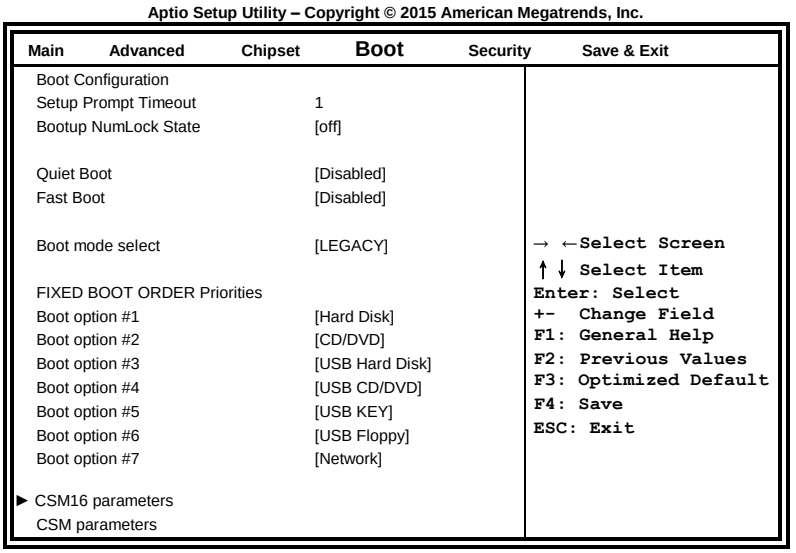
OnChip SATA Channel
Enabled / Disabled Serial ATA.

OnChip SATA Type
Select OnChip SATA Type.

OnChip IDE mode
Sata IDE Controller Mode.

SATA IDE Combined Mode
SATA IDE Controller Combined Mode

Boot Settings
This section allows you to configure the boot settings.



Setup Prompt Timeout
Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State
Select the keyboard NumLock state.

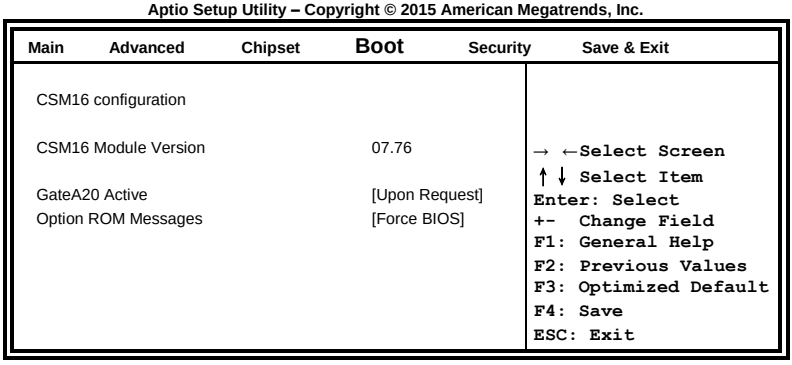
Quiet Boot
Enables or Disables Quiet Boot option.

Fast Boot
Enables or Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

Boot mode select
Select boot mode LEGACY/UEFI

Boot Option Priorities
Sets the system boot order.

CSM16 parameters
CSM16 configuration Enable/Disable, Option ROM execution settings,etc.

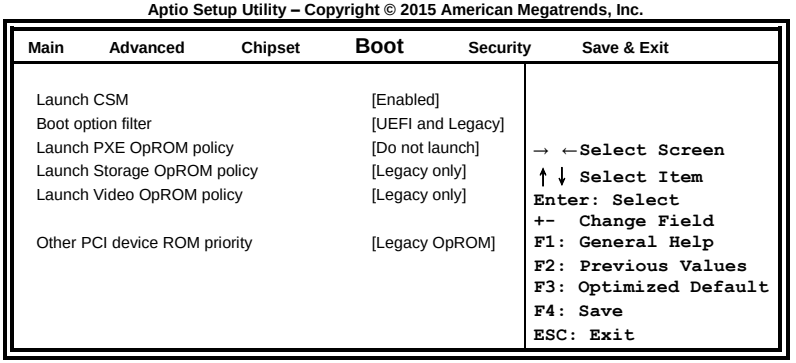


GateA20 Active
UPON REQUEST – GA20 can be disabled using BIOS services.
ALWAYS – do not allow disabling GA20 ; this option is useful when any RT code is executed above 1MB

Option ROM Messages
Set display mode for Option ROM

CSM parameters

OpROM execution, boot options filter,etc.



Launch CSM

This option controls if CSM will be launched.

Boot option filter

This option controls what devices system can boot to.

Launch PXE OpROM policy

Controls the execution of UEFI and Legacy PXE OpROM.

Launch Storatge OpROM policy

Controls the execution of UEFI and Legacy Storage OpROM.

Launch Video OpROM policy

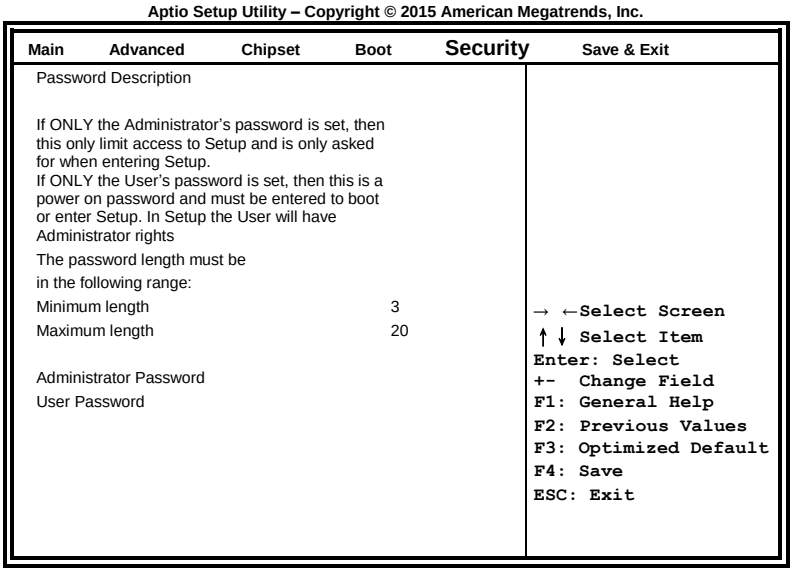
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI device ROM priority

For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



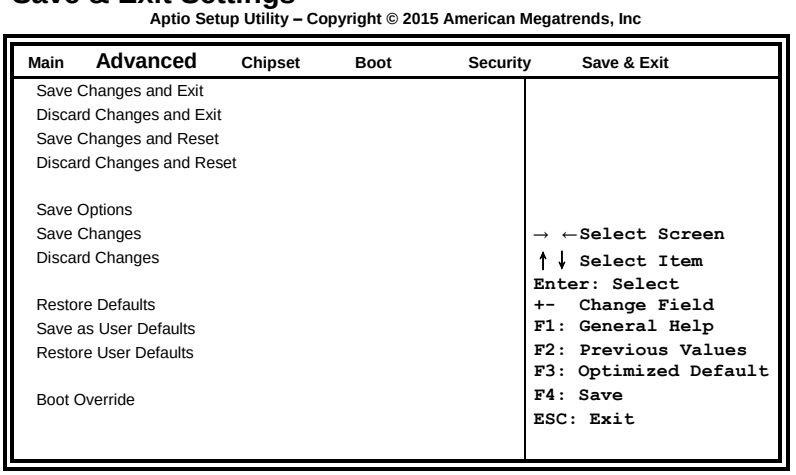
Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings



Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

.

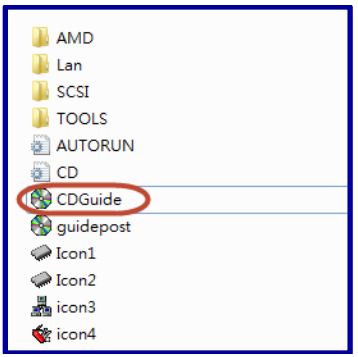
Drivers Installation

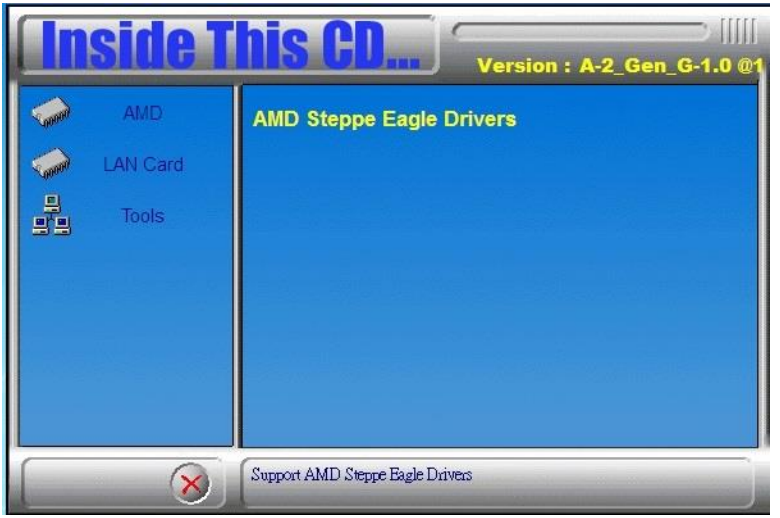
This section describes the installation procedures for software and drivers. The software and drivers are included with the board. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

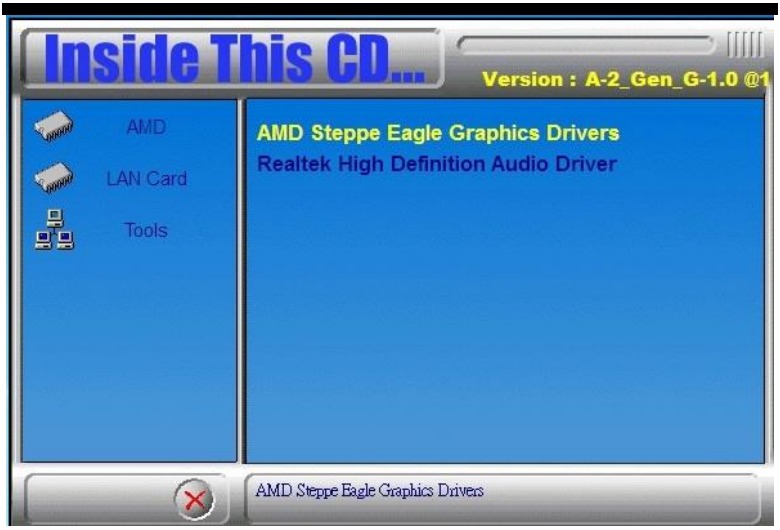
Chipset Software Installation Utility

1. In the Drvier folder, execute the CDGulde file. Click ***AMD***, then ***AMD Steppe Eagle Drivers***.

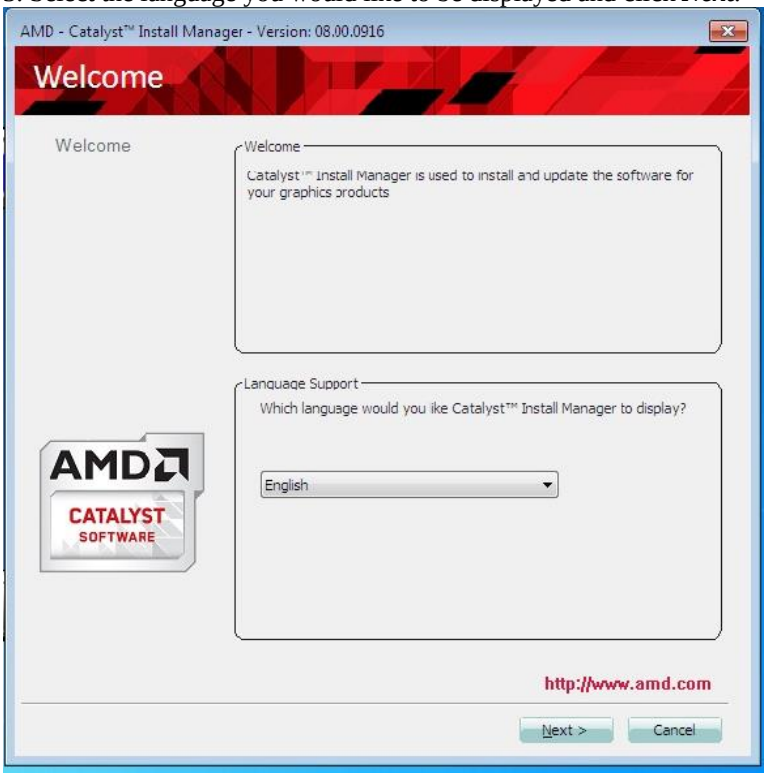




2. Click ***AMD Steppe Eagle Graphics Drivers***.

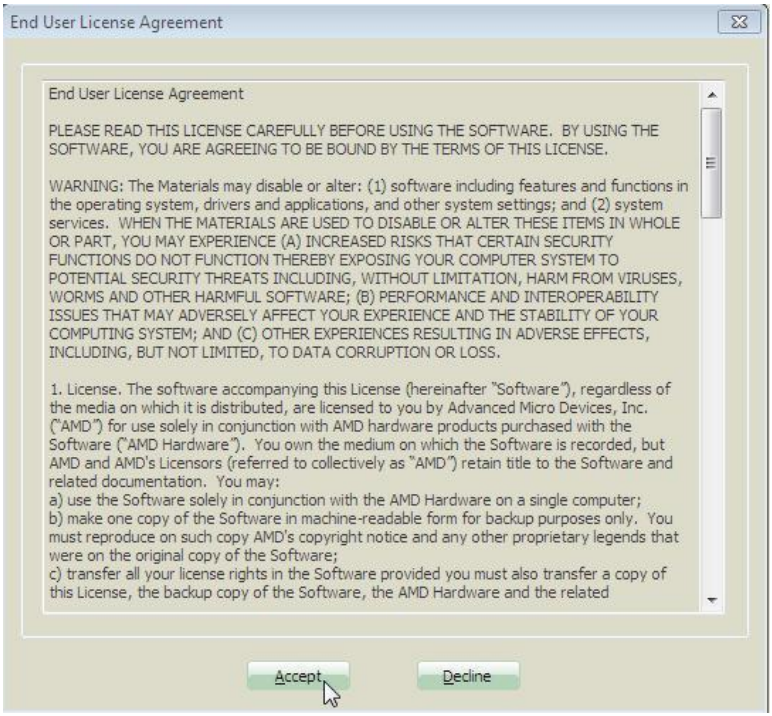

Inside This CD...
Version : A-2_Gen_G-1.0 @1
AMD
LAN Card
Tools
AMD Steppe Eagle Graphics Drivers
Realtek High Definition Audio Driver
AMD Steppe Eagle Graphics Drivers

3. Select the language you would like to be displayed and click ***Next***.

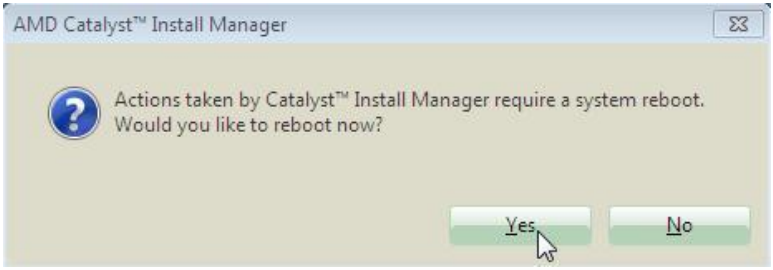


4. Select **Express** and the **installation location** and click ***Next***.

5. Click ***Accept*** to accept the End User License Agreement.



6. To reboot the system, click ***Yes***.



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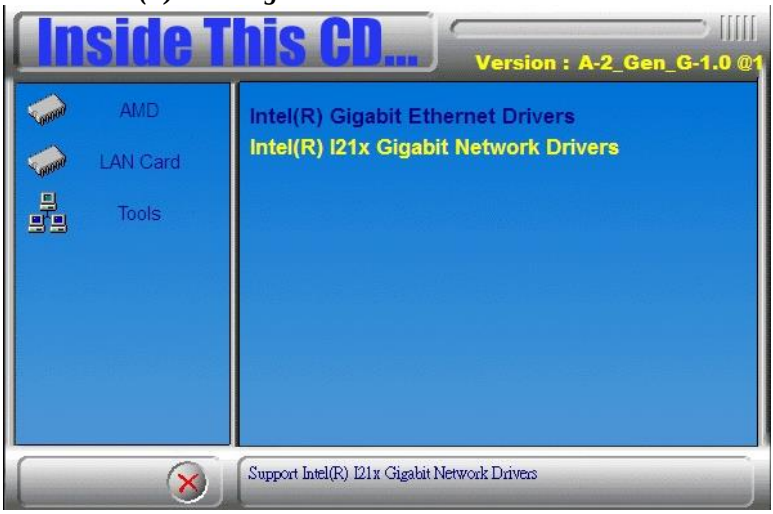
LAN Drivers Installation

1. In the Drvier folder, execute the CDGulde file.

2. Click ***LAN Card*** and then ***Intel LAN Controller Drivers***.

3.Click ***Intel(R) I21x Gigabit Network Drivers***



4. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.

5. When the Ready to Install the Program screen appears, click ***Install*** to continue.

6. When InstallShield Wizard is complete, click ***Finish***.

Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses, which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0000h-03AFh	PCI bus
0000h-000Fh	Direct memory access controller
0010h-001Fh	Motherboard resources
0020h-0021h	Programmable interrupt controller
0040h-0043h	System timer
0061h-0061h	System speaker
0070h-0071h	System CMOS/real time clock
0072h-007Fh	Motherboard resources
0081h-0083h	Direct memory access controller
0084h-0086h	Motherboard resources
0087h-0087h	Direct memory access controller
00A0h-00A1h	Programmable interrupt controller
00A2h-00BFh	Motherboard resources
00C0h-000Dh	Direct memory access controller
00F0h-00FFh	Numeric data processor
02F8h-02FFh	Communications Port (COM2)
03B0h-03BBh	PCI Express standard Root Port
03B8h-03DFh	PCI bus
03F8h-03FFh	Communications Port (COM1)
0CD8h-0CDFh	Motherboard resources
F000h-F00Fh	AMD SATA Controller

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 0	System timer
IRQ 3	Communications Port (COM2)
IRQ 4	Communications Port (COM1)
IRQ 8	High precision event timer
IRQ 13	Numeric data processor
IRQ 18	Standard Enhanced PCI to USB Host Controller
IRQ 18	Standard Enhanced PCI to USB Host Controller
IRQ 19	AMD SATA Controller
IRQ81	Microsoft ACPI-Compliant System
IRQ82	Microsoft ACPI-Compliant System
IRQ83	Microsoft ACPI-Compliant System
IRQ84	Microsoft ACPI-Compliant System

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

File of the NCT5523D.H

```
//-----------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//-----------------------------------------------------------------------------
#ifndef __NCT5523D_H
#define __NCT5523D_H 1
//-----------------------------------------------------------------------------
#define NCT5523D_INDEX_PORT (NCT5523D_BASE)
#define NCT5523D_DATA_PORT (NCT5523D_BASE+1)
//-----------------------------------------------------------------------------
#define NCT5523D_REG_LD 0x07
//-----------------------------------------------------------------------------
#define NCT5523D_UNLOCK 0x87
#define NCT5523D_LOCK 0xAA
//-----------------------------------------------------------------------------
unsigned int Init_NCT5523D(void);
void Set_NCT5523D_LD( unsigned char);
void Set_NCT5523D_Reg( unsigned char, unsigned char);
unsigned char Get_NCT5523D_Reg( unsigned char);
//-----------------------------------------------------------------------------
#endif //__NCT5523D_H
```

File of the MAIN.CPP.

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "NCT5523D.H"
//---------------------------------------------------------------------------
int main (void);
void WDTInitial(void);
void WDTEnable(unsigned char);
void WDTDisable(void);
//---------------------------------------------------------------------------
int main (void)
{
char SIO;
SIO = Init_NCT5523D();
if (SIO == 0)
{
printf("Can not detect Nuvoton NCT5523D, program abort.\n");
return(1);
}
WDTInitial();
WDTEnable(10);
WDTDisable();
return 0;
}
//---------------------------------------------------------------------------
void WDTInitial(void)
{
unsigned char bBuf;
Set_NCT5523D_LD(0x08); //switch to logic device 8
bBuf = Get_NCT5523D_Reg(0x30);
bBuf &= (~0x01);
Set_NCT5523D_Reg(0x30, bBuf); //Enable WDTO
}
//---------------------------------------------------------------------------
```

```
void WDTEnable(unsigned char NewInterval)
{
unsigned char bBuf;
Set_NCT5523D_LD(0x08); //switch to logic device 8
Set_NCT5523D_Reg(0x30, 0x01); //enable timer
bBuf = Get_NCT5523D_Reg(0xF0);
bBuf &= (~0x08);
Set_NCT5523D_Reg(0xF0, bBuf); //count mode is second
Set_NCT5523D_Reg(0xF1, NewInterval); //set timer
}
//-----------------------------------------------------------------------------
void WDTDisable(void)
{
Set_NCT5523D_LD(0x08); //switch to logic device 8
Set_NCT5523D_Reg(0xF1, 0x00); //clear watchdog timer
Set_NCT5523D_Reg(0x30, 0x00); //watchdog disabled
}
//-----------------------------------------------------------------------------
```