



SU968
COM Express Compact Module
User's Manual

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COM Express Specification Reference

PICMG® COM Express Module™ Base Specification.

http://www.picmg.org/

FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

Notice:

- The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
- 2. Shielded interface cables must be used in order to comply with the emission limits.

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About this Manual

This manual can be downloaded from the website, or acquired as an electronic file included in the optional CD/DVD. The manual is subject to change and update without notice, and may be based on editions that do not resemble your actual products. Please visit our website or contact our sales representatives for the latest editions.

Warranty

- Warranty does not cover damages or failures that arised from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.
- 2. The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.
- Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.
- 4. We will not be liable for any indirect, special, incidental or consequencial damages to the product that has been modified or altered.

Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

- To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.
- 2. Wear an antistatic wrist strap.
- 3. Do all preparation work on a static-free surface.
- 4. Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.
- Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.



Important:

Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

Safety Measures

To avoid damage to the system:

Use the correct AC input voltage range.

To reduce the risk of electric shock:

Unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- One SU968 board
- One Heat Sink (Height: 23.8mm)

Optional Items

- COM332-B Carrier Board Kit
- Heat spreader (Height: 11mm)

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

Before Using the System Board

Before using the system board, prepare basic system components.

If you are installing the system board in a new system, you will need at least the following internal components.

• Storage devices such as hard disk drive, CD-ROM, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

Chapter 1 - Introduction

Specifications

SYSTEM Processor 6th Generation Intel® Core™ Processors, BGA 1356 Intel® Core™ i7-6600U Processor, Dual Core, 4M Cache, 2.6GHz (3 Intel® Core™ i5-6300U Processor, Dual Core, 3M Cache, 2.4GHz (3 Intel® Core™ i3-6100U Processor, Dual Core, 3M Cache, 2.3GHz, 1 Intel® Celeron® Processor 3955U, Dual Core, 2M Cache, 2.0GHz, 1	
	5W
Memory Two 204-pin SODIMM up to 16GB Dual Channel DDR3L 1600MHz	
BIOS Insyde SPI 128Mbit	
GRAPHICS Controller Intel® HD Graphics	
Feature OpenGL 5.0, DirectX 12, OpenCL 2.1 HW Decode: AVC/H.264, MPEG2, VC1/WMV9, JPEG/MJPEG, HEVC/H2 HW Encode: AVC/H.264, MPEG2, JPEG, HEVC/H265, VP8, VP9	265, VP8, VP9
Display 1 x VGA/DDI (DDI available upon request) 1 x LVDS/eDP (eDP available upon request) 1 x DDI VGA: resolution up to 1920x1200 @ 60Hz LVDS: dual channel 24-bit, resolution up to 1920x1200 @ 60Hz HDMI: resolution up to 4096x2160 @ 24Hz or 2560x1600 @ 60Hz DP++: resolution up to 4096x2304 @ 60Hz eDP: resolution up to 4096x2304 @ 60Hz	
Triple Displays VGA + LVDS + DDI DDI + eDP + DDI	
EXPANSION Interface 5 PCIe x1 or 4 PCIe x1 + 1 PCIe x4 or 3 PCIe x1 + 2 PCIe x2 (supplemental supplemental su	pport up to 5
AUDIO Interface HD Audio	
ETHERNET Controller 1 x Intel® 1219LM with iAMT11.0 PCIe (10/100/1000Mbps) (only Core i7/i5 supports iAMT)	
1/O USB 4 x USB 3.0 8 x USB 2.0	
SATA 3 x SATA 3.0 (up to 6Gb/s) RAID 0/1/5/10	
DIO 1 x 8-bit DIO	

WATCHDOG TIMER	Output & Interval	System Reset, Programmable via Software from 1 to 255 Seconds			
SECURITY	TPM	Available Upon Request			
POWER	Туре	12V, 5VSB, VCC_RTC (ATX mode) 12V, VCC_RTC (AT mode)			
	Consumption	Typical: I7-6600U: 12V @ 0.86A (10.28Watt) Max.: I7-6600U: 12V @ 1.372A (16.46Watt)			
OS SUPPORT		Windows 7/WES7 (32/64-bit) Windows 8.1 (64-bit) Windows 10 IoT Enterprise 64-bit Ubuntu 16.04 (Intel graphic driver available)			
ENVIRONMENT	Temperature	Operating : 0 to 60°C : -40 to 85°C (with heat spreader) Storage: -40 to 85°C			
	Humidity	Operating: 5 to 90% RH Storage: 5 to 90% RH			
	MTBF	921,923 hrs @ 25°C; 460,715 hrs @ 45°C; 256,677 hrs @ 60°C Calculation Model: Telcordia Issue 2, Method Case 3 Environment: GB, GC – Ground Benign, Controlled			
MECHANICAL	Dimensions	COM Express® Compact 95mm (3.74") x 95mm (3.74")			
	Compliance	PICMG COM Express® R2.1, Type 6			

Chapter 1 Introduction www.dfi.com

Features

Watchdog Timer

The Watchdog Timer function allows your application to regularly "clear" the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

• DDR3L

DDR3L SDRAM provides backward compatibility to DDR3 memory modules but can operate at the same or at a lower power level.

Graphics

The integrated Intel® HD graphics engine delivers an excellent blend of graphics performance and features to meet business needs. It provides excellent video and 3D graphics with outstanding graphics responsiveness. These enhancements deliver the performance and compatibility needed for today's and tomorrow's business applications. It supports VGA/DDI, LVDS/eDP and DDI interfaces for triple display outputs.

Serial ATA

Serial ATA is a storage interface that is compliant with SATA 1.0a specification. With speed of up to 6Gb/s (SATA 3.0), it improves hard drive performance to be faster than the standard parallel ATA, which only has data transfer rate of 100MB/s. The bandwidth of the SATA 3.0 will be limited by carrier board design.

Gigabit LAN

The Intel® I219LM with iAMT11.0 Gigabit LAN controller supports up to 1Gbps data transmission (only Core i7/i5 supports iAMT).

• USB

The system board supports the new USB 3.0. It is capable of running at a maximum transmission speed of up to 5 Gbit/s (625 MB/s) and is faster than USB 2.0 (480 Mbit/s, or 60 MB/s) and USB 1.1 (12Mb/s). USB 3.0 reduces the time required for data transmission, reduces power consumption, and is backward compatible with USB 2.0. It is a marked improvement in device transfer speeds between your computer and a wide range of simultaneously accessible external Pluq and Play peripherals.

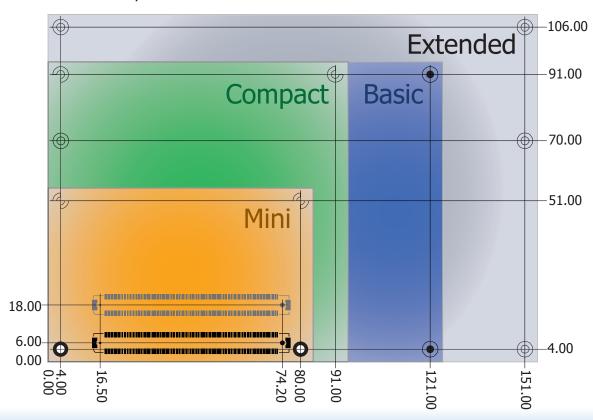
Chapter 2 - Concept

COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules.

SU968 is a COM Express Compact module. The dimension is 95mm x 95mm.

- O Common for all Form Factors
- Extended only
- Basic only
- **©** Compact only
- [♠] Compact and Basic only



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Specification Comparison Table

The table below shows the COM Express standard specifications and the corresponding specifications supported on the SU968 module.

			1
		COM Express Module Base	DFI SU968
Connector	Feature	Specification Type 6	Type 6
Connector	reature	(No IDE or PCI, add DDI+ USB3)	
		Min / Max	
A-B		System I/O	<u> </u>
A-B	PCI Express Lanes 0 - 5	1/6	6
A-B	LVDS Channel A	0 / 1	1
A-B	LVDS Channel B	0 / 1	1
A-B	eDP on LVDS CH A pins	0 / 1	1
A-B	VGA Port	0 / 1	0/1 (Option : DDI2 or VGA)
A-B	TV-Out	NA	NA
A-B	DDI 0	NA	NA
A-B ⁵	Serial Ports 1 - 2	0 / 2	2
A-B	CAN interface on SER1	0 / 1	0
A-B	SATA / SAS Ports	1 / 4	3 (with Intel® Celeron®: 2)
A-B	AC'97 / HDA Digital Interface	0 / 1	1
A-B	USB 2.0 Ports	4 / 8	8
A-B	USB Client	0 / 1	0
A-B	USB 3.0 Ports	NA	NA
A-B	LAN Port 0	1 / 1	1
A-B	Express Card Support	1/2	2
A-B	LPC Bus	1 / 1	1
A-B	SPI	1 / 2	1
A-B		System Manageme	ent
A-B ⁶	SDIO (muxed on GPIO)	0 / 1	0
A-B	General Purpose I/O	8 / 8	8
A-B	SMBus	1 / 1	1
A-B	I2C	1 / 1	1
A-B	Watchdog Timer	0 / 1	1
A-B	Speaker Out	1 / 1	1
A-B	External BIOS ROM Support	0 / 2	1
A-B	Reset Functions	1 / 1	1

- 5 Indicates 12V-tolerant features on former VCC_12V signals.
- 6 Cells in the connected columns spanning rows provide a rough approximation of features sharing connector pins.

Connector	Feature	COM Express Module Base Specification Type 6 (No IDE or PCI, add DDI+ USB3) Min / Max	DFI SU968 Type 6
A-B		Power Manageme	nt
A-B	Thermal Protection	0 / 1	1
A-B	Battery Low Alarm	0 / 1	1
A-B	Suspend/Wake Signals	0/3	1
A-B	Power Button Support	1 / 1	1
A-B	Power Good	1 / 1	1
A-B	VCC_5V_SBY Contacts	4 / 4	4
A-B ⁵	Sleep Input	0 / 1	1
A-B ⁵	Lid Input	0 / 1	1
A-B ⁵	Fan Control Signals	0 / 2	2
A-B	Trusted Platform Modules	0 / 1	1
A-B		Power	
A-B	VCC_12V Contacts	12 / 12	12

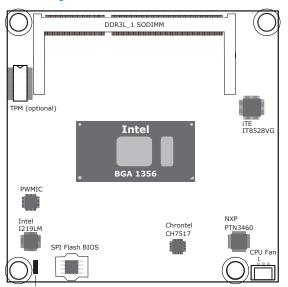
Module Pin-out - Required and Optional Features C-D Connector. PICMG® COM.0 Revision 2.1

Connector	Feature	COM Express Module Base Specification Type 6 (No IDE or PCI, add DDI+ USB3) Min / Max	DFI SU968 Type 6
C-D		System I/O	
	PCI Express Lanes 16 - 31	0 / 16	0
	PCI Express Graphics (PEG)	0 / 1	0
C-D ⁶	Muxed SDVO Channels 1 - 2	NA	NA
	PCI Express Lanes 6 - 15	0 / 2	2
	PCI Bus - 32 Bit	NA	NA
	PATA Port	NA	NA
	LAN Ports 1 - 2	NA	NA
	DDIs 1 - 3	0/3	1/2 (Option : DDI2 or VGA)
C-D ⁶	USB 3.0 Ports	0 / 4	4
C-D		Power	
C-D	VCC_12V Contacts	12 / 12	12

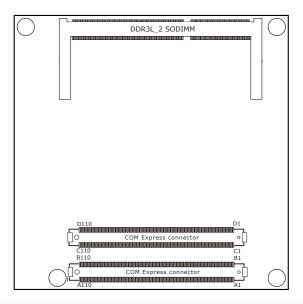
Chapter 2 Concept www.dfi.com

Chapter 3 - Hardware Installation

Board Layout

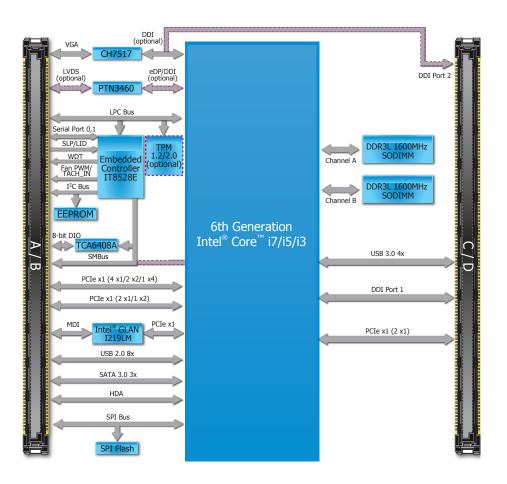


Top View



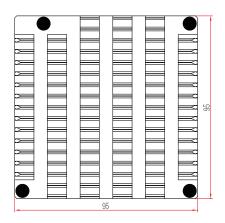
Bottom View

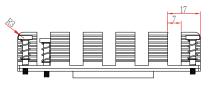
Block Diagram

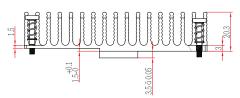


Mechanical Diagram

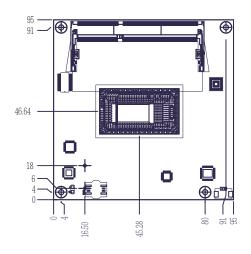
Heat Sink



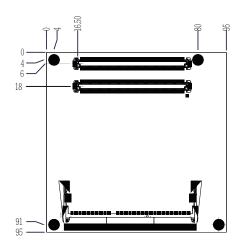




SU968 Module



Top View



Bottom View



Important:

Electrostatic discharge (ESD) can damage your board, processor, disk drives, add-in boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

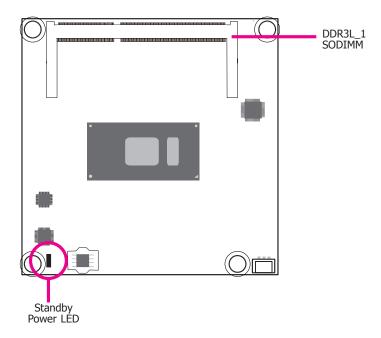
System Memory

The system board is equipped with two 204-pin SODIMM sockets supporting up to 16GB system memory and dual channel DDR3L 1600MHz memory interface.

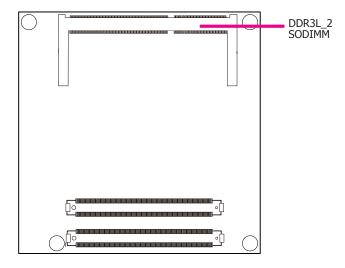


Important:

When the Standby Power LED is red, it indicates that there is power on the board. Power-off the PC then unplug the power cord prior to installing any devices. Failure to do so will cause severe damage to the board and components.



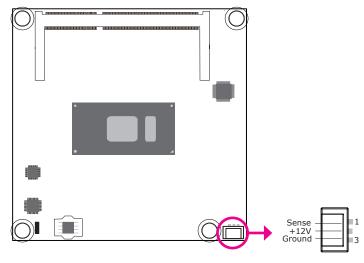
Top View



Bottom View

Connectors

CPU Fan Connector



Connect the CPU fan's cable connector to the CPU fan connector on the board. The cooling fan will provide adequate airflow throughout the chassis to prevent overheating the CPU and board components.

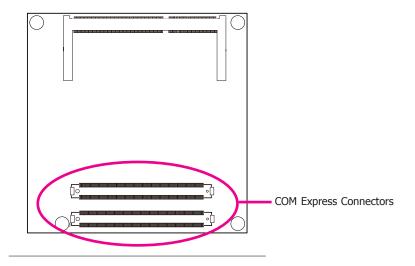
BIOS Setting

"PC Health Status" submenu in the Advanced menu of the BIOS will display the current speed of the cooling fan. Refer to chapter 4 of the manual for more information.

COM Express Connectors

The COM Express connectors are used to interface the SU968 COM Express board to a carrier board. Connect the COM Express connectors (located on the solder side of the board) to the COM Express connectors on the carrier board.

Refer to the "Installing SU968 onto a Carrier Board" section in this chapter for more information.



Refer to the following pages for the pin functions of these connectors.

COM Express Connectors

Row A		Row B	}	Row A		Row B	
A1	GND (FIXED)	B1	GND (FIXED)	A56	PCIE_TX4-	B56	PCIE_RX4-
A2	GBE0 MDI3-	B2	GBE0 ACT#	A57	GND	B57	GPO2
A3	GBE0 MDI3+	В3	LPC FRAME#	A58	PCIE TX3+	B58	PCIE RX3+
A4	GBE0 LINK100#	B4	LPC_AD0	A59	PCIE TX3-	B59	PCIE RX3-
A5	GBE0 LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0 MDI2-	В6	LPC AD2	A61	PCIE TX2+	B61	PCIE RX2+
A7	GBE0 MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_INK#	B8	NA	A63	GPI1	B63	GPO3
A9	GBE0 MDI1-	B9	NA	A64	PCIE TX1+	B64	PCIE RX1+
A10	GBE0 MDI1+	B10	LPC CLK	A65	PCIE TX1-	B65	PCIE RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0 MDI0-	B12	PWRBTN#	A67	GPI2	B67	NA NA
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE TX0+	B68	PCIE_RX0+
A14	GBE0 CTREF	B14	SMB DAT	A69	PCIE TX0-	B69	PCIE RX0-
A15	SUS S3#	B15	SMB_ALERT#	A70	GND(FIXED)	B70	GND (FIXED)
	_			A71	LVDS A0+	B71	LVDS B0+
A16	SATAO_TX+	B16	SATA1_TX+	A72	LVDS_A0+	B72	LVDS_B0-
A17	SATA0_TX-	B17	SATA1_TX-		_	B73	LVDS_B0-
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B74	
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-		LVDS_B1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	LVDS_B2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	LVDS_B2-
A22	SATA2_TX+	B22	NA	A77	LVDS_VDD_EN	B77	LVDS_B3+
A23	SATA2_TX-	B23	NA	A78	LVDS_A3+	B78	LVDS_B3-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	SATA2_RX+	B25	NA	A80	GND (FIXED)	B80	GND (FIXED)
A26	SATA2_RX-	B26	NA	A81	LVDS_A_CK+	B81	LVDS_B_CK+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	LVDS_B_CK-
A28	(S)ATA_ACT#	B28	NA	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	AC/HDA_SYNC	B29	AC/HDA _SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	AC/HDA _RST#	B30	AC/HDA _SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	AC/HDA _BITCLK	B32	SPKR	A87	RSVD	B87	VCC_5V_SBY
A33	AC/HDA _SDOUT	B33	I2C_CK	A88	PCIE0_CK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE0_CK_REF-	B89	VGA_RED
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	VGA_GRN
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	VGA_BLU
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GP00	B93	VGA_HSYNC
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	VGA_VSYNC
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	VGA_I2C_CK
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	VGA_I2C_DAT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	RSVD
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	RSVD
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	EXCD1_PERST#	A102	SER1_RX	B102	FAN_TACHIN
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	A103	LID#	B103	SLEEP#
A49	EXCD0_CPPE#	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	PCIE_TX5+	B52	PCIE_RX5+	A107	VCC_12V	B107	VCC_12V
A53	PCIE_TX5-	B53	PCIE_RX5-	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	PCIE_TX4+	B55	PCIE_RX4+	A110	GND (FIXED)	B110	GND (FIXED)
		-			()		(

Row C	Row C		Row D		Row C		Row D	
C1	GND (FIXED)	D1	GND (FIXED)	C56	NA	D56	NA	
C2	GND	D2	GND	C57	TYPE1#	D57	TYPE2#	
C3	USB_SSRX0-	D3	USB_SSTX0-	C58	NA	D58	NA	
C4	USB_SSRX0+	D4	USB_SSTX0+	C59	NA	D59	NA	
C5	GND	D5	GND	C60	GND (FIXED)	D60	GND (FIXED)	
C6	USB_SSRX1-	D6	USB_SSTX1-	C61	NA	D61	NA	
C7	USB_SSRX1+	D7	USB_SSTX1+	C62	NA	D62	NA	
C8	GND	D8	GND	C63	RSVD	D63	RSVD	
C9	USB_SSRX2-	D9	USB_SSTX2-	C64	RSVD	D64	RSVD	
C10	USB_SSRX2+	D10	USB_SSTX2+	C65	NA	D65	NA	
C11	GND (FIXED)	D11	GND (FIXED)	C66	NA	D66	NA	
C12	USB_SSRX3-	D12	USB_SSTX3-	C67	RSVD	D67	GND	
C13	USB_SSRX3+	D13	USB_SSTX3+	C68	NA	D68	NA	
C14	GND	D14	GND	C69	NA	D69	NA	
C15	NA	D15	DDI1_CTRLCLK_AUX+	C70	GND (FIXED)	D70	GND (FIXED)	
C16	NA	D16	DDI1 CTRLDATA AUX-	C71	NA	D71	NA	
C17	RSVD	D17	RSVD	C72	NA	D72	NA	
C18	RSVD	D18	RSVD	C73	GND	D73	GND	
C19	PCIE_RX6+	D19	PCIE_TX6+	C74	NA	D74	NA	
C20	PCIE RX6-	D20	PCIE TX6-	C75	NA	D75	NA	
C21	GND (FIXED)	D21	GND (FIXED)	C76	GND	D76	GND	
C22	PCIE RX7+	D22	PCIE_TX7+	C77	RSVD	D77	RSVD	
C23	PCIE RX7-	D23	PCIE TX7-	C78	NA	D78	NA	
C24	DDI1 HPD	D24	RSVD	C79	NA	D79	NA	
C25	NA	D25	RSVD	C80	GND (FIXED)	D80	GND (FIXED)	
C26	NA	D26	DDI1 PAIR0+	C81	NA	D81	NA	
C27	RSVD	D27	DDI1 PAIR0-	C82	NA	D82	NA	
C28	RSVD	D28	RSVD	C83	RSVD	D83	RSVD	
C29	NA	D29	DDI1 PAIR1+	C84	GND	D84	GND	
C30	NA	D30	DDI1_PAIR1-	C85	NA	D85	NA	
C31	GND (FIXED)	D31	GND (FIXED)	C86	NA	D86	NA	
C32	DDI2_CTRLCLK_AUX+	D32	DDI1 PAIR2+	C87	GND	D87	GND	
C33	DDI2_CTRLDATA_AUX-	D33	DDI1 PAIR2-	C88	NA	D88	NA	
C34	DDI2_DDC_AUX_SEL	D34	DDI1_DDC_AUX_SEL	C89	NA	D89	NA	
C35	RSVD	D35	RSVD	C90	GND (FIXED)	D90	GND (FIXED)	
C36	NA	D36	DDI1 PAIR3+	C91	NA	D91	NA	
C37	NA	D37	DDI1 PAIR3-	C92	NA	D92	NA	
C38	NA	D38	RSVD	C93	GND	D93	GND	
C39	NA	D39	DDI2 PAIR0+	C94	NA	D94	NA	
C40	NA	D40	DDI2 PAIR0-	C95	NA	D95	NA	
C41	GND (FIXED)	D41	GND (FIXED)	C96	GND	D96	GND	
C42	NA	D42	DDI2_PAIR1+	C97	RSVD	D97	RSVD	
C43	NA	D43	DDI2_PAIR1-	C98	NA	D98	NA	
C44	NA	D44	DDI2_HPD	C99	NA	D99	NA	
C45	RSVD	D45	RSVD	C100	GND (FIXED)	D100	GND (FIXED)	
C46	NA	D46	DDI2 PAIR2+	C101	NA	D101	NA	
C47	NA	D47	DDI2 PAIR2-	C102	NA	D102	NA	
C48	RSVD	D48	RSVD	C103	GND	D103	GND	
C49	NA	D49	DDI2 PAIR3+	C104	VCC 12V	D104	VCC 12V	
C50	NA NA	D50	DDI2_PAIR3-	C104	VCC_12V	D104	VCC_12V	
C51	GND (FIXED)	D51	GND (FIXED)	C106	VCC_12V	D106	VCC 12V	
C52	NA	D52	NA	C107	VCC_12V	D100	VCC_12V	
C53	NA	D53	NA	C107	VCC_12V	D107	VCC_12V	
C54	TYPE0#	D54	PEG_LANE_REV#	C109	VCC 12V	D100	VCC 12V	
C55	NA	D55	NA	C110	GND (FIXED)	D110	GND (FIXED)	
200	1			0110	OUD (LIVED)	טווע	OUD (LIVED)	

COM Express Connectors Signals and Descriptions

Pin Types
I Input to the Module
O Output from the Module
I/O Bi-directional input / output signal
OD Open drain output

AC97/HDA Signals and	AC97/HDA Signals and Descriptions										
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description					
AC/HAD_RST#	A30	O CMOS	3.3V Suspend/3.3V		Connect to CODEC pin 11 RESET#	Reset output to CODEC, active low.					
AC/HDA_SYNC	A29	O CMOS	3.3V/3.3V		Connect to CODEC pin 10 SYNC	Sample-synchronization signal to the CODEC(s).					
AC/HDA_BITCLK	A32	I/O CMOS	3.3V/3.3V		Connect to CODEC pin 6 BIT_CLK	Serial data clock generated by the external CODEC(s).					
AC/HDA_SDOUT	A33	O CMOS	3.3V/3.3V		Connect to CODEC pin 5 SDATA_OUT	Serial TDM data output to the CODEC.					
AC/HDA_SDIN2	B28	I/O CMOS	3.3V Suspend/3.3V	NA							
AC/HDA_SDIN1	B29	I/O CMOS	3.3V Suspend/3.3V			Serial TDM data inputs from up to 2 CODECs.					
AC/HDA_SDIN0	B30	I/O CMOS	3.3V Suspend/3.3V		Connect 33 Ω in series to CODEC0 pin 8 SDATA_IN						

Gigabit Ethernet Sign	Sigabit Ethernet Signals and Descriptions									
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description				
GBE0_MDI0+	A13	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI0+/-	Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:				
GBE0_MDI0-	A12	I/O Analog	3.3V max Suspend							
GBE0_MDI1+	A10	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI1+/-					
GBE0_MDI1-	A9	I/O Analog	3.3V max Suspend							
GBE0_MDI2+	A7	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI2+/-					
GBE0_MDI2-	A6	I/O Analog	3.3V max Suspend							
GBE0_MDI3+	A3	I/O Analog	3.3V max Suspend		Connect to Magnetics Module MDI3+/-					
GBE0_MDI3-	A2	I/O Analog	3.3V max Suspend	•						
GBE0_ACT#	B2	OD CMOS	3.3V Suspend/3.3V	•	Connect to LED and recommend current limit resistor 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 activity indicator, active low.				
GBE0_LINK#	A8	OD CMOS	3.3V Suspend/3.3V		NC	Gigabit Ethernet Controller 0 link indicator, active low.				
GBE0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V	•		Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low.				
GBE0_LINK100#	A4	OD CMOS	3.3V Suspend/3.3V	•	Connect to LED and recommend current limit resistor 150 Ω to 3.3VSB	Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low.				
GBE0_LINK1000#	A5	OD CMOS	3.3V Suspend/3.3V		Connect to LED and recommend current limit resistor 150 Ω to 3.3VSB	Gigabit Eulernet Controller o 1000 Pibit / Sec IIIIk Indicator, active low.				

SATA Signals and D	escriptions					
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
SATA0_TX+	A16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA0 Conn TX pin	Serial ATA or SAS Channel 0 transmit differential pair.
SATA0_TX-	A17	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATAO Conn TX pin	Serial ATA OF SAS Channel O transmit differential pair.
SATA0_RX+	A19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATAO Conn RX pin	Serial ATA or SAS Channel 0 receive differential pair.
SATA0_RX-	A20	I SATA	AC coupled on Module	AC Coupling capacitor	Conflect to SATAO Confl RX pin	Serial ATA 01 SAS Chairner o receive differential pair.
SATA1_TX+	B16	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn TX pin	Serial ATA or SAS Channel 1 transmit differential pair.
SATA1_TX-	B17	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATAT Conn TX pin	Serial ATA OF SAS Channel 1 dansinit differential pair.
SATA1_RX+	B19	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA1 Conn RX pin	Serial ATA or SAS Channel 1 receive differential pair.
SATA1_RX-	B20	I SATA	AC coupled on Module	AC Coupling capacitor	CONNECT TO SATAT CONTINA PIN	Serial ATA 01 3A3 Channel 1 receive dimerchal pair.
SATA2_TX+	A22	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA2 Conn TX pin	Serial ATA or SAS Channel 2 transmit differential pair.
SATA2_TX-	A23	O SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATAZ Conn TX pin	Scharzer of Sec channel 2 dansmit directed pair.
SATA2_RX+	A25	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATA2 Conn RX pin	Serial ATA or SAS Channel 2 receive differential pair.
SATA2_RX-	A26	I SATA	AC coupled on Module	AC Coupling capacitor	Connect to SATAZ Conn to pin	Serial ATA 01 3A3 Channel 2 receive differential pair.
SATA3_TX+	B22	O SATA	AC coupled on Module	NA		Serial ATA or SAS Channel 3 transmit differential pair.
SATA3_TX-	B23	O SATA	AC coupled on Module	NA		Serial ATA 01 SAS Chariner 5 danishiik diliferendal pair.
SATA3_RX+	B25	I SATA	AC coupled on Module	NA		Serial ATA or SAS Channel 3 receive differential pair.
SATA3_RX-	B26	I SATA	AC coupled on Module	NA		Serial ATA OF SAS Chariller S receive differential pair.
ATA_ACT#	A28	I/O CMOS	3.3V / 3.3V	PU 10K to 3.3V	Connect to LED and recommend current limit resistor 220Ω to 3.3V	ATA (parallel and serial) or SAS activity indicator, active low.

Chapter 3

PCI Express Lanes Signals a	nd Descriptions	1				
Signal		Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
PCIE_TX0+	A68	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 0
PCIE_TX0-	A69 B68			AC Coupling capacitor		
PCIE_RX0+ PCIE_RX0-	B69	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF Slot - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 0
PCIE_TX1+	A64	O DOTE	AC accorded on Madula	AC Coupling capacitor		DCI Fireman Differential Transmit Dains 1
PCIE_TX1-	A65	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 1
PCIE_RX1+ PCIE_RX1-	B64 B65	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF Slot - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 1
PCIE_TX2+	A61			AC Coupling capacitor		
PCIE_TX2-	A62	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 2
PCIE_RX2+	B61	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 2
PCIE_RX2- PCIE_TX3+	B62 A58		· ·	AC Coupling capacitor	Slot - Connect to PCIE Conn pin	, , , , , , , , , , , , , , , , , , ,
PCIE TX3-	A59	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 3
PCIE_RX3+	B58	I PCIE	AC coupled off Module		Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 3
PCIE_RX3- PCIE_TX4+	B59 A55		· ·	AC Coupling capacitor	Slot - Connect to PCIE Conn pin	·
PCIE_TX4+	A56	O PCIE	AC coupled on Module	AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 4
PCIE_RX4+	B55	I PCIE	AC coupled off Module	J.,	Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 4
PCIE_RX4-	B56	11012	ne coupled on module	AC Counting and the	Slot - Connect to PCIE Conn pin	TO EXPLOSE STREETING RECEIVE FOILS T
PCIE_TX5+ PCIE_TX5-	A52 A53	O PCIE	AC coupled on Module	AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 5
PCIE_RX5+	B52	I PCIE	AC coupled off Module	ne coupling capacitor	Device - Connect AC Coupling cap 0.1uF	PCI Express Differential Receive Pairs 5
PCIE_RX5-	B53	1 LOTE	AC Coupled on Module		Slot - Connect to PCIE Conn pin	FCI Express Differential Receive Pails 3
PCIE_TX6+ PCIE_TX6-	D19 D20	O PCIE	AC coupled on Module	AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 6
PCIE_IX6- PCIE_RX6+	C19	I PCIE	AC assurated aff Mark 1	ме соприну сарасног	Device - Connect AC Coupling cap 0.1uF	DCI Common Differential Descript Point C
PCIE_RX6-	C20	I PCIE	AC coupled off Module		Slot - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 6
PCIE_TX7+ PCIE_TX7-	D22 D23	O PCIE	AC coupled on Module	AC Coupling capacitor AC Coupling capacitor	Connect to PCIE device or slot	PCI Express Differential Transmit Pairs 7
PCIE_TX7- PCIE RX7+	D23 C22		· ·	AC Coupling capacitor	Device - Connect AC Coupling cap 0.1uF	
PCIE_RX7-	C23	I PCIE	AC coupled off Module		Slot - Connect to PCIE Conn pin	PCI Express Differential Receive Pairs 7
PCIE0_CK_REF+	A88	O PCIE	PCIE		Connect to PCIE device, PCIe CLK Buffer or slot	Reference clock output for all PCI Express and PCI Express Graphics
PCIE0_CK_REF-	A89	OFCIL	rcit		Connect to PCIE device, PCIE CER Bullet of Slot	lanes.
DEC Signals and Description	15					
PEG Signals and Description Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
PEG TX0+	D52			NA		
						DCI Everage Graphics transmit differential pairs 0
PEG_TX0-	D53	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 0
PEG_TX0- PEG_RX0+	C52	I PCIE	AC coupled on Module AC coupled off Module	NA NA NA	<u>-</u>	PCI Express Graphics transmit differential pairs 0 PCI Express Graphics receive differential pairs 0
PEG_TX0-	C52 C53 D55	I PCIE	AC coupled off Module	NA NA NA		PCI Express Graphics receive differential pairs 0
PEG_TX0- PEG_RX0+ PEG_RX0- PEG_TX1+ PEG_TX1-	C52 C53 D55 D56		· ·	NA NA NA NA		· · · · · · · · · · · · · · · · · · ·
PEG_TX0- PEG_RX0+ PEG_RX0- PEG_TX1+ PEG_TX1- PEG_RX1+	C52 C53 D55 D56 C55	I PCIE	AC coupled off Module	NA NA NA NA NA		PCI Express Graphics receive differential pairs 0
PEG_TX0- PEG_RX0+ PEG_RX0- PEG_TX1+ PEG_TX1-	C52 C53 D55 D56	I PCIE O PCIE I PCIE	AC coupled off Module AC coupled on Module AC coupled off Module	NA NA NA NA		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1
PEG TX0- PEG_RX0+ PEG_RX0- PEG TX1- PEG_TX1- PEG_RX1- PEG_RX1- PEG_RX1- PEG_TX2- PEG_TX2-	C52 C53 D55 D56 C55 C56 D58	I PCIE O PCIE	AC coupled off Module AC coupled on Module	NA		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1
PEG TX0- PEG RX0+ PEG RX0- PEG TX1+ PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG TX2+ PEG TX2+ PEG TX2-	C52 C53 D55 D56 C55 C56 D58 D59 C58	I PCIE O PCIE I PCIE	AC coupled off Module AC coupled on Module AC coupled off Module	NA NA NA NA NA NA NA NA		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1
PEG TX0- PEG_RX0+ PEG_RX0- PEG RX1- PEG RX1- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX2- PEG_RX2- PEG_RX2- PEG_RX2-	C52 C53 D55 D56 C55 C55 C56 D58 D59 CS8	I PCIE O PCIE I PCIE O PCIE I PCIE	AC coupled off Module AC coupled on Module AC coupled off Module AC coupled on Module AC coupled off Module	NA N		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 2 PCI Express Graphics receive differential pairs 2
PEG TX0- PEG RX0+ PEG RX0- PEG TX1+ PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG TX2- PEG TX2- PEG TX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3-	C52 C53 D55 D56 C56 C56 C56 C58 C59 D61 D61	I PCIE O PCIE I PCIE O PCIE	AC coupled off Module AC coupled on Module AC coupled off Module AC coupled on Module	NA N		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 2
PEG TX0- PEG RX0+ PEG RX0- PEG TX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3- PEG TX3- PEG TX3- PEG TX3-	CS2 CS3 DS5 DS6 CS5 DS6 CS6 DS8 DS9 CS8 CS9 D61 D62 C661	I PCIE O PCIE I PCIE O PCIE I PCIE	AC coupled off Module AC coupled on Module AC coupled off Module AC coupled on Module AC coupled off Module	NA N		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 2 PCI Express Graphics receive differential pairs 2
PEG TX0- PEG RX0+ PEG RX0- PEG TX1+ PEG RX1- PEG RX1- PEG RX1- PEG TX2+ PEG TX2- PEG RX2- PEG RX3- PEG RX3-	C52 C53 D55 D56 C56 C56 C56 C58 C59 D61 D61	I PCIE O PCIE I PCIE O PCIE I PCIE I PCIE I PCIE	AC coupled off Module AC coupled on Module AC coupled off Module AC coupled on Module AC coupled off Module AC coupled on Module AC coupled off Module	NA N		PCI Express Graphics transmit differential pairs 1 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics receive differential pairs 3
PEG TX0- PEG RX0+ PEG RX0- PEG TX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3- PEG TX3- PEG TX3- PEG TX3-	C52 C53 D55 D56 C55 C56 C56 D58 D59 C58 C59 D61 D61 D62 C62	I PCIE O PCIE I PCIE O PCIE I PCIE O PCIE	AC coupled off Module AC coupled on Module AC coupled off Module AC coupled off Module AC coupled off Module AC coupled off Module	NA N		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics transmit differential pairs 3
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PEG TX0- PEG RX0+ PEG RX0- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3- PEG RX4- PEG RX4- PEG RX4- PEG RX4- PEG RX4-	CS2 CS3 DS5 DS6 DS6 CS6 DS8 DS9 CS8 CS9 D61 D62 C61 C62 C66 C66 C66 C66	I PCIE O PCIE I PCIE O PCIE I PCIE O PCIE I PCIE I PCIE I PCIE	AC coupled off Module AC coupled on Module AC coupled off Module AC coupled off Module	NA		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics transmit differential pairs 4 PCI Express Graphics receive differential pairs 4
PEG TX0- PEG_RX0+ PEG_RX0- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX2- PEG_RX2- PEG_RX2- PEG_RX2- PEG_RX3- PEG_RX3- PEG_RX3- PEG_RX3- PEG_RX3- PEG_RX3- PEG_RX4- PEG_RX5-	CS2 CS3 DS5 DS6 CS6 DS8 DS9 CS8 DS9 DS9 CS9 D61 D62 C61 C62 D65 D66 C66 C65	I PCIE O PCIE I PCIE O PCIE I PCIE I PCIE O PCIE I PCIE O PCIE	AC coupled off Module AC coupled on Module AC coupled off Module	NA N		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 3
PEG TX0- PEG RX0+ PEG RX0- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG TX2- PEG TX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3- PEG TX3- PEG RX3- PEG RX3- PEG RX3- PEG RX4- PEG RX5- PEG RX5- PEG RX5- PEG RX4- PEG RX5- PEG RX5-	CS2 CS3 CS5 CS6 CS6 CS6 CS9 CS9 CS9 CS9 CS6 CS9 CS6 CS6	I PCIE O PCIE I PCIE O PCIE I PCIE O PCIE I PCIE I PCIE O PCIE I PCIE O PCIE	AC coupled off Module AC coupled on Module AC coupled off Module	NA N		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 4 PCI Express Graphics receive differential pairs 4 PCI Express Graphics transmit differential pairs 5
PEG TX0- PEG RX0+ PEG RX0- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3- PEG RX4- PEG TX4- PEG RX4- PEG RX4- PEG RX4- PEG RX4- PEG RX5- PEG RX5- PEG RX5-	CS2 CS3 DS5 DS6 CS5 DS6 CS5 CS6 DS8 DS9 DS9 D61 D62 CS8 CS9 D61 D62 C61 C62 C66 C66 D66 D66 C65 C66 D69 C68 D69	I PCIE O PCIE I PCIE O PCIE I PCIE O PCIE I PCIE I PCIE O PCIE I PCIE I PCIE I PCIE	AC coupled off Module AC coupled on Module AC coupled off Module AC coupled off Module	NA		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics transmit differential pairs 4 PCI Express Graphics receive differential pairs 4
PEG TX0- PEG_RX0+ PEG_RX0+ PEG_RX0- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX1- PEG_RX2- PEG_RX2- PEG_RX2- PEG_RX2- PEG_RX3- PEG_RX3- PEG_RX3- PEG_RX3- PEG_RX3- PEG_RX4- PEG_RX5-	CS2 CS3 DS5 DS6 DS6 DS6 CS5 CS6 DS8 DS9 D61 D62 C61 D62 C66 C66 C66 D68 D68 D68 D68 D68 D68 D68 D68 D68 D	I PCIE O PCIE I PCIE O PCIE I PCIE O PCIE I PCIE I PCIE O PCIE I PCIE O PCIE	AC coupled off Module AC coupled on Module AC coupled off Module	NA N		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 4 PCI Express Graphics receive differential pairs 4 PCI Express Graphics transmit differential pairs 5
PEG TX0- PEG RX0+ PEG RX0- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3- PEG TX3- PEG TX3- PEG TX3- PEG TX4- PEG RX3- PEG TX4- PEG RX3- PEG TX5- PEG RX1- PEG RX5- PEG RX5- PEG RX5- PEG RX5- PEG RX6- PEG TX6-	CS2 CS3 DS5 DS6 DS6 CS5 CS6 DS8 DS9 CS9 D61 D62 C61 C62 C66 C66 D68 D68 D68 D69 D71 D72 C71	I PCIE O PCIE	AC coupled off Module AC coupled on Module AC coupled off Module	NA N		PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 4 PCI Express Graphics receive differential pairs 4 PCI Express Graphics transmit differential pairs 5 PCI Express Graphics receive differential pairs 5 PCI Express Graphics transmit differential pairs 6
PEG TX0- PEG RX0+ PEG RX0- PEG RX0- PEG TX1+ PEG RX1- PEG RX1- PEG RX1- PEG RX1- PEG TX2+ PEG TX2- PEG TX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3- PEG TX3- PEG RX4- PEG RX5- PEG TX5- PEG TX5- PEG TX5- PEG TX5- PEG TX5- PEG RX6- PEG RX5- PEG RX6- PEG RX6-	CS2 CS3 DS5 DS6 CS6 DS7 CS9 DS8 DS9 CS8 DS9 CS9 D61 CS9 D62 C61 C62 D65 D66 C66 C66 C66 C66 C68 C69 D71 D72 C71	I PCIE O PCIE I PCIE O PCIE I PCIE O PCIE I PCIE I PCIE O PCIE I PCIE I PCIE I PCIE	AC coupled off Module AC coupled on Module AC coupled off Module	NA N		PCI Express Graphics receive differential pairs 0 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 4 PCI Express Graphics receive differential pairs 4 PCI Express Graphics transmit differential pairs 5 PCI Express Graphics receive differential pairs 5
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PEG TX0- PEG RX0+ PEG RX0- PEG RX1- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3- PEG TX3- PEG RX3- PEG TX3- PEG TX3- PEG TX3- PEG TX3- PEG RX3- PEG TX4- PEG RX3- PEG TX5- PEG RX3- PEG TX6- PEG RX6- PEG RX7- PEG RX8-	CS2 CS3 CS5 CS6 CS5 CS6 CS5 CS6 CS6 CS6 CS7 CS8 CS9 CS9	I PCIE O PCIE I PCIE O PCIE I PCIE O PCIE I PCIE O PCIE I PCIE I PCIE O PCIE	AC coupled off Module AC coupled on Module AC coupled off Module AC coupled off Module AC coupled off Module AC coupled on Module AC coupled on Module AC coupled off Module	NA		PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics receive differential pairs 3 PCI Express Graphics receive differential pairs 3 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics transmit differential pairs 4 PCI Express Graphics receive differential pairs 4 PCI Express Graphics receive differential pairs 5 PCI Express Graphics transmit differential pairs 5 PCI Express Graphics receive differential pairs 6 PCI Express Graphics transmit differential pairs 6 PCI Express Graphics transmit differential pairs 7 PCI Express Graphics transmit differential pairs 7 PCI Express Graphics receive differential pairs 8
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PEG TX0- PEG RX0+ PEG RX0- PEG RX1- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX2- PEG RX3- PEG TX3- PEG TX3- PEG TX3- PEG TX3- PEG RX4- PEG RX5- PEG TX5- PEG RX5- PEG RX5- PEG RX6- PEG RX6- PEG RX6- PEG RX7- PEG RX8- PEG RX7- PEG RX8- PEG RX8- PEG RX7- PEG RX7- PEG RX7- PEG RX8- PEG RX8- PEG RX7- PEG RX7- PEG RX8-	CS2 CS3 CS5 CS6 CS5 CS6 CS5 CS6 CS6 CS6 CS6 CS7 CS8 CS9 CS9	I PCIE O PCIE I PCIE	AC coupled off Module AC coupled on Module AC coupled off Module	NA		PCI Express Graphics transmit differential pairs 1 PCI Express Graphics transmit differential pairs 1 PCI Express Graphics receive differential pairs 1 PCI Express Graphics transmit differential pairs 2 PCI Express Graphics receive differential pairs 2 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics transmit differential pairs 3 PCI Express Graphics transmit differential pairs 4 PCI Express Graphics receive differential pairs 4 PCI Express Graphics receive differential pairs 5 PCI Express Graphics transmit differential pairs 5 PCI Express Graphics transmit differential pairs 6 PCI Express Graphics receive differential pairs 6 PCI Express Graphics transmit differential pairs 7 PCI Express Graphics receive differential pairs 7 PCI Express Graphics receive differential pairs 8 PCI Express Graphics receive differential pairs 8 PCI Express Graphics receive differential pairs 8

PEG Signals and Descriptions						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
PEG_TX10+	D85		1	NA NA	Estation bound	T
PEG TX10-	D86	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 10
PEG_RX10+	C85	I DCIE	AC coupled off Mc dul-	NA NA		DCT Evanora Crambian receive differential pairs 10
PEG_RX10-	C86	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 10
PEG_TX11+	D88	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 11
PEG_TX11-	D89	OFCIL	no coupled on module	NA		i et express oraphics dansinicalitati pans 11
PEG_RX11+	C88	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 11
PEG_RX11-	C89			NA		. ac any sac anapone sector direction pure 11
PEG_TX12+	D91	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 12
PEG_TX12-	D92	 		NA NA		, ,
PEG_RX12+	C91	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 12
PEG_RX12- PEG_TX13+	C92 D94	†	-	NA NA		
PEG_TX13+ PEG_TX13-	D94 D95	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 13
PEG_IX13- PEG_RX13+	C94	†		NA NA		
PEG_RX13+	C95	I PCIE	AC coupled off Module	NA NA		PCI Express Graphics receive differential pairs 13
PEG_TX14+	D98	O DOTE	AC	NA NA		DCI Formus Complies Amount differential point 14
PEG_TX14-	D99	O PCIE	AC coupled on Module	NA NA		PCI Express Graphics transmit differential pairs 14
PEG_RX14+	C98	I PCIE	AC coupled off Modul-	NA		DCT Evarence Graphics receive differential pairs 14
PEG_RX14-	C99	1 PUE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 14
PEG_TX15+	D101	O PCIE	AC coupled on Module	NA		PCI Express Graphics transmit differential pairs 15
PEG_TX15-	D102	O I CIL	, to coupied on rioddle	NA		or Express scapilica duristiit differential palls 15
PEG_RX15+	C101	I PCIE	AC coupled off Module	NA		PCI Express Graphics receive differential pairs 15
PEG_RX15-	C102	L	p on module	NA		
PEG_LANE_RV#	D54	I CMOS	3.3V / 3.3V	PU 10K to 3.3V		PCI Express Graphics lane reversal input strap. Pull low on the Carrier
. EG_DARE_KV#	551	1 31103	3.34 / 3.34	10 101 10 3.34		board to reverse lane order.
EverosoCard Circula and De-	orintion -	-	-			
ExpressCard Signals and Des	Din#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
EXCD0 CPPE#	A49			PU 10k to 3.3V	Carriel DUdIU	
EXCD1 CPPE#	B48	I CMOS	3.3V /3.3V	PU 10k to 3.3V		PCI ExpressCard: PCI Express capable card request, active low, one per card
_				PU 10K TO 3.3V		Caru
EXCD0_PERST# EXCD1_PERST#	A48 B47	O CMOS	3.3V /3.3V			PCI ExpressCard: reset, active low, one per card
EVCD1_LEK91#	ודט	1	1	1		
DDI Signals and Descriptions	;					
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
DDI1_PAIR0+/SDVO1_RED+	D26	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 0 differential pairs/Serial Digital Video B red output differential pair
DDI1_PAIR0-/SDVO1_RED- DDI1_PAIR1+/SDVO1_GRN+	D27 D29	1			Connect AC Coupling Capacitors 0.1uF to Device Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR1+/3DVO1_GRN+ DDI1_PAIR1-/SDVO1_GRN-	D30	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1ulr to Device Connect AC Coupling Capacitors 0.1ulr to Device	DDI 1 Pair 1 differential pairs/Serial Digital Video B green output differential pair
DDI1_PAIR2+/SDVO1_BLU+	D32	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 2 differential pairs/Serial Digital Video B blue output differential pair
DDI1_PAIR2-/SDVO1_BLU-	D33	OFCIE	AC Coupled on Module		Connect AC Coupling Capacitors 0.1uF to Device	DD1 1 Faii 2 uniferentiai pairs/Seriai Digital Video D bide output uniferential pair
DDI1_PAIR3+/SDVO1_CK+	D36	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 1 Pair 3 differential pairs/Serial Digital Video B clock output differential pair.
DDI1_PAIR3-/SDVO1_CK- DDI1_PAIR4+/SDVO1_INT+	D37 C25			NA NA	Connect AC Coupling Capacitors 0.1uF to Device	
DDI1_PAIR4+/SDVO1_INT+ DDI1_PAIR4-/SDVO1_INT-	C26	I PCIE	AC coupled off Module	NA NA		Serial Digital Video B interrupt input differential pair.
DDI1_PAIR5+/SDVO1_TVCLKIN+	C29	I PCIE	AC coupled off Mad 1	NA NA		Social Digital Video TVOLIT cynchronization clock input differential pair
DDI1_PAIR5-/SDVO1_TVCLKIN-	C30	i raic	AC coupled off Module	NA		Serial Digital Video TVOUT synchronization clock input differential pair.
DDI1_PAIR6+/SDVO1_FLDSTALL+	C15	I PCIE	AC coupled off Module	NA		Serial Digital Video Field Stall input differential pair.
DDI1_PAIR6-/SDVO1_FLDSTALL-	C16			NA NA		
		I/O PCIE	AC coupled on Module	PD 100K to GND (S/W IC between Rpu/PCH)	Connect to DP AUX+	DP AUX+ function if DDI1_DDC_AUX_SEL is no connect
DDIA CTRICIK AUV. (CD.) C. CTRI C	DIE		,			=
DDI1_CTRLCLK_AUX+/SDVO1_CTRLCLK	D15	1/0 OD C140C		PU 4.7K to 3.3V, PD 100K to GND	Comment to UDM/DM 72C CTDI CIV	UDAT/DIG TOC CTDLCLY (CDTA, DDC, ALIV, CTL.); and hall be to
		I/O OD CMOS	3.3V / 3.3V	(S/W IC between Rpu/Rpd resistor)	Connect to HDMI/DVI 12C CTRECEK	HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high
	1	1	1	PU 100K to 3.3V		
		I/O PCIE	AC coupled on Module	(S/W IC between Rpu/PCH)	Connect to DP AUX-	DP AUX- function if DDI1_DDC_AUX_SEL is no connect
DDI1_CTRLCLK_AUX-/SDVO1_CTRLDATA	D16		1	PU 4.7K to 3.3V/PU 100K to 3.3V		
		I/O OD CMOS	3.3V / 3.3V	(S/W IC between 4.7K/100K	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high
	<u> </u>		<u></u>	resistor)	<u> </u>	= = 4
DDI1_HPD	C24	I CMOS	3.3V / 3.3V		PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
	ļ	100			- 2	
						Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX
DDI1_DDC_AUX_SEL	D34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel.
						Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort
DDI3 DATRO	D39	 			Connect: AC Coupling Connectors 0 1 uE to Dovice	
DDI2_PAIR0+ DDI2_PAIR0-	D39 D40	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 0 differential pairs
DDI2_PAIR0*	D40	o per			Connect AC Coupling Capacitors 0.1ur to Device	DDT 2 Do A. M. Wesselvel and a
DDI2_PAIR1-	D43	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 1 differential pairs
DDI2_PAIR2+	D46	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 2 differential pairs
DDI2_PAIR2-	D47	O I CIL	ne coupica on moutile		Connect AC Coupling Capacitors 0.1uF to Device	SSEET ON E-ONIGINATION POINS
DDI2_PAIR3+ DDI2_PAIR3-	D49 D50	O PCIE	AC coupled off Module		Connect AC Coupling Capacitors 0.1uF to Device	DDI 2 Pair 3 differential pairs
DDIZ_PAIK3-	טכע	 		PD 100K to GND	Connect AC Coupling Capacitors 0.1uF to Device	· · · · · · · · · · · · · · · · · · ·
	1	I/O PCIE	AC coupled on Module	(S/W IC between Rpu/PCH)	Connect to DP AUX+	DP AUX+ function if DDI2_DDC_AUX_SEL is no connect
DDI2_CTRLCLK_AUX+	C32			PU 4.7K to 3.3V, PD 100K to GND		
		I/O OD CMOS	3.3V / 3.3V	(S/W IC between Rpu/Rpd resistor)	Connect to HDMI/DVI I2C CTRLCLK	HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high
1	1		1 .			

DDI Signals and Descriptio						
ignal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
		I/O PCIE	AC coupled on Module	PU 100K to 3.3V (S/W IC between Rpu/PCH)	Connect to DP AUX-	DP AUX- function if DDI2_DDC_AUX_SEL is no connect
DI2_CTRLCLK_AUX-	C33	I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V/PU 100K to 3.3V (S/W IC between 4.7K/100K resistor)	Connect to HDMI/DVI I2C CTRLDATA	HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high
DI2 HPD	D44	I CMOS	3.3V / 3.3V	resistor)	PD 1M and Connect to device Hot Plug Detect	DDI Hot-Plug Detect
DDI2_DDC_AUX_SEL	C34	I CMOS	3.3V / 3.3V	PD 1M to GND	PU 100K to 3.3V for DDC(HDMI/DVI)	Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to jin 13 of the DisplayPort
DDI3 PAIRO+	C39			NA		
DI3_PAIR0-	C40	O PCIE	AC coupled off Module	NA NA		DDI 3 Pair 0 differential pairs
DI3 PAIR1+	C42			NA NA		
DI3 PAIR1-	C43	O PCIE	AC coupled off Module	NA		DDI 3 Pair 1 differential pairs
DDI3 PAIR2+	C46			NA NA		
DI3 PAIR2-	C47	O PCIE	AC coupled off Module	NA NA		DDI 3 Pair 2 differential pairs
DI3_PAIR3+	C49			NA NA		
DI3_PAIR3-	C50	O PCIE	AC coupled off Module	NA NA		DDI 3 Pair 3 differential pairs
-		I/O PCIE	AC coupled on Module	NA NA		DP AUX+ function if DDI3_DDC_AUX_SEL is no connect
DI3_CTRLCLK_AUX+	C36	I/O OD CMOS	3.3V / 3.3V	NA		HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high
DI3_CTRLCLK_AUX-	C37	I/O PCIE	AC coupled on Module	NA		DP AUX- function if DDI3_DDC_AUX_SEL is no connect
DDID_CTRECER_AUX-	٠	I/O OD CMOS	3.3V / 3.3V	NA		HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high
		1.5				
DI3_HPD	C44	I CMOS	3.3V / 3.3V	NA		DDI Hot-Plug Detect
DI3_DDC_AUX_SEL	C38	I CMOS	3.3V / 3.3V	NA		Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX DDI[n]_DDC_AUX_SEL shall be pulled to 3.3V on the Carrier with a 100K Ohm resistor to configure the DDI[n]_AUX pair as the DDC channel. Carrier DDI[n]_DDC_AUX_SEL should be connected to pin 13 of the DisplayPort
JSB Signals and Descriptio Ignal ISB0+	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board Connect 90	Description
ISB0-	A45	I/O USB	3.3V Suspend/3.3V		connector	USB differential pairs 0
JSB1+	B46		+	+		
	B45	I/O USB	3.3V Suspend/3.3V		Connect 90 @ @100MHz Common Choke in series and ESD suppressors to GND to USB connector	USB differential pairs 1
JSB1-			-			
JSB2+	A43	I/O USB	3.3V Suspend/3.3V		Connect 90	USB differential pairs 2
ISB2-	A42	,			connector	11 11 11 11 11 11 11 11 11 11 11 11 11
ISB3+	B43	I/O USB	3.3V Suspend/3.3V		Connect 90	USB differential pairs 3
ISB3-	B42	2,0 000	5.51 Suspendy 5.51		connector	obb american pane s
JSB4+	A40	I/O USB	3.3V Suspend/3.3V		Connect 90	USB differential pairs 4
SB4-	A39	1/0 035	3.54 Suspend/3.54		connector	oss anterental pars 1
SB5+	B40	I/O USB	2 21/ 6		Connect 90	USB differential pairs 5
SB5-	B39	1/U USB	3.3V Suspend/3.3V		connector	USB differential pairs 5
SB6+	A37	7/0 LISD	2 20 / 6 / 1/2 20 /		Connect 90	usp in the contract of the con
SB6-	A36	I/O USB	3.3V Suspend/3.3V		connector	USB differential pairs 6
JSB7+	B37				Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	
ISB7-	B36	I/O USB	3.3V Suspend/3.3V		connector	USB differential pairs 7
JSB_0_1_OC#	B44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3_DU	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
JSB_2_3_OC#	A44	I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3_DU	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
ISB_4_5_OC#	B38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3_DU	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.
JSB_6_7_OC#	A38	I CMOS	3.3V Suspend/3.3V	PU 10k to 3V3_DU	Connect to Overcurrent of USB Power Switch	USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board.

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connector

connector

connector

connector

Connect 90

@ 100MHz Common Choke in series and ESD suppressors to GND to USB

Connect 90 \,\text{\Omega} \,\text{\@100MHz Common Choke in series and ESD suppressors to GND to USB

Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB

Connect $90\,$ @ 100MHz Common Choke in series and ESD suppressors to GND to USB

Additional transmit signal differential pairs for the SuperSpeed USB data path.

Additional receive signal differential pairs for the SuperSpeed USB data path.

Additional transmit signal differential pairs for the SuperSpeed USB data path.

Additional receive signal differential pairs for the SuperSpeed USB data path.

Additional transmit signal differential pairs for the SuperSpeed USB data path.

AC Coupling capacitor

AC Coupling capacitor

AC Coupling capacitor
AC Coupling capacitor

AC Coupling capacitor
AC Coupling capacitor

USB_SSTX0+ USB_SSTX0-

USB_SSRX0+ USB_SSRX0-USB_SSTX1+

USB_SSTX1-

USB_SSRX1+ USB_SSRX1-

USB_SSTX2+ USB_SSTX2O PCIE

I PCIE

O PCIE

I PCIE

O PCIE

AC coupled on Module

AC coupled off Modul

AC coupled on Module

AC coupled off Modul

AC coupled on Module

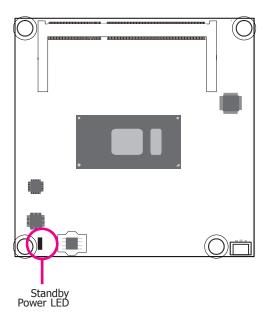
Chapter 3

USB Signals and Description	ic .					
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
USB_SSRX2+	C10	I PCIE	AC coupled off Modul		Connect 90 \(\Omega \) @100MHz Common Choke in series and ESD suppressors to GND to USB	Additional receive signal differential pairs for the SuperSpeed USB data path.
USB_SSRX2-	C9	I FCIL	AC Coupled on Modul		connector	Additional receive signal differential pairs for the Superspeed OSD data path.
USB_SSTX3+	D13	O PCIE	AC coupled on Module	AC Coupling capacitor	Connect 90	Additional transmit signal differential pairs for the SuperSpeed USB data path.
USB_SSTX3- USB_SSRX3+	D12 C13		,	AC Coupling capacitor	connector Connect 90 ♀ @100MHz Common Choke in series and ESD suppressors to GND to USB	
USB SSRX3-	C12	I PCIE	AC coupled off Modul		connector	Additional receive signal differential pairs for the SuperSpeed USB data path.
		•				•
LVDS Signals and Description		I	I			I =
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description Description
LVDS_A0+	A71	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential pairs Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-,
LVDS_A0-	A72				0 11 11/00	LVDS B CK+/-) shall have 100Ω terminations across the pairs at the destination. These
LVDS_A1+	A73	O LVDS	LVDS		Connect to LVDS connector	terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_A1-	A74					on-board
LVDS_A2+	A75	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A2-	A76					
LVDS_A3+	A78	O LVDS	LVDS		Connect to LVDS connector	
LVDS_A3-	A79					
LVDS_A_CK+	A81	O LVDS	LVDS		Connect to LVDS connector	LVDS Channel A differential clock
LVDS_A_CK-	A82 B71				Connect to LVDS connector	
LVDS_B0+ LVDS_B0-	B72	O LVDS	LVDS		Connect to LVDS connector	
LVDS B1+	B73	O LV/DC	IV/DC		Connect to LVDS connector	LVDS Channel B differential pairs
LVDS_B1-	B74	O LVDS	LVDS			Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/ LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These
LVDS_B2+	B75	O LVDS	LVDS		Connect to LVDS connector	terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer
LVDS_B2-	B76				Comment to 10/DC comments	on-board
LVDS_B3+ LVDS_B3-	B77 B78	O LVDS	LVDS		Connect to LVDS connector	
LVDS_B_CK+	B81	O LVDS	LVDS		Connect to LVDS connector	LVDC Channel D differential deals
LVDS_B_CK-	B82	O LVDS	LVDS			LVDS Channel B differential clock
LVDS_VDD_EN	A77	O CMOS	3.3V / 3.3V		Connect to enable control of LVDS panel power circuit	LVDS panel power enable
LVDS_BKLT_EN	B79	O CMOS	3.3V / 3.3V		Connect to enable control of LVDS panel backlight power circuit.	LVDS panel backlight enable
LVDS_BKLT_CTRL LVDS_I2C_CK	B83 A83	O CMOS I/O OD CMOS	3.3V / 3.3V 3.3V / 3.3V	PU 4.7K to 3.3V	Connect to brightness control of LVDS panel backlight power circuit. Connect to DDC clock of LVDS panel	LVDS panel backlight brightness control I2C clock output for LVDS display use
LVDS_I2C_DAT	A84	I/O OD CMOS	3.3V / 3.3V	PU 4.7K to 3.3V	Connect to DDC data of LVDS panel	IZC data line for LVDS display use
EVB0_1E0_B/11	prio i	170 00 01100	3.51 / 3.51	10 11/1 (0 5.5)	Connect to 550 data of 1755 panel	and the for the display dec
LPC Signals and Description						
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
LPC_AD0	B4 B5					
LPC_AD1 LPC_AD2	B6	I/O CMOS	3.3V / 3.3V		Connect to LPC device	LPC multiplexed address, command and data bus
LPC AD3	B7				Connect to bi e device	
LPC_FRAME#	B3	O CMOS	3.3V / 3.3V			LPC frame indicates the start of an LPC cycle
LPC_DRQ0#	B8	I CMOS	3.3V / 3.3V	PU 10K to 3.3V	NC .	LPC serial DMA request
LPC_DRQ1#	B9 A50	I/O CMOS	3.3V / 3.3V	PU 10K to 3.3V PU 10K to 3.3V	NC .	
LPC_SERIRQ LPC_CLK	B10	O CMOS	3.3V / 3.3V 3.3V / 3.3V	PU 10K to 3.3V	Connect to LPC device	LPC serial interrupt LPC clock output - 24MHz nominal
El C_CEN	1010	O CINOS	3.34 / 3.34			El C dock output 2 from a normalia
SPI Signals and Description	S					
Signal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
SPI_CS# SPI_MISO	B97 A92	O CMOS I CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V		Connect to Carrier Board SPI Device CS# pin Connect a series resistor 33 Ω to Carrier Board SPI Device SO pin	Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1 Data in to Module from Carrier SPI
SPI_MISO SPI_MOSI	A92 A95	O CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V		Connect a series resistor 33 Ω to Carrier Board SPI Device SO pin Connect a series resistor 33 Ω to Carrier Board SPI Device SI pin	Data out from Module to Carrier SPI
SPI_CLK	A94	O CMOS	3.3V Suspend/3.3V		Connect a series resistor 33 Ω to Carrier Board SPI Device SCK pin	Clock from Module to Carrier SPI
						Power supply for Carrier Board SPI – sourced from Module – nominally
CDI DOWED	401	0	2 2V Cuene - 4/2 2V			3.3V. The Module shall provide a minimum of 100mA on SPI_POWER.
SPI_POWER	A91	U	3.3V Suspend/3.3V			Carriers shall use less than 100mA of SPI_POWER. SPI_POWER
						shall only be used to power SPI devices on the Carrier
						Selection straps to determine the BIOS boot device.
						The Carrier should only float these or pull them low, please refer to
			1			COM Express Module Base Specification Revision 2.1 for strapping options of BIOS disable signals.
BIOS_DIS0#	A34					
BIOS_DISO#	A34					
BIOS_DISO#	A34					BIOS BIOS Chipset Chipset Carrier SPI Bios Ref
BIOS_DISO#	A34	-			_	DIS1# DIS0# SPI CS1# SPI CS0# SPI_CS# Descriptor Entry Line
BIOS_DISO#	A34	_			_	DIS1# DIS0# SPI CS1# SPI CS0# SPL CS# Descriptor Entry Line Destination
BIOS_DISO#	A34	I CMOS	NA .			DIS1# DIS0# SPI CS1# SPI CS0# SPI_CS# Descriptor Entry Line
BIOS_DISO#	A34	I CMOS	NA			DIS1# DIS0# SPI CS1# SPI CS0# SPL CS# Descriptor Entry Line Destination
BIOS_DISO#	A34	I CMOS	NA		_	DIS1# DIS0# SPI CS1# SPI CS0# SPI CS0# Descriptor Entry Line
BIOS_DIS0#	A34	I CMOS	NA			DIS1# DIS0# SPI CS1# Destination SPI CS0# SPI CS# Descriptor Entry Line
		I CMOS	NA			DIS1# DIS0# SPI CS1# SPI CS0# SPI_CS# Descriptor Entry Line
		I CMOS	NA			DIS1# DIS0# SPI CS1# SPI CS0# SPI CS0# Descriptor Entry Line
		I CMOS	NA			DIS1# DIS0# SPI CS1# SPI CS0# SPI_CS# Descriptor Entry Line
		I CMOS	NA			DIS1# DIS0# SPI CS1# SPI CS0# SPI_CS# Descriptor Entry Line
		I CMOS	NA			DIS1# DIS0# SPI CS1# SPI CS0# SPI_CS# Descriptor Entry Line

VGA Signals and Des		Modulo Din Ture	Dur Dail /Tolorans	CHOSE	Couries Reard	Description
gnal GA_RED	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968 PD 150 to GND	Carrier Board	Description Ped for monitor, Apples output
	B89 B91	O Analog	Analog		PD 150R,connect to VGA connector with EMI filter & ESD protect component.	Red for monitor. Analog output
GA_GRN GA_BLU	B92	O Analog O Analog	Analog Analog	PD 150 to GND PD 150 to GND	PD 150R,connect to VGA connector with EMI filter & ESD protect component. PD 150R,connect to VGA connector with EMI filter & ESD protect component.	Green for monitor. Analog output Blue for monitor. Analog output
GA HSYNC	B93	O CMOS	3.3V / 3.3V	FB 130 to GNB	Connect to VGA connector with a3.3V Buffer IC to isolate PCH & Display Device	Horizontal sync output to VGA monitor
GA VSYNC	B94	O CMOS	3.3V / 3.3V		Connect to VGA connector with a 33V Buffer IC to isolate PCH & Display Device	Vertical sync output to VGA monitor
GA_I2C_CK	B95	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	Connect to VGA connector with a 3.3V to 5V Level shift circuit.	DDC clock line (I2C port dedicated to identify VGA monitor capabilities)
GA I2C DAT	B96	I/O OD CMOS	3.3V / 3.3V	PU 2.2K to 3.3V	Connect to VGA connector with a 3.3V to 5V Level shift circuit.	DDC data line.
erial Interface Sign	als and Description	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
Ildi	PIII#			30908		General purpose serial port 0 transmitter
R0_TX	A98	O CMOS	5V / 12V		PD 4.7K to GND	(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC 12V)
R0_RX	A99	I CMOS	5V / 12V	PU 10K to 3.3V		General purpose serial port 0 receiver
					+	(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC 12V) General purpose serial port 1 transmitter
R1_TX	A101	O CMOS	5V / 12V		PD 4.7K to GND	(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC 12V)
R1_RX	A102	I CMOS	5V / 12V	PU 10K to 3.3V		General purpose serial port 1 receiver
	1					(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC 12V)
iscellaneous Signa	l and Descriptions					
nal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description
C_CK	B33	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		General purpose I2C port clock output
C_DAT	B34	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		General purpose I2C port data I/O line
						Output for audio enunciator - the "speaker" in PC-AT systems.
PKR	B32	O CMOS	3.3V / 3.3V			This port provides the PC beep signal and is mostly intended for
						debugging purposes.
DT	B27	O CMOS	3.3V / 3.3V			Output indicating that a watchdog time-out event has occurred.
AN DWMOUT	B101	O OD CMOS	2 21/ / 2 21/			Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM.
AN_PWNOUT	R101	O OD CMOS	3.3V / 3.3V			(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)
AN_TACHIN	B102	I OD CMOS	3.3V / 3.3V	PU 47K to 3V3		Fan tachometer input for a fan with a two pulse output.
	5102	1 00 0.103	3.54 / 3.54	10 171 10 343		(Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)
						Trusted Platform Module (TPM) Physical Presence pin. Active high.
PM_PP	A96	I CMOS	3.3V / 3.3V			TPM chip has an internal pull down. This signal is used to indicate
						Physical Presence to the TPM.
						Physical Presence to the TPM.
ower and System M	Management Signal	s and Descriptions	<u> </u>			
ower and System M	1anagement Signal	s and Descriptions Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Physical Presence to the TPM. Description
ower and System M	1anagement Signal	s and Descriptions Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	
gnal	Management Signals Pin# B12	s and Descriptions Module Pin Type I CMOS	Pwr Rail /Tolerance 3.3V Suspend/3.3V	SU968 PU 10K to 3V3_DU_EC	Carrier Board PU 4.7K to 3V3_SB	Description
gnal	Pin#	Module Pin Type	Pwr Rail / Tolerance			Description A falling edge creates a power button event. Power button events can
gnal	Pin#	Module Pin Type	Pwr Rail / Tolerance			Description A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down.
ignal WRBTN#	Pin# B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot.
ignal WRBTN#	Pin#	Module Pin Type	Pwr Rail / Tolerance			Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is
ignal WRBTN#	Pin# B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot.
Power and System Nignal WRBTN# SYS_RESET#	Pin# B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$YS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used.
ignal WRBTN#	Pin# B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by
gnal WRBTN# /S_RESET#	Pin# B12 B49	I CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$YS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$YS_RESET# input, a low
gnal VRBTN# /S_RESET#	Pin# B12	I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum
gnal WRBTN# YS_RESET#	Pin# B12 B49	I CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$YS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$YS_RESET# input, a low
gnal WRBTN# /S_RESET#	Pin# B12 B49	I CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$YS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$YS_RESET# ii input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software.
gnal WRBTN# YS_RESET# B_RESET#	B12 B49 B50	I CMOS I CMOS O CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the
gnal WRBTN# /S_RESET# B_RESET#	Pin# B12 B49	I CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PVR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to
yrbtn# S_reset# B_reset#	B12 B49 B50	I CMOS I CMOS O CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$YS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$YS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based PFAGs or other configurable devices time to be
vrbtn# s_reset# s_reset#	B12 B49 B50 B24	I CMOS I CMOS I CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed.
gnal WRBTN# /S_RESET# B_RESET# WR_OK	B12 B49 B50	I CMOS I CMOS O CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Indicates imminent suspend operation; used to notify LPC devices.
rretn# S_RESET# _RESET# /R_OK S_STAT#	B12 B49 B50 B24 B18	I CMOS I CMOS O CMOS I CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND PU 10K to 3V3	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$YS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$YS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Indicates imminent suspend operation; used to notify LPC devices. Indicates system is in Suspend to RAM state. Active low output. An
rretn# S_RESET# _RESET# /R_OK S_STAT#	B12 B49 B50 B24	I CMOS I CMOS I CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Indicates imminent suspend operation; used to notify LPC devices. Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to
reset# reset# reset# reset# reset# reset# reset# reset#	B12 B49 B50 B24 B18 A15	I CMOS I CMOS O CMOS O CMOS O CMOS	3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V 3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND PU 10K to 3V3	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PVR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based PPGAs or other configurable devices time to be programmed. Indicates imminent suspend operation; used to notify LPC devices. Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SIQS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply.
raal //RBTN# S_RESET# RESET# //R_OK S_STAT# S_S3# S_54#	B12 B49 B50 B24 B18 A15	I CMOS I CMOS O CMOS O CMOS O CMOS O CMOS O CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND PU 10K to 3V3 PD 100K to GND PD 100K to GND	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$7\$C, RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$7\$C, RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_53# on the Carrier Board may be used to enable the non-standby power on a typical ATN supply. Indicates system is in Suspend to Disk state. Active low output.
VRBTN# S_RESET# B_RESET# VR_OK IS_STAT# IS_S3# IS_S4# IS_S5#	B12 B49 B50 B24 B18 A15 A18 A24	I CMOS I CMOS I CMOS O CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND PU 10K to 3V3 PD 100K to GND PD 100K to GND PD 100K to GND PD 100K to GND	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGs or other configurable devices time to be programmed. Indicates imminent suspend operation; used to notify LPC devices. Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply. Indicates system is in Suspend to Disk state. Active low output. Indicates system is in Suspend to Disk state. Active low output.
gnal WRBTN# /S_RESET# B_RESET# WR_OK JS_STAT# JS_S3# JS_S4# JS_S5#	B12 B49 B50 B24 B18 A15	I CMOS I CMOS O CMOS O CMOS O CMOS O CMOS O CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND PU 10K to 3V3 PD 100K to GND PD 100K to GND	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$7\$C, RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$7\$C, RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_53# on the Carrier Board may be used to enable the non-standby power on a typical ATN supply. Indicates system is in Suspend to Disk state. Active low output.
WRBTN# YS_RESET# B_RESET# WR_OK US_STAT# US_S3# US_S4# US_S5# VAKEO#	B12 B49 B50 B24 B18 A15 A18 A24 B66	I CMOS I CMOS I CMOS O CMOS O CMOS O CMOS O CMOS O CMOS O CMOS I CMOS O CMOS I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND PU 10K to GND PD 100K to GND PD 100K to GND PD 100K to GND PD 100K to GND PU 1K to 3V3_DU	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$YS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$YS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Indicates imminent suspend operation; used to notify LPC devices. Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_53# on the Carrier Board may be used to enable the non-standby power on a typical ATN supply. Indicates system is in Suspend to Disk state. Active low output. Indicates system is in Suspend to Disk state. Active low output. Indicates system is in Suspend to Disk state. Active low output.
WRBTN# WYS_RESET# US_STAT# US_S3# US_S4# US_S5# VAKEO#	B12 B49 B50 B24 B18 A15 A18 A24	I CMOS I CMOS I CMOS O CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND PU 10K to 3V3 PD 100K to GND PD 100K to GND PD 100K to GND PD 100K to GND	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of 55 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Indicates imminent suspend operation; used to notify LPC devices. Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply. Indicates system is in Suspend to Disk state, Active low output. Indicates system is in Suspend to Disk state. Active low output.
wrbtn#	B12 B49 B50 B24 B18 A15 A18 A24 B66	I CMOS I CMOS I CMOS O CMOS O CMOS O CMOS O CMOS O CMOS O CMOS I CMOS O CMOS I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND PU 10K to GND PD 100K to GND PD 100K to GND PD 100K to GND PD 100K to GND PU 1K to 3V3_DU	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$YS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$YS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Indicates imminent suspend operation; used to notify LPC devices. Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_53# on the Carrier Board may be used to enable the non-standby power on a typical ATN supply. Indicates system is in Suspend to Disk state. Active low output. Indicates system is in Suspend to Disk state. Active low output. Indicates system is in Suspend to Disk state. Active low output.
gnal WRBTN# YS_RESET# B_RESET# WR_OK US_STAT# US_S3# US_S5# US_S5# US_S5#	B12 B49 B50 B24 B18 A15 A18 A24 B66	I CMOS I CMOS I CMOS O CMOS O CMOS O CMOS O CMOS O CMOS O CMOS I CMOS O CMOS I CMOS	3.3V Suspend/3.3V	PU 10K to 3V3_DU_EC PU 10K to 3V3_DU PD 100K to GND PU 10K to GND PD 100K to GND PD 100K to GND PD 100K to GND PD 100K to GND PU 1K to 3V3_DU	PU 4.7K to 3V3_SB	Description A falling edge creates a power button event. Power button events can be used to bring a system out of \$5 soft off and other suspend states, as well as powering the system down. Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when \$YS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low \$YS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. Indicates imminent suspend operation; used to notify LPC devices. Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_53# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply. Indicates system is in Suspend to Disk state. Active low output. Indicates system is in Suspend to Disk state. Active low output. Indicates system is in Suspend to Disk state. Active low output. Indicates system is in Suspend to Disk state. Active low output. Indicates system is in Suspend to Disk state. Active low output. General purpose wake up signal.

Power and System Ma		nd Descriptions	5						
nal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description			
D#	A103	I OD CMOS	3.3V Suspend/12V	PU 47K to 3V3_DU_EC		LID switch. Low active signal used by the ACPI operating system for a LID switch. (Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)			
EEP#	B103	I OD CMOS	3.3V Suspend/12V	PU 10K to 3V3_DU		Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. (Recommend add Protecting Logic Level Signals on Pins Reclaimed from VCC_12V)			
HRM#	B35	I CMOS	3.3V / 3.3V	PU 4.7K to 3V3		Input from off-Module temp sensor indicating an over-temp situation.			
HRMTRIP#	A35	O CMOS	3.3V / 3.3V	PU 10K to 3.3V		Active low output indicating that the CPU has entered thermal shutdown.			
MB CK	B13	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3 DU EC		System Management Bus bidirectional clock line.			
1B_DAT	B14	I/O OD CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus bidirectional data line.			
IB_DAT		1	3.3V Suspenu/3.3V	F0 2.2K t0 3V3_D0_EC					
4B_ALERT#	B15	I CMOS	3.3V Suspend/3.3V	PU 2.2K to 3V3_DU_EC		System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system.			
PIO Signals Descript	ions								
nal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description			
PO0	A93		rain / roicianice	55555	Corner Board				
PO1	B54	٦	L			General purpose output pins.			
iPO2	B57	O CMOS	3.3V / 3.3V			Upon a hardware reset, these outputs should be low.			
PO3	B63	1							
PIO	A54	1		PU 100K to 3.3V					
PI1	A63	╡		PU 100K to 3.3V		General purpose input pins.			
PI2	A67	I CMOS	I CMOS	I CMOS	I CMOS	3.3V / 3.3V	PU 100K to 3.3V		Pulled high internally on the Module.
PI3	A85	-		PU 100K to 3.3V PU 100K to 3.3V		ance man internally on the rioture.			
F13	A85	ı		PU 100K to 3.3V					
Power and GND Signa	l Descriptions								
ignal	Pin#	Module Pin Type	Pwr Rail /Tolerance	SU968	Carrier Board	Description			
igilai	A104~A109	Plodule Fill Type	FWI Rail / Tolerance	30900	Carrier Board	Description			
CC_12V	B104~B109 C104~C109 D104~D109	Power				Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used.			
CC_5V_SBY	B84~B87	Power				Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design.			
CC_RTC	A47	Power				Real-time clock circuit-power input. Nominally +3.0V.			
ind	A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21, B31, B41, B51, B60, B70, B80, B90, B100, B110, C1, C2, C5, C8, C11 C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C33, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110	Power				Ground - DC power and signal and AC signal return path. All available GND connector pins shall be used and tied to Carrier Board GND plane.			

Standby Power LED



This LED will be lit when the system is in standby mode.

Cooling Option

Heat Sink

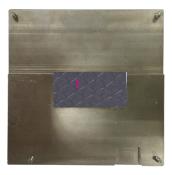


Note:

The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.



Top View of the Heat Sink



Bottom View of the Heat Sink

 \bullet "1" denotes the location of the thermal pad designed to contact the corresponding components that are on the SU968.



Important:

Remove the plastic covering from the thermal pads prior to mounting the heat sink onto the SU968.

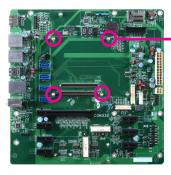
Installing SU968 onto a Carrier Board

Important:



The carrier board (COM332-B) and COM Express module used in this section are for reference purpose only and may not resemble you carrier board and the acutal SU968 module. These illustrations are mainly to guide you on how to install SU968 onto the carrier board of your choice.

1. Install the module and heat sink assembly onto the carrier board. The photo below shows the location of the mounting holes on the carrier board.



Mounting standoffs

2. Grasp SU968 by its edges and position it on top of the carrier board with the mounting holes of SU968 aligning with the standoffs on the carrier board. This will also align the COM Express connectors of the two boards to each other.



COM Express connectors on SU968



COM Express connectors on the carrier board

3. Press SU968 down firmly to seat it in the COM Express connectors of the carrier board.

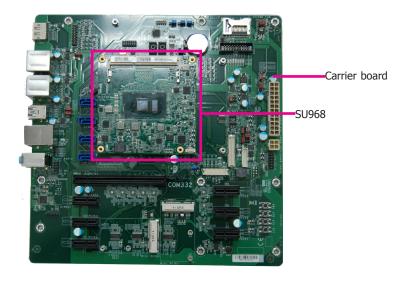


Note:

The illustration above shows the pressing points of the module onto the carrier board. Be careful when pressing the module to avoid damages to the connectors.

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4. Verify that SU968 is firmly seated in the COM Express connectors of the carrier board.



5. Install a heat sink onto the SU968 with the carrier board. The photo below shows the heat sink installed on SU968.



Installing the COM Express Debug Card

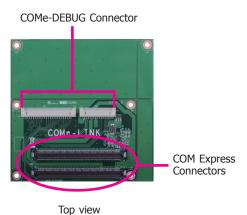


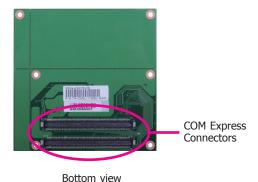
Note:

The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.

 COMe-LINK1 is the COM Express debug card designed for COM Express Compact modules to debug and display signals and codes of COM Express modules.

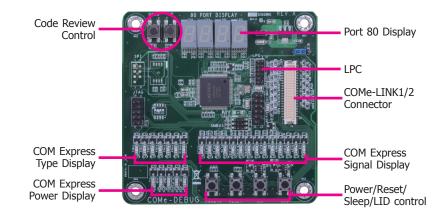
COMe-LINK1

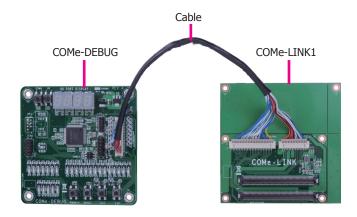




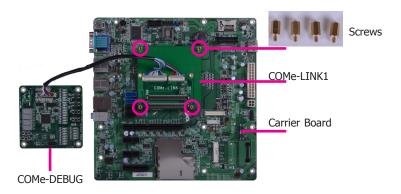
2. Connect the COMe-DEBUG card to COMe-LINK1 via a cable.

COMe-DEBUG

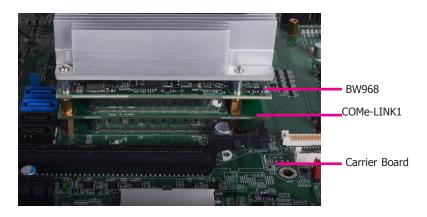




3. Use the provided screws to fix the COMe-LINK1 debug card onto the carrier board.



4. Then use the instructions from the previous section to install SU968 and heat sink on the top of the COMe-LINK1 debug card.



Side View of the Module, Debug Card and Carrier Board

Chapter 4 - BIOS Setup

Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.



Note:

The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.

The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message "Press DEL to run setup" will appear on the screen. If the message disappears before you respond, restart the system or press the "Reset" button. You may also restart the system by pressing the <Ctrl> <Alt> and keys simultaneously.

Legends

KEYs	Function
Right and Left Arrows	Moves the highlight left or right to select a menu.
Up and Down Arrows	Moves the highlight up or down between submenus or fields.
<esc></esc>	Exits to the BIOS setup utility
<f1></f1>	Displays general help
<f5 f6=""></f5>	Changes the highlighted value
<f9></f9>	Changes to the default setup
<f10></f10>	Saves and exits the setup program.
<enter></enter>	Press <enter> to enter the highlighted submenu</enter>

Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

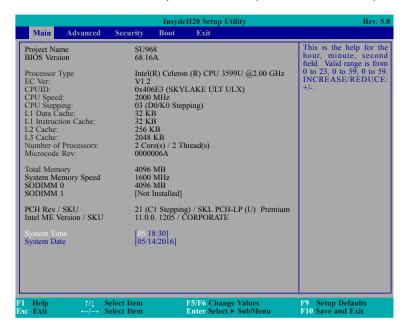
Submenu

When "▶" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

Insyde BIOS Setup Utility

Main

The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.



System Date

The date format is <month>, <date>, <year>. Month displays the month, from January to December. Date displays the date, from 1 to 31. Year displays the year, from 1980 to 2099.

System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

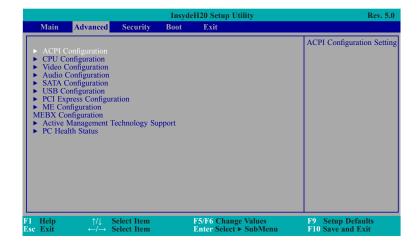
Advanced

The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.



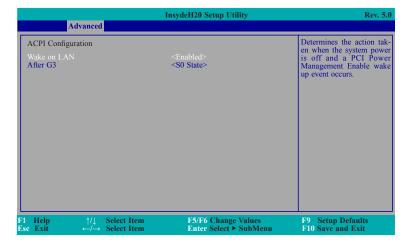
Important:

Setting incorrect field values may cause the system to malfunction.



ACPI Settings

This section configures the ACPI settings.



Wake on LAN

Set this field to enable the system to be waken up via the onboard LAN or via a LAN card that supports the remote wake up function.

State After G3

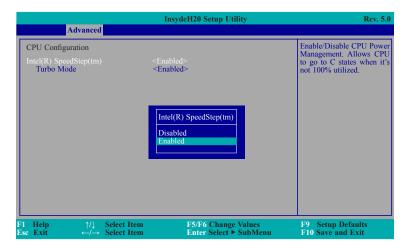
This field is to specify what state to go when power is re-applied after a power failure (G3 state).

SO State Power on the system when power is re-applied after AC power loss.

S5 State The system appears to be off when power is re-applied after AC power loss.

CPU Configuration

This section configures the CPU.



Intel® SpeedStep™

This field is used to enable or disable the Enhanced Intel SpeedStep® Technology, which helps optimize the balance between system's power consumption and performance.

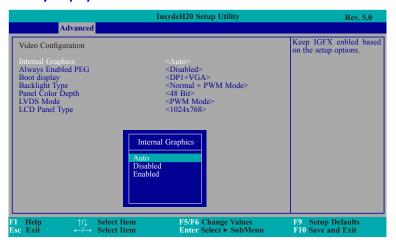
Turbo Mode

This field is used to enable or disable processor turbo mode (requires that EMTTM is enabled too), which allows the processor core to automatically run faster than the base frequency when the processor's power, temperature, and specification are within the limits of TDP.

Video Configuration

This section configures the video settings.

Primary Display



Internal Graphics

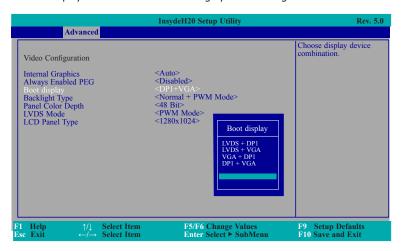
Keep IGFX enabled or disabled based on the setup options.

Always Enabled PEG

Enable or disable the PCIe graphics function.

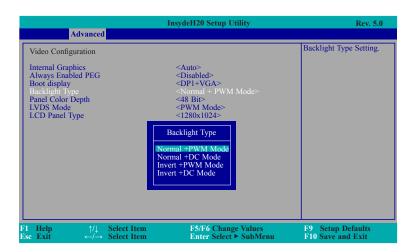
Boot display

Set the display device combination during system booting.



Backlight Type

Select the backlight type.



Panel Color Depth

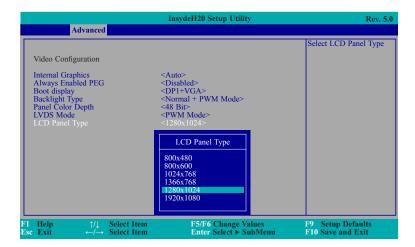
Select the LFP panel color depth: 18 bit, 24 bit, 36 bit, and 48 bit.

LVDS Mode

Select PTN3460 (eDP to LVDS bridge IC) LVDS Mode: PWM Mode and DC Mode

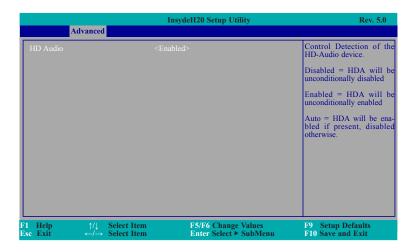
LCD Panel Type

Select the LCD panel type.



Audio Configuration

This section configures the audio settings.



HD Audio

Control the detection of the high-definition audio device.

Disabled

The high-definition audio will be unconditionally disabled.

Enabled

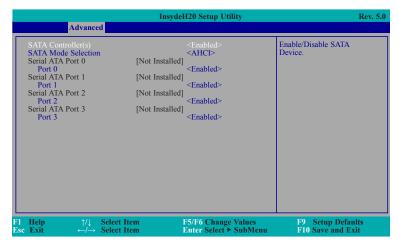
The high-definition audio will be unconditionally enabled.

Auto

The high-definition audio will be enabled if present and disabled otherwise.

SATA Configuration

This section configures the SATA controller.



SATA Controller(s)

This field is used to enable or disable Serial ATA devices.

SATA Mode Selection

The mode selection configures the SATA controller(s).

AHCI Mode

This option allows the Serial ATA devices to use AHCI (Advanced Host Controller Interface).

RAID Mode

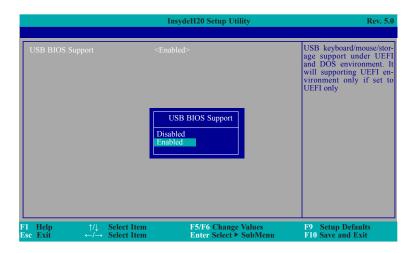
This option allows you to create RAID or Intel Matrix Storage configurations on Serial ATA devices.

Serial ATA Port 0, 1, 2, and 3

This field is used to enable or disable each serial ATA port.

USB Configuration

This section configures the parameters of the USB devices.



USB BIOS Support

Disabled

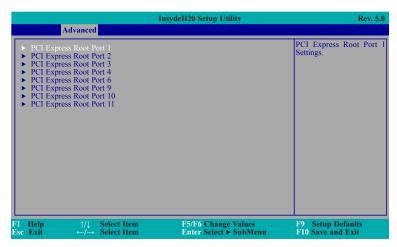
Disable the USB keyboard/mouse/storage support.

Enabled

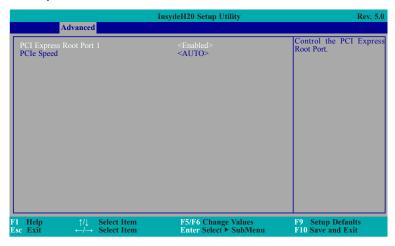
Enable the USB keyboard/mouse/storage support under UEFI and DOS environment.

PCI Express Configuration

This section configures settings of PCI Express root ports.



PCI Express Root Ports



PCI Express Root Port

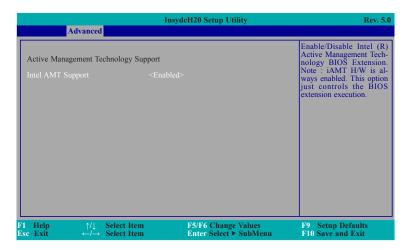
This field is used to enable or disable the PCI Express Root Port.

PCIe Speed

Select the speed of the PCI Express Root Port: Auto, Gen1, Gen2 or Gen3.

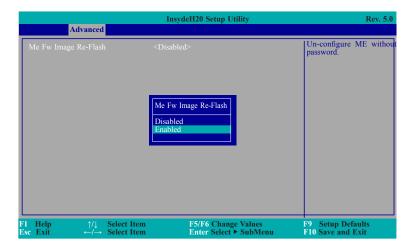
Active Management Technology Support

The section allows users to enable or disable the Intel® Active Management Technology (Intel® AMT) BIOS extension. Please refer to Chapter 7- Intel AMT Settings for more information.



ME Configuration

This section configures flashing of Intel® Active Management Engine region.

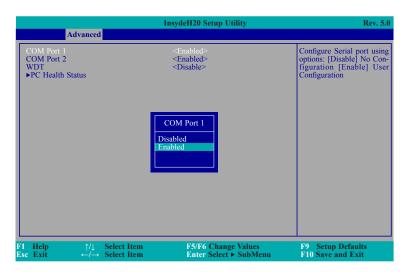


Me Fw Image Re-Flash

Enable or disable flashing of the Intel® ME region.

PC Health Status

This section configures the Embedded Controller (EC) settings.



COM Port 1 and COM Port 2

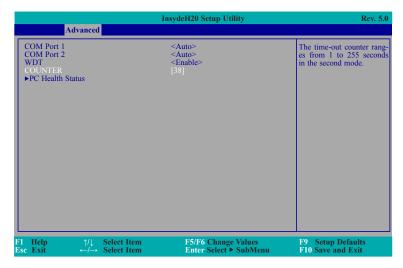
Configure the settings of the serial ports.

Disable Disable the serial port.

Enable Enable the serial port.

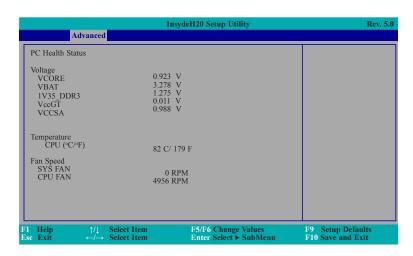
WDT

Enable or disable the watchdog function. A counter will appear if you select to enable WDT. Input any value between 1 to 255 seconds.



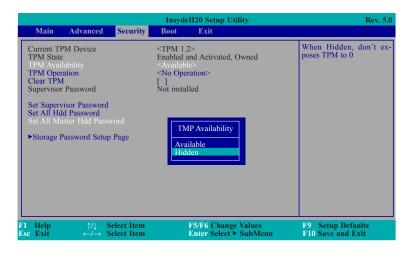
PC Health Status

This screen displays PC health information.



Security

This section configures the trusted platform module (TPM) and storage security.



TPM Availability

Show or hide the TPM availability and its configurations.

TPM Operation

Enable or disable the TPM function. It displays the following options:

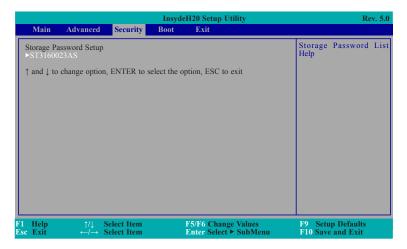
- No Operation: No changes to the current state.
- Disable: Disable and deactivate TPM.
- Enable: Enable and activate TPM.

Clear TPM

Remove all TPM ownership contents.

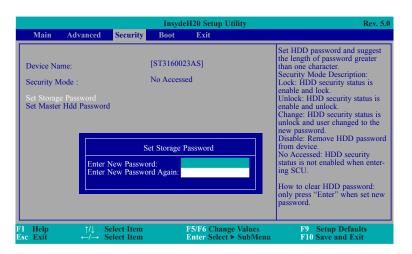
Storage Password Setup Page

Enhance the HDD security by using a password.



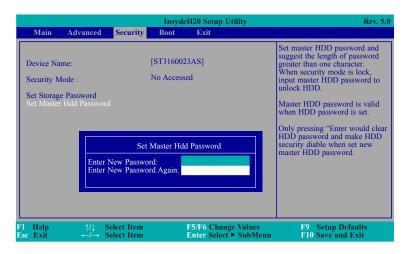
Set Storage Password

Set all HDD password. The length of the password must be greater than one character.



Set Master HDD Password

Set a password for the master HDD.

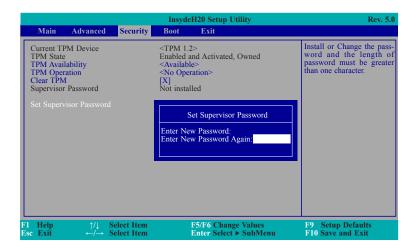


Set Master Hdd Password

Set master HDD password. The length of password must be greater than one character. When the security mode is set to Lock, input the master HDD password to unlock the HDD. Clear the HDD password by pressing "Enter" to set HDD security to be disabled and set a new master HDD password.

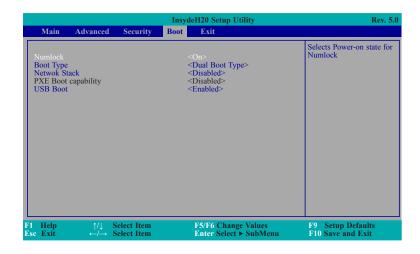
Set Supervisor Password

Set the administrative passwords. The length of the password must be greater than one character.



Boot

This section configures boot options.



Numlock

Select the power-on state for numlock.

Boot Type

Select the boot type. The options include Dual Boot Type, Legacy Boot Type, and UEFI Boot Type.

Network stack

Enable or disable UEFI network stack. It supports the operation of these functions or software: Windows 8 BitLocker Network Unlock, UEFI IPv4/IPv6 PXE and legacy PXE Option ROM.

USB Boot

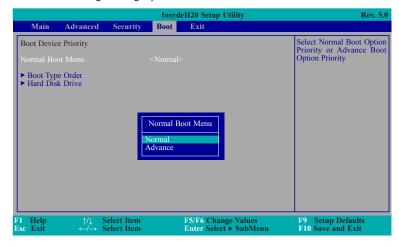
Enable or disable the booting to USB boot devices.

Note:

If the boot type is set to UEFI, the method for RAID volume creation will be different. Please refer to Chapter 6 – RAID for more information.

Legacy

This section configures legacy boot order.



Normal Boot Menu

Normal

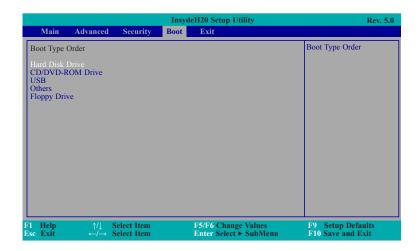
Select the boot menu type: normal or advanced.

For the advanced menu type: Use + and - keys to arrange the priority of the listed boot devices.

For normal menu type: Select the "Boot Type Order" or "Hard Disk Drive" category to view and arrange the order of the detected devices.

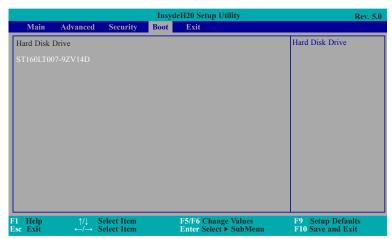
Boot Type Order

Use + and - keys to arrange the sequence of storage devices that the system's hardware will check in the operating system's boot files. The first device in the order list has the first boot priority.



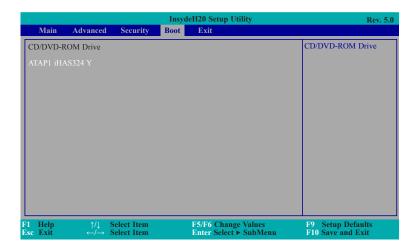
Hard Disk Drive

All installed hard disk drives will be displayed in this field. Use + and - keys to arrange the sequence of hard disk drives that the system's hardware will check in the operating system's boot files.



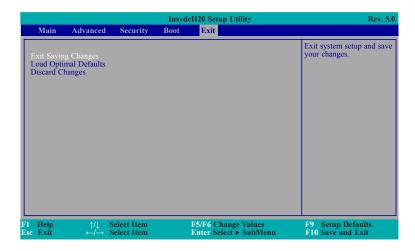
CD/DVD-ROM Drive

All installed CD/DVD-ROM drives will be displayed in this field. Use + and - keys to arrange the sequence of CD/DVD-ROM drives that the system's hardware checks for the operating system's boot files.



Exit

This section configures the parameters for exiting the BIOS menu.



Exit Saving Changes

Select this field and then press <Enter> to exit the BIOS setup and save your changes.

Load Optimal Defaults

Select this field and then press <Enter> to load optimal defaults.

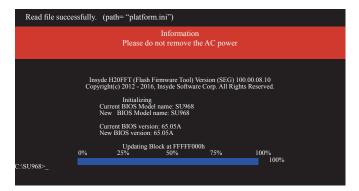
Discard Changes

Select this field and then press <Enter> to exit the BIOS setup without saving your changes.

Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files and specific instructions about how to update BIOS with the flash utility.

When you download the given BIOS file, you may find a BIOS flash utility attached with the BIOS file. This is the utility for performing BIOS updating procedure. For your convenience, we will also provide you with an auto-execution file in the BIOS file downloaded. This auto-execution file will bring you directly to the flash utility menu soon after system boots up and finishes running the boot files in your boot disk.



Notice: BIOS SPI ROM

- The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.
- 2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.
- 3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

意

Note:

- a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.
- b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not

Chapter 5 - Supported Software

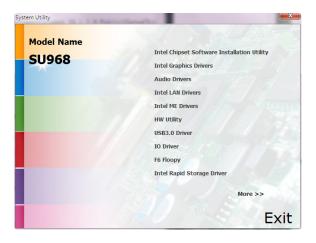
Install drivers, utilities and software applications that are required to facilitate and enhance the performance of the system board. You may acquire the software from your sales representatives, from an optional DVD included in the shipment, or from the website download page at https://www.dfi.com/DownloadCenter.

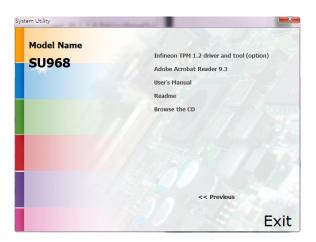
Auto Run Page (For Windows 10)





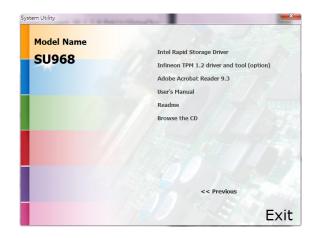
Auto Run Page (For Windows 8.1)





Auto Run Page (For Windows 7)







This step can be ignored if the applications are standalone files.

Intel Chipset Software Installation Utility

The Intel Chipset Software Installatn Utility is used for updating Windows® INF files so that the Intel chipset can be recognized and configured properly in the system.

To install the utility, click "Intel Chipset Software Installation Utility" on the main menu.

1. Setup is ready to install the utility. Click "Next".



2. Read the license agreement then click "Yes".



 Go through the readme document for more installation tips then click "Next".



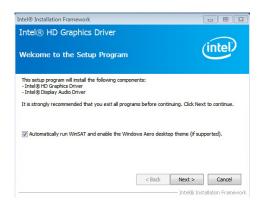
4. After completing installation, click "Finish" to exit setup.



Intel Graphics Drivers

To install the driver, click "Intel Graphics Drivers" on the main menu.

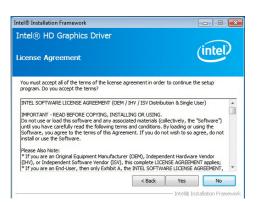
 Setup is now ready to install the graphics driver. Click "Next".



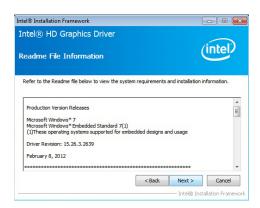
By default, the "Automatically run WinSAT and enable the Windows Aero desktop theme" is enabled. With this enabled, after installing the graphics driver and the system rebooted, the screen will turn blank for 1 to 2 minutes (while WinSAT is running) before the Windows 7/ Windows 8.1/ Windows 10 desktop appears. The "blank screen" period is the time Windows is testing the graphics performance.

We recommend that you skip this process by disabling this function then click "Next".

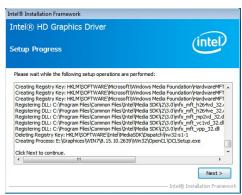
2. Read the license agreement then click "Yes".



3. Go through the readme document for system requirements and installation tips then click "Next".



4. Setup is now installing the driver. Click "Next" to continue.



5. Click "Yes, I want to restart this computer now" then click "Finish".

Restarting the system will allow the new software installation to take effect.



Audio Drivers (For COM332-B Carrier Board)

To install the driver, click "Audio Drivers (for COM332-B Carrier Board)" on the main menu.

- 1. Setup is now ready to install the audio driver. Click "Next".
- 2. Follow the remainder of the steps on the screen; clicking "Next" each time you finish a step.



3. Click "Yes, I want to restart my computer now" then click "Finish".

Restarting the system will allow the new software installation to take effect.



Intel LAN Drivers

To install the driver, click "Intel LAN Drivers" on the main menu.

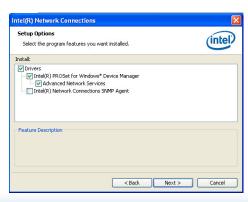
1. Setup is ready to install the driver. Click "Next".



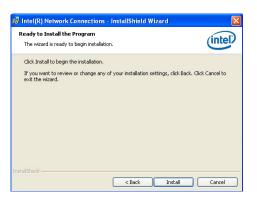
Click "I accept the terms in the license agreement" then click "Next".



Select the program featuers you want installed then click "Next".



4. Click "Install" to begin the installation.



5. After completing installation, click "Finish".



Kernel Mode Driver (For Windows 7 only)

To install the driver, click "Kernel Mode Driver Framework" on the main menu.

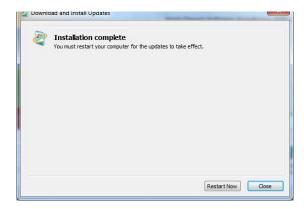
1. Click "Yes" to install the update.



2. The update is installed now.



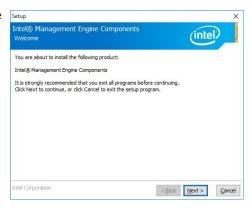
3. Click "Restart Now" to restart your computer when the installation is complete.



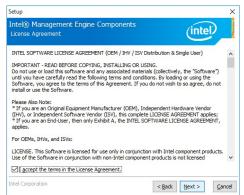
Intel Management Engine Drivers

To install the driver, click "Intel Management Engine Drivers" on the main menu.

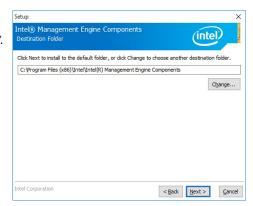
1. Setup is ready to install the Setup driver. Click "Next".



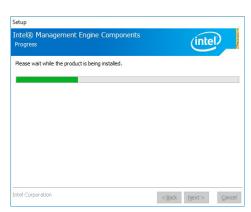
2. Read the license agreement | Setup then click "Next".



3. Setup is currently installing the driver. After installation has completed, click "Next".



4. Please wait while the product is being installed.



5. After completing installation, click "Finish".



HW Utility

HW Utility provides information about the board, Watchdog, and DIO. To access the utility, click "HW Utility" on the main menu.



Note:

If you are using Windows 7 or later versions, you need to access the operating system as an administrator to be able to install the utility.

1. Setup is ready to install the driver.



2. Click "Next" to continue.



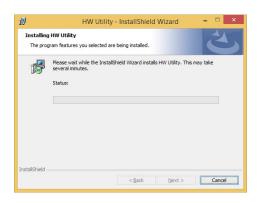
 Read the license agreement then click "I accept the terms in the license agreement". Click "Next".



4. The wizard is ready to begin installation. Click "Install".



5. Please wait while the program features are being installed.



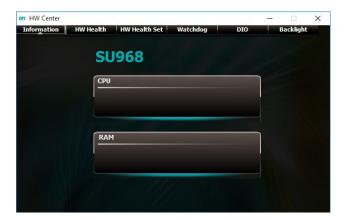
www.dfi.com

Chapter 5 Supported Software

6. After completing installation, click "Finish".



The HW Utility icon will appear on the desktop. Double-click the icon to open the utility.



事

Note:

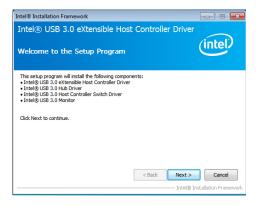
Note: The screenshot displayed above is for illustrative purpose only, and may not resemble the actual screen.

The SU968 HW Utility features the following tabs: Information, HW Health, HW Healthset, Watchdog, DIO and Backlight. Click on the tabs to access information about the board.

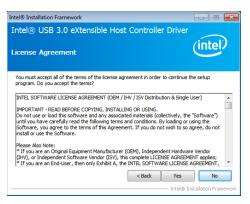
Intel USB 3.0 Drivers

To install the driver, click "Intel USB 3.0 Driver" on the main menu.

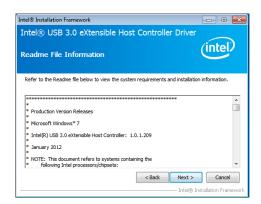
 Setup is ready to install the driver. Click "Next".



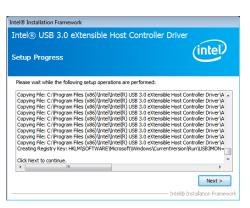
Read the license agreement then click "Yes".



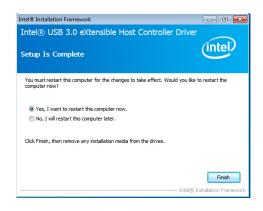
 Go through the readme document for more installation tips then click "Next".



 Setup is currently installing the driver. After installation has completed, click "Next".



5. After completing installation, click "Finish".



Microsoft Framework 4.5.2 (For Windows 7)

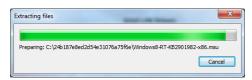


Note:

Before installing Microsoft Framework 4.5.2, make sure you have updated your Windows 7 operating system to Service Pack 1.

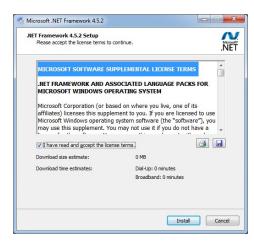
To install the driver, click "Microsoft Framework 4.5.2" on the main menu.

1. Setup is now extracting files.

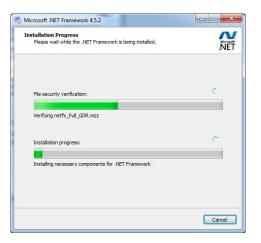


2. Read the license agreement carefully.

Click "I have read and accept the terms of the License Agree ment" then click "Install".



3. Setup is now installing the driver.



4. Click "Finish".



Intel Rapid Storage Technology

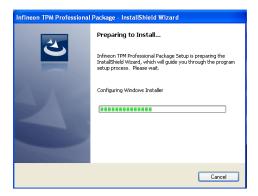
The Intel Rapid Storage Technology is a utility that allows you to monitor the current status of the SATA drives. It enables enhanced performance and power management for the storage subsystem.

To install the driver, click "Intel Rapid Storage Technology" on the main menu. Please refer to **Chapter 6** for more information.

Infineon TPM 1.2 Driver and Tool (Optional)

To install the driver, click "Infineon TPM driver and tool (option)" on the main menu.

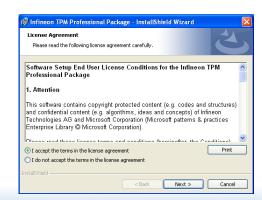
1. The setup program is preparing to install the driver.



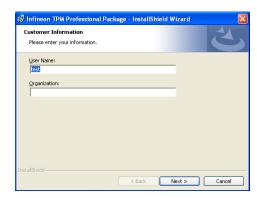
2. The setup program is now ready to install the utility. Click "Next".



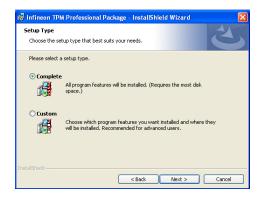
Click "I accept the terms in the license agreement" and then click "Next".



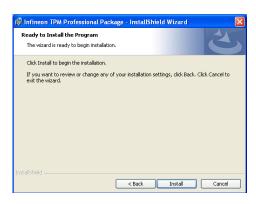
4. Enter the necessary information and then click "Next".



5. Select a setup type and then click "Next".



6. Click "Install".



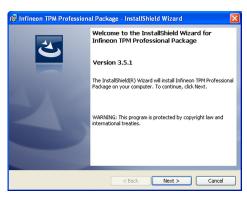
7. TPM requires installing the Microsoft Visual C++ package prior to installing the utility. Click "Install".



8. The setup program is currently installing the Microsoft Visual C++ package.

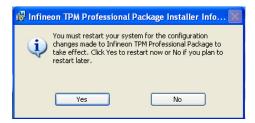


9. Click "Finish".



10. Click "Yes" to restart your system.

Chapter 5 Supported Software



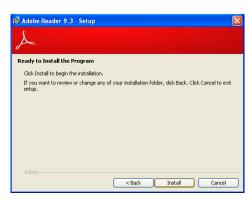
Adobe Acrobat Reader 9.3

To install the reader, click "Adobe Acrobat Reader 9.3" on the main menu.

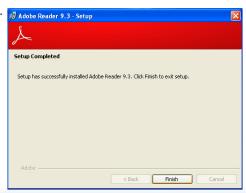
 Click Next to install or click Change Destination Folder to select another folder.



2. Click "Install" to begin installation.



3. Click "Finish" to exit installation.



Chapter 6 - RAID

The system board allows configuring RAID on Serial ATA drives. It supports RAID 0, RAID 1, RAID 5 and RAID 10.

RAID Levels

RAID 0 (Striped Disk Array without Fault Tolerance)

RAID 0 uses two new identical hard disk drives to read and write data in parallel, interleaved stacks. Data is divided into stripes and each stripe is written alternately between two disk drives. This improves the I/O performance of the drives at different channel; however it is not fault tolerant. A failed disk will result in data loss in the disk array.

RAID 1 (Mirroring Disk Array with Fault Tolerance)

RAID 1 copies and maintains an identical image of the data from one drive to the other drive. If a drive fails to function, the disk array management software directs all applications to the other drive since it contains a complete copy of the drive's data. This enhances data protection and increases fault tolerance to the entire system. Use two new drives or an existing drive and a new drive but the size of the new drive must be the same or larger than the existing drive.

RAID 5

RAID 5 stripes data and parity information across hard drives. It is fault tolerant and provides better hard drive performance and more storage capacity.

RAID 10 (Mirroring and Striping)

RAID 10 is a combination of data striping and data mirroring providing the benefits of both RAID 0 and RAID 1. Use four new drives or an existing drive and three new drives for this configuration.

RAID Level	Min. Drives	Protection	Description
RAID 0	2	None	Data striping without redundancy
RAID 1	2	Single Drive Failure	Disk mirroring
RAID 5	3	Single Drive Failure	Block-level data striping with distributed parity
RAID 10	4	1 Disk Per Mirrored Stripe (not same mirror)	Combination of RAID 0 (data striping) and RAID 1 (mirroring)

Settings

To enable the RAID function, the following settings are required.

- 1. Connect the Serial ATA drives.
- 2. Enable Serial ATA in the Insyde BIOS.
- 3. Create a RAID volume.
- 4. Install the Intel Rapid Storage Technology Utility.

Step 1: Connect the Serial ATA Drives

Refer to Chapter 2 for details on connecting the Serial ATA drives.



Important:

- 1. Make sure you have installed the Serial ATA drives and connected the data cables otherwise you won't be able to enter the RAID BIOS utility.
- Treat the cables with extreme caution especially while creating RAID. A damaged cable will ruin the entire installation process and operating system. The system will not boot and you will lost all data in the hard drives. Please give special attention to this warning because there is no way of recovering back the data.

Step 2: Enable RAID in the Insyde BIOS

- 1. Power-on the system then press to enter the main menu of the Insyde BIOS.
- 2. Go to "Advanced" menu, and select the "SATA Configuration" menu.
- 3. Change the "SATA Mode Selection" to "RAID" mode.
- 4. Save the changes in the "Save & Exit" menu.
- Reboot the system.

Chapter 6 RAID www.dfi.com

Step 3: Create a RAID Volume

- 1. When the Intel® RST option ROM status screen displays during POST, press <Ctrl> and <I> simultaneously to enter the option ROM user interface.
- 2. Select 1: Create RAID Volume and press <Enter>.
- 3. Use the up or down arrow keys to select the RAID level and press <Enter>.
- 4. Use the up or down arrow keys to select the strip size and press <Enter>.
- 5. Press <Enter> to select the physical disks.
- Use the up or down arrow keys to scroll through the list of hard drives and press <Space> to select the drive.
- 7. Press <Enter>.
- 8. Select the volume size and press <Enter>. You must select less than one hundred percent of the available volume space to leave space for the second volume.
- 9. Press <Enter> to create the volume.
- 10. At the prompt, press <Y> to confirm volume creation.
- 11. Select 4: Exit and press <Enter>.
- 12. Press <Y> to confirm exit.



Note

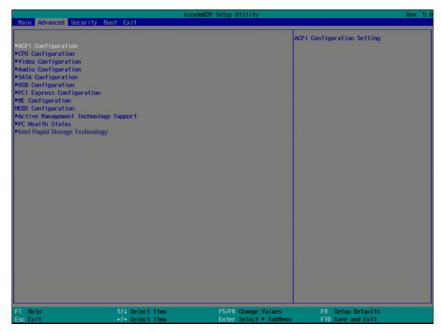
Chapter 6 RAID

These steps are cited from the Intel® Suppot site, "Set Up a System with Intel® Matrix RAID Technology" (Article ID: 000005789). http://www.intel.com/content/www/us/en/support/boards-and-kits/000005789.htm

Step 3-1: Create a RAID Volume if the boot type is UEFI

If the boot type is set to UEFI, RAID volume creation will be different. Please use the following steps to create RAID volumes. To set the boot type, enter the Insyde BIOS and go to "Boot" > "Boot type".

- 1. Go to the "Advanced" menu of the Insyde BIOS.
- 2. The "Intel® Rapid Storage Technology" menu appears. Enter this menu.



- 3. The screen displays all available drives. Select "Create RAID volume" to create a RAID volume".
- 4. Use the up or down arrow keys to select the RAID level and press <Enter>.
- Use the up or down arrow keys to scroll through the list of hard drives and press <Space> to select the drive.
- 6. Press <Enter>.

- 7. Use the up or down arrow keys to select the strip size and press <Enter>.
- 8. Enter the volume size and press <Enter>.
- 9. At the prompt, press <Y> to confirm volume creation.

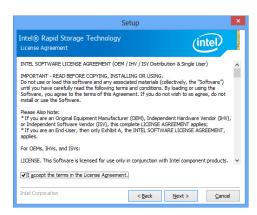
Step 4: Install the Intel Rapid Storage Technology Utility

The Intel Rapid Storage Technology Utility can be installed from within Windows. It allows RAID volume management (create, delete, migrate) from within the operating system. It will also display useful SATA device and RAID volume information. The user interface, tray icon service and monitor service allow you to monitor the current status of the RAID volume and/ or SATA drives. It enables enhanced performance and power management for the storage subsystem.

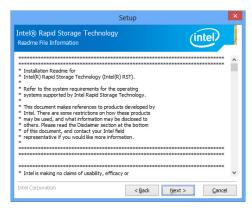
- 1. Insert the provided DVD into an optical drive.
- 2. Click "Intel Rapid Storage Technology Utility" on the main menu.
- 3. Setup is ready to install the utility. Click "Next".



 Read the license agreement and click "I accept the terms in the License Agreement." Then, click "Next".



 Go through the readme document to view system requirements and installation information then click "Next".



 Click "Next" to install to the default folder or click change to choose another destination folder.



7. Confirm the installation and click "Next".



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8. Click "Yes, I want to restart this computer now" to complete the installation and then click "Finish".



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Chapter 7 - Intel AMT Settings

Overview

Intel Active Management Technology (Intel® AMT) combines hardware and software solution to provide maximum system defense and protection to networked systems.

The hardware and software information are stored in non-volatile memory. With its built-in manageability and latest security applications, Intel® AMT provides the following functions.

Discover

Allows remote access and management of networked systems even while PCs are powered off; significantly reducing desk-side visits.

Repair

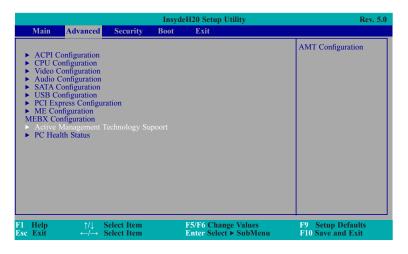
Remotely repair systems after OS failures. Alerting and event logging help detect problems quickly to reduce downtime.

Protect

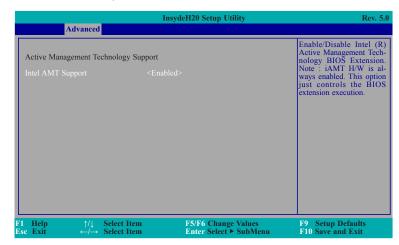
Intel AMT's System Defense capability remotely updates all systems with the latest security software. It protects the network from threats at the source by proactively blocking incoming threats, reactively containing infected clients before they impact the network, and proactively alerting when critical software agents are removed.

Enable Intel® AMT in the Insyde BIOS

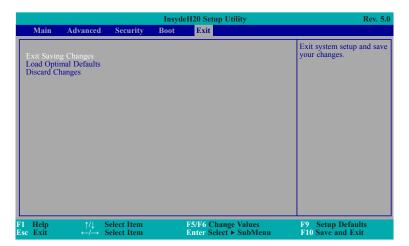
- 1. Power-on the system then press to enter the main menu of the Insyde BIOS.
- 2. In the **Advanced** menu, select **AMT Configuration**.



3. In the **Advanced** menu, select **Enable** in the **AMT** field.

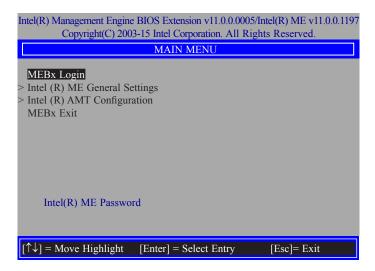


4. In the Save & Exit menu, select Save Changes and Reset then select OK.



Enable Intel® AMT in the Intel® Management Engine BIOS Extension (MEBX) Screen

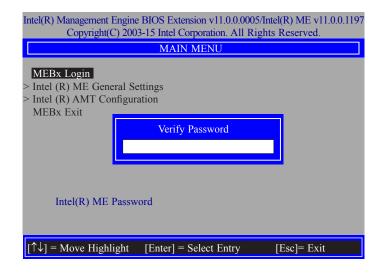
 When the system reboots, you will be prompted for a password. The default password is "admin". Enter the default password in the space provided under Intel(R) ME Password then press Enter.



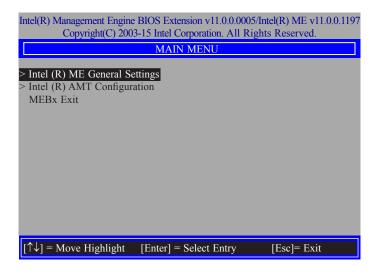
- 2. Enter a new password in the space provided under Intel(R) ME New Password then press Enter. The password must include:
 - 8-32 characters
 - Strong 7-bit ASCII characters excluding:, and " characters
 - At least one digit character (0, 1, ...9)
 - At least one 7-bit ASCII non alpha-numeric character, above 0x20, (e.g. !, \$, ;)
 - Both lower case and upper case characters



You will be asked to verify the password. Enter the same new password in the space provided under Verify Password then press Enter.



4. Select Intel(R) ME General Settings then press Enter.



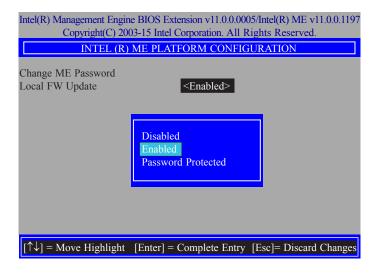
5. Select **Change Intel(R) ME Password** then press Enter.

You will be prompted for a password. The default password is "admin". Enter the default password in the space provided under Intel(R) ME New Password then press Enter.

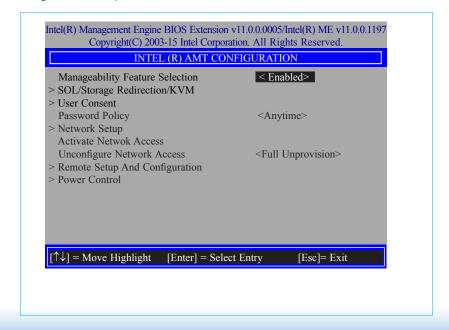
- 8-32 characters
- Strong 7-bit ASCII characters excluding:, and " characters
- At least one digit character (0, 1, ...9)
- At least one 7-bit ASCII non alpha-numeric character, above 0x20, (e.g. !, \$, ;)
- Both lower case and upper case characters



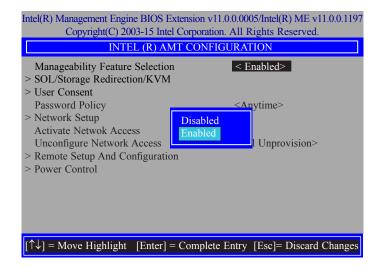
6. Select **Local FW Update** then press Enter. Select **Enabled** then press Enter.



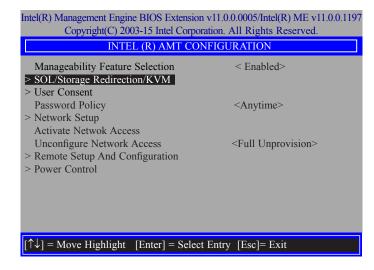
Select Previous Menu until you return to the Main Menu. Select Intel(R) AMT Configuration then press Enter.



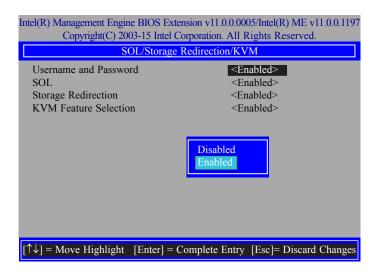
 In the Intel(R) AMT Configuration menu, select Manageability Feature Selection then press Enter. Select Enabled or Disabled then press Enter.



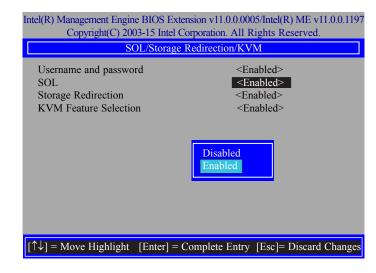
 In the Intel(R) AMT Configuration menu, select SOL/Storage Redirection/KVM then press Enter.



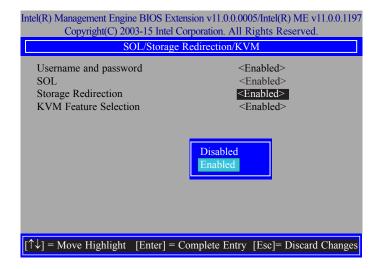
 In the SOL/Storage Redirection/KVM menu, select Username and Password then press Enter. Select Enabled or Disabled then press Enter.



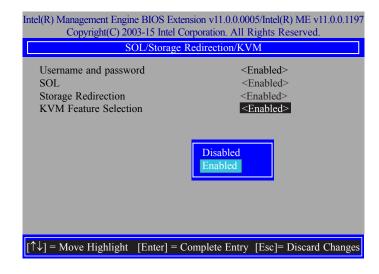
 In the SOL/Storage Redirection/KVM menu, select SOL then press Enter. Select Enabled or Disabled then press Enter.



12. In the **SOL/Storage Redirection/KVM** menu, select **Storage Redirection** then press Enter. Select **Enabled** or **Disabled** then press Enter.



 In the SOL/Storage Redirection/KVM menu, select KVM Feature Selection then press Enter. Select Enabled or Disabled then press Enter.



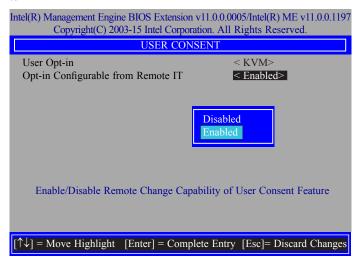
14. Select Previous Menu until you return to the **Intel(R) AMT Configuration** menu. Select **User Consent** then press Enter.



 In the User Consent menu, select User Opt-in then press Enter. Select None or KVM or ALL then press Enter.

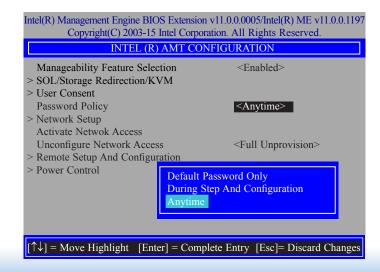


16. In the User Consent menu, select Opt-in Configurable from Remote IT then press Enter. Select Enabled or Disable Remote Control of KVM Opt-in Policy then press Enter.

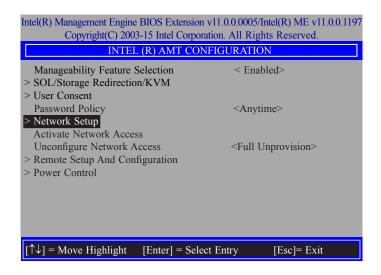


 Select Previous Menu until you return to the Intel(R) AMT Configuration menu. Select Password Policy then press Enter.

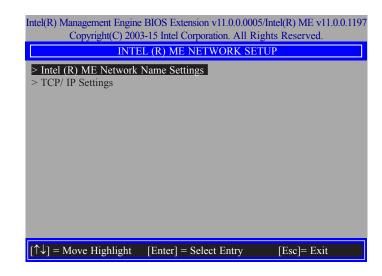
You may choose to use a password only during setup and configuration or to use a password anytime the system is being accessed.



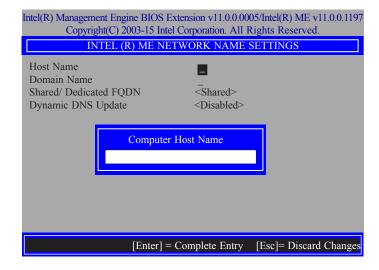
18. In the Intel(R) AMT Configuration menu, select Network Setup then press Enter.



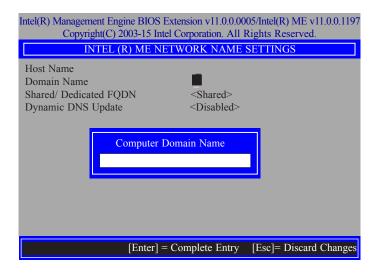
In the Intel(R) ME Network Setup menu, select Intel(R) ME Network Name Settings then press Enter.



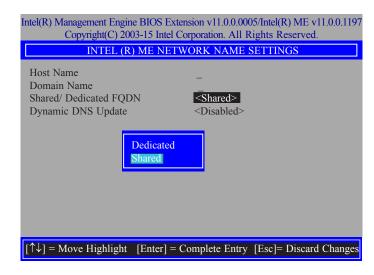
20. In the **Intel(R) ME Network Name Settings** menu, select **Host Name** then press Enter. Enter the computer's host name then press Enter.



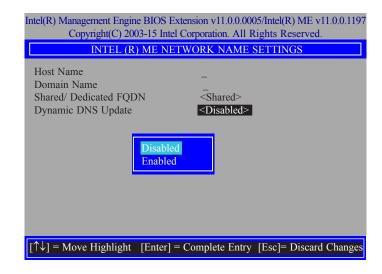
21. Select **Domain Name** then press Enter. Enter the computer's domain name then press Enter.



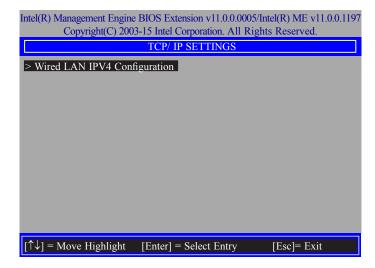
 Select Shared/Dedicated FQDN then press Enter. Select Shared or Dedicated then press Enter.



23. Select **Dynamic DNS Update** then press Enter. Select **Enabled** or **Disabled** then press Enter.



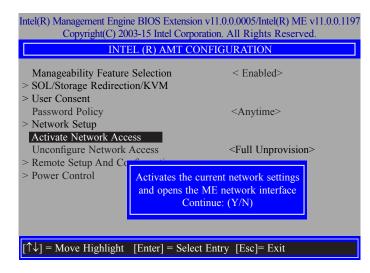
24. Select Previous Menu until you return to the **Intel(R) ME Network Setup** menu. Select **TCP/IP Settings** then press Enter.



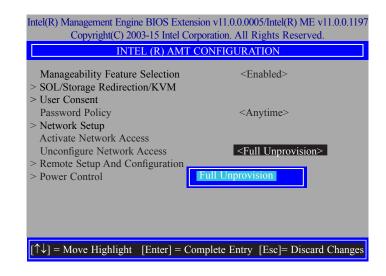
25. In the **TCP/IP Settings** menu, select **Wired LAN IPV4 Configuration** then press Enter. Select **Enabled** or **Disable IPV4 DHCP Mode** then press Enter.



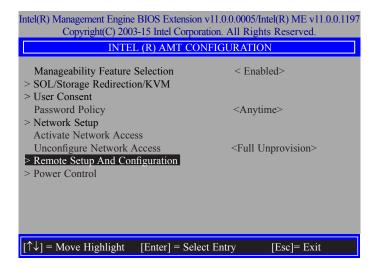
26. In the Intel(R) AMT Configuration menu, select Activate Network Access then press Enter. Press Y then press Enter.



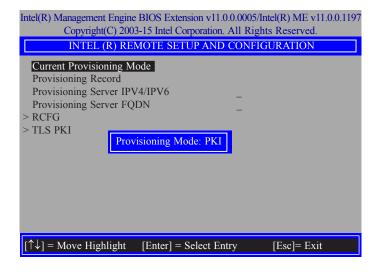
 In the Intel(R) AMT Configuration menu, select Unconfigure Network Access then press Enter.



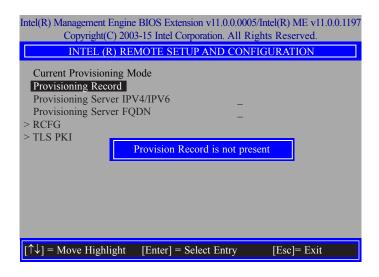
28. In the Intel(R) AMT Configuration menu, select Remote Setup And Configuration then press Enter.



 In the Intel(R) Remote Setup And Configuration menu, select Current Provisioing Mode then press Enter.



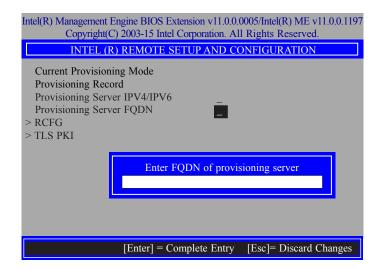
In the Intel(R) Remote Setup And Configuration menu, select Provisioning Record then press Enter.



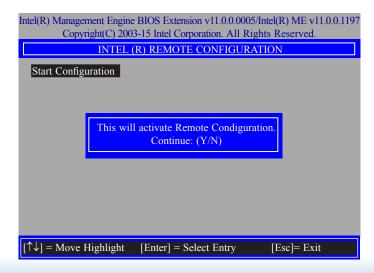
31. In the Intel(R) Remote Setup And Configuration menu, select Provisioning server IPV4/IPV6, enter the Provisioning server address then press Enter.



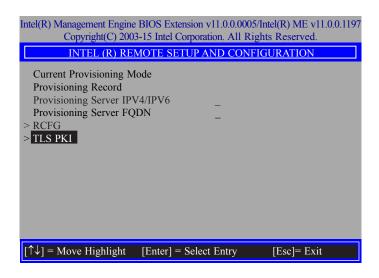
32. In the Intel(R) Remote Setup And Configuration menu, select Provisioning server FQDN, enter the FQDN of Provisioning server then press Enter.



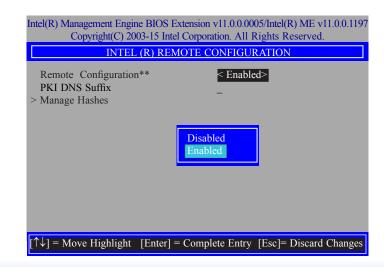
33. In the **Intel(R) Remote Setup And Configuration** menu, select **RCFG** then press Enter, and select **Start Configuration** then press enter. Type **Y** then press enter.



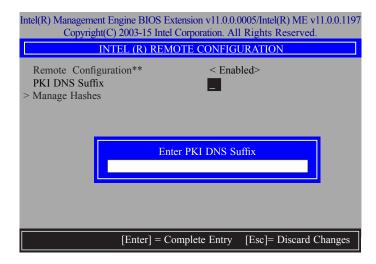
 In the Intel(R) Remote Setup And Configuration menu, select TLS PKI then press Enter.



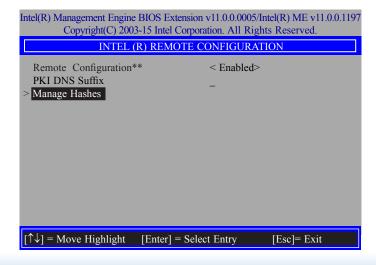
35. In the Intel(R) Remote Configuration menu, select Remote Configuration** then press Enter, select Enabled or Disabled then press Enter.



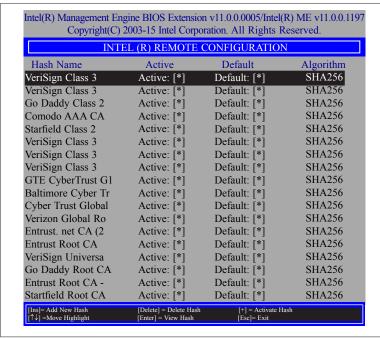
36. In the **Intel(R) Remote Configuration** menu, select **PKI DNS Suffix** then press Enter. Type PKI DNS Suffix then press Enter.



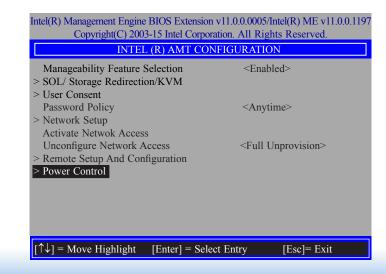
37. Select **Manage Hashes** then press Enter, and select one of hash name.



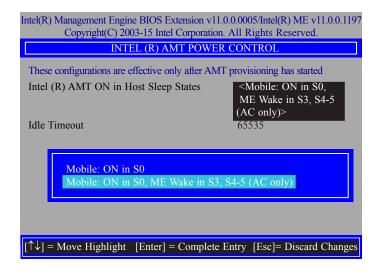
38. In the Intel(R) Remote Configuration menu, select Manage Hashes then press Enter.



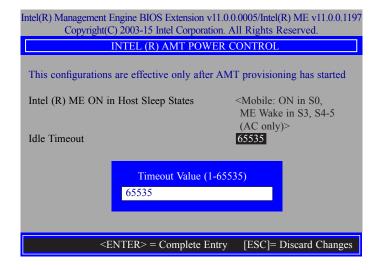
39. In the Intel(R) AMT Configuration menu, select Power Control then press Enter.



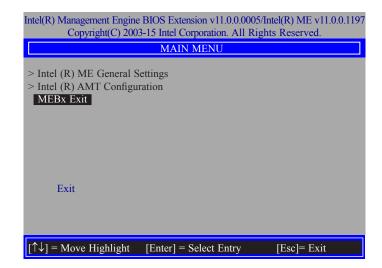
40. In the Intel(R) AMT Power Control menu, select Intel(R) AMT ON in Host Sleep States then press Enter. Select an option then press Enter.



41. In the **Intel(R) AMT Power Control** menu, select **Idle Timeout** then press Enter. Enter the timeout value (1-65535).



42. Select Previous Menu until you return to the **Main Menu**. Select **Exit** then press Enter. Type **Y** then press Enter.



Appendix A - Troubleshooting

Troubleshooting Checklist

This chapter of the manual is designed to help you with problems that you may encounter with your personal computer. To efficiently troubleshoot your system, treat each problem individually. This is to ensure an accurate diagnosis of the problem in case a problem has multiple causes.

Some of the most common things to check when you encounter problems while using your system are listed below.

- 1. The power switch of each peripheral device is turned on.
- 2. All cables and power cords are tightly connected.
- 3. The electrical outlet to which your peripheral devices are connected is working. Test the outlet by plugging in a lamp or other electrical device.
- 4. The monitor is turned on.
- 5. The display's brightness and contrast controls are adjusted properly.
- 6. All add-in boards in the expansion slots are seated securely.
- 7. Any add-in board you have installed is designed for your system and is set up correctly.

Monitor/Display

If the display screen remains dark after the system is turned on:

- 1. Make sure that the monitor's power switch is on.
- 2. Check that one end of the monitor's power cord is properly attached to the monitor and the other end is plugged into a working AC outlet. If necessary, try another outlet.
- 3. Check that the video input cable is properly attached to the monitor and the system's display adapter.
- 4. Adjust the brightness of the display by turning the monitor's brightness control knob.

The picture seems to be constantly moving.

- 1. The monitor has lost its vertical sync. Adjust the monitor's vertical sync.
- 2. Move away any objects, such as another monitor or fan, that may be creating a magnetic field around the display.
- 3. Make sure your video card's output frequencies are supported by this monitor.

The screen seems to be constantly wavering.

1. If the monitor is close to another monitor, the adjacent monitor may need to be turned off. Fluorescent lights adjacent to the monitor may also cause screen wavering.

Power Supply

When the computer is turned on, nothing happens.

- 1. Check that one end of the AC power cord is plugged into a live outlet and the other end properly plugged into the back of the system.
- 2. Make sure that the voltage selection switch on the back panel is set for the correct type of voltage you are using.
- 3. The power cord may have a "short" or "open". Inspect the cord and install a new one if necessary.

Appendix A Troubleshooting www.dfi.com

Hard Drive

Hard disk failure.

- 1. Make sure the correct drive type for the hard disk drive has been entered in the BIOS.
- 2. If the system is configured with two hard drives, make sure the bootable (first) hard drive is configured as Master and the second hard drive is configured as Slave. The master hard drive must have an active/bootable partition.

Excessively long formatting period.

If your hard drive takes an excessively long period of time to format, it is likely a cable connection problem. However, if your hard drive has a large capacity, it will take a longer time to format.

Serial Port

The serial device (modem, printer) doesn't output anything or is outputting garbled

characters.

- 1. Make sure that the serial device's power is turned on and that the device is on-line.
- 2. Verify that the device is plugged into the correct serial port on the rear of the computer.
- 3. Verify that the attached serial device works by attaching it to a serial port that is working and configured correctly. If the serial device does not work, either the cable or the serial device has a problem. If the serial device works, the problem may be due to the onboard I/O or the address setting.
- 4. Make sure the COM settings and I/O address are configured correctly.

Keyboard

Nothing happens when a key on the keyboard was pressed.

- 1. Make sure the keyboard is properly connected.
- 2. Make sure there are no objects resting on the keyboard and that no keys are pressed during the booting process.

System Board

- 1. Make sure the add-in card is seated securely in the expansion slot. If the add-in card is loose, power off the system, re-install the card and power up the system.
- 2. Check the jumper settings to ensure that the jumpers are properly set.
- 3. Verify that all memory modules are seated securely into the memory sockets.
- 4. Make sure the memory modules are in the correct locations.
- 5. If the board fails to function, place the board on a flat surface and seat all socketed components. Gently press each component into the socket.
- 6. If you made changes to the BIOS settings, re-enter setup and load the BIOS defaults.

Appendix A Troubleshooting www.dfi.com

Appendix B - Insyde BIOS Standard Status POST Code

SEC Phase 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
SEC_SYSTEM_POWER_ON	01	CPU power on and switch to Protected mode
SEC_AFTER_MICROCODE_PATCH	03	Setup Cache as RAM
SEC_ACCESS_CSR	04	PCIE MMIO Base Address initial
SEC_GENERIC_MSRINIT	05	CPU Generic MSR initialization
SEC_CPU_SPEEDCFG	06	Setup CPU speed
SEC_SETUP_CAR_OK	07	Cache as RAM test
SEC_FORCE_MAX_RATIO	08	Tune CPU frequency ratio to maximum level
SEC_GO_TO_SECSTARTUP	09	Setup BIOS ROM cache
SEC_GO_TO_PEICORE	0A	Enter Boot Firmware Volume

PEI Phase 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
PEI_SIO_INIT	70	Super I/O initialization
PEI_CPU_REG_INIT	71	CPU Early Initialization
PEI_CPU_AP_INIT	72	Multi-processor Early initialization
PEI_CPU_HT_RESET	73	HyperTransport initialization
PEI_PCIE_MMIO_INIT	74	PCIE MMIO BAR Initialization
PEI_NB_REG_INIT	75	North Bridge Early Initialization
PEI_SB_REG_INIT	76	South Bridge Early Initialization
PEI_PCIE_TRAINING	77	PCIE Training
PEI_TPM_INIT	78	TPM Initialization
PEI_MEMORY_INSTALL	80	Simple Memory test
PEI_TXTPEI	81	TXT function early initialization
PEI_MEMORY_CALLBACK	83	Set cache for physical memory

DXE Phase 8-Bit POST Code Values

Functionality Name	Post Code Values	Description
DXE_SB_SPI_INIT	41	South bridge SPI initialization
DXE_VARIABLE_RECLAIM	61	Variable store garbage collection and reclaim operation
DXE_FLASH_PART_NONSUPPORT	62	Flash part not supported.

BDS Phase 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
BDS_ENTER_BDS	10	Enter BDS entry
BDS_INSTALL_HOTKEY	11	Install Hotkey service
BDS_ASF_INIT	12	ASF Initialization
BDS_PCI_ENUMERATION_START	13	PCI enumeration
BDS_BEFORE_PCIIO_INSTALL	14	PCI resource assign complete
BDS_PCI_ENUMERATION_END	15	PCI enumeration complete
BDS_CONNECT_CONSOLE_IN	16	Keyboard Controller, Keyboard and Mouse initializatio
BDS_CONNECT_CONSOLE_OUT	17	Video device initialization
BDS_CONNECT_STD_ERR	18	Error report device initialization
BDS_CONNECT_USB_HC	19	USB host controller initialization
BDS_CONNECT_USB_BUS	1A	USB BUS driver initialization
BDS_CONNECT_USB_DEVICE	1B	USB device driver initialization
BDS_NO_CONSOLE_ACTION	1C	Console device initialization fail
BDS_ENUMERATE_ALL_BOOT_OPTIO	27	Get boot device information
BDS_ENTER_SETUP	29	Enter Setup Menu
BDS_ENTER_BOOT_MANAGER	2A	Enter Boot manager
BDS_READY_TO_BOOT_EVENT	2E	Last Chipset initialization before boot to OS
BDS_GO_LEGACY_BOOT	2F	Start to boot Legacy OS
BDS_GO_UEFI_BOOT	30	Start to boot UEFI OS
BDS_LEGACY16_PREPARE_TO_BOOT	31	Prepare to Boot to Legacy OS
BDS_EXIT_BOOT_SERVICES	32	Send END of POST Message to ME via HECI

PostBDS Phase 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
POST_BDS_NO_BOOT_DEVICE	F9	No Boot Device
POST_BDS_JUMP_BOOT_SECTOR	FE	Try to Boot with INT 19

ACPI 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
ASL_ENTER_S1	51	Prepare to enter S1
ASL ENTER S3	53	Prepare to enter S3
ASL_ENTER_S4	54	Prepare to enter S4
ASL_ENTER_S5	55	Prepare to enter S5
ASL_WAKEUP_S1	E1	System wakeup from S1
ASL_WAKEUP_S3	E3	System wakeup from S3
ASL_WAKEUP_S4	E4	System wakeup from S4
ASL_WAKEUP_S5	E5	System wakeup from S5

SMM 8-Bit POST Code Values

Functionality Name	POST Code Value	Description
SMM_ACPI_ENABLE_END	A7	ACPI enable function complete
SMM_S1_SLEEP_CALLBACK	A1	Enter S1
SMM_S3_SLEEP_CALLBACK	A3	Enter S3
SMM_S4_SLEEP_CALLBACK	A4	Enter S4
SMM_S5_SLEEP_CALLBACK	A5	Enter S5