innodisk

Total Solution For
Industrial Flash Storage

EDC 1ME

Standard

Customer: _____

Customer Part Number: _____

InnoDisk Part Number: _____

InnoDisk Model Name: _____

Date: _____

InnoDisk Approver	Customer Approver

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REVISION HISTORY

Revision	Description	Date
1.0	Official Release	September, 2014
1.1	Add mechanical dimension	October, 2014
1.2	Add power consumption Edit for Toshiba 15nm flash	JAN., 2016
1.3	Modify mechanical drawing for 44 pin horizontal B type Update RoHS and REACH declaration certificate	AUG., 2016
1.4	Update Power Supply Requirement: Add +3.3V	AUG., 2016
1.5	Edit for power consumption Remove Toshiba A19 performance	SEP., 2016
1.6	Modify Mechanical Dimensions of 44 pin vertical version	MAY, 2017
1.7	Add C~F Type Mechanical Dimensions Picture Update Innodisk Part Number Rule Code 5: %=A~F	JUL., 2018

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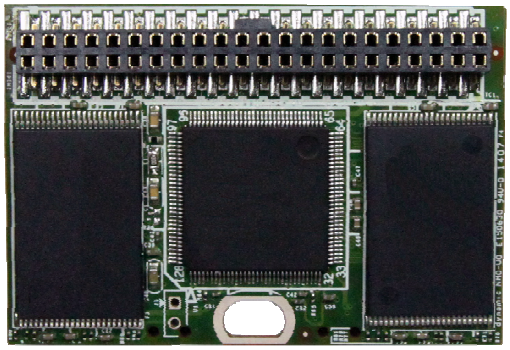
1 Product Overview

1.1 Introduction to Embedded DISK CARD 1ME

Embedded DISK CARD 1ME (EDC 1ME) products provide high capacity solid-state flash memory that electrically complies with the Personal Computer Memory Card International Association ATA standard. InnoDisk Embedded DISK CARD 1ME (EDC 1ME) is embedded solid-state data storage systems for industrial work place. Embedded DISK CARD 1ME (EDC 1ME) features an extremely light weight, reliable, low-profile form factor.

Embedded DISK CARD 1ME (EDC 1ME) supports advanced PIO (0-6), Multi Word DMA (0-4), Ultra DMA (0-6) transfer modes, multi-sector transfers, and LBA addressing.



1.2 Features

The Industrial ATA products provide the following system features:

- Capacities:
  - Vertical type: 8GB to 128GB
  - Horizontal type: 8GB to 256GB
- Fully compatible with the IDE standard interface, ATA Standard
- Access modes: True IDE Mode
- ECC (Error Correction Code) function: 72 bits/ per 1 Kbyte
- +3.3V/+5V single power supply operation
- Support Auto Stand-by and Sleep Mode.
- Power Consumption

Mode	Power Consumption(mA)
Read	140
Write	160
Idle	4

- Support transfer modes: PIO(0-6), Multiword DMA (0-4) and Ultra DMA(0-6)
- MTBF 3,000,000 hours
- R/W performance:

Table 1: 15nm MLC Performance

Cpacity	8GB	16GB	32GB	64GB	128GB	256GB
Sequential Read (max.)	75 MB/s	75 MB/s	110 MB/s	110 MB/s	110 MB/s	110 MB/s
Sequential Write (max.)	25 MB/s	25 MB/s	40 MB/s	75 MB/s	75 MB/s	75 MB/s

- Operating temperature range:
  - Standard Grade: 0℃ ~ +70℃
  - Industrial Grade: -40℃ ~ +85℃
- Storage temperature range: -55℃ ~ +95℃

1.3 Pin Assignment

EDC 1ME uses a standard IDE pin-out. See Table 1 for EDC 1ME pin assignments.

Table 2: EDC 1ME Pin Assignment

Pin No.	Name	Function	Pin No.	Name	Function
1	HRESET	Host Reset	2	GND	Ground
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11
11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15
19	GND	Ground	20	40-pin VCC[1]	Supply Voltage
				44pin KEY[1]	NC
21	DMARQ	DMA Request	22	GND	Ground
23	HIOW[3]	Host I/O Write	24	GND	Ground
	STOP[4]	Stop Ultra DMA burst			
25	HIOR[3]	Host I/O Read	26	GND	Ground
	HDMARDY[4]	Ultra DMA ready			
	HSTROBE[4]	Ultra DMA data strobe			
27	IORDY[3]	I/O Ready	28	CSEL	NC
	DDMARDY[4]	Ultra DMA ready			
	DSTROBE[4]	Ultra DMA data strobe			
29	DMACK	DMA Acknowledge	30	GND	Ground
31	INTRQ	Interrupt Request	32	RES	NC
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic
Pin No.	Name	Function	Pin No.	Name	Function
35	HAB[0]	Host Address Bit 0	36	HAB[2]	Host Address Bit 2
37	CS0	Chip Select 0	38	CS1	Chip Select 1
39	DASP	Drive Active	40	GND	Ground
41[2]	VCC	Supply Voltage	42[2]	VCC	Supply Voltage
43[2]	GND	Ground	44[2]	NC	Not Connected

1. In the 40-pin version, this pin is defined as VCC to reduce the need for an external power connector. In the 44-pin version, this pin is defined as KEY, according to the ATA standard.
2. The 40-pin version does not contain pins 41-44.
3. NC = These pins are not connected internally.
4. Signal usage in PIO & Multiword DMA mode.
5. Signal usage in Ultra DMA mode.

1.4 Pin Description

Table 2 describes the pin descriptions for EDC 1ME

Table 3: EDC 1ME Pin Description

Pin Name	Pin No.	Description	I/O
Host side pins			
HRESET-	1	Host reset signal, High: Reset.	I
CS0-	37	Chip select CS0	I
CS1-	38	Chip select CS1	I
INTRQ	31	Host interrupt signal.	O
HIOR-[3]	25	I/O read strobe signal.	I
HDMARDY-[4]		DMA ready during Ultra DMA data in burst	
HSTROBE[4]		Data strobe during Ultra DMA data out burst	
HIOW-[3]	23	I/O write strobe signal.	I
STOP[4]		Stop during Ultra DMA data bursts	
IOCS16-	32	Asserted in 16-bit access..	NA
IORDY[3]	27	I/O Ready Signal	O
DDMARDY-[4]		DMA ready during Ultra DMA data out burst	
DSTROBE[4]		Data strobe during Ultra DMA data in burst	
HDB[15:0]	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	Host data bus	I/O
HAB[2:0]	33, 35, 36	Host Address bus	I/O
CSEL-	28	Master/Slave select signal (cable select signal). Low: Device operates as a master, High: Device operates as a slave. Switch used.	NA
DASP-	39	Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.	I/O
PDIAG-	34	Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.	I/O
DMARQ	21	DMA Request.	O
DMACK-	29	DMA Acknowledge.	I
Power and Ground			
VCC	20[1], 41[2], 42[2]	Connect to VCC	VCC
GND	2, 19, 22, 24, 26, 30, 40, 43[2]	Connect to GND.	GND
Other pins			
NC	44[2]	Not used. Please do not connect.	N/A

1. In the 40-pin version, this pin is defined as VCC to reduce the need for an external power connector. In the 44-pin version, this pin is defined as KEY, according to the ATA standard.
2. The 40-pin version does not contain pins 41-44.
   NC = These pins are not connected internally.
3. Signal usage in PIO & Multiword DMA mode.
4. Signal usage in Ultra DMA mode.

2 Theory of operation

2.1 Overview

Figure 1 shows EDC 1ME operation from the system level, including the major hardware blocks.

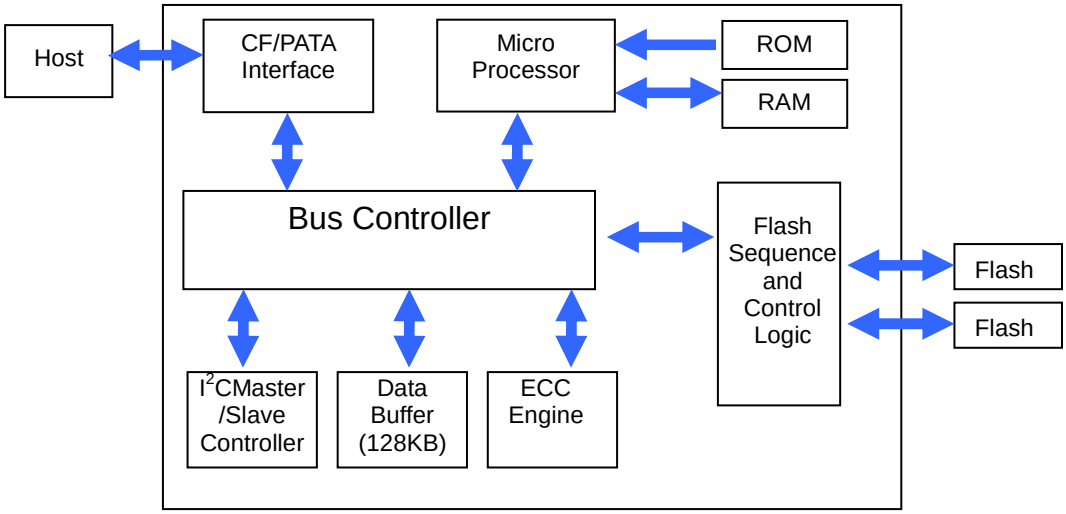


Figure 1: EDC 1ME Block Diagram

EDC 1ME integrates an IDE controller and flash devices. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

2.2 Controller

The controller is a 128-pin TQFP Package. It is Lead-free and RoHS compliant. It supports ATA-7 interface and Nand Flash chip.

2.3 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements an algorithm that can correct 72 bits per 1 Kbytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.4 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

EDC 1ME uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

3 Installation Requirements

3.1 EDC 1ME Pin Directions

From figure 2 is shown for the EDC 1ME 44pin pin directions.

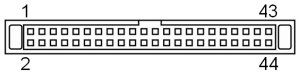


Figure 2: 44-pin Connector Layout (Female)

3.2 Electrical Connections for EDC 1ME

EDC 1ME can be connected to the host by placing it directly on the on-board socket. If a cable is used, it should be no longer than 20 inches (457mm), and should be aligned as follows:

- For 44-pin EDC 1ME:

  Pin 1 of the cable must be aligned with pin 1 of the EDC 1ME connector.

  Pin 44 of the cable must be aligned with pin 44 of the EDC 1ME connector.

3.3 Installing EDC 1ME in a Two-Drive Configuration (Master/Slave)

If EDC 1ME is being installed as an additional IDE drive using the same IDE I/O port, Switch S1 in “M” position will be the master, whereas in “S” position it becomes the slave.

4 Power Management

EDC 1ME supports the following two operation modes:

Sleep Mode: Internal clock is halted (for EDC 1ME, the standby mode defined in the ATA specification is the same as this mode)

Active Mode: Internal clock operates normally (for EDC 1ME, the idle mode defined in the ATA specification is the same as this mode)

5 Specifications

5.1 CE and FCC Compatibility

EDC 1ME conforms to CE and FCC requirements.

5.2 RoHS Compliance

EDC 1ME is fully compliant with RoHS directive.

5.3 Write-Protect Function Support

InnoDisk EDC 1ME with the write-protect function could prevent EDC 1ME from modification and deletion. Write-protected data in EDC 1ME could only be read, that is, users could not write to it, edit it, append data to it, or delete it.

When users would like to make sure that neither themselves nor others could modify or destroy the file, users could switch on write-protection. Thus InnoDisk EDC 1ME would process write-protect mechanism and disable flash memory to be written-in any data. Only while the system power-off, users could switch on write-protection. Write-protection could not be switched-on, after OS booting.

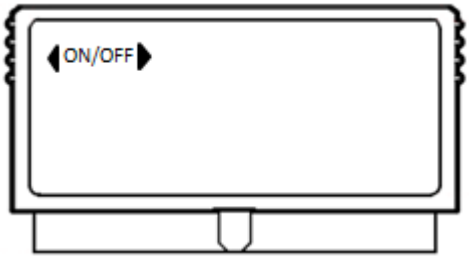


Figure 3: Write Protect Switch On/Off Direction*

* The “Multi-functional Switch” of Vertical type EDC 1ME is default to switch between Master and Slave, it can be set to write-protect function upon request.

5.4 Environmental Specifications

5.4.1 Temperature Ranges

- Operating Temperature Range:
  - Standard Grade: 0℃ to +70℃
  - Industrial Grade: -40℃ to +85℃ (SLC only)
- Storage Temperature Range: -55℃ to +95℃

5.4.2 Humidity

Relative Humidity: 10-95%, non-condensing

5.4.3 Shock and Vibration

Table 4: Shock/Vibration Testing for EDC 1ME

Reliability	Test Conditions
Vibration	44pin: 80 Hz to 2000 Hz, 20G, 3 axes
Mechanical Shock	1500 G, 3 axes

5.4.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various EDC 1ME configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 5: EDC 1ME MTBF

Product	Condition	MTBF (Hours)
44-pin	Telcordia SR-332 GB, 25℃	> 3,000,000

5.5 Mechanical Dimensions

44pin Vertical (DEE4H-XXXD53XXXXX).

Mechanical Dimension: 50.3x27.3x5.8mm (W/T/H)

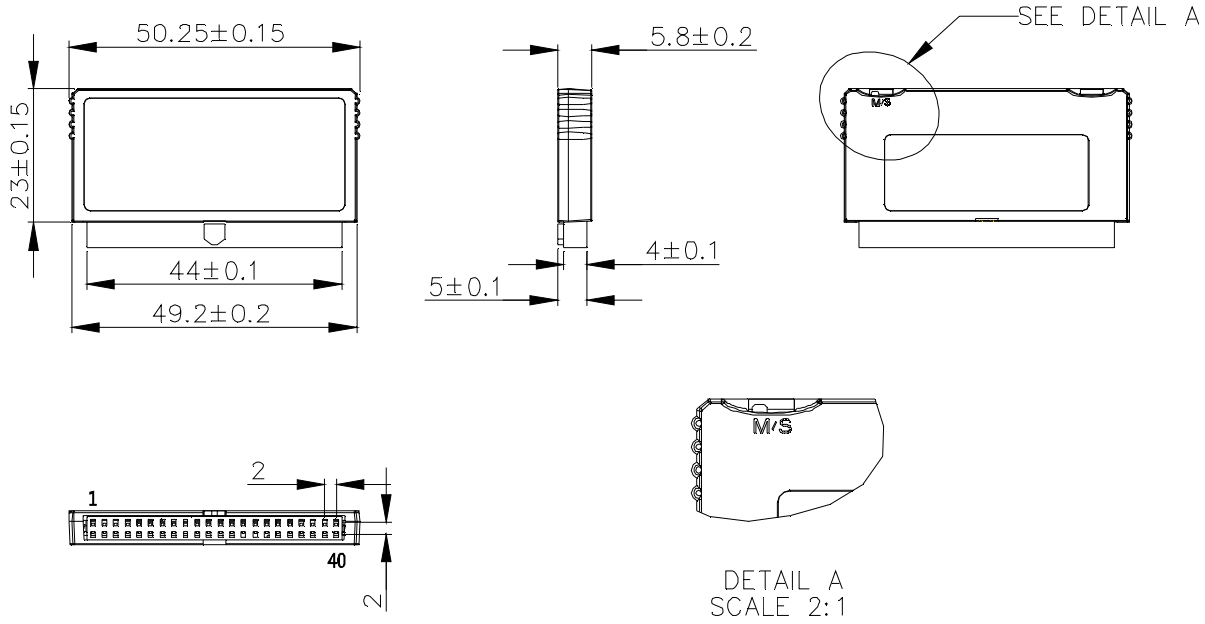


Figure 4: Mechanical Dimension of EDC 1ME 44-pin (Vertical Version)

44pin Horizontal A type (DEE4A-XXXD53XXXXX).

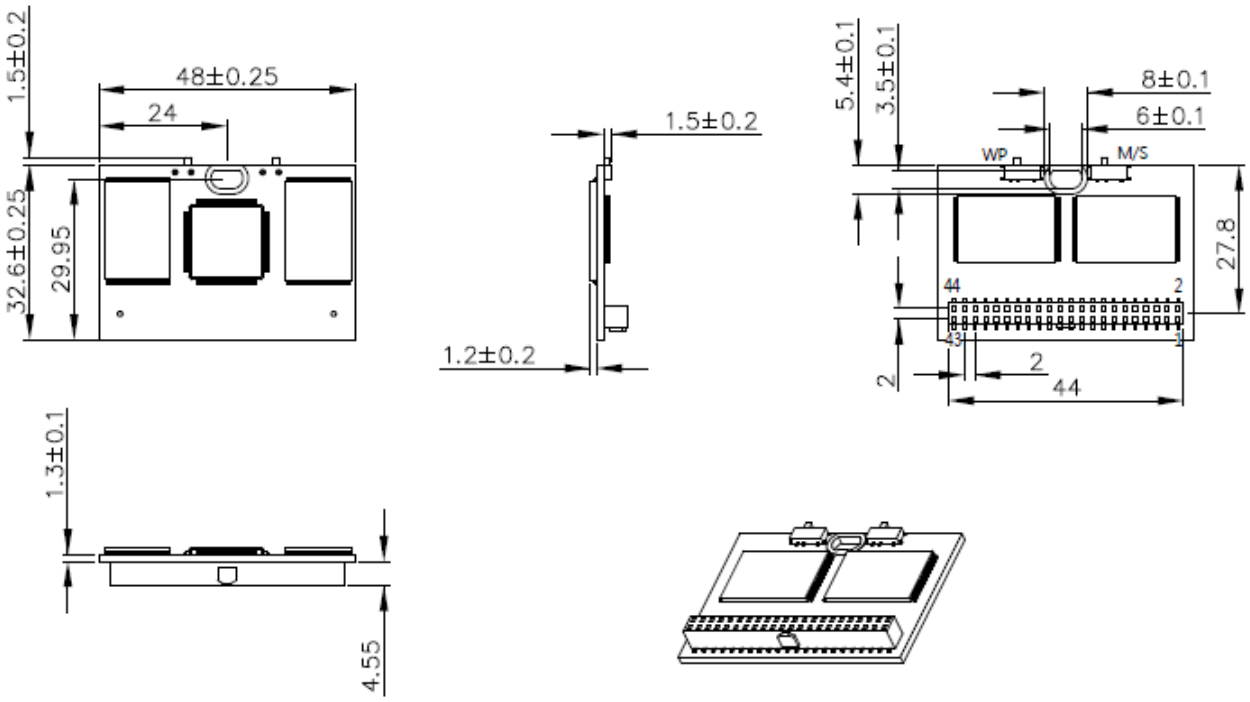


Figure 5: Mechanical Dimension of EDC 1ME 44-pin (Horizontal A type Version)

44pin Horizontal B type (DEE4B-XXXD53XXXXX).

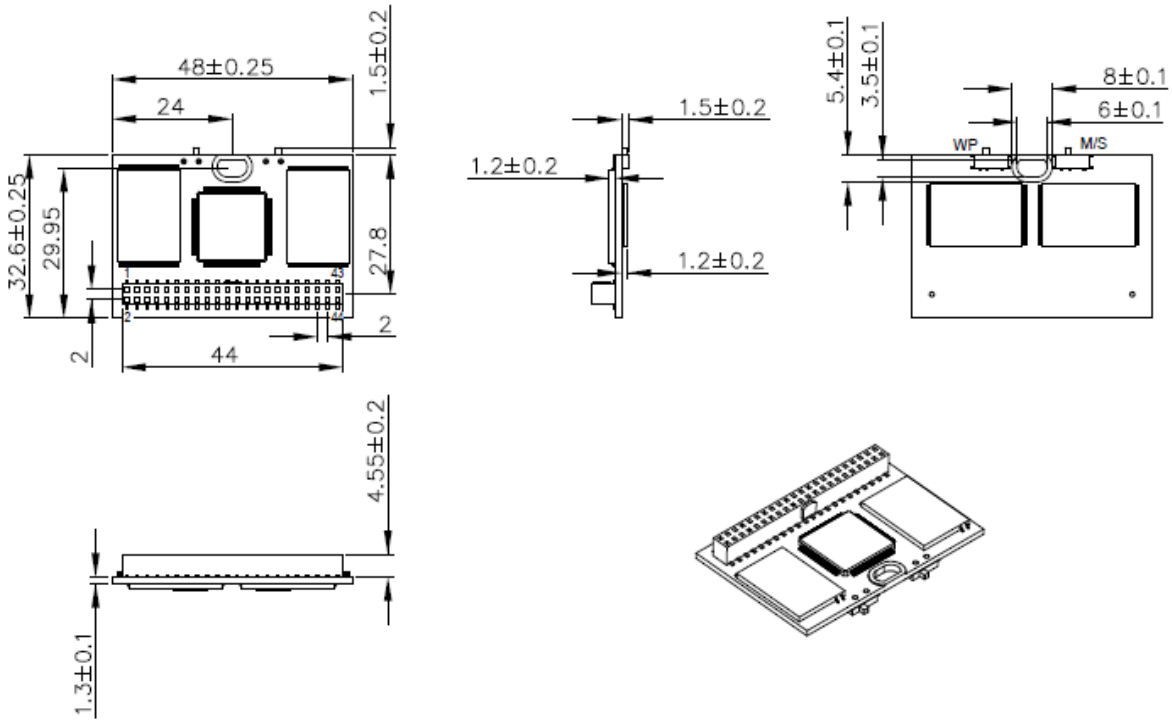


Figure 6: Mechanical Dimension of EDC 1ME 44-pin (Horizontal B type Version)

44pin Horizontal C type (DEE4C-XXXD53XXXXX).

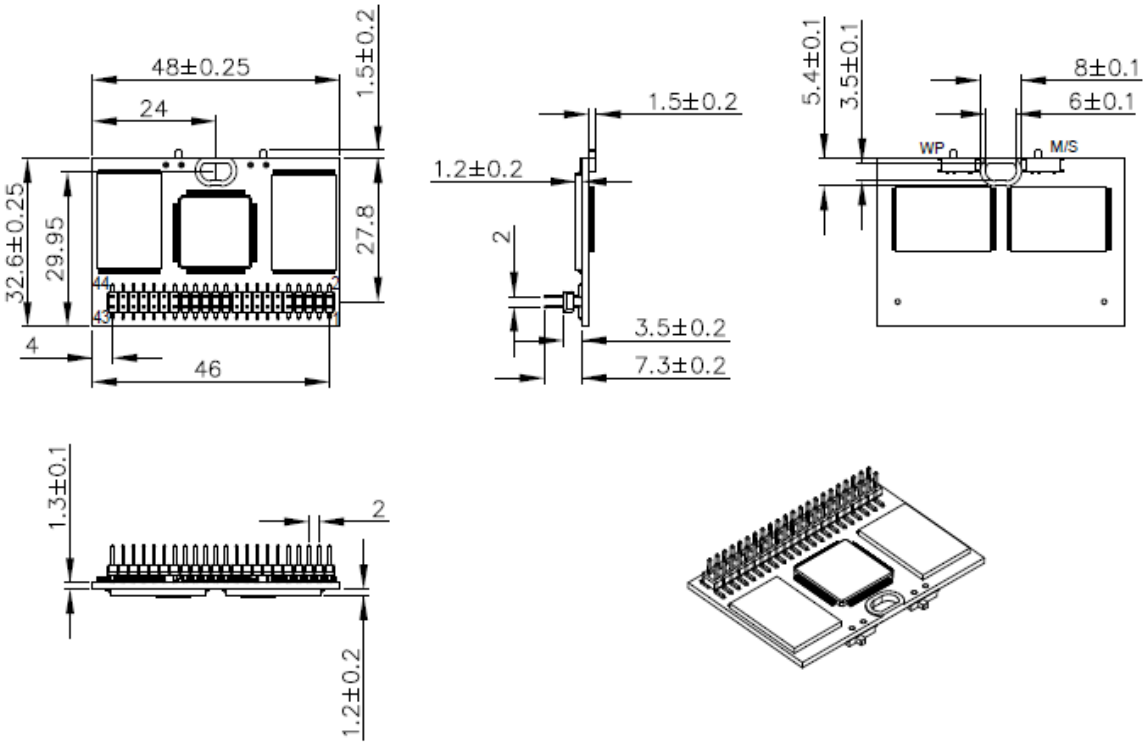


Figure 7: Mechanical Dimension of EDC 1ME 44-pin (Horizontal C type Version)

44pin Horizontal D type (DEE4D-XXXD53XXXXX).

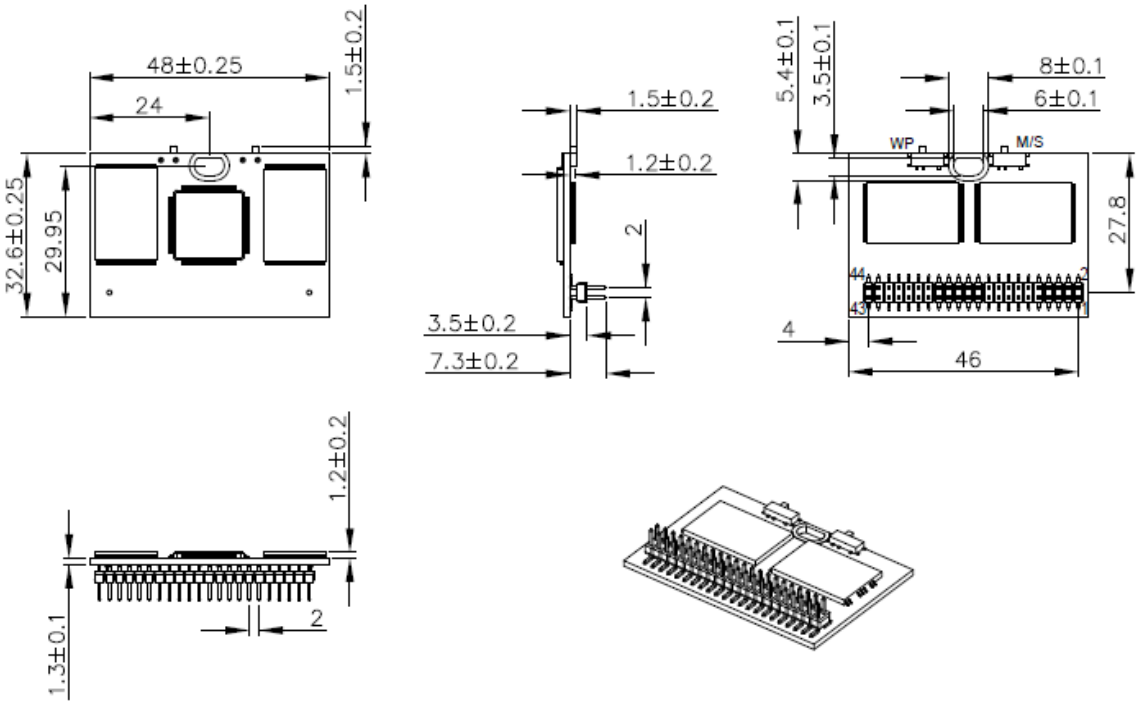


Figure 8: Mechanical Dimension of EDC 1ME 44-pin (Horizontal D type Version)

44pin Horizontal E type (DEE4E-XXXD53XXXXX).

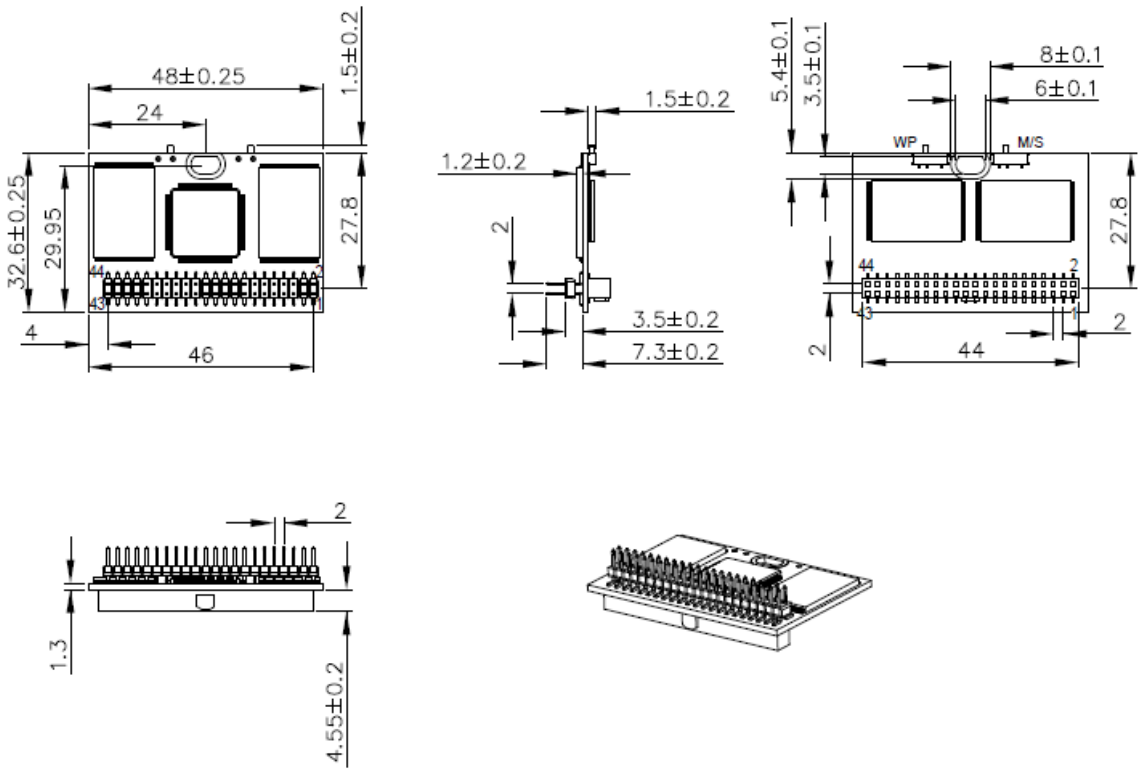


Figure 9: Mechanical Dimension of EDC 1ME 44-pin (Horizontal E type Version)

44pin Horizontal F type (DEE4E-XXXD53XXXXX).

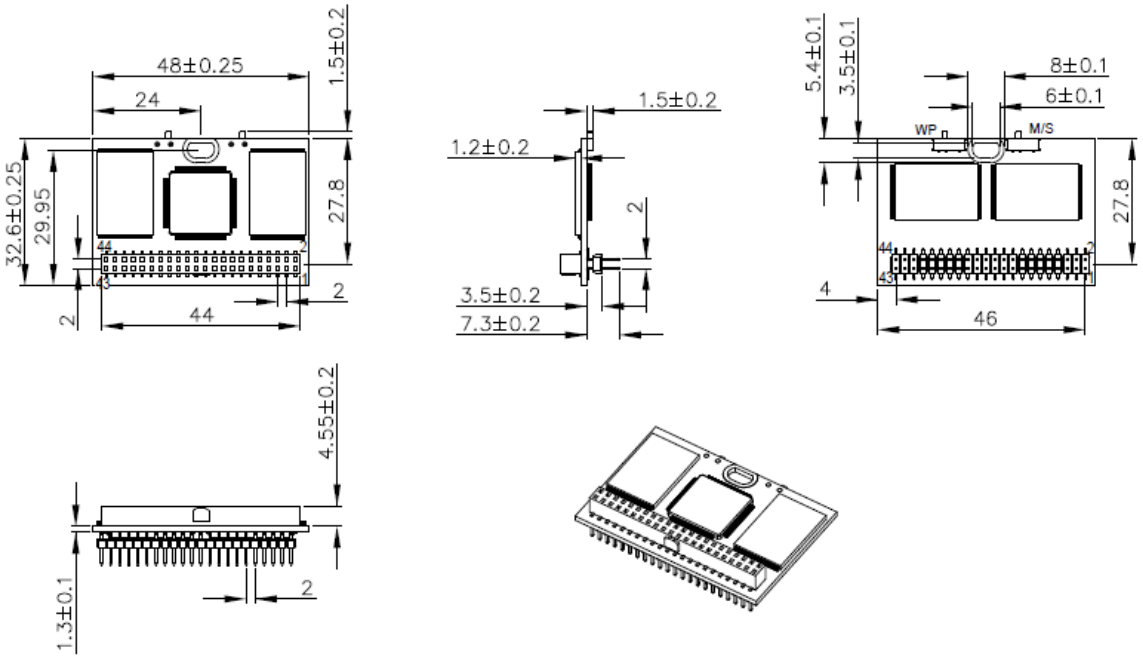


Figure 10: Mechanical Dimension of EDC 1ME 44-pin (Horizontal F type Version)

5.6 Electrical Specifications

5.6.1 DC Characteristic

Power supply requirement: +3.3V/+5V±10% DC

5.6.2 Timing Specifications

5.6.2.1 PIO Mode

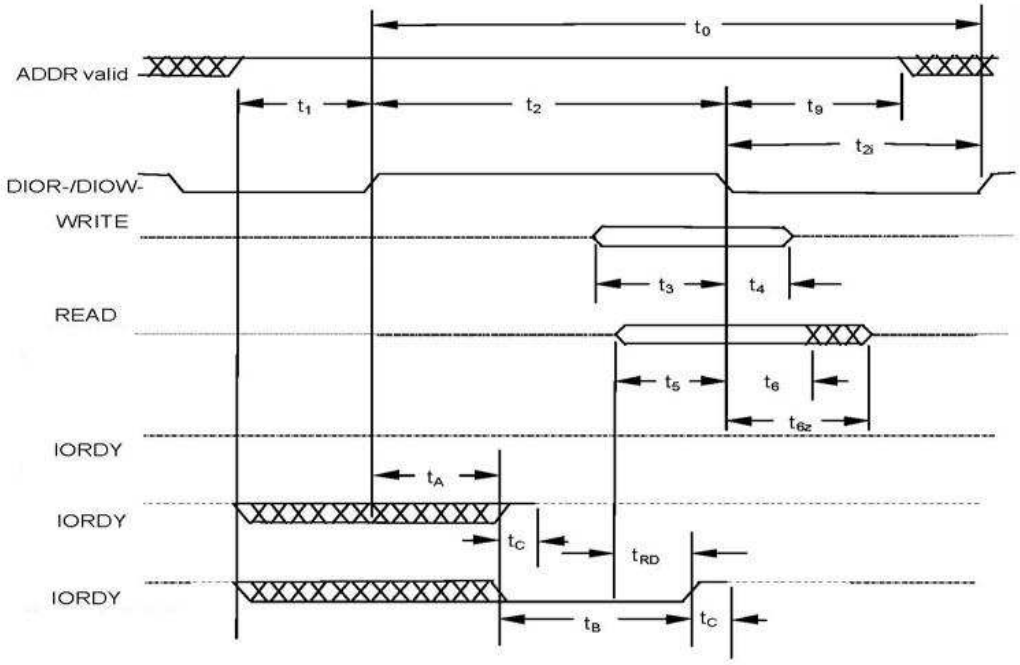


Figure 11: Read/Write Timing Diagram, PIO Mode

Table 6: Read/Write Timing Specifications, PIO Mode 0-4

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_0	Cycle time (min.)	600	383	240	180	120
t_1	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25
t_2	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70
t_2	HIOR-/HIOW- Register 8-bit (min.)	290	290	290	80	70
t_{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25
t_3	HIOW- data setup (min.)	60	45	30	30	20
t_4	HIOW- data hold (min.)	30	20	15	10	10
t_5	HIOR- data setup (min.)	50	35	20	20	20
t_6	HIOR- data hold (min.)	5	5	5	5	5
t_{6z}	HIOR- data tri-state (max.)	30	30	30	30	30
t_7	Address valid to IOCS16- assertion (max.)	90	50	40	n/a	n/a
t_8	Address valid to IOCS16- released (max.)	60	45	30	n/a	n/a
t_9	HIOR-/HIOW- to address valid hold	20	15	10	10	10
t_{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0
t_A	IORDY setup time	35	35	35	35	35
t_B	IORDY pulse width (max.)	1250	1250	1250	1250	1250
t_C	IORDY assertion to release (max.)	5	5	5	5	5

5.6.2.2 Multiword DMA

Figure 12: Read/Write Timing Diagram, Multiword DMA Mode

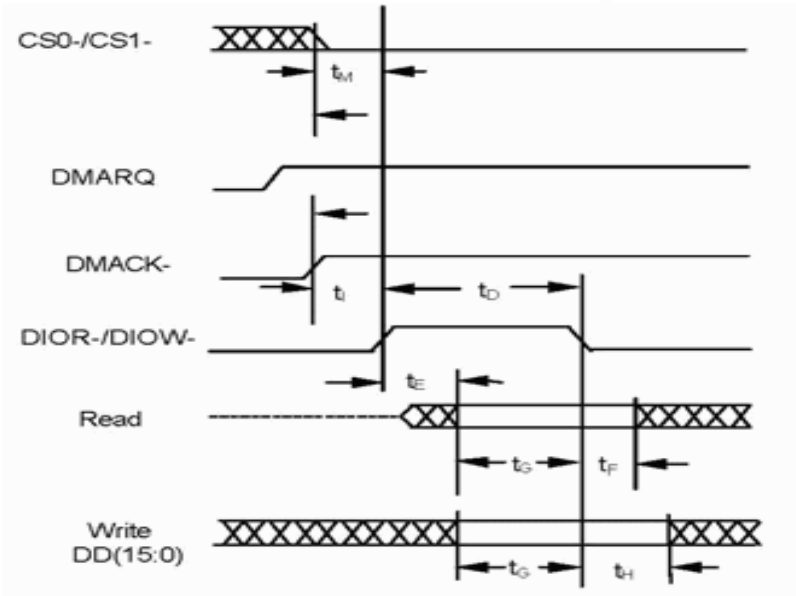


Table 7: Read/Write Timing Specifications, Multiword DMA Mode 0-2

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2
t_0	Cycle time (min.)	480	150	120
t_D	HIOR-/HIOW- assertion width (min.)	215	80	70
t_E	HIOR- data access (max.)	150	60	50
t_F	HIOR- data hold (min.)	5	5	5
t_G	HIOR-/HIOW- data setup (min.)	100	30	20
t_H	HIOW- data hold (min.)	20	15	10
t_I	DMACK to HIOR-/HIOW- setup (min.)	0	0	0
t_J	HIOR-/HIOW- to DMACK hold (min.)	20	5	5
t_{KR}	HIOR- negated width (min.)	50	50	25
t_{KW}	HIOW- negated width (min.)	215	50	25
t_{LR}	HIOR- to DMARQ delay (max.)	120	40	35
t_{LW}	HIOW- to DMARQ delay (max.)	40	40	35
t_M	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25
t_N	CS1-, CS0- hold	15	10	10
t_Z	DMACK-	20	25	25

5.6.2.3 Ultra DMA mode

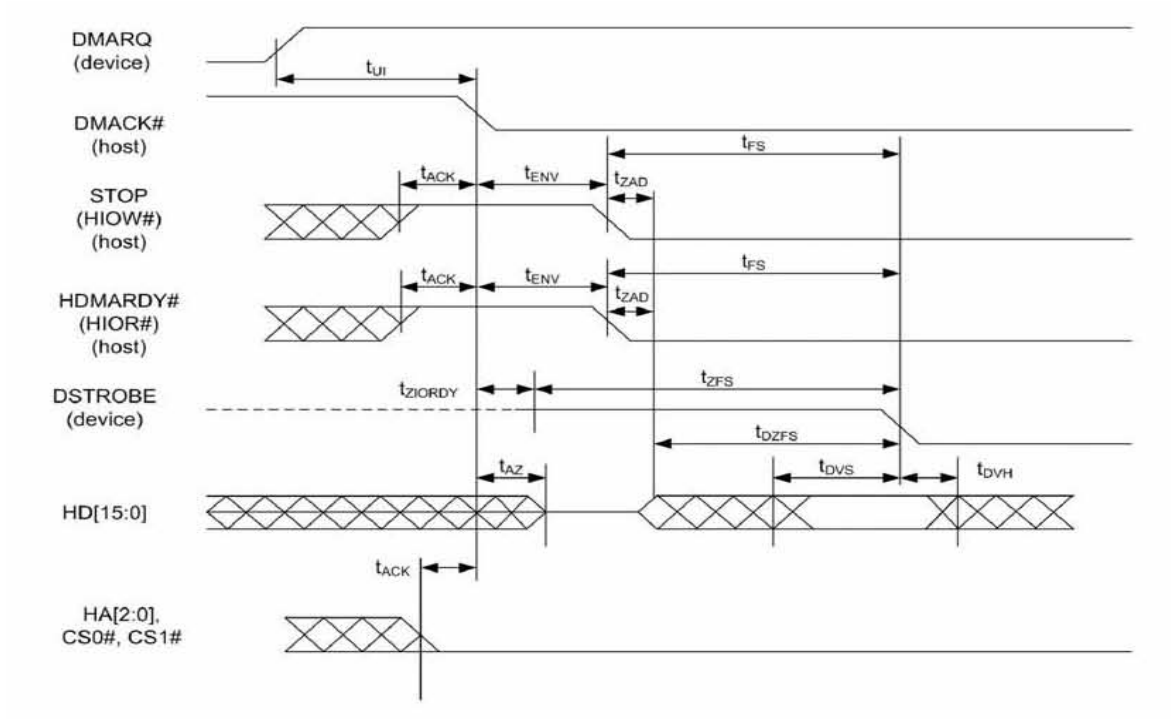


Figure 13: Ultra DMA Mode Data-in Burst Initiation Timing Diagram

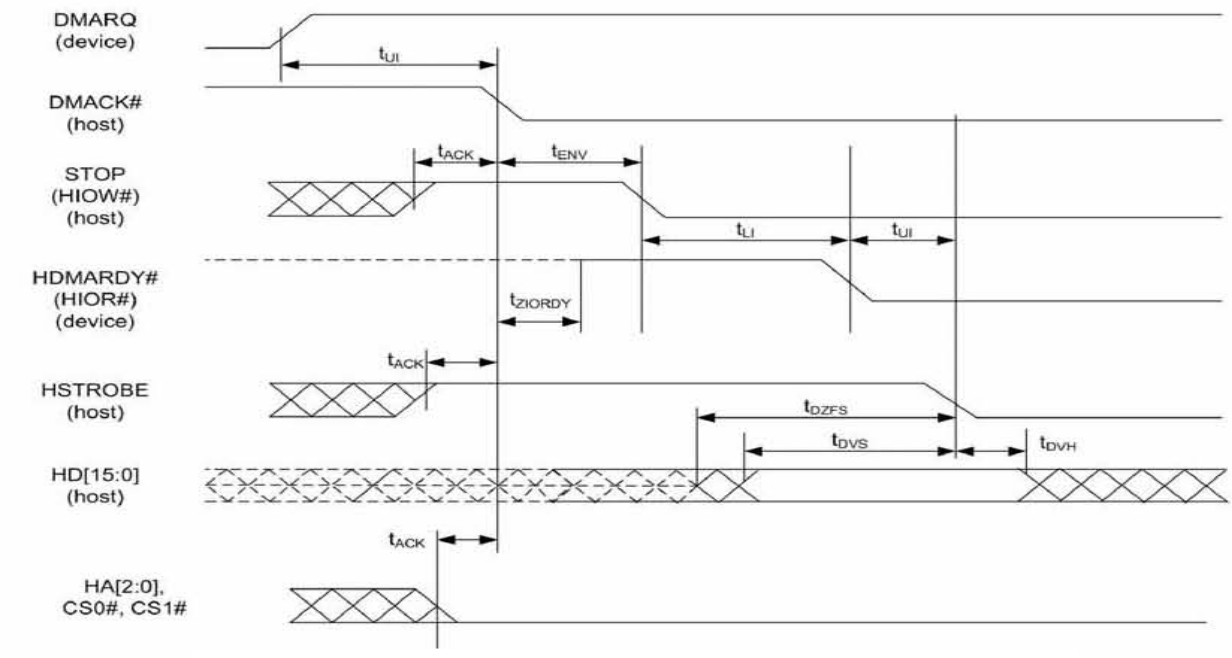


Figure 14: Ultra DMA Mode Data-out Burst Initiation Timing Diagram

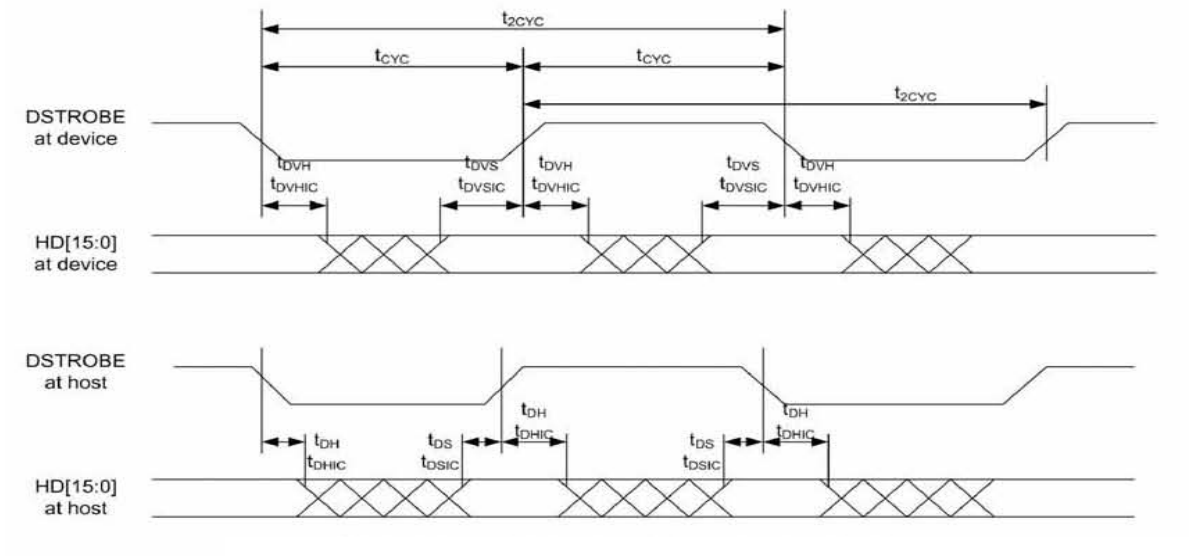


Figure 15: Sustained Ultra DMA Mode Data-in Burst Timing Diagram

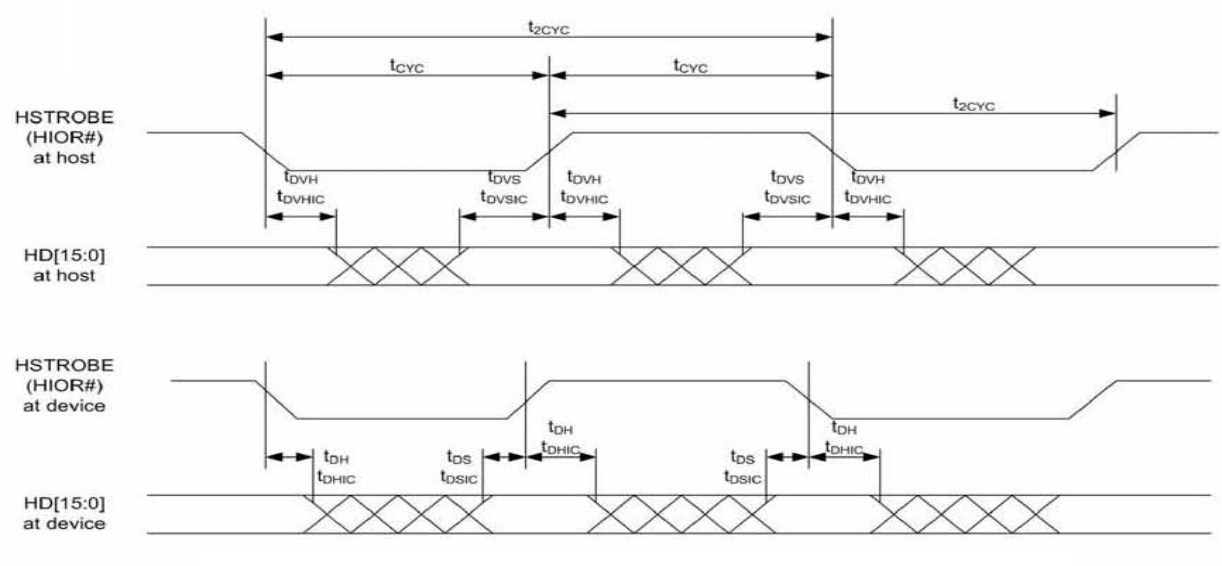


Figure 16: Sustained Ultra DMA Mode Data-out Burst Timing Diagram

Table 8: Timing Diagram, Ultra DMA Mode 0-6

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Mode 5		Mode 6	
		Min.	Max.	Min.	Max.	Min.	Min.	Max.	Min.	Max.	Max.	Max.	Min.	Max.	Max.
t_{2CYC}	Typical sustained average two cycle time	240	-	160	-	90	-	60	-	60	-	40	-	30	-
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	39	-	25	-	25	-	16.8	-	13	-
t_{2CYC}	Two cycle time allowing	230	-	153	-	86	-	57	-	57	-	38	-	29	-

	for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)														
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	5	-	5	-	4	-	2.6	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-	4.6	-	3.5	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	20	-	6.7	-	6.7	-	4.8	-	4	-
t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-	4.8	-	4	-
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	230	-	200	-	130	-	120	-	120	-	90	-	80
t_{LI}	Limited interlock time	0	150	0	150	0	100	0	100	0	100	0	75	0	60
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-	20	-	20	-
t_{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10	-	10	-	10
t_{ZAH}	Minimum delay time required for output drivers to assert or negate (from released state)	20	-	20	-	20	-	20	-	20	-	20	-	20	-
t_{ZAD}		0	-	0	-	0	-	0	-	0	-	0	-	0	-
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	55	20	55	20	55	20	50	20	50
t_{RFS}	Ready-to-final-STROBE	-	75	-	70	-	60	-	60	-	60	-	50	-	50

	time (no STROBE edges shall be sent this long after negation of DMARDY-)														
t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-	85	-	85	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	50	-	50	-	50	-	50	-

6 Supported ATA Commands

EDC 1ME supports the commands listed in Table 9.

Table 9: IDE Commands

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	98H or E5H	-	-	-	-	D	-
1	Execute Device Diagnostic	90H	-	-	-	-	D	-
1	Erase Sector(s)	C0H	-	Y	Y	Y	Y	Y
2	Format Track	50H	-	Y	-	Y	Y	Y
1	Identify Device	ECH	-	-	-	-	D	-
1	Idle	97H or E3H	-	Y	-	-	D	-
1	Idle immediate	95H or E1H	-	-	-	-	D	-
1	Initialize Device Parameters	91H	-	Y	-	-	Y	-
1	NOP	00H	-	-	-	-	D	-
1	Read Buffer	E4H	-	-	-	-	D	-
1	Read DMA	C8H	-	Y	Y	Y	Y	Y
1	Read Long Sector	22H or 23H	-	-	Y	Y	Y	Y
1	Read Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40H or 41H	-	Y	Y	Y	Y	Y
1	Recalibrate	1XH	-	-	-	-	D	-
1	Request Sense	03H	-	-	-	-	D	-
1	Seek	7XH	-	-	Y	Y	Y	Y
1	Set Features	EFH	Y	-	-	-	D	-
1	Set Multiple Mode	C6H	-	Y	-	-	D	-
1	Set Sleep Mode	99H or E6H	-	-	-	-	D	-
1	Standby	96H or E2H	-	-	-	-	D	-
1	Standby Immediate	94H or E0H	-	-	-	-	D	-
2	Write Buffer	E8H	-	-	-	-	D	-
2	Write DMA	CAH	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
2	Write Sector(s) without Erase	38H	-	Y	Y	Y	Y	Y

Defines:

FR: Feature Register

SC: Sector Count Register

SN: Sector Number Register

CY: Cylinder Registers

DH: Card/Device/Head Register

LBA: LBA Block Address Mode Supported

Y: The register contains a valid parameter for this command. For Card/Device/Head Register Y means both the

CompactFlash Storage Card and head parameter are used; D – only the CompactFlash Storage Card parameter is valid and not the head parameter; C – The register contains command specific data (see command description for use).

6.1 Check power mode – 98H or E5H

Table 10: Check power mode information

Register	7	6	5	4	3	2	1	0
Command(7)	98h or E5h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command checks the power mode. If the CompactFlash Storage is in, going to, or recovering from the sleep mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the ompactFlash Storage Card is in idle mode, the CompactFlash Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

6.2 Execute Device Diagnostic – 90H

Table 11: Execute device diagnostic information

Register	7	6	5	4	3	2	1	0
Command(7)	90h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command performs the internal diagnostic tests implemented by the CompactFlash Storage Card. When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices. The Diagnostic codes are shown in Table 34. Diagnostic Codes are returned in the Error Register at the end of the command.

Table 12: Diagnostic

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controller Microprocessor Error

8Xh	Slave Error in True IDE Mode

6.3 Erase Sector(s) – C0H

Table 13: Erase sector information

Register	7	6	5	4	3	2	1	0
Command(7)	C0h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

6.4 Format Track – 50H

Table 14: Format track information

Register	7	6	5	4	3	2	1	0
Command(7)	50h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	X (LBA 7-0)							
Sector Count(2)	Count(LBA mode only)							
Feature(1)	X							

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the CompactFlash Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the CompactFlash Storage Card. If LBA=1 then the number of sectors to format is taken from the Sec Cnt register (0=256). The use of this command is not recommended.

6.5 Identify Device – ECH

Table 15: Identify device information

Register	7	6	5	4	3	2	1	0
Command(7)	Ech							
C/D/H(6)	X	X	X	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							

Sector Count(2)	X
Feature(1)	X

The Identify Device command enables the host to receive parameter information from the CompactFlash Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 35. All reserved bits or words are zero. Hosts should not depend in Obsolete words in Identify Device containing 0. Table 35 specifies each filed in the data returned by the Identify Device Command. In Table 35, X indicates a numeric nibble vale specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Table 16: IDENTIFY DEVICE information

Word	Description	Value
0	General configuration bit-significant information: 15 0 = ATA device 14-8 Retired 7 1 = removable media device 6 Obsolete 5-3 Retired 2 Response incomplete 1 Retired 0 Reserved	044Ah
1	Obsolete	XXXXh
2	Specific configuration	0000h
3	Obsolete	00XXh
4-5	Retired	XXXXh
6	Obsolete	XXXXh
7-8	Reserved for assignment by the CompactFlash™ Association	XXXXh
9	Retired	0000h
10-19	Serial number (20 ASCII characters)	20 ASCII characters
20-21	Retired	0002h
22	Obsolete	0004h
23-26	Firmware revision (8 ASCII characters)	8 ASCII characters
27-46	Model number (40 ASCII characters)	40 ASCII characters
47	15-8 80h 7-0 00h = Reserved 01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands	8001h

48	Reserved	0000h
49	Capabilities 15-14 Reserved for the IDENTIFY PACKET DEVICE command. 13 1 = Standby timer values as specified in this standard are supported 0 = Standby timer values shall be managed by the device 12 Reserved for the IDENTIFY PACKET DEVICE command. 11 1 = IORDY supported 0 = IORDY may be supported 10 1 = IORDY may be disabled 9 1 = LBA supported 8 1 = DMA supported. 7-0 Retired	0F00h
50	Capabilities 15 Shell be cleared to zero 14: Shall be set to one 13-2 Reserved 1 Obsolete 0 Shall be set to one to indicate a device specific Standby timer value minimum.	0000h
51	Obsolete	0200h
52	Obsolete	0000h
53	15-3 Reserved 2 1 = the fields reported in word 88 are valid Reserved 0 = the fields reported in word 88 are not valid 1 1 = the fields reported in words (70:64) are valid 0 = the fields reported in words (70:64) are not valid 0 Obsolete	0007h
54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
59	15-9 Reserved 8 1 = Multiple sector setting is valid 7-0 xxh = Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command	01XXh
60-61	Total number of user addressable sectors	XXXXXXXXh
62	Obsolete	0000h
63	15-11 Reserved 10 1 = Multiword DMA mode 2 is selected 0 = Multiword DMA mode 2 is not selected	XX07h

	9 1 = Multiword DMA mode 1 is selected 0 = Multiword DMA mode 1 is not selected 8 1 = Multiword DMA mode 0 is selected 0 = Multiword DMA mode 0 is not selected 7-3 Reserved 2 1 = Multiword DMA mode 2 and below are supported 1 1 = Multiword DMA mode 1 and below are supported 0 1 = Multiword DMA mode 0 is supported	
64	15-8 Reserved 7-0 PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time 15-0 Cycle time in nanoseconds	0078h
67	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds	0078h
68	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds	0078h
69-70	Reserved (for future command overlap and queuing)	0000h
71-74	Reserved for the IDENTIFY PACKET DEVICE command.	0000h
75	Queue depth 15-5 Reserved 4-0 Maximum queue depth – 1	0000h
76-79	Reserved for Serial ATA	0000h 0000h 0000h 0000h
80	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA/ATAPI-14 13 Reserved for ATA/ATAPI-13 12 Reserved for ATA/ATAPI-12 11 Reserved for ATA/ATAPI-11 10 Reserved for ATA/ATAPI-10 9 Reserved for ATA/ATAPI-9 8 Reserved for ATA/ATAPI-8 7 1 = supports ATA/ATAPI-7 6 1 = supports ATA/ATAPI-6	0080h

	5 1 = supports ATA/ATAPI-5 4 1 = supports ATA/ATAPI-4 3 Obsolete 2 Obsolete 1 Obsolete 0 Reserved	
81	Minor version number 0000h or FFFFh = device does not report version 0001h-FFFEh = See 6.17.41	0000h
82	Command set supported. 15 Obsolete 14 1 = NOP command supported 13 1 = READ BUFFER command supported 12 1 = WRITE BUFFER command supported 11 Obsolete 10 1 = Host Protected Area feature set supported 9 1 = DEVICE RESET command supported 8 1 = SERVICE interrupt supported 7 1 = release interrupt supported 6 1 = look-ahead supported 5 1 = write cache supported 4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. 3 1 = mandatory Power Management feature set supported 2 1 = Removable Media feature set supported 1 1 = Security Mode feature set supported 0 1 = SMART feature set supported	742Bh
83	Command sets supported. 15 Shall be cleared to zero 14 Shall be set to one 13 1 = FLUSH CACHE EXT command supported 12 1 = mandatory FLUSH CACHE command supported 11 1 = Device Configuration Overlay feature set supported 10 1 = 48-bit Address feature set supported 9 1 = Automatic Acoustic Management feature set supported 8 1 = SET MAX security extension supported 7 See Address Offset Reserved Area Boot, INCITS TR27:2001 6 1 = SET FEATURES subcommand required to spinup after power-up 5 1 = Power-Up In Standby feature set supported	5100h

	4	1 = Removable Media Status Notification feature set supported	
	3	1 = Advanced Power Management feature set supported	
	2	1 = CFA feature set supported	
	1	1 = READ/WRITE DMA QUEUED supported	
	0	1 = DOWNLOAD MICROCODE command supported	
84	Command set/feature supported extension		4003h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report	
	11	Reserved for technical report	
	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64-bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported	
	5	1 = General Purpose Logging feature set supported	
	4	1 = Streaming feature set supported	
	3	1 = Media Card Pass Through Command feature set supported	
	2	1 = Media serial number supported	
	1	1 = SMART self-test supported	
	0	1 = SMART error logging supported	
85	Command and feature sets supported or enabled		
	15	Obsolete	0
	14	1 = NOP command enabled	0
	13	1 = READ BUFFER command enabled	0
	12	1 = WRITE BUFFER command enabled	0
	11	Obsolete	0
	10	1 = Host Protected Area feature set enabled	1
	9	1 = DEVICE RESET command enabled	0
	8	1 = SERVICE interrupt enabled	0
	7	1 = release interrupt enabled	0
	6	1 = look-ahead enabled	0
	5	1 = Write Cache enabled	1
	4	Shall be cleared to zero to indicate that the PACKET Command feature set is not supported.	0
	3	1 = Power Management feature set enabled	0
	2	1 = Removable Media feature set enabled	0

	1	1 = Security Mode feature set enabled	X
	0	1 = SMART feature set enabled	X
86	Command set/feature enabled		1000h
	15-14	0 = Reserved	
	13	1 = FLUSH CACHE EXT command supported	
	12	1 = FLUSH CACHE command supported	
	11	1 = Device Configuration Overlay supported	
	10	1 = 48-bit Address features set supported	
	9	1 = Automatic Acoustic Management feature set enabled	
	8	1 = SET MAX security extension enabled by SET MAX SET PASSWORD	
	7	See Address Offset Reserved Area Boot, INCITS TR27:2001	
	6	1 = SET FEATURES subcommand required to spin-up after power-up	
	5	1 = Power-Up In Standby feature set enabled	
	4	1 = Removable Media Status Notification feature set enabled	
	3	1 = Advanced Power Management feature set enabled	
	2	1 = CFA feature set enabled	
	1	1 = READ/WRITE DMA QUEUED command supported	
	0	1 = DOWNLOAD MICROCODE command supported	
87	Command and feature sets supported or enabled		0003h
	15	Shall be cleared to zero	
	14	Shall be set to one	
	13	1 = IDLE IMMEDIATE with UNLOAD FEATURE supported	
	12	Reserved for technical report-	
	11	Reserved for technical report-	
	10	1 = URG bit supported for WRITE STREAM DMA EXT and WRITE STREAM EXT	
	9	1 = URG bit supported for READ STREAM DMA EXT and READ STREAM EXT	
	8	1 = 64 bit World wide name supported	
	7	1 = WRITE DMA QUEUED FUA EXT command supported	
	6	1 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA EXT commands supported	
	5	1 = General Purpose Logging feature set supported	
	4	1 = Valid CONFIGURE STREAM command has been executed	
	3	1 = Media Card Pass Through Command feature set enabled	
	2	1 = Media serial number is valid	
	1	1 = SMART self-test supported	
	0	1 = SMART error logging supported	
88	15	Reserved	XX7Fh
	14	1 = Ultra DMA mode 6 is selected 0 = Ultra DMA mode 6 is not selected	
	13	1 = Ultra DMA mode 5 is selected	

	0 = Ultra DMA mode 5 is not selected 12 1 = Ultra DMA mode 4 is selected 0 = Ultra DMA mode 4 is not selected 11 1 = Ultra DMA mode 3 is selected 0 = Ultra DMA mode 3 is not selected 10 1 = Ultra DMA mode 2 is selected 0 = Ultra DMA mode 2 is not selected 9 1 = Ultra DMA mode 1 is selected 0 = Ultra DMA mode 1 is not selected 8 1 = Ultra DMA mode 0 is selected 0 = Ultra DMA mode 0 is not selected 7 Reserved 6 1 = Ultra DMA mode 6 and below are supported 5 1 = Ultra DMA mode 5 and below are supported 4 1 = Ultra DMA mode 4 and below are supported 3 1 = Ultra DMA mode 3 and below are supported 2 1 = Ultra DMA mode 2 and below are supported 1 1 = Ultra DMA mode 1 and below are supported 0 1 = Ultra DMA mode 0 is supported	
89	Time required for security erase unit completion	0001h
90	Time required for Enhanced security erase completion	0000h
91	Current advanced power management value	0000h
92	Master Password Revision Code	FFFEh
93	Hardware reset result. The contents of bits (12:0) of this word shall change only during the execution of a hardware reset. 15 Shall be cleared to zero. 14 Shall be set to one. 13 1 = device detected CBLID- above ViH 0 = device detected CBLID- below ViL	XXXXh

	12-8 Device 1 hardware reset result. Device 0 shall clear these bits to zero. Device 1 shall set these bits as follows: 12 Reserved. 11 0 = Device 1 did not assert PDIAG-. 1 = Device 1 asserted PDIAG-. 10-9 These bits indicate how Device 1 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 8 Shall be set to one.	
	7-0 Device 0 hardware reset result. Device 1 shall clear these bits to zero. Device 0 shall set these bits as follows: 407 Reserved. 407 0 = Device 0 does not respond when Device 1 is selected. 1 = Device 0 responds when Device 1 is selected. 5 0 = Device 0 did not detect the assertion of DASP-. 1 = Device 0 detected the assertion of DASP-. 4 0 = Device 0 did not detect the assertion of PDIAG-. 1 = Device 0 detected the assertion of PDIAG-. 3 0 = Device 0 failed diagnostics. 1 = Device 0 passed diagnostics. 2-1 These bits indicate how Device 0 determined the device number: 00 = Reserved. 01 = a jumper was used. 10 = the CSEL signal was used. 11 = some other method was used or the method is unknown. 0 Shall be set to one.	
94	15-8 Vendor's recommended acoustic management value. 7-0 Current automatic acoustic management value.	0000h
95	Stream Minimum Request Size	0000h
96	Streaming Transfer Time – DMA	0000h
97	Streaming Access Latency – DMA and PIO	0000h
98-99	Streaming Performance Granularity	0000h
100-103	Maximum user LBA for 48-bit Address feature set.	0000h
104	Streaming Transfer Time – PIO	0000h
105	Reserved	0000h
106	Physical sector size / Logical Sector Size 15 Shall be cleared to zero 14 Shall be set to one	0000h

	13 1 = Device has multiple logical sectors per physical sector. 12 1= Device Logical Sector Longer than 256 Words 11-4 Reserved 3-0 2^X logical sectors per physical sector	
107	Inter-seek delay for ISO-7779 acoustic testing in microseconds	0000h
108	15-12 NAA (3:0) 11-0 IEEE OUI (23:12)	0000h
109	15-4 IEEE OUI (11:0) 3-0 Unique ID (35:32)	0000h
110	15-0 Unique ID (31:16)	0000h
111	15-0 Unique ID (15:0)	0000h
112-115	Reserved for world wide name extension to 128 bits	0000h
116	Reserved for technical report-	0000h
117-118	Words per Logical Sector	0000h
119-120	Reserved	0000h
121-126	Reserved	0000h
127	Removable Media Status Notification feature set support 15-2 Reserved 1-0 00 = Removable Media Status Notification feature set not supported 01 = Removable Media Status Notification feature supported 10 = Reserved 11 = Reserved	0000h
128	Security Status 15-9 Reserved 8 Security level 0 = high, 1 = Maximum 7-6 Reserved 5 1= Enhanced security erase supported 4 1= Security count expired 3 1 = Security frozen 2 1 = Security locked 1 1 = Security enabled 0 1 = Security supported	0 X 0 0 0 X X X 1
129-159	Vendor specific	0000h
160	CFA power mode 1 15 Word 160 supported 14 Reserved 13 CFA power mode 1 is required for one or more commands implemented by the device 12 CFA power mode 1 disabled 11-0 Maximum current in ma	0000h

161-175	Reserved for assignment by the CompactFlash™ Association	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15-8 Checksum 7-0 Signature	XXXXh

6.6 Idle -97H or E3H

Table 17: Idle information

Register	7	6	5	4	3	2	1	0
Command(7)	97h or E3h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Timer Count (5 msec increments)							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec) is different from the ATA specification.

6.7 Idle immediate – 95H or E1H

Table 18: Idle immediate information

Register	7	6	5	4	3	2	1	0
Command(7)	95h or E1h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt.

6.8 Initialize Device Parameters – 91H

Table 19: Initialize device parameters information

Register	7	6	5	4	3	2	1	0
Command(7)	91h							

C/D/H(6)	X	O	X	Drive	Max Head (no. of heads-1)
Cylinder High(5)	X				
Cylinder Low(4)	X				
Sector Number(3)	X				
Sector Count(2)	Number of sectors				
Feature(1)	X				

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Device/Head registers are used by this command.

6.9 NOP – 00H

Table 20: NOP information

Register	7	6	5	4	3	2	1	0
Command(7)	00h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command always fails with the CompactFlash Storage Card returning command aborted.

6.10 Read Buffer – E4H

Table 21: Read buffer information

Register	7	6	5	4	3	2	1	0
Command(7)	E4h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Read Buffer command enables the host to read the current contents of the CompactFlash Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

6.11 Read DMA – C8H

Table 22: Read DMA information

Register	7	6	5	4	3	2	1	0
Command(7)	C8							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16							
Cylinder Low(4)	Cylinder Low (LBA 15-8							

Sector Number(3)	Sector Numbe(LBA 7-0
Sector Count(2)	Sector Count
Feature(1)	X

This command uses DMA mode to read from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 request 256 sectors. The transfer begins at he sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, cleat BSY. The Card asserts DMAREQ while data is available to be transferred. The Card asserts DMAREQ while data is available to be transferred. The host then reads the (512 & sector –count) bytes of data from the Card using DMA. While DMAREQ is asserted by the Card, the Host asserts –DMACK while it is ready to transfer data by DMA and asserts –IORD once for each 16 bit word to be transferred to the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecoverable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder, head, and sector number of the sector where the occurred. The amount of data transferred is indeterminate. When a Read DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

6.12 Read Long Sector – 22H or 23H

Table 23: Read long sector information

Register	7	6	5	4	3	2	1	0
Command(7)	22h or 23h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	X							
Feature(1)	X							

The Read Long command performs similarly to the Read Sector(s) command except that is returns 516 bytes of data instead of 512 bytes. During a Read Long command, the CompactFlash Storage Card does not check the ECC bytes to determine if there consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

6.13 Read Sector(s) – 20H or 21H

Table 24: Read sector information

Register	7	6	5	4	3	2	1	0
Command(7)	20h or 21h							

C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)
Cylinder High(5)	Cylinder High (LBA 23-16)				
Cylinder Low(4)	Cylinder Low (LBA 15-8)				
Sector Number(3)	Sector Number (LBA 7-0)				
Sector Count(2)	Sector Count				
Feature(1)	X				

This command reads from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has buffer, sets DRQ, cleats BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The command Block Registers contain the cylinder head, and sector number of the sector 2where the error occurred. The flawed data is pending in the sector buffer.

6.14 Read Verify Sector(s) – 40H or 41H

Table 25: Read verify sector information

Register	7	6	5	4	3	2	1	0
Command(7)	40h or 41h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the CompactFlash Storage Card sets BSY. When the requested sectors have been verified, the CompactFlash Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified. If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

6.15 Recalibrate – 1XH

Table 26: Recalibrate information

Register	7	6	5	4	3	2	1	0
Command(7)	1Xh							
C/D/H(6)	1	LBA	1	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							

Sector Number(3)	X
Sector Count(2)	X
Feature(1)	X

This command is effectively a NOP command to the CompactFlash Storage Card and is provided for compatibility.

6.16 Request Sense – 03H

Table 27: Request sense information

Register	7	6	5	4	3	2	1	0
Command(7)	03h							
C/D/H(6)	1	LBA	1	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command requests extended error information for the previous command. Table36 defines the valid extended error codes for the CompactFlash Storage Card Series product. The extended error code is returned to the host in the Error Register.

Table 28: Extended Error Codes

Extended Error Code	Description
00h	No Error Detected
01h	Self Test OK
09h	Miscellaneous Error
20h	Invalid Command
21h	Invalid Address
2Fh	Address Overflow
35h, 36h	Supply or generated Voltage Out of Tolerance
11h	Uncorrected ECC Error
18h	Corrected ECC Error
05h,30-34h, 37h, 3Eh	Self Test or Diagnostic Falied
10h, 14h	ID Not Found
3Ah	Spare Sectors Exhausted
1Fh	Data Transfer Error/Aborted Command
0Ch, 38h,3Bh,3Ch,3Fh	Corrupted Media Format
03h	Write/ Erase Failed
22h	Power Level 1 Disabled

6.17 Seek – 7XH

Table 29: Seek information

Register	7	6	5	4	3	2	1	0
Command(7)	7Xh							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	X (LBA 7-0)							
Sector Count(2)	X							
Feature(1)	X							

This command is effectively a NOP command to the CompactFlash Storage Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

6.18 Set Features – EFH

Table 30: Set feature information

Register	7	6	5	4	3	2	1	0
Command(7)	Efh							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Config							
Feature(1)	Feature							

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the CompactFlash Storage Card shall return command aborted. Table 37: Feature Supported defines all features that are supported.

Table 31: Feature Supported

Feature	Operation
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Counter register.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft reset.
82h	Disable Write cache.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
Aah	Enable Read Look Ahead.
BBh	4 Bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

6.19 Set Multiple Mode – C6H

Table 32: Set multiple mode information

Register	7	6	5	4	3	2	1	0
Command(7)	C6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command enables the CompactFlash Storage Card to perform Read and Write Multiple operations and establishes the block count for these commands. The Sector Count Register is loaded with the number of sectors per block. Upon receipt of the command, the CompactFlash Storage Card sets BSY to 1 and checks the Sector Count Register. If the Sector Count Register contains a valid value and the block count is supported, the value is loaded and execution is enabled for all subsequent Read Multiple and Write Multiple commands. If the Sector Count Register contains 0 when the command is issued, Read and Write Multiple commands are disabled. At power on, or after a hardware or (unless disabled by a Set Feature command) software reset, the default mode is Read and Write multiple disabled.

6.20 Set Sleep Mode – 99H or E6H

Table 33: Set sleep mode information

Register	7	6	5	4	3	2	1	0
Command(7)	99h or E6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds.

6.21 Standby – 96H or E2H

Table 34: Standby information

Register	7	6	5	4	3	2	1	0
Command(7)	96h or E2h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							

Sector Count(2)	X
Feature(1)	X

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, cleat BSY and return interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.22 Standby Immediate – 94H or E0H

Table 35: Standby immediate information

Register	7	6	5	4	3	2	1	0
Command(7)	94h or E0h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the CompactFlash Storage Card to set BSY, enter the Sleep mode, clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.23 Write Buffer – E8H

Table 36: Write buffer information

Register	7	6	5	4	3	2	1	0
Command(7)	E8h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Write Buffer command enables the host to overwrite contents of the CompactFlash Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfer 512 bytes.

6.24 Write DMA – CAH

Table 37: Write DMA information

Register	7	6	5	4	3	2	1	0
Command(7)	Cah							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low(LBA 15-8)							

Sector Number(3)	Sector Number (LBA 7-0)
Sector Count(2)	Sector Count
Feature(1)	X

This command uses DMA mode to write from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued the CompactFlash Storage Card sets BSY, puts all or part of the sector of data in the buffer. The Card is then permitted, although not required, to set DRQ, clear BSY. The Card asserts DMAREQ while data is available to be transferred. The host then writes the (512*sector count) bytes of data to the Card using DMA. While DMAREQ is asserted by the Card, the host asserts –DMACK while it is ready to transfer data by DMA and asserts –IOWR once for each 16 bit word to be transferred from the Host.

Interrupts are not generated on every sector, but upon completion of the transfer of the entire number of sectors to be transferred or upon the occurrence of an unrecovertable error. At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector where the error occurred. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The amount of data transferred is indeterminate. When a write DMA command is received by the Card and 8 bit transfer mode has been enabled by the Set Features command, the Card shall return the Aborted error.

6.25 Write Sector(s) – 30H or 31H

Table 38: Write sector information

Register	7	6	5	4	3	2	1	0
Command(7)	30h or 31h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the CompactFlash Storage Card sets BST, then sets DRQ and clears BSDY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated. If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read

the command block to determine what error has occurred, and on which sector.

6.26 Security

6.26.1 Security Set Password

6.26.1.1 Command Code

F1h

6.26.1.2 Feature Set

Security Mode feature set

6.26.1.3 Protocol

PIO data-out

6.26.1.4 Inputs

Table 39: Security set password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F1h							

Device –

DEV shall specify the selected device.

Normal Outputs

Table 40: Security set password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

6.26.1.5 Error Outputs

Table 41: Security set password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

6.26.1.6 Prerequisites

DRDY set to one.

6.26.1.7 Description

This command transfer 512 byte of data from the host. Table 10 defines the content of this information. The data transferred controls the function of this command. Table 11 defines the interaction of the identifier and security level bits.

The revision code field shall be returned in the IDENTIFY DEVICE word 92. The valid revision codes are 0001h through FFFEh. A value of 0000h or FFFFh indicates that the Master Password Revision Code is not supported.

Table 42: Security set password command's data content

Word	Content
0	Control Word Bit 0 Identifier 0=set User password 1=set Master password Bits (7:1) Reserved Bit(8) Security level 0=High 1=Maximum Bits(15:9) Reserved
1-16	Password(32 bytes)
17	Master Password Revision Code()
18-255	Reserved

Table 43: Security Set password command's identifier and security level bit interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall than be unlocked by either the User password it the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be unlock
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed. Master password revision code set to the value in Master Password Revision Code field.

6.26.2 Security Unlock

6.26.2.1 Command Code

F2h

6.26.2.2 Feature Set

Security Mode feature set

6.26.2.3 Protocol

PIO data-out

6.26.2.4 Inputs

Table 44: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F2h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 45: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

6.26.2.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 46: Security unlock command for inputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							

LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

6.26.2.6 Prerequisites

DRDY set to one.

6.26.2.7 Description

This command transfers 512 bytes of data from the host. Table13 defines the content of this information. If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device shall compare the supplied password with the stored User password. If the password compare fails then the device shall return command aborted to the host and decrements the unlock counter. This counter shall be initially set to five and shall decremented for each password mismatch when SECURITY UNLOCK and SECURITY ERASE UNIT commands shall be command aborted until a power-on reset or a hardware reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

6.26.3 Security Erase Prepare

6.26.3.1 Command Code

F3h

6.26.3.2 Feature Set

Security Mode feature set

6.26.3.3 Protocol

Non-data

6.26.3.4 Inputs

Table 47: Security erase prepare command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na			
Command	F3h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 48: Security erase prepare command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) will be set to zero.

DRQ will be cleared to zero

ERR will be set to zero.

6.26.3.5 Error Outputs

The device shall return aborted if the device is in Frozen mode.

Table 49: Security erase prepare command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na

Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode. ABRT may be set to one if the device is not able to complete the action requested by the command

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

6.26.3.6 Prerequisites

DRDY set to one.

6.26.3.7 Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental loss of data on the device.

6.26.4 Security Erase Unit

6.26.4.1 Command Code

F4h

6.26.4.2 Feature Set

Security Mode feature set

6.26.4.3 Protocol

PIO data-out.

6.26.4.4 Inputs

Table 50: Security erase unit command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							

Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F4h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 51: Security erase unit command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

6.26.4.5 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 52: Security erase unit command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							

Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

6.26.4.6 Prerequisites

DRDY set to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

6.26.4.7 Description

This command transfer 512 bytes of data from the host. Table12 defines the content of this information. If the password does not match the password previously saved by the device, the device shall reject the command with command aborted.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device shall command abort the SECURITY ERASE UNIT command.

When Normal Erase mode is specified, the SECURITY ERASE UNIT command shall write binary zeroes to all user data areas. The Enhanced Erase mode is optional. When Enhanced Erase Mode is specified, the device shall write predetermined data patterns to all user areas. In Enhanced Erase mode, all previously written user data shall be overwritten, including sectors that are no longer in use due to reallocation.

This command shall disable the device Lock mode, however, the Master password shall still be stored internally within the device and may be reactivated later a new User password is set.

Table 53: Security erase unit password information

Word	Content
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit 1 Erase mode 0=Normal Erase 1=Enhanced Erase Bit(15:2) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

6.26.5 Security Freeze Lock

6.26.5.1 Command Code

F5h

6.26.5.2 Feature Set

Security Mode feature set

6.26.5.3 Protocol

Non-data.

6.26.5.4 Inputs

Table 54: Security freeze lock for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	Na	Na	Na	Na	Na
Command	F5h							

Device register–

DEV shall specify the selected device.

6.26.5.5 Normal Outputs

Table 55: Security freeze lock for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

6.26.5.6 Error Outputs

The device shall return aborted if the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, if Enhance Erase is specified but not supported, or if the data area is not successfully overwritten.

Table 56: Security freeze lock for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT shall be set to one if the device is in locked mode. ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

6.26.5.7 Prerequisites

DRDY set to one.

6.26.5.8 Description

The SECURITY FREEZE LOCK command shall set the device to Frozen mode. After command completion any other commands that update the device Lock mode shall be command aborted. Frozen mode shall be disabled by power-off or hardware reset. If SECURITY FREEZE LOCK shall be issued when the device in Frozen mode, the command executes and the device shall remain in Frozen mode.

Command disabled by SECURITY FREEZE LOCK are:

- SECUIRTY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT

6.26.6 Security Disable Password

6.26.6.1 Command Code

F6h

6.26.6.2 Feature Set

Security Mode feature set

6.26.6.3 Protocol

PIO data-out.

6.26.6.4 Inputs

Table 57: Security disable password command for inputs information

Register	7	6	5	4	3	2	1	0
Features	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	Na	Na	Na	Na	Na
Command	F6h							

Device register–

DEV shall specify the selected device.

Normal Outputs

Table 58: Security disable password command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device register

DEV shall indicate the selected device.

Status register

BSY shall be cleared to zero indicating command completion

DRDY shall be set to one.

DF (Device Fault) will be set to zero.

DRQ shall be cleared to zero

ERR shall be cleared to zero.

6.26.6.5 Error Outputs

The device shall return aborted if the device is in Locked mode, or device is in Frozen mode.

Table 59: Security disable password command for error outputs information

Register	7	6	5	4	3	2	1	0
Error	Na	Na	Na	Na	Na	ABRT	Na	Na
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	obs	Na	obs	DEV	Na			
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Error Register

ABRT may be set to one if the device is not able to complete the action requested by the command.

Device register

DEV shall indicate the selected device.

Status register

BSY will be cleared to zero indicating command completion

DRDY will be set to one.

DF (Device Fault) should be set to one if a device fault has occurred.

DRQ will be cleared to zero

ERR will be set to one if an Error register bit is set to one.

6.26.6.6 Prerequisites

DRDY set to one. Device shall be in Unlocked mode.

6.26.6.7 Description

The SECURITY DISABLE PASSWORD command transfer 512 bytes of data from the host. Table 13 defines the content of this information. If the password selected by word 0 matches the password previously saved by the device, the device shall disable the Lock mode. This command shall not change the Master password. The Master password shall be reactivated when a User password if set.

Table 60: Security disable password command content

Word	Content
0	Control Word Bit 0 Identifier 0=Compare User password 1= Compare Master password Bit(15:1) Reserved
1-16	Password (32 Bytes)
17-255	Reserved

6.27 SMART

Individual SMART commands are identified by the value placed in the Feature register.

Table 61: SMART Feature register values

Value	Command
D0h	SMATR Read Data
D8h	SMART ENABLE OPERATIONS
D9h	SMART DISABLE OPERATIONS

6.27.1 SMART Read Data

6.27.1.1 Command Code

B0h with a Feature register value of D0h

6.27.1.2 Feature Set

Smart Feature Set

- Operation when the SMART feature set is implemented.

6.27.1.3 Protocol

PIO data-in

6.27.1.4 Inputs

Table 62: SMART command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D0h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

6.27.1.5 Normal Outputs

Table 63: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.27.1.6 Prerequisites

DRDY set to one. SMART enabled.

6.27.1.7 Description

This command returns the Device SMART data structure to the host.

Table 64: ID of SMART data structure

BYTE	Description
0-1	Revision code
2-361	Vendor specific
362	Off-line data collection status
363	Self-test execution status byte
364-365	Total time in seconds to complete off-line data collection activity
366	Vendor specific
367	Off-line data collection capability
368-369	SMART capability
370	Error logging capability *7-1 Reserved *0 1 = Device error logging supported
371	Vendor specific
372	Short self-test routine recommended polling time (in minutes)
373	Extended self-test routine recommended polling time (in minutes)
374	Conveyance self-test routine recommended polling time (in minutes)
375-385	Reserved
386-395	Firmware Version/Date Code
396-399	Reserved
400-406	'SMI2236'
407-511	Reserved
511	Checksum

ID: E9h

Table 65: Smart command for ECC fail record information

Byte	Function	Description
0	ECC fail number	When failure bit is bigger than "ECC Fail number", this block will be marked as Bad Block.
1	Row address 3	Flash Block Address
2	Row address 2	Flash Block Address
3	Row address 1	Flash Block Address
4	Channel number of last ECC fail	NA
5	Bank number of last ECC fail	NA
6	Reserved	NA
7	Reserved	NA

ID: Eah

Table 66: Smart command for average/max erase count information

Byte	Function	Description
0	Average Erase Count (High Byte)	Average erase count of all blocks.
1	Average Erase Count	
2	Average Erase Count (Low Byte)	
3	Max Erase Count (High Byte)	Indicate a block which's erase count is the largest.
4	Max Erase Count	

5	Max Erase Count (Low Byte)	
6	Reserved	NA
7	Reserved	NA

- When the Maximum erase count is 255 bigger than average erase count, the wear-leveling will be executed.

ID: Ebh

Table 67: Smart command for good/system block count information

Byte	Function	Description
0	Good Block Count (High Byte)	Total used blocks of SSD
1	Good Block Count	
2	Good Block Count (Low Byte)	
3	System(Free) Block Count (High Byte)	Free block of SSD. Free block has to be bigger than 20. When the free block count is less than 20, the SSD will be locked.
4	System(Free) Block Count (Low Byte)	
5	Reserved	NA
6	Reserved	NA
7	Reserved	NA

6.27.2 SMART ENABLE OPERATIONS

6.27.2.1 Command Code

B0h with a Feature register value of D8h

6.27.2.2 Feature Set

Smart Feature Set

6.27.2.3 Protocol

Non-data

6.27.2.4 Inputs

Table 68: SMART Enable command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	Na							
LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

6.27.2.5 Normal Outputs

Table 69: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.27.2.6 Prerequisites

DRDY set to one.

6.27.2.7 Description

This command enables access to all SMART capabilities within device.

6.27.3 SMART DISABLE OPERATIONS

6.27.3.1 Command Code

B0h with a Feature register value of D9h

6.27.3.2 Feature Set

Smart Feature Set

6.27.3.3 Protocol

Non-data

6.27.3.4 Inputs

Table 70: SMART DISABLE Command for inputs information

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	Na							

LBA Low	Na							
LBA Mid	4Fh							
LBA High	C2h							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Command	B0h							

Device register-

DEV shall specify the selected device.

6.27.3.5 Normal Outputs

Table 71: SMART command for normal outputs information

Register	7	6	5	4	3	2	1	0
Error	Na							
Sector Count	Na							
LBA Low	Na							
LBA Mid	Na							
LBA High	Na							
Device	Obs	Na	obs	DEV	Na	Na	Na	Na
Status	BSY	DRDY	DF	Na	DRQ	Na	Na	ERR

Device Register-

DEV shall indicate the selected device.

Status register-

BSY will be cleared to zero indicating command completion.

DRDY will be set to one.

DF (Device Fault) will be cleared to zero.

DRQ shall be cleared to zero.

ERR shall be cleared to zero.

6.27.3.6 Prerequisites

DRDY set to one. SMART enabled.

6.27.3.7 Description

This command disables all SMART capabilities within device.

7 Device Parameters

EDC 1ME device parameters listed in Table 71.

Table 72: Device parameters

Capacity	Cylinders	Heads	Sectors	LBA	Capacity(MB)
4GB	7,785	16	63	7,847,280	3,831.68
8GB	15,538	16	63	15,662,304	7,647.61
16GB	31,045	16	63	31,293,360	15,279.96
32GB	62,041	16	63	62,537,328	30,535.80
64GB	16,383	15	63	125,059,072	61,064.00
128GB	16,383	15	63	250,085,376	122,112.00
256GB	16,383	15	63	500,170,752	122,112.00

8 InnoDisk Part Number Rule

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	D	**E**	**E**	**4**	**%**	**-**	**0**	**4**	**G**	**D**	**5**	**3**	**B**	**C**	**1**	**D**	**C**	**-**	**X**
Description	Disk	EDC 1ME				-	Capacity			Controller			Flash Mode	Operation Temp.	Internal Control	Ch.	Flash		Customized Code

Definition	
Code 1st ~ 2nd (Disk)	**Code 14th (Operation Temperature)**
DE:Embedded Disk	C：Standard Grade (0 ~ +70 ℃)
	W：Industrial Grade (-40 ~ +85 ℃)
Code 3rd ~ 5th (Form Factor)	
E4%：EDC, 44P Horizontal Type,	**Code 15th (Internal Control)**
%= A~F (Horizontal type),H (Vertical type)	1: default setting
Code 7th ~9th (Capacity)	**Code 16th (Channel of data transfer)**
08G：8GB	S: Single Channel
16G：16GB	D: Dual Channel
32G：32GB	
64G: 64GB	**Code 17th (Flash Type)**
A28: 128GB	C: Toshiba MLC
B56: 256GB	
	Code 19th (Customized Code/Internal Code)
	4: Preformat, Fixed Mode + PIO Mode 4
Code 10th ~ 12th (Controller)	5: Pre-formatted+ UltraDMA 4
D53：ID202	7: Fixed Mode + PIO Mode 4
	8: Fixed Mode + MwDMA Mode 2
Code 13th (Flash Mode)	
B: Toshiba 15nm MLC	

9 Appendix(CE/FCC/RoHS/REACH)

Certificate

Issue Date: September 11, 2014
Ref. Report No. ISL-14LE382CE

Product Name	:	EDC 1ME 44pin Horizontal
Model(s)	:	DEE4@-XXXD53*#%※&
Brand	:	Innodisk
Responsible Party	:	Innodisk Corporation
Address	:	5F.No.237, Sec. 1, Datong Rd., Xizhi Dist., New Taipei City 221, Taiwan (R.O.C.)

We, **International Standards Laboratory**, hereby certify that:

The device bearing the trade name and model specified above has been shown to comply with the applicable technical standards as indicated in the measurement report and was tested in accordance with the measurement procedures specified in European Council Directive- EMC Directive 2004/108/EC. The device was passed the test performed according to :

CE

Standards:

EN 55022: 2010+AC2011 and CISPR 22: 2008 (modified)
EN 61000-3-2: 2006+A1:2009 +A2:2009 and IEC 61000-3-2: 2005+A1:2008 +A2:2009
EN 61000-3-3: 2013 and IEC 61000-3-3: 2013
EN 55024: 2010 and CISPR 24: 2010
EN 61000-4-2: 2009 and IEC 61000-4-2: 2008
EN 61000-4-3: 2006+A1: 2008 +A2: 2010 and
IEC 61000-4-3:2006+A1: 2007+A2: 2010
EN 61000-4-4: 2004 +A1:2010 and IEC 61000-4-4: 2004 +A1:2010

I attest to the accuracy of data and all measurements reported herein were performed by me or were made under my supervision and are correct to the best of my knowledge and belief. I assume full responsibility for the completeness of these measurements and vouch for the qualifications of all persons taking them.

International Standards Laboratory

Jim Chu / Director

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Nemko ELA113A

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Nemko ELA113B

Certificate

Issue Date: September 11, 2014
Ref. Report No. ISL-14LE382FB

Product Name	:	EDC 1ME 44pin Horizontal
Model(s)	:	DEE4@-XXXD53*#%※&
Brand	:	Innodisk
Applicant	:	Innodisk Corporation
Address	:	5F.No.237, Sec. 1, Datong Rd., Xizhi Dist., New Taipei City 221, Taiwan (R.O.C.)

We, **International Standards Laboratory**, hereby certify that:

The device bearing the trade name and model specified above has been shown to comply with the applicable technical standards as indicated in the measurement report and was tested in accordance with the measurement procedures specified. (refer to Test Report if any modifications were made for compliance).

Standards:

FCC CFR Title 47 Part 15 Subpart B: 2012- Section 15.107 and 15.109
ANSI C63.4-2009
Industry Canada Interference-Causing Equipment Standard ICES-003 Issue 5: 2012

Class B

I attest to the accuracy of data and all measurements reported herein were performed by me or were made under my supervision and are correct to the best of my knowledge and belief. I assume full responsibility for the completeness of these measurements and vouch for the qualifications of all persons taking them.

International Standards Laboratory

Jim Chu / Director

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宜鼎國際股份有限公司
Innodisk Corporation
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RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
鉛（Pb）	< 1000 ppm
汞（Hg）	< 1000 ppm
鎘（Cd）	< 100 ppm
六價鉻（Cr 6+）	< 1000 ppm
多溴聯苯（PBBs）	< 1000 ppm
多溴二苯醚（PBDEs）	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2016 / 08 / 04

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

REACH Declaration of Conformity

Manufacturer Product: All Innodisk EM Flash and Dram products

1.宜鼎國際股份有限公司（以下稱本公司）特此保證此售予貴公司之產品，皆符合歐盟化學品法案(Registration , Evaluation and Authorization of Chemicals：REACH)之規定(http://www.echa.europa.eu/de/candidate-list-table **last updated: 20/06/2016**)。所提供之產品包含：(1) 產品或產品所使用到的所有原物料；(2)包裝材料；(3)設計、生產及重工過程中所使用到的所有原物料。

We Innodisk Corporation hereby declare that our products are in compliance with the requirements according to the REACH Regulation (http://www.echa.europa.eu/de/candidate-list-table **last updated: 20/06/2016**).
Products include： 1) Product and raw material used by the product； 2) Packaging material ：3) Raw material used in the process of design, production and rework

2.本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

InnoDisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

立 保 證 書 人 (Guarantor)

Company name 公司名稱： InnoDisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2016 / 06 / 23