Approval Sheet

Customer	
Product Number	**M4R0-4GSSCCRG**
Module speed	**PC4-2133**
Pin	**288pin**
Cl-tRCD-tRP	**15-15-15**
SDRAM Operating Temp	**0℃~85℃**
Date	**1st September 2016**

Approval by Customer

P/N:
Signature:
Date:

Sales: **Sr. Technical Manager: John Hsieh**

Rev 1.0

1. Features

- 288-pin Registered Dual Inline Memory Module (RDIMM)
- Organization: 512Mx72 based on 512Mx8(4Gb) * 9 components / 1 Rank
- CL-tRCD-tRP : 15-15-15
- JEDEC standard 1.2V (± 0.06V) Power Supply
- VDDQ = 1.2V (± 0.06V)
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10,11,12,13,14,15,16,17,18
- Burst Length: 8(Interleave/nibble sequential)
- Bi-directional Differential Data-Strobe
- On Die Termination (ODT)
- Average Refresh Period 7.8us at lower than a T_{CASE} 85°C, 3.9us at 85°C < TCASE < 95 °C
- RoHS Compliant
- Asynchronous Reset
- PCB Height 18.75mm

2. Address Configuration

Module Organization	Row address	Column Address	Bank Group Address	Bank Address	Auto Precharge
512Mx72	A0-A14	A0-A9	BG0-BG1	BA0-BA1	A10/AP

3. Pin Description

Pin Name	Description	Pin Name	Description
A0-A17	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0-SA2	I2C slave address select for SPD/TS and register
RAS_n	Register row address strobe input	PAR	Register parity input
CAS_n	Register column address strobe input	VDD	SDRAM core power supply
WE_n	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input activate input	ALERT_n	Register ALERT_n output
DQ0-DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0-CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t-DQS17_t	Data buffer data strobes (positive)	VTT	SDRAM I/O termination supply
DQS0_c-DQS17_c	Data buffer data strobes (negative)	RFU	Reserved for future use
CK0_t,CK1_t	Register clock input (positive)		
CK0_c, CK1_c	Register clock input (negative)		

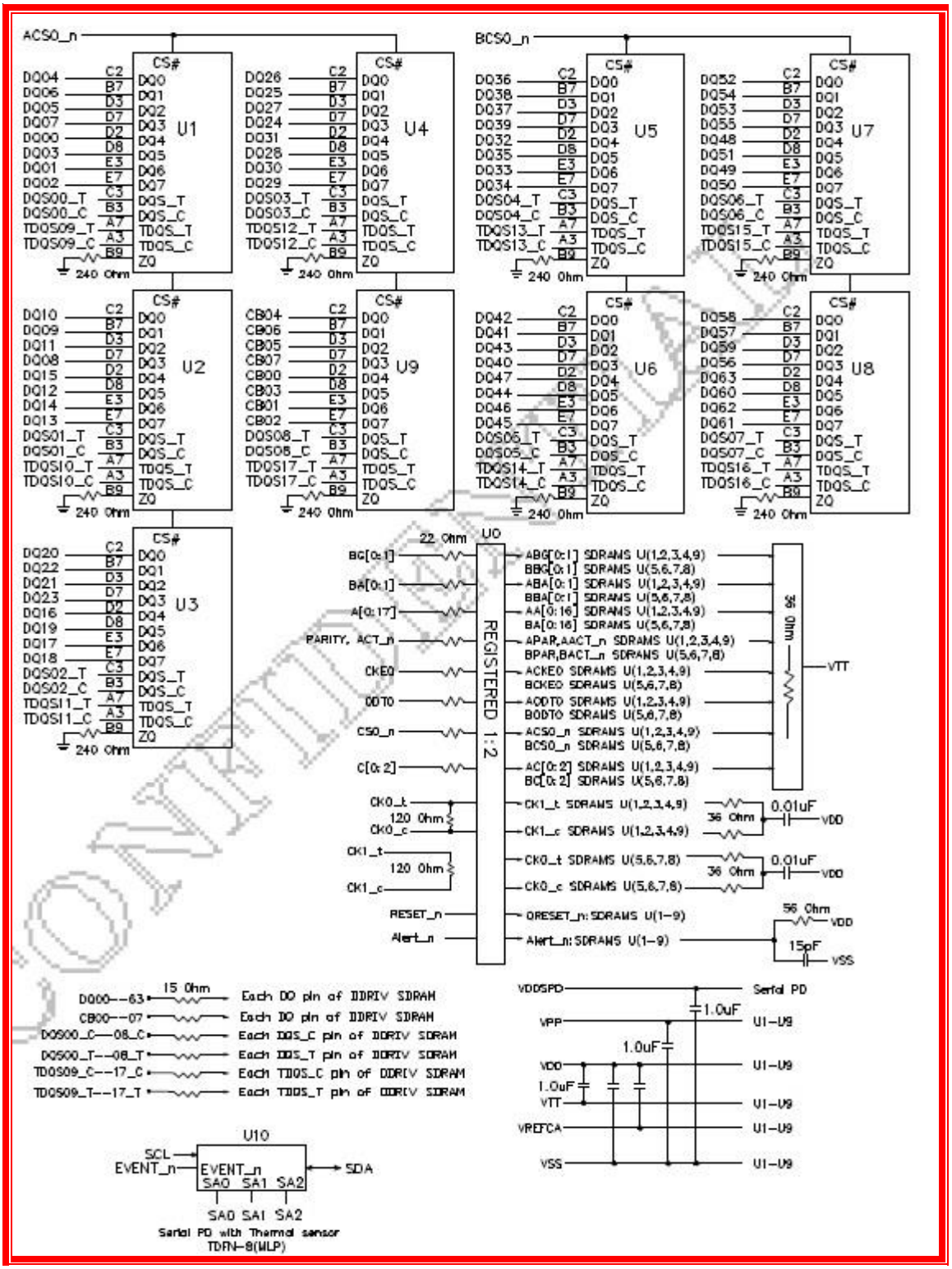
4. Pin Configuration (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	12V[3],NC	145	12V[3],NC	40	TDQS12_t, DQS12_t	184	VSS	78	EVENT_n	222	PARITY	117	DQ52	261	VSS
2	VSS	146	VREFCA	41	TDQS12_c, DQS12_c	185	DQS3_c	79	A0	223	VDD	118	VSS	262	DQ53
3	DQ4	147	VSS	42	VSS	186	DQS3_t	80	VDD	224	BA1	119	DQ48	263	VSS
4	VSS	148	DQ5	43	DQ30	187	VSS	81	BA0	225	A10/AP	120	VSS	264	DQ49
5	DQ0	149	VSS	44	VSS	188	DQ31	82	RAS_n/A16	226	VDD	121	TDQS15_t, DQS15_t	265	VSS
6	VSS	150	DQ1	45	DQ26	189	VSS	83	VDD	227	RFU	122	TDQS15_c, DQS15_c	266	DQS6_c
7	TDQS9_t, DQS9_t	151	VSS	46	VSS	190	DQ27	84	S0_n	228	WE_n/A14	123	VSS	267	DQS6_t
8	TDQS9_c, DQS9_c	152	DQS0_c	47	CB4	191	VSS	85	VDD	229	VDD	124	DQ54	268	VSS
9	VSS	153	DQS0_t	48	VSS	192	CB5	86	CAS_n/A15	230	NC	125	VSS	269	DQ55
10	DQ6	154	VSS	49	CB0	193	VSS	87	ODT0	231	VDD	126	DQ50	270	VSS
11	VSS	155	DQ7	50	VSS	194	CB1	88	VDD	232	A13	127	VSS	271	DQ51
12	DQ2	156	VSS	51	TDQS17_t, DQS17_t	195	VSS	89	S1_n	233	VDD	128	DQ60	272	VSS
13	VSS	157	DQ3	52	TDQS17_c, DQS17_c	196	DQS8_c	90	VDD	234	A17	129	VSS	273	DQ61
14	DQ12	158	VSS	53	VSS	197	DQS8_t	91	ODT1	235	NC,C2	130	DQ56	274	VSS
15	VSS	159	DQ13	54	CB6	198	VSS	92	VDD	236	VDD	131	VSS	275	DQ57
16	DQ8	160	VSS	55	VSS	199	CB7	93	C0,CS2_n,NC	237	NC,CS3_c,C1	132	TDQS16_t, DQS16_t	276	VSS
17	VSS	161	DQ9	56	CB2	200	VSS	94	VSS	238	SA2	133	TDQS16_c, DQS16_c	277	DQS7_c
18	TDQS10_t, DQS10_t	162	VSS	57	VSS	201	CB3	95	DQ36	239	VSS	134	VSS	278	DQS7_t
19	TDQS10_c, DQS10_c	163	DQS1_c	58	RESET_n	202	VSS	96	VSS	240	DQ37	135	DQ62	279	VSS
20	VSS	164	DQS1_t	59	VDD	203	CKE1	97	DQ32	241	VSS	136	VSS	280	DQ63
21	DQ14	165	VSS	60	CKE0	204	VDD	98	VSS	242	DQ33	137	DQ58	281	VSS
22	VSS	166	DQ15	61	VDD	205	RFU	99	TDQS13_t, DQS13_t	243	VSS	138	VSS	282	DQ59
23	DQ10	167	VSS	62	ACT_n	206	VDD	100	TDQS13_c, DQS13_c	244	DQS4_c	139	SA0	283	VSS
24	VSS	168	DQ11	63	BG0	207	BG1	101	VSS	245	DQS4_t	140	SA1	284	VDDSPD
25	DQ20	169	VSS	64	VDD	208	ALERT_n	102	DQ38	246	VSS	141	SCL	285	SDA
26	VSS	170	DQ21	65	A12/BC_n	209	VDD	103	VSS	247	DQ39	142	VPP	286	VPP
27	DQ16	171	VSS	66	A9	210	A11	104	DQ34	248	VSS	143	VPP	287	VPP
28	VSS	172	DQ17	67	VDD	211	A7	105	VSS	249	DQ35	144	RFU	288	VPP[4]
29	TDQS11_t, DQS11_t	173	VSS	68	A8	212	VDD	106	DQ44	250	VSS				
30	TDQS11_c, DQS11_c	174	DQS2_c	69	A6	213	A5	107	VSS	251	DQ45				
31	VSS	175	DQS2_t	70	VDD	214	A4	108	DQ40	252	VSS				
32	DQ22	176	VSS	71	A3	215	VDD	109	VSS	253	DQ41				
33	VSS	177	DQ23	72	A1	216	A2	110	TDQS14_t, DQS14_t	254	VSS				
34	DQ18	178	VSS	73	VDD	217	VDD	111	TDQS14_c, DQS14_c	255	DQS5_c				
35	VSS	179	DQ19	74	CK0_t	218	CK1_t	112	VSS	256	DQS5_t				
36	DQ28	180	VSS	75	CK0_c	219	CK1_c	113	DQ46	257	VSS				
37	VSS	181	DQ29	76	VDD	220	VDD	114	VSS	258	DQ47				
38	DQ24	182	VSS	77	VTT	221	VTT	115	DQ42	259	VSS				
39	VSS	183	DQ25	KEY				116	VSS	260	DQ43				

Ordering Information

DDR4 VLP RDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M4R0-4GSSCCRG	4GB	PC4-2133	512Mx72	9	1	Y

5. Block Diagram



6. IDD Specification Parameter

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions	Value	Units
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	270	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	288	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	360	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	387	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	135	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	162	mA
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	144	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	99	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	135	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	108	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	135	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	90	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	117	mA

IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	243	mA
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	252	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	117	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	756	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	783	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	783	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	648	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	684	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	648	mA
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	594	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	702	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1710	mA

IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	1440	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	1080	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	117	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	180	mA
IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - TBD (~35-45)°C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	90	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;Partial Array Self-Refresh (PASR): Full Array; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	117	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1314	mA
IDD8	Maximum Power Down Current	58.5	mA

7. Absolute Maximum DC ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA to Vss	-0.3 ~ 1.5	V	1
T_{STG}	Storage Temperature	-55 to +100	^{0}C	1,2

NOTE :
1. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

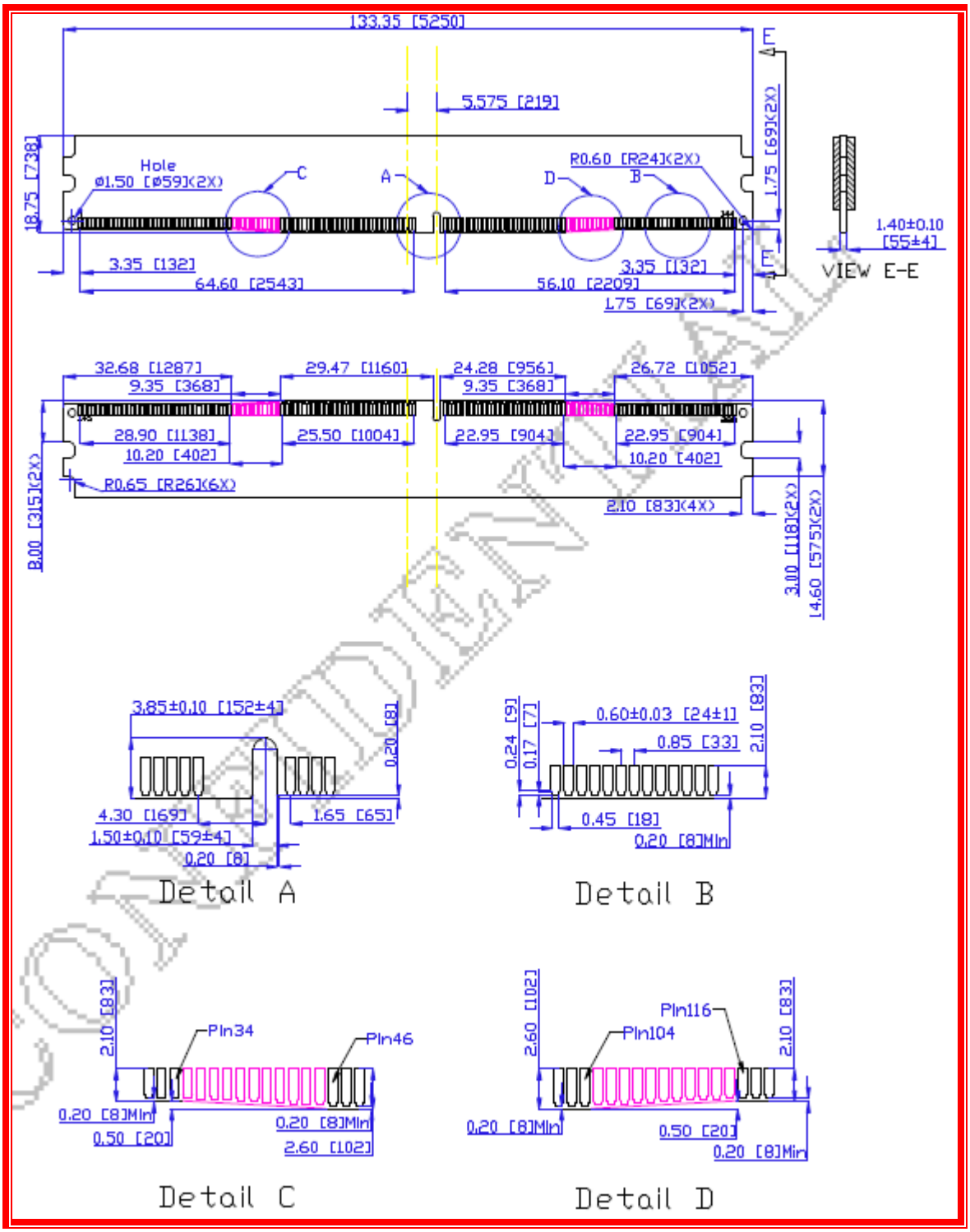
8. AC and DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1,2,3
V_{DDQ}	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
V_{PP}		2.375	2.5	2.75	V	3

NOTE:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

9. Physical Dimension (drawing not in scale) Units : in Millimeters



10. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI（Cr+6）	< 1000 ppm
Polybromodiphenyl ether（PBDE）	< 1000 ppm
Polybrominated Biphenyls（PBB）	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Richard Lee 李鐘亮

Company Representative Title 公司代表人職稱： CEO 執行長

Date 日期： 2014 / 07 / 29

(Company Stamp/公司大小章)

Revision Log

Rev	Date	Modification
0.1	1st September 2016	Preliminary Edition
1.0	1st September 2016	Official Released