MI982

Intel® H81 Based Mini-ITX board

Mini ITX Motherboard

USER'S MANUAL

Version 1.0

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Introduction

Product Description

The MI982 Mini ITX motherboard is based on the latest Intel® H81 chipset. The platform supports Intel® 4th Generation Core™ DT i7/i5/i3 processors. The latest Intel® processors provide advanced performance in both computing and graphics quality. This meets the requirement of customers in the gaming, POS, digital signage and server market segment.

The platform supports two SO-DIMM sockets that can accommodate up to 16GB of DDR3-1600 Non ECC memory. The Intel® 4th Gen. Core™ DT processor integrated HD graphics supports 3 independent displays, Direct X 11.1, OpenGL 3.2, and Open CL 1.2. Display interfaces are for HDMI, DisplayPort and VGA CRT.

With two Gigabit Ethernets, the MI982 Mini ITX board utilizes the dramatic increase in performance provided Intel's latest cutting-edge technology. Expansion is provided by PCIe(16x), one full sized MiniPCIe and a half sized MiniPCIe. Onboard connectors support 4x SATA III, 4x or 6x USB 2.0 depending on the MI982 model and 6x COM ports. The board measures 170mm x 170mm.

Checklist

Your MI982 package should include the items listed below.

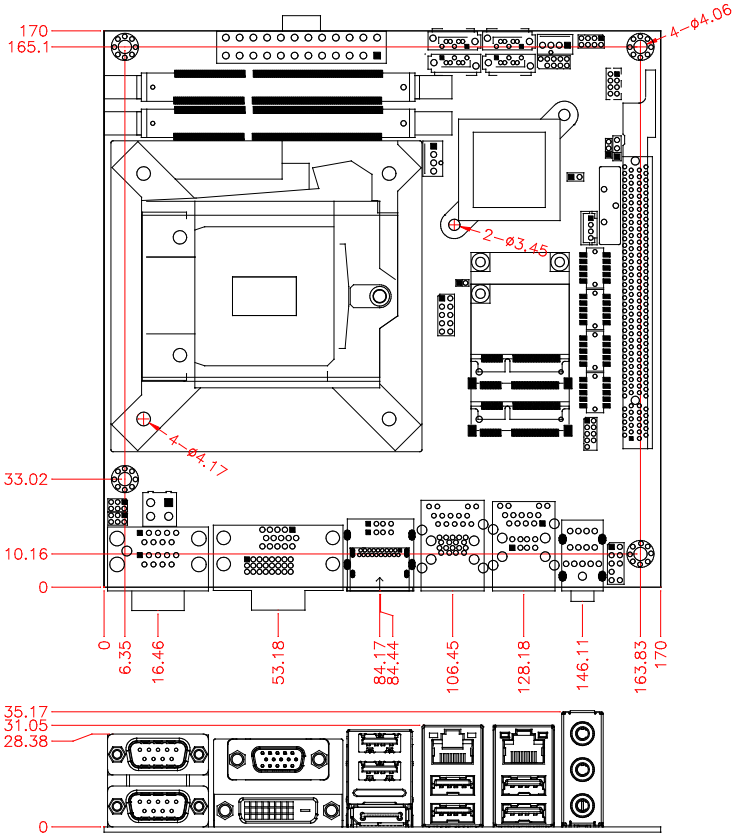
- The MI982 MINI ITX motherboard
- This User's Manual
- 1 CD containing chipset drivers and flash memory utility

MI982 Specifications

Model Name	MI982EF
Form Factor	Mini ITX
CPU Type	- Haswell Refresh 4th Generation Intel® Core™ i7/i5/i3/Pentium DT processor & FCLGA1150 package [37.5 mm x 37.5mm] - TDP: 35W ~ 84W
CPU Speed	Up to 4.0GHz
Cache Size	Up to 8MB
CPU Socket	LGA1150 (Socket H3)
Chipset	Intel® H81 PCH Package =23 mm x 22 mm, 0.65 mm ball pitch
BIOS	AMI BIOS
Memory	Haswell Refresh 4th Generation Intel® Core™ DT processors integrated memory controller, - DDR3-1600 MHz@1.5V - SO-DIMM x 2, Max. **16**GB (Non-ECC)
VGA	Haswell Refresh 4th Generation Intel® DT processor integrated HD Gfx, supports 3 independent displays, Direct X 11.1, OpenGL 3.2, Open CL 1.2 - DVI-D x 1 (Thru port C, with level shifter ASM1442K) - DisplayPort x 1 (Thru port D) - VGA x 1 (Thru PCH)
LAN	1. Intel® I217LM PHY GbE 2. Intel® I211AT PCIe GbE as 2nd LAN
USB	USB 2.0 host controller [H81 Integrated], support 8 ports - 4 ports via the rear panel I/O - 2 ports via MiniPCIe socket - 2 ports via pin-header USB 3.0 host controller [H81 Integrated], support 2 ports - 2 ports via the rear panel I/O
Serial ATA	Intel® H81 PCH built-in SATA controller, support 4 ports - 2 x SATA III (6Gbps) + 2 x SATA II (3Gbps)
Audio	Intel® H81 PCH built-in High Definition Audio controller + Realtek ALC892 w/ 7.1 channels
LPC I/O	Fintek **F81866AD-I** (128-pin LQFP [14mm x 14 mm]) - COM #1 (RS232/422/485) support ring-in with power @500 mA (selectable for 5V or 12V) [EXAR SP339EER1 232/422/485 transceiver x 1 for jumper-less] - COM #2~COM #6 (RS232 only) Hardware Monitor (2 thermal inputs,4 voltage monitor inputs & 2 Fan headers) - CPU FAN x 1(PWN Fan type, 4-pin connector) - SYS fan x 1(PWM Fan type, 4-pin connector)]
Digital IO	4 in & 4 out

Expansion Slots	- PCI-Express (16x) x1 [Gen 2.0 PEG] - Mini PCI-Express x 2 port [1 x Full-sized,1 x Half-sized] , both support USB 2.0 signal
Edge Connectors	Dual DB9 stack connector for COM #1 / #2 VGA + DVI-D stack connector x1 DisplayPort + dual USB (2.0) stack connector x1 RJ-45 + dual USB (3.0) stack connector x1 RJ-45 + dual USB (2.0) stack connector x1 Triplet type Jack 3x1 for Audio port [Line-in / Line-out / Mic-in]
Onboard Header/Connector	2 ports x SATA **III** [Blue color] 2 ports x SATA **II** DF-11 2x4 header x 1 for 2 ports USB 2.0 DF-11 2x5 box header x 4 for COM 3/4/5/6 (RS232 only) 2x5 header for Digital IO 2x5 header for front Audio 2x4 header for front panel I/O (2.54 pitch) 2x2 pin ATX power connector x1 1x ATX standard 24-pin type for power connector
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec/min)
System Voltage	ATX standard 24-pins type 4 pin type (+12V only)
Other	- LAN Wakeup - EuP/ErP - iSMART 3.0
Environment	Operation Temperature: 0~60 degree C Storage Temperature: -20~80 degree C Relative humidity: 0~90%, non-condensing
Board Size	170mm x 170mm
Operation System	Windows 7, Windows 8, Linux

Board Dimensions



Installations

This section provides information on how to use the jumpers and connectors on the MI982 in order to set up a workable system. The topics covered are:

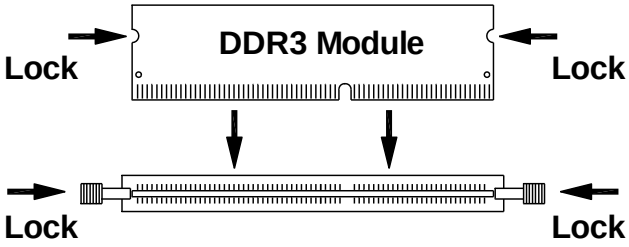
Installing the Memory

The MI982 board supports two DDR3 memory modules for a maximum total of 16GB in DDR3 SODIMM memory type.

Installing and Removing Memory Modules

To install the DDR3 modules, locate the memory slot on the board and perform the following steps:

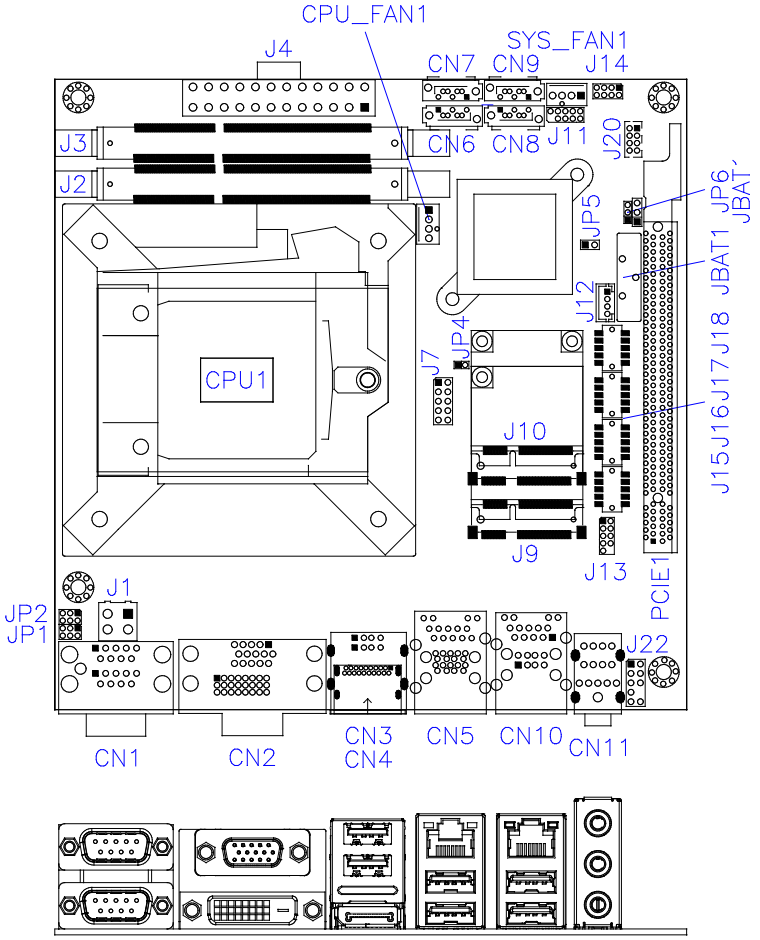
1. Hold the DDR3 module so that the key of the DDR3 module aligned with that on the memory slot.
2. Gently push the DDR3 module in an upright position until the clips of the slot close to hold the DDR3 module in place when the DDR3 module touches the bottom of the slot.
3. To remove the DDR3 module, press the clips with both hands.



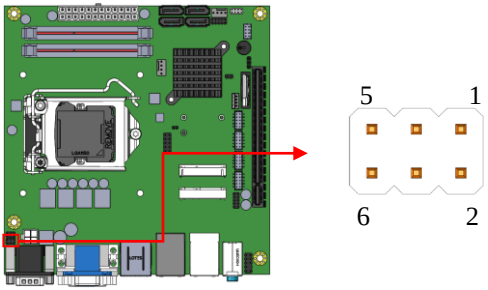
Setting the Jumpers

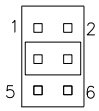
Jumpers are used on MI982 to select various settings and features according to your needs and applications. Contact your supplier if you have doubts about the best configuration for your needs. The following lists the connectors on MI982 and their respective functions.

Jumper Locations on MI982

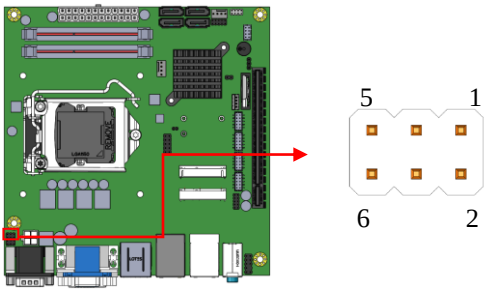


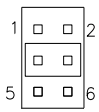
JP1: COM2 RS232 RI/+5V/+12V Power Setting



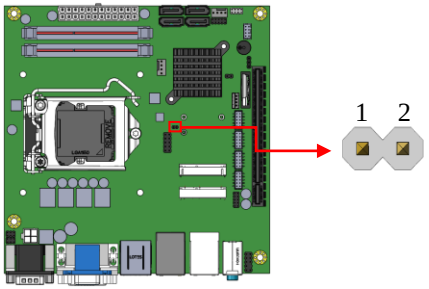
JP1	Setting	Function
	Pin 1-3 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 3-5 Short/Closed	+5V

JP2: COM1 RS232 RI/+5V/+12V Power Setting



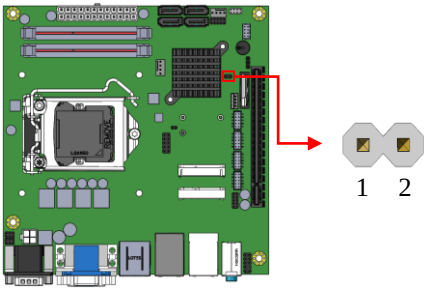
JP2	Setting	Function
	Pin 1-3 Short/Closed	+12V
	Pin 3-4 Short/Closed	RI
	Pin 3-5 Short/Closed	+5V

JP4: Power Good Selection



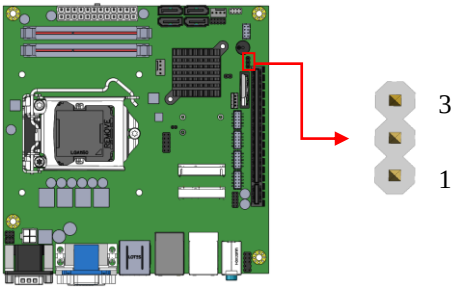
JP4	Function
Short	Factory use only
Open	Normal

JP5: Flash Descriptor Security Override (Factory use only)



JP5	Flash Descriptor Security Override
Open	Disabled (Default)
Close	Enabled

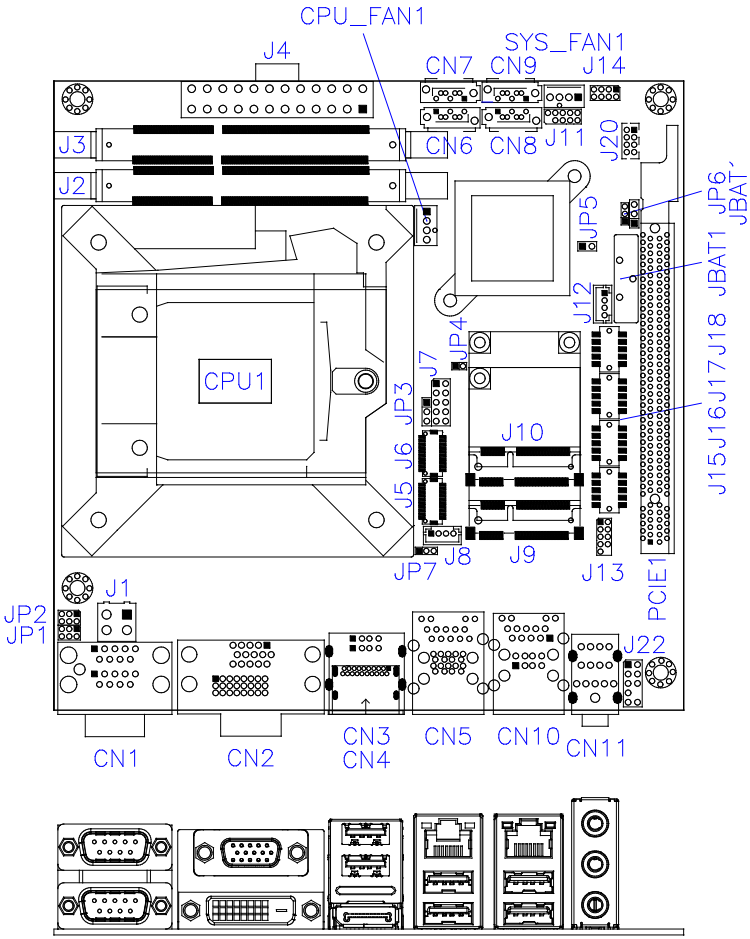
JBAT1: Clear CMOS Contents



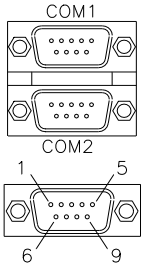
JBAT1	Setting	Function
	Pin 1-2 Short/Closed	Normal
	Pin 2-3 Short/Closed	Clear CMOS

Connectors on MI982

Connector Locations on MI982

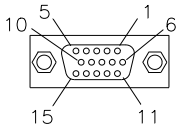


CN1: COM1 and COM2 Serial Ports



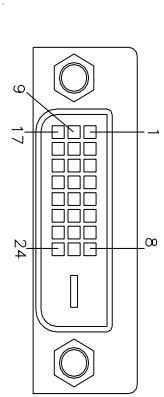
Pin #	Signal Name		
	RS-232	R2-422	RS-485
1	DCD	TX-	DATA-
2	RX	TX+	DATA+
3	TX	RX+	NC
4	DTR	RX-	NC
5	Ground	Ground	Ground
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC
10	NC	NC	NC

CN2: VGA and DVI-D Connector



VGA

Signal Name	Pin #	Pin #	Signal Name
Red	1	2	Green
Blue	3	4	N.C.
GND	5	6	GND
GND	7	8	GND
N.C.	9	10	GND
N.C.	11	12	DDCDATA
HSYNC	13	14	VSYNC
DDCCLK	15		



Signal Name	Pin #	Pin #	Signal Name
DATA 2-	1	16	HOT POWER
DATA 2+	2	17	DATA 0-
GROUND	3	18	DATA 0+
N.C.	4	19	GROUND
N.C.	5	20	N.C.
DDC CLOCK	6	21	N.C.
DDC DATA	7	22	GROUND
N.C	8	23	CLOCK +
DATA 1-	9	24	CLOCK -
DATA 1+	10		
GROUND	11		
N.C.	12		
N.C.	13		
DDC POWER	14		
GROUND	15		

CN3: USB2.0 Connector

CN4: DP Connector

CN5: Gigabit LAN (Intel I217LM) / USB3.0

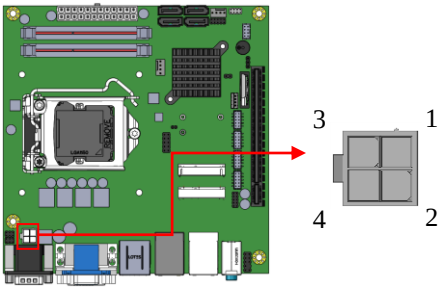
CN6, CN7: SATA3 Connectors

CN8, CN9: SATA2 Connectors

CN10: Gigabit LAN (Intel I211AT) / USB2.0

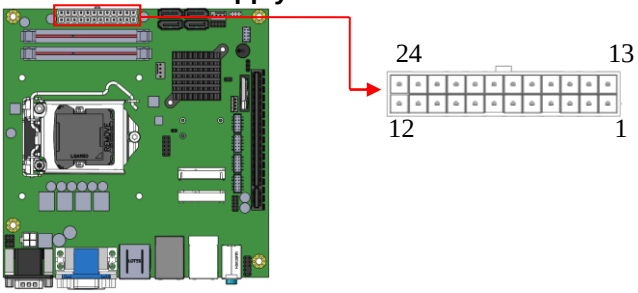
CN11: HD Audio Connector

J1: ATX 12V Power Connector



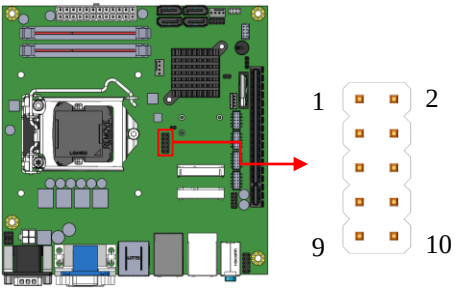
Pin #	Signal Name
1	Ground
2	Ground
3	+12V
4	+12V

J4: ATX Power Supply Connector



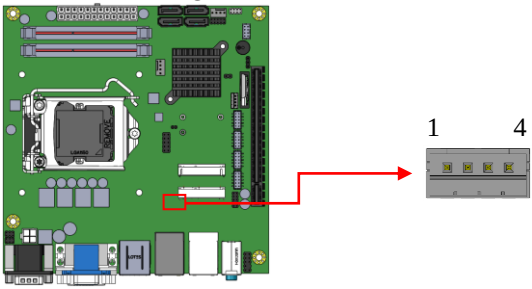
Signal Name	Pin #	Pin #	Signal Name
3.3V	13	1	3.3V
-12V	14	2	3.3V
Ground	15	3	Ground
PS-ON	16	4	+5V
Ground	17	5	Ground
Ground	18	6	+5V
Ground	19	7	Ground
-5V	20	8	Power good
+5V	21	9	5VSB
+5V	22	10	+12V
+5V	23	11	+12V
Ground	24	12	+3.3V

J7: Digital I/O



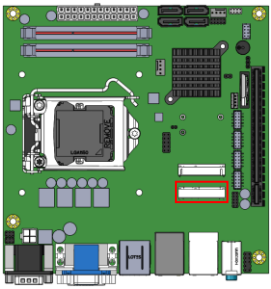
Signal Name	Pin	Pin	Signal Name
GND	1	2	VCC
OUT3	3	4	OUT1
OUT2	5	6	OUT0
IN3	7	8	IN1
IN2	9	10	IN0

J8: LCD Backlight Connector

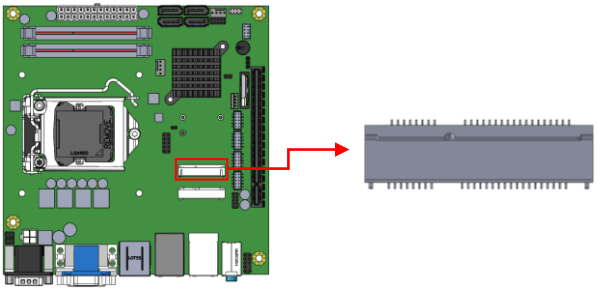


Pin #	Signal Name
1	Backlight Power
2	Backlight Enable
3	Brightness Control
4	Ground

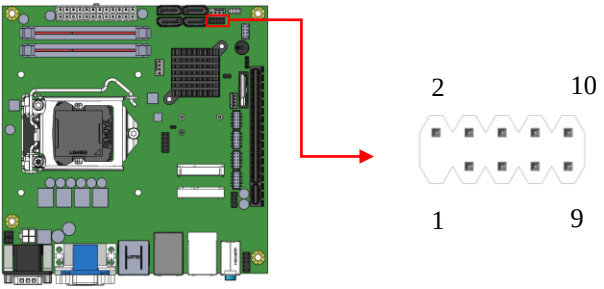
J9: Mini PCIE Connector



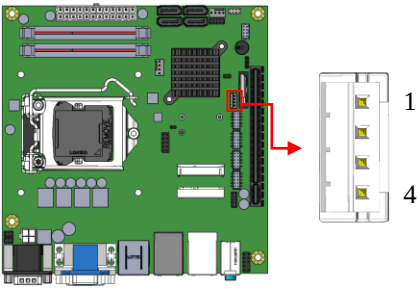
J10: Mini PCIE Connector



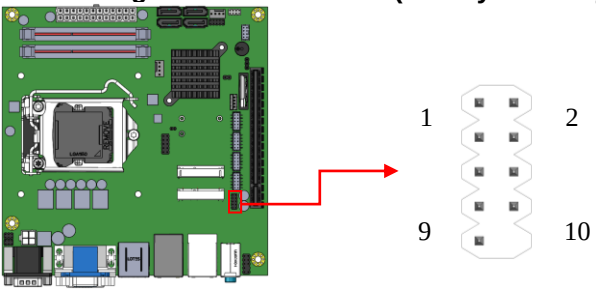
J11: SPI Flash Connector (Factory use only)



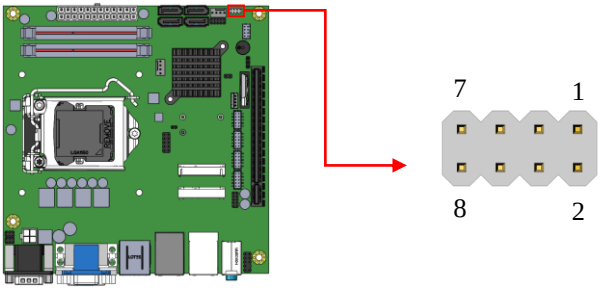
J12: MCU Flash Connector (factory use only)



J13: Debug 80 Port Connector (factory use only)



J14: Front Panel Function Connector



ATX Power ON Switch: Pins 1 and 2
This 2-pin connector is an "ATX Power Supply On/Off Switch" on the system that connects to the power switch on the case. When pressed, the power switch will force the system to power on. When pressed again, it will force the system to power off.

Hard Disk Drive LED Connector: Pins 3 and 4
This connector connects to the hard drive activity LED on control panel. This LED will flash when the HDD is being accessed.

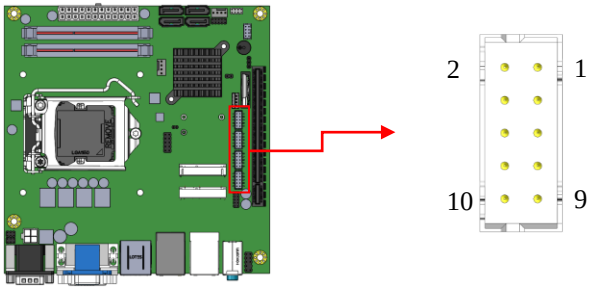
Pin #	Signal Name
4	HDD Active
3	3.3V

Reset Switch: Pins 5 and 6
The reset switch allows the user to reset the system without turning the main power switch off and then on again. Orientation is not required when making a connection to this header.

Power LED: Pins 7 and 8

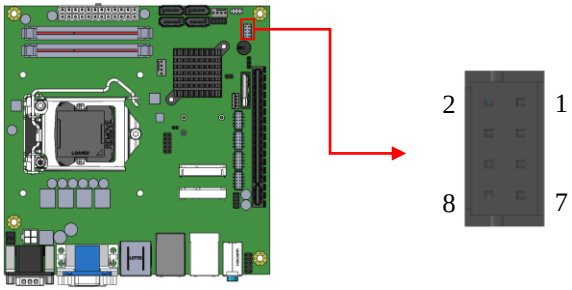
Pin #	Signal Name
7	+5V
8	GND

J15, J16, J17, J18: COM3/COM4/COM5/COM6 Connector



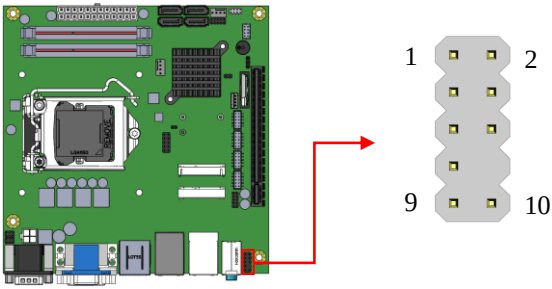
Signal Name	Pin #	Pin #	Signal Name
DCD, Data carrier detect	1	2	RXD, Receive data
TXD, Transmit data	3	4	DTR, Data terminal ready
GND, ground	5	6	DSR, Data set ready
RTS, Request to send	7	8	CTS, Clear to send
RI, Ring indicator	9	10	Not Used

J20: USB Connectors



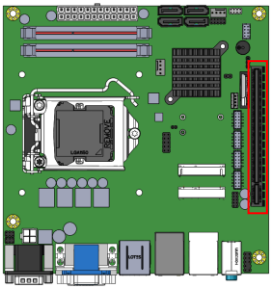
Signal Name	Pin	Pin	Signal Name
VCC	1	2	GND
D0-	3	4	D1+
D0+	5	6	D1-
GND	7	8	VCC

J22: Audio Front Header

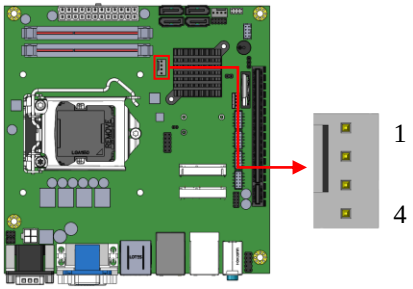


Signal Name	Pin #	Pin #	Signal Name
MIC2_L	1	2	Ground
MIC2_R	3	4	Presence#
Line2_R	5	6	MIC2_ID
Sense	7	8	NC
Line2_L	9	10	Line2_ID

PCIE1: PCI-E X16 Slot

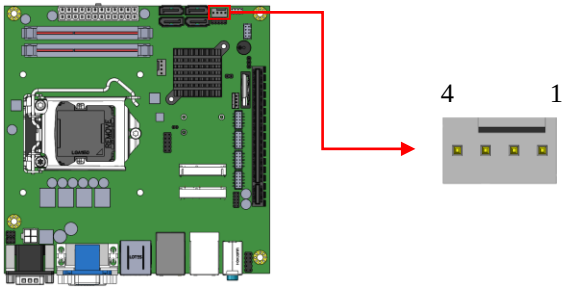


CPU_FAN1: CPU Fan Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Control

SYS_FAN1: System Fan1 Power Connector



Pin #	Signal Name
1	Ground
2	+12V
3	Rotation detection
4	Control

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BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

BIOS Introduction

The BIOS (Basic Input/Output System) installed in your computer system's ROM supports Intel processors. The BIOS provides critical low-level support for a standard device such as disk drives, serial ports and parallel ports. It also has password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Pressing the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup. If you still wish to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again. The following message will appear on the screen:

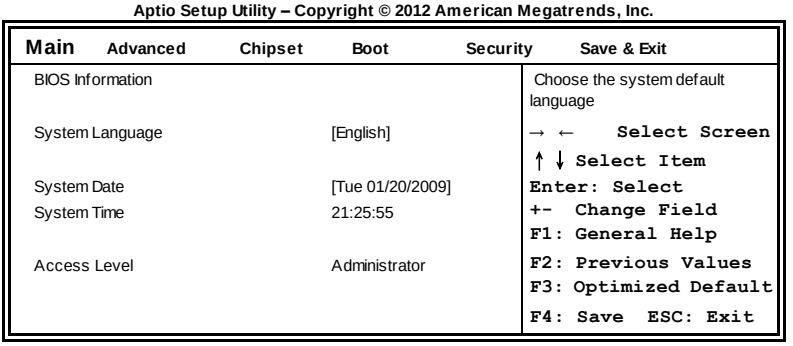
```
Press  <DEL>  to  Enter  Setup
```

In general, you press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help and <Esc> to quit.

When you enter the Setup utility, the Main Menu screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: *It is strongly recommended that you avoid making any changes to the chipset defaults. These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could cause the system to become unstable and crash in some cases.*

Main Settings

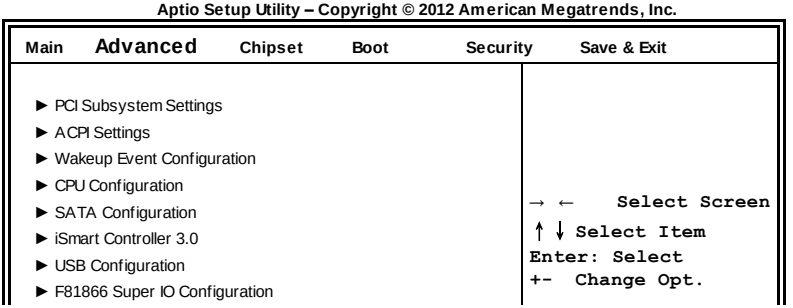


System Language
Choose the system default language.

System Date
Set the Date. Use Tab to switch between Date elements.

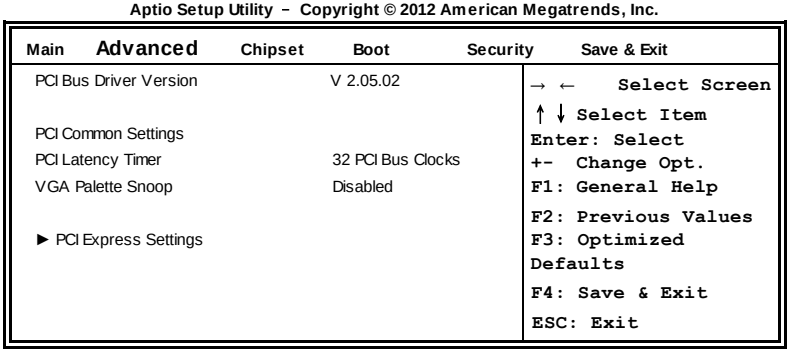
System Time
Set the Time. Use Tab to switch between Time elements.

Advanced Settings
This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



► F81866 H/W Monitor	F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

PCI Subsystem Settings



PCI Latency Timer

Value to be programmed into PCI Latency Timer Register.

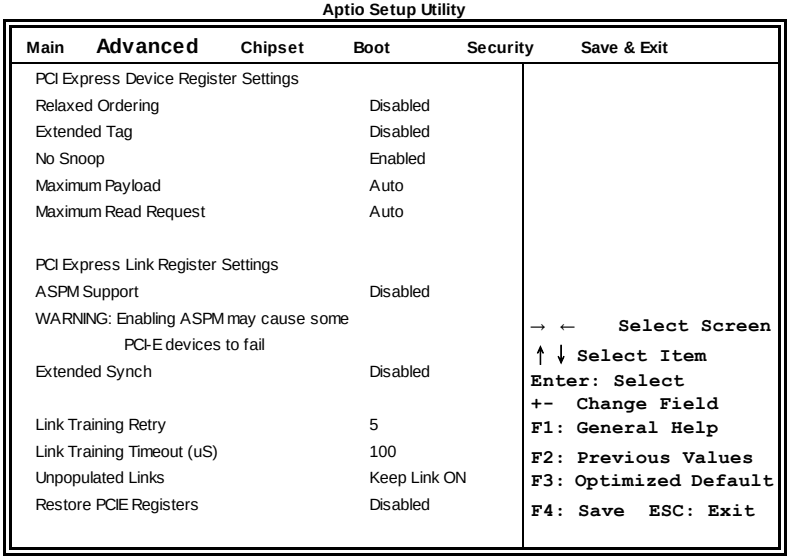
VGA Palette Snoop

Enables or disables VGA Palette Registers Snooping.

PCI Express Settings

Change PCI Express devices settings.

PCI Express Settings



Relaxed Ordering
Enables or disables PCI Express Device Relaxed Ordering.

Extended Tag
If ENABLED allows device to use 8-bit Tag field as a requester.

No Snoop
Enables or disables PCI Express Device No Snoop option.

Maximum Payload
Set Maximum Payload of PCI Express Device or allow System BIOS to select the value.

Maximum Read Request
Set Maximum Read Request Size of PCI Express Device or allow System BIOS to select the value.

ASPM Support
Set the ASPM Level: Force L0s – Force all links to L0s State: AUTO – BIOS auto configure: DISABLE – Disables ASPM.

Extended Synch
If ENABLED allows generation of Extended Synchronization patterns.

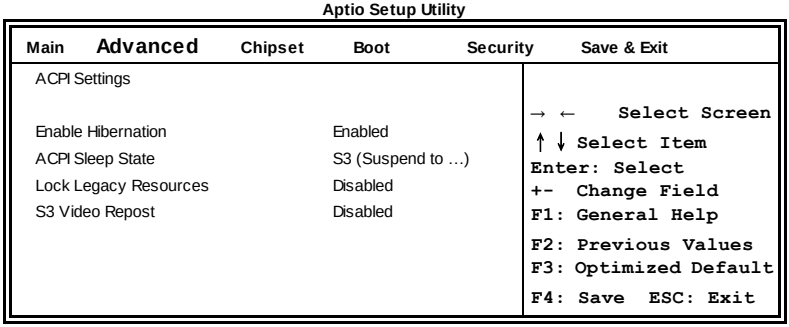
Link Training Retry
Defines number of Retry Attempts software will take to retrain the link if previous training attempt was unsuccessful.

Link Training Timeout (uS)
Defines number of Microseconds software will wait before polling 'Link Training' bit in Link Status register. Value range from 10 to 1000 uS.

Unpopulated Links
In order to save power, software will disable unpopulated PCI Express links, if this option set to 'Disable Link'.

Restore PCIE Registers
On non-PCI Express aware OS's (Pre Windows Vista) some devices may not be correctly reinitialized after S3.Enabling this restore PCI Express device configuration on S3 resume
Warning: Enabling this may cause issues with other hardware after S3 resume.

ACPI Settings



Enable Hibernation

Enables or Disables System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.

ACPI Sleep State

Select ACPI sleep state the system will enter, when the *SUSPEND* button is pressed.

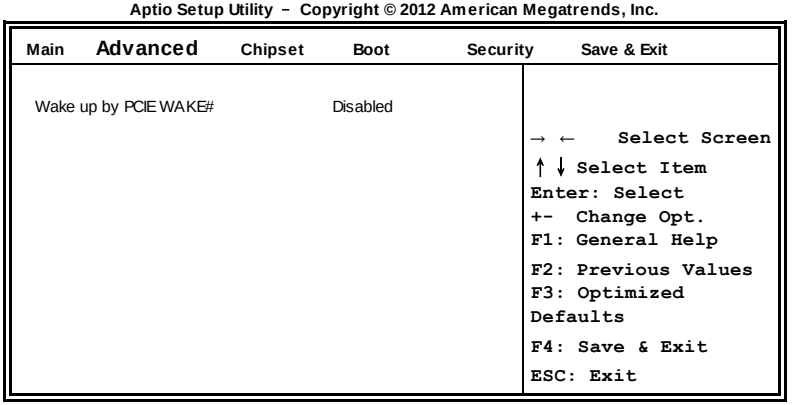
Lock Legacy Resources

Enabled or Disabled Lock of Legacy Resources.

S3 Video Repost

Enable or disable S3 Video Repost.

Wakeup Event Configuration

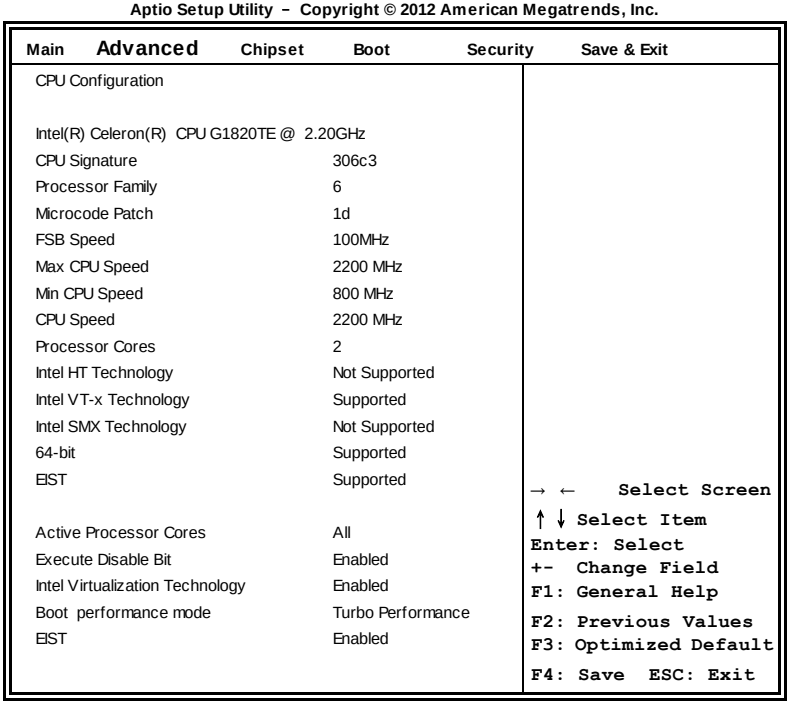


Wake up by PCIE WAKE#

The options are Disabled and Enabled.

CPU Configuration

This section shows the CPU configuration parameters.



Active Processor Cores

Number of cores to enable in each processor package.

Execute Disable Bit

XD can prevent certain classes of malicious buffer overflow attacks when combined with a supporting OS

Intel Virtualization Technology

When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Boot Performance Mode

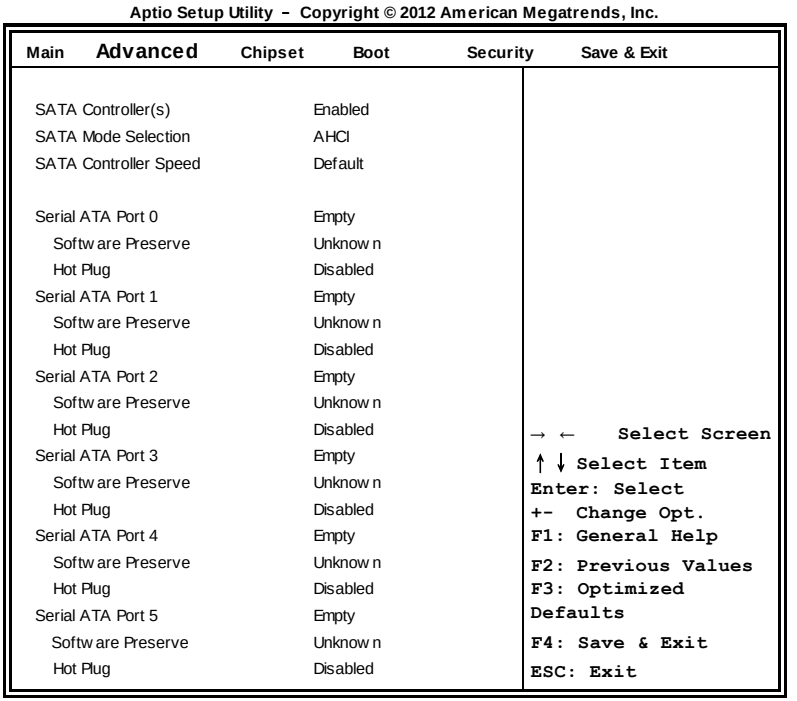
Select the performance state that the BIOS will set before OS handoff.

EIST

Enabled/Disabled Intel Speedstep.

SATA Configuration

SATA Devices Configuration.



SATA Controller(s)

Enable or disable SATA Device.

SATA Mode Selection

Determines how SATA controller(s) operate.
(1) IDE Mode.
(2) AHCI Mode.
(3) RAID Mode. (MI982AF only)

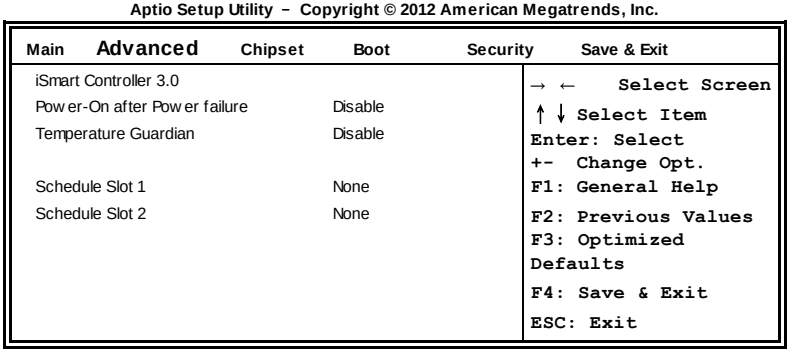
SATA Controller Speed

Indicates the maximum speed the SATA controller can support.

Hot Plug

Designates this port as Hot Pluggable.

iSmart Controller 3.0



Power-On after Power failure

This field sets the system power status whether *Disable or Enable* when power returns to the system from a power failure situation.

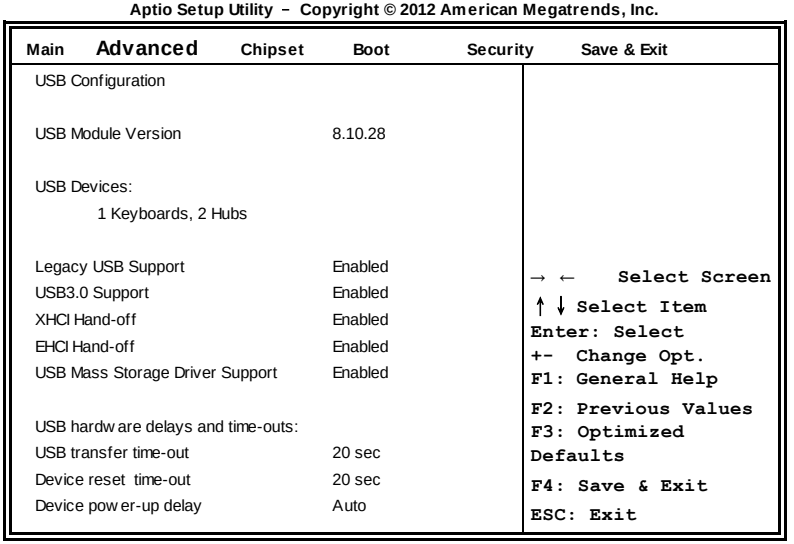
Temperature Guardian

Generate the reset signal when system hangs up on POST

Schedule Slot 1 / 2

Setup the hour/minute for system power on.

USB Configuration



Legacy USB Support

Enables Legacy USB support.
AUTO option disables legacy support if no USB devices are connected. DISABLE option will keep USB devices available only for EFI applications.

USB3.0 Support

Enable/Disable USB3.0 (XHCI) Controller support.

XHCI Hand-off

This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.

EHCI Hand-off
This is a workaround for OSes without EHCI hand-off support. The XHCI ownership change should be claimed by EHCI driver.

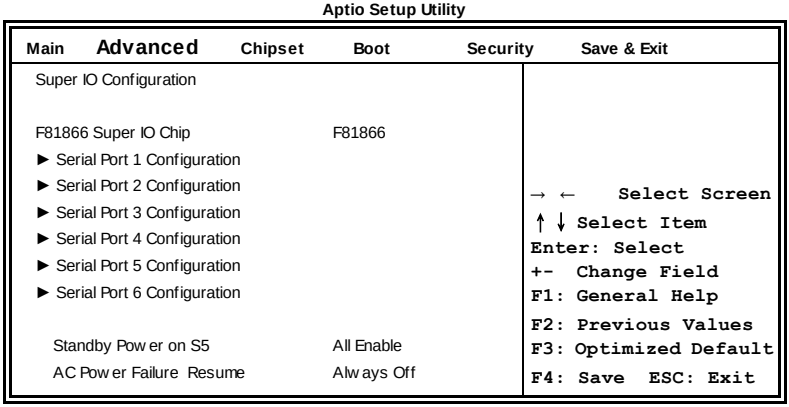
USB Mass Storage Driver Support
Enable/Disable USB Mass Storage Driver Support.

USB Transfer time-out
The time-out value for Control, Bulk, and Interrupt transfers.

Device reset tine-out
USB mass Storage device start Unit command time-out.

Device power-up delay
Maximum time the device will take before it properly reports itself to the Host Controller. 'Auto' uses default value: for a Root port it is 100ms, for a Hub port the delay is taken from Hub descriptor.

F81866 Super IO Configuration



Serial Port Configuration
Set Parameters of Serial Ports. User can Enable/Disable the serial port and Select an optimal settings for the Super IO Device.

F81866 H/W Monitor

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
Pc Health Status					
CPU smart fan control		Disabled			
System smart fan control		Disabled			
ACPI Shutdown Temperature		Disabled			
CPU Temperature		: +31 C			
SYS Temperature		: +28 C			
Fan1 Speed		: N/A			
Fan2 Speed		: 4021 RPM			
Vcore		: +1.736V			
+5V		: +5.171V			
+12V		: +12.232V			
+1.5V		: +1.512V			

→ ← Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

CPU/System smart fan control

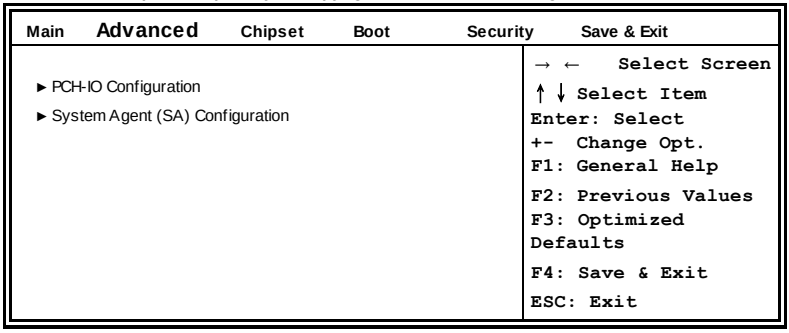
This field enables or disables the smart fan feature.
Disabled (default)
50 ℃
60 ℃
70 ℃
80 ℃
90 ℃

Temperatures/Voltages

These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

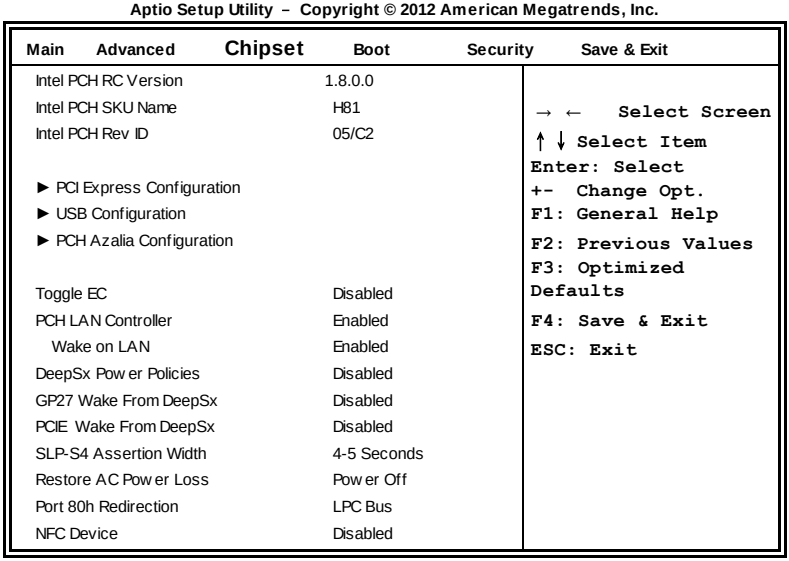
Chipset Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



PCH-IO Configuration

This section allows you to configure the North Bridge Chipset.



PCH LAN Controller

Enable or disable onboard NIC.

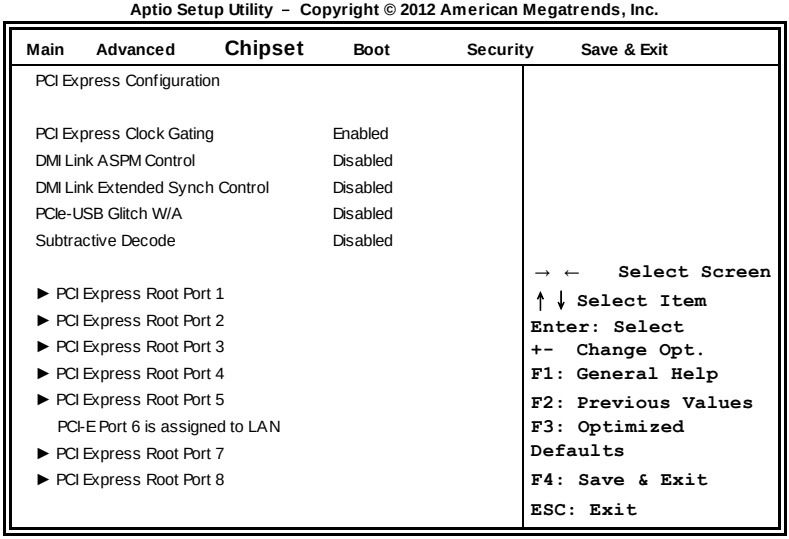
Wake on LAN

Enable or disable integrated LAN to wake the system. (The Wake On LAN cannot be disabled if ME is on at Sx state.)

SLP_S4 Assertion Width

Select a minimum assertion width of the SLP_S4# signal.

PCI Express Configuration



DMI Link ASPM Control

The control of Active State Power Management on both NB side and SB side of the DMI Link.

DMI Link Extended Synch Control

The control of Extended Synch on SB side of the DMI Link.

PCIe-USB Glitch W/A

PCIe-USB Glitch W/A for bad USB device(s) connected behind PCIE/PEG port.

Subtractive Decode

Enable or disable PCI Express Subtractive Decode.

USB Configuration

Main	Advanced	Chipset	Boot	Security	Save & Exit
USB Configuration					
USB Precondition			Disabled		
XHCI Mode			Auto		
BTCG			Disabled		
USB Ports Per-Port Disable Control			Disabled		

→ ← Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

USB Precondition

Precondition work on USB host controller and root ports for faster enumeration.

PCH Azalia Configuration

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Main	Advanced	Chipset	Boot	Security	Save & Exit
PCH Azalia Configuration					
Azalia			Auto		

→ ← Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Azalia

Control Detection of the Azalia device.
Disabled = Azalia will be unconditionally disabled.
Enabled Azalia will be unconditionally Enabled.
Auto = Azalia will be enabled if present, disabled otherwise.

System Agent (SA) Configuration

Aptio Setup Utility

Main	Advanced	Chipset	Boot	Security	Save & Exit
System Agent Bridge Name			Haswell		
System Agent RC Version			1.6.2.0		
VT-d Capability			Unsupported		
CHAP Device (B0:D7:F0)			Disabled		
Thermal Device (B0:D4:F0)			Disabled		
CPU SA Audio Device (B0:D3:F0)			Enabled		
Enable NB CRID			Disabled		
BDAT ACPI Table Support			Disabled		
► Graphics Configuration					
► Memory Configuration					

→ ← Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Field
F1: General Help
F2: Previous Values
F3: Optimized Default
F4: Save ESC: Exit

VT-d

Check to enable VT-d function on MCH.

Enable NB CRID

Enable or disable NB CRID WorkAround.

Graphics Configuration

Aptio Setup Utility – Copyright © 2012 American Megatrends, Inc.

Main	Advanced	Chipset	Boot	Security	Save & Exit
Graphics Configuration					
IGFX VBIOS Version			2179		
IGfx Frequency			700 MHz		
Primary Display			Auto		
Primary PEG			Auto		
Primary PCIE			Auto		
Internal Graphics			Auto		
Aperture Size			256MB		
DVMT Pre-Allocated			32M		
DVMT Total Gfx Mem			256MB		

→ ← Select Screen
↑ ↓ Select Item
Enter: Select
+- Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit

Primary Display

Select which of IGFX/PEG/PCI graphics device should be Primary Display or select SG for switchable Gfx.

Primary PEG
Select PEG0/PEG1/PEG2/PEG3 Graphics device should be Primary PEG.

Primary PCIE
Select PCIE0/PCIE1/PCIE2/PCIE3/PCIE4/PCIE5/PCIE6PCIE7 Graphics device should be Primary PCIE.

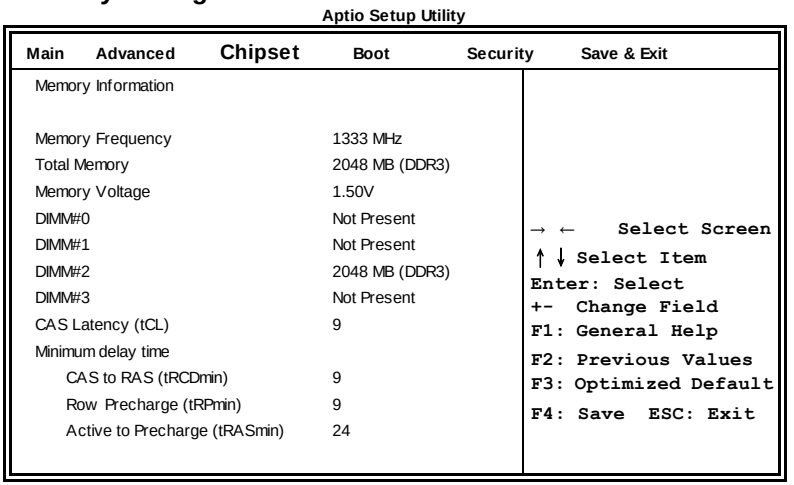
Internal Graphics
Keep IGD enabled based on the setup options.

Aperture Size
Select the Aperture Size.

DVMT Pre-Allocated
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory Size used by the Internal Graphics Device.

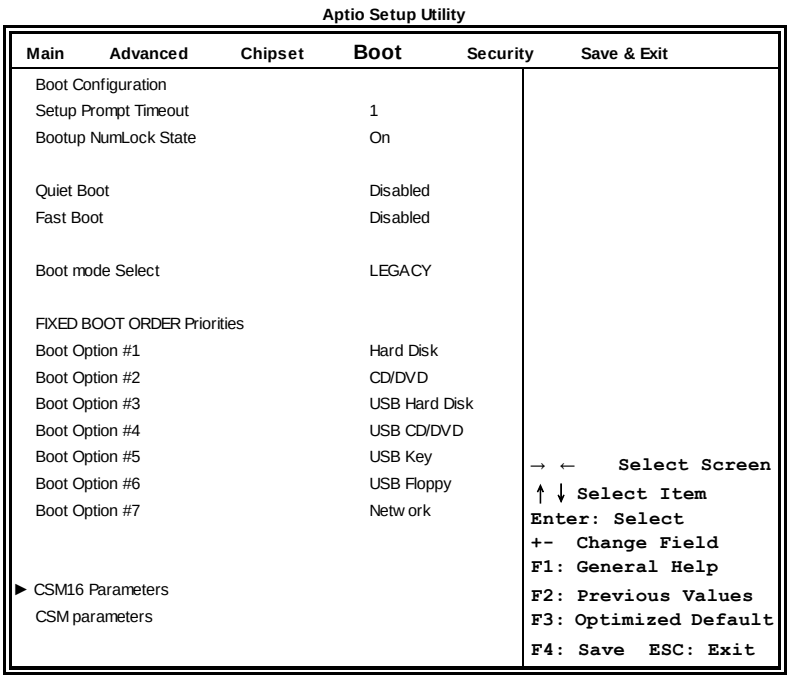
DVMT Total Gfx Mem
Select DVMT 5.0 Total Graphics Memory Size used by the Internal Graphics Device.

Memory Configuration



Boot Settings

This section allows you to configure the boot settings.



Setup Prompt Timeout

Number of seconds to wait for setup activation key.
65535(0xFFFF) means indefinite waiting.

Bootup NumLock State

Select the keyboard NumLock state.

Quiet Boot

Enables/Disables Quiet Boot option.

Fast Boot

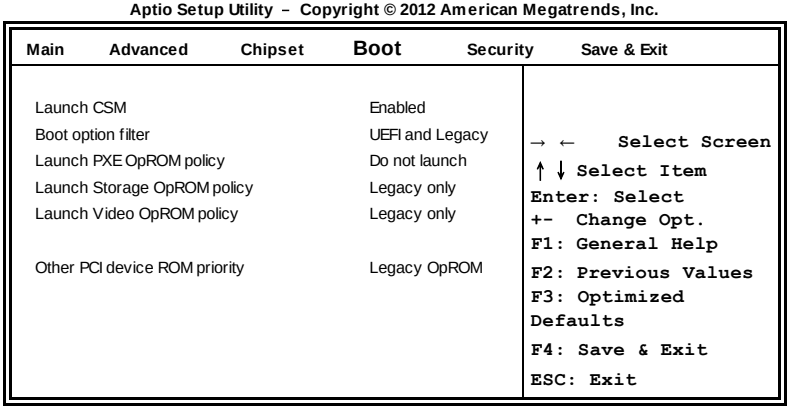
Enables/Disables boot with initialization of a minimal set of devices required to launch active boot option. Has no effect for BBS boot options.

FIXED BOOT ORDER Priorities

Sets the system boot order.

CSM parameters

This section allows you to configure the boot settings.



Launch CSM

This option controls if CSM will be launched.

Boot option filter

This option controls what devices system can boot to.

Launch PXE OpROM policy

Controls the execution of UEFI and Legacy PXE OpROM.

Launch Storatge OpROM policy

Controls the execution of UEFI and Legacy Storage OpROM.

Launch Video OpROM policy

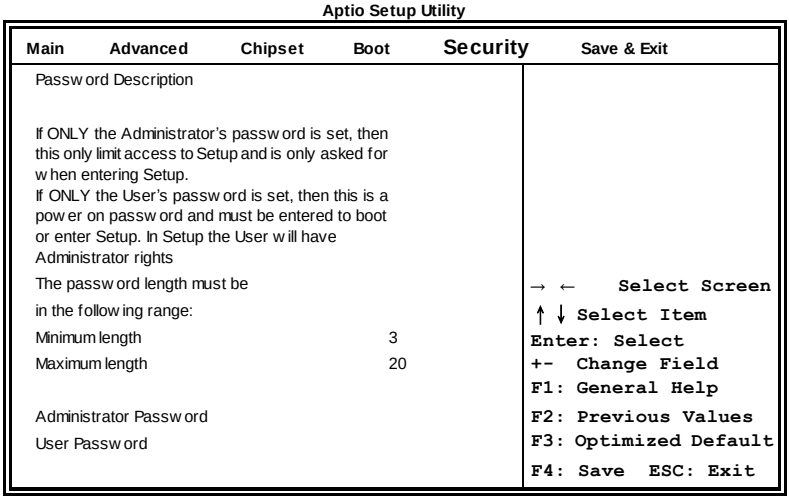
Controls the execution of UEFI and Legacy Video OpROM.

Other PCI device ROM priority

For PCI devices other than Network, Mass storage or Video defines which OpROM to launch.

Security Settings

This section allows you to configure and improve your system and allows you to set up some system features according to your preference.



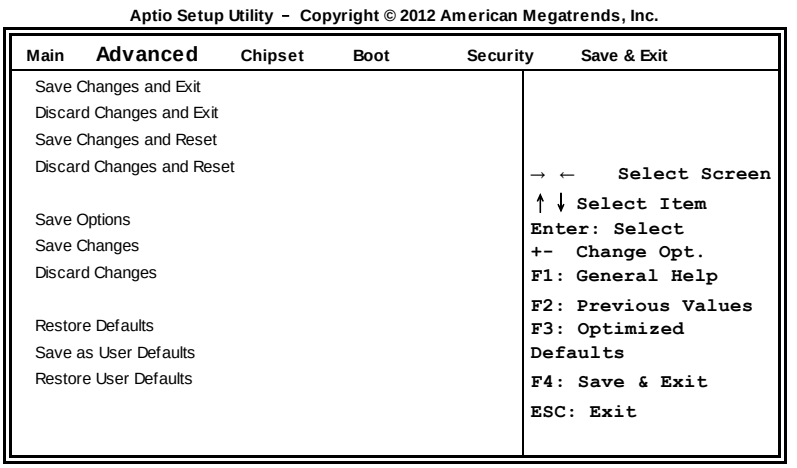
Administrator Password

Set Setup Administrator Password.

User Password

Set User Password.

Save & Exit Settings



Save Changes and Exit
Exit system setup after saving the changes.

Discard Changes and Exit
Exit system setup without saving any changes.

Save Changes and Reset
Reset the system after saving the changes.

Discard Changes and Reset
Reset system setup without saving any changes.

Save Changes
Save Changes done so far to any of the setup options.

Discard Changes
Discard Changes done so far to any of the setup options.

Restore Defaults
Restore/Load Defaults values for all the setup options.

Save as User Defaults
Save the changes done so far as User Defaults.

Restore User Defaults
Restore the User Defaults to all the setup options.

Drivers Installation

This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find the items missing, please contact the vendor where you made the purchase. The contents of this section include the following:

IMPORTANT NOTE:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the drivers installation.

Intel Chipset Software Installation Utility

The Intel Chipset Drivers should be installed first before the software drivers to enable Plug & Play INF support for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***.

2. Click ***Intel(R) Chipset Software Installation Utility.***

3. When the Welcome screen to the Intel® Chipset Device Software appears, click ***Next*** to continue.

4. Click ***Yes*** to accept the software license agreement and proceed with the installation process.

5. On the Readme File Information screen, click ***Next*** to continue the installation.

6. The Setup process is now complete. Click ***Finish*** to restart the computer and for changes to take effect.

VGA Drivers Installation

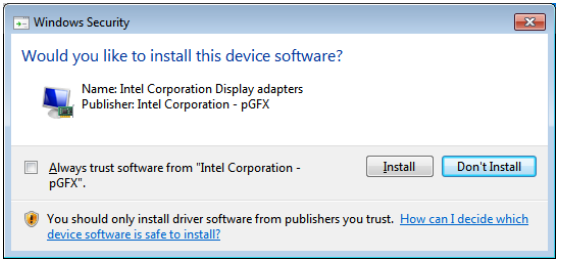
1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***. Click ***Intel(R) Graphics Driver.***

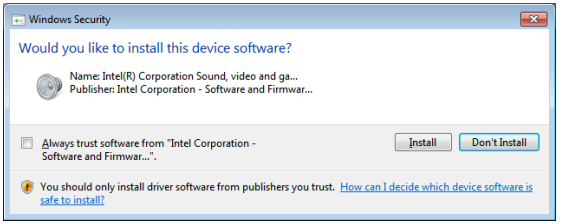
2. When the Welcome screen appears, click ***Next*** to continue.

3. Click ***Yes*** to to agree with the license agreement and continue the installation.

4. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® HD Graphics Driver.

5. On the screen shown below, click ***Install*** to continue.





6. On the Setup Progress screen, click ***Next*** to continue.

7. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

Realtek HD Audio Driver Installation

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***. Click ***Realtek High Definition Audio Driver.***

2. On the Welcome to the InstallShield Wizard screen, click ***Next*** to proceed with and complete the installation process.

3. The InstallShield Wizard Complete. Click ***Finish*** to restart the computer and for changes to take effect.

LAN Drivers Installation

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***. Click ***Intel(R) PRO LAN Network Drivers.***

2. Click ***Install Drivers and Software.***

4. When the Welcome screen appears, click ***Next***.

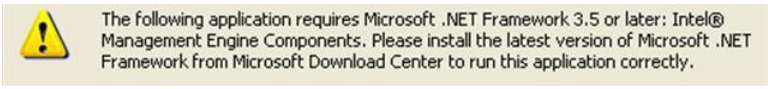
5. Click ***Next*** to to agree with the license agreement.

6. Click the checkbox for **Drivers** in the Setup Options screen to select it and click **Next** to continue.

7. The wizard is ready to begin installation. Click ***Install*** to begin the installation.

8. When InstallShield Wizard is complete, click ***Finish***.

Intel® Management Engine Interface



Follow the steps below to install the Intel Management Engine.

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers*** and then ***Intel(R) ME 9.0 Drivers***.

2. When the Welcome screen to the InstallShield Wizard for Intel® Management Engine Components, click the checkbox for **Install Intel® Control Center** & click ***Next***.

3. Click ***Yes*** to to agree with the license agreement.

4. When the Setup Progress screen appears, click ***Next***. Then, click ***Finish*** when the setup progress has been successfully installed.

Intel® USB 3.0 Drivers

1. Insert the DVD that comes with the board. Click ***Intel*** and then ***Intel(R) 8 Series Chipset Drivers***. Click ***Intel(R) USB 3.0 Drivers.***

2. When the Welcome screen to the InstallShield Wizard for Intel® USB 3.0 eXtensible Host Controller Driver, click ***Next***.

3. Click ***Yes*** to to agree with the license agreement and continue the installation.

4. On the Readme File Information screen, click ***Next*** to continue the installation of the Intel® USB 3.0 eXtensible Host Controller Driver.

5. When the Setup Progress screen appears, click ***Next***. Setup complete. Click ***Finish*** to restart the computer and for changes to take effect.

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Appendix

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0000h-001Fh	Direct memory access controller
0000h-001Fh	PCI bus
0040h-0043h	System timer
0050h-0053h	System timer
0070h-0077h	System CMOS/real time clock
0081h-0091h	Direct memory access controller
0093h-009Fh	Direct memory access controller
00C0h-00DFh	Direct memory access controller
00F0h-00F0h	Numeric data processor
02E0h-02E7h	Communications Port (COM6)
02E8h-02EFh	Communications Port (COM4)
02F0h-02F7h	Communications Port (COM5)
02F8h-02FFh	Communications Port (COM2)
03B0h-03BBh	Intel(R) HD Graphics 4600
03C0h-03DFh	Intel(R) HD Graphics 4600
03E8h-03EFh	Communications Port (COM3)
03F8h-03FFh	Communications Port (COM1)
0D00h-FFFFh	PCI bus
E000h-EFFFh	Intel(R) 8 Series/C220 Series PCI Express Root Port #3 - 8C14
F000h-F03Fh	Intel(R) HD Graphics 4600
F040h-F05Fh	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
F060h-F07Fh	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
F0A0h-F0A3h	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
F0B0h-F0B7h	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
F0C0h-F0C3h	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
F0D0h-F0D7h	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ0	System Timer
IRQ3	Serial Port #2
IRQ4	Serial Port #1
IRQ7	Serial Port #3
IRQ7	Serial Port #4
IRQ8	System CMOS/real time clock
IRQ 10	Intel(R) 8 Series/C220 Series SMBus Controller - 8C22
IRQ 13	Numeric data processor
IRQ 16	High Definition Audio Controller
IRQ 16	Intel(R) 8 Series/C220 Series USB EHCI #2 - 8C2D
IRQ 16	Intel(R) Management Engine Interface
IRQ 19	Intel(R) 8 Series/C220 Series SATA AHCI Controller - 8C02
IRQ 22	High Definition Audio Controller
IRQ 23	Intel(R) 8 Series/C220 Series USB EHCI #1 - 8C26

C. Watchdog Timer Configuration

The WDT is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven. Under normal circumstance, the user will restart the WDT at regular intervals before the timer counts to zero.

SAMPLE CODE:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81866.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81866 watch dog program\n");

        SIO = Init_F81866();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81866, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf(" Parameter incorrect!!\n");
                return (1);
        }

        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime);       }
        else
        {       DisableWDT();       }
```

```
return 0;
```

```
}
//---------------------------------------------------------------------------
void EnableWDT(int interval)
{
	unsigned char bBuf;

	bBuf = Get_F81866_Reg(0x2B);
	bBuf &= (~0x20);
	Set_F81866_Reg(0x2B, bBuf);			//Enable WDTO

	Set_F81866_LD(0x07);				//switch to logic device 7
	Set_F81866_Reg(0x30, 0x01);			//enable timer

	bBuf = Get_F81866_Reg(0xF5);
	bBuf &= (~0x0F);
	bBuf |= 0x52;
	Set_F81866_Reg(0xF5, bBuf);			//count mode is second

	Set_F81866_Reg(0xF6, interval);		//set timer

	bBuf = Get_F81866_Reg(0xFA);
	bBuf |= 0x01;
	Set_F81866_Reg(0xFA, bBuf);			//enable WDTO output

	bBuf = Get_F81866_Reg(0xF5);
	bBuf |= 0x20;
	Set_F81866_Reg(0xF5, bBuf);			//start counting
}
//---------------------------------------------------------------------------
void DisableWDT(void)
{
	unsigned char bBuf;

	Set_F81866_LD(0x07);				//switch to logic device 7

	bBuf = Get_F81866_Reg(0xFA);
	bBuf &= ~0x01;
	Set_F81866_Reg(0xFA, bBuf);			//disable WDTO output

	bBuf = Get_F81866_Reg(0xF5);
	bBuf &= ~0x20;
	bBuf |= 0x40;
	Set_F81866_Reg(0xF5, bBuf);			//disable WDT
}
//---------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81866.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81866_BASE;
void Unlock_F81866 (void);
void Lock_F81866 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81866(void)
{
	unsigned int result;
	unsigned char ucDid;

	F81866_BASE = 0x4E;
	result = F81866_BASE;

	ucDid = Get_F81866_Reg(0x20);
	if (ucDid == 0x07)                                  //Fintek 81866
	{	goto Init_Finish;	}

	F81866_BASE = 0x2E;
	result = F81866_BASE;

	ucDid = Get_F81866_Reg(0x20);
	if (ucDid == 0x07)                                  //Fintek 81866
	{	goto Init_Finish;	}

	F81866_BASE = 0x00;
	result = F81866_BASE;

Init_Finish:
	return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81866 (void)
{
	outportb(F81866_INDEX_PORT, F81866_UNLOCK);
	outportb(F81866_INDEX_PORT, F81866_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81866 (void)
{
	outportb(F81866_INDEX_PORT, F81866_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81866_LD( unsigned char LD)
{
	Unlock_F81866();
	outportb(F81866_INDEX_PORT, F81866_REG_LD);
	outportb(F81866_DATA_PORT, LD);
	Lock_F81866();
}
//---------------------------------------------------------------------------
void Set_F81866_Reg( unsigned char REG, unsigned char DATA)
{
	Unlock_F81866();
	outportb(F81866_INDEX_PORT, REG);
	outportb(F81866_DATA_PORT, DATA);
```

```
        Lock_F81866();
}
//---------------------------------------------------------------------------
```

```
unsigned char Get_F81866_Reg(unsigned char REG)
{
        unsigned char Result;
        Unlock_F81866();
        outportb(F81866_INDEX_PORT, REG);
        Result = inportb(F81866_DATA_PORT);
        Lock_F81866();
        return Result;
}
//-----------------------------------------------------------------------------
```

```
//-----------------------------------------------------------------------------
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//
//-----------------------------------------------------------------------------
#ifndef __F81866_H
#define __F81866_H                             1
//-----------------------------------------------------------------------------
#define         F81866_INDEX_PORT               (F81866_BASE)
#define         F81866_DATA_PORT                (F81866_BASE+1)
//-----------------------------------------------------------------------------
#define         F81866_REG_LD                   0x07
//-----------------------------------------------------------------------------
#define F81866_UNLOCK                   0x87
#define         F81866_LOCK                             0xAA
//-----------------------------------------------------------------------------
unsigned int Init_F81866(void);
void Set_F81866_LD( unsigned char);
void Set_F81866_Reg( unsigned char, unsigned char);
unsigned char Get_F81866_Reg( unsigned char);
//-----------------------------------------------------------------------------
#endif //__F81866_H
```