innodisk

Approval Sheet

Customer	
Product Number	**M4R0-AGS1BCRG**
Module speed	**PC4-2133**
Pin	**288pin**
Cl-tRCD-tRP	**15-15-15**
Operating Temp	**0℃~85℃**
Date	**13rd July 2017**

The Total Solution For
Industrial Flash Storage

Rev 1.0

1. Features

- 288-pin Registered Dual Inline Memory Module (RDIMM)
- Organization: 2Gx72 based on 1Gx8 * (18 components) / 2 Ranks
- CL-tRCD-tRP : 15-15-15
- JEDEC standard 1.2V (± 0.06V) Power Supply
- VDDQ = 1.2V (± 0.06V)
- 16 Banks (4 Bank Groups)
- Programmable CAS Latency: 10,11,12,13,14,15,16,17,18
- Burst Length: 8(Interleave/nibble sequential)
- Bi-directional Differential Data-Strobe
- On Die Termination (ODT)
- Average Refresh Period 7.8us at lower than a T_{CASE} 85°C, 3.9us at 85°C < TCASE < 95 °C
- RoHS Compliant
- Asynchronous Reset

2. Address Configuration

Module Organization	Row address	Column Address	Bank Address	BG Address	Auto Precharge
2Gx72	A0-A15	A0-A9	BA0-BA1	BG0-BG1	A10/AP

3. Pin Description

Pin Name	Description	Pin Name	Description
A0-A17	Register address input	SCL	I2C serial bus clock for SPD/TS and register
BA0, BA1	Register bank select input	SDA	I2C serial bus data line for SPD/TS and register
BG0, BG1	Register bank group select input	SA0-SA2	I2C slave address select for SPD/TS and register
RAS_n	Register row address strobe input	PAR	Register parity input
CAS_n	Register column address strobe input	VDD	SDRAM core power supply
WE_n	Register write enable input	VPP	SDRAM activating power supply
CS0_n, CS1_n, CS2_n, CS3_n	DIMM Rank Select Lines input	VREFCA	SDRAM command/address reference supply
CKE0, CKE1	Register clock enable lines input	VSS	Power supply return (ground)
ODT0, ODT1	Register on-die termination control lines input	VDDSPD	Serial SPD/TS positive power supply
ACT_n	Register input activate input	ALERT_n	Register ALERT_n output
DQ0-DQ63	DIMM memory data bus	RESET_n	Set Register and SDRAMs to a Known State
CB0-CB7	DIMM ECC check bits	EVENT_n	SPD signals a thermal event has occurred
DQS0_t-DQS17_t	Data buffer data strobes (positive)	VTT	SDRAM I/O termination supply
DQS0_c-DQS17_c	Data buffer data strobes (negative)	RFU	Reserved for future use
CK0_t,CK1_t	Register clock input (positive)	TDQS9_t-TDQS17_t, TDQS9_c-TDQS17_t	Provides a dummy load for x8 based RDIMMs where mixed populations of X4 and x8 based RDIMMs are present.
CK0_c, CK1_c	Register clock input (negative)		

4. Pin Configuration (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	NC	**145**	NC	**37**	VSS	**181**	DQ29	**73**	VDD	**217**	VDD	**109**	VSS	**253**	DQ41
2	VSS	**146**	VREFCA	**38**	DQ24	**182**	VSS	**74**	CK0_t	**218**	CK1_t	**110**	DQS14_t/ TDQS14_t	**254**	VSS
3	DQ4	**147**	VSS	**39**	VSS	**183**	DQ25	**75**	CK0_c	**219**	CK1_c	**111**	DQS14_c/ TDQS14_c	**255**	DQS5_c
4	VSS	**148**	DQ5	**40**	DQS12_t/ TDQS12_t	**184**	VSS	**76**	VDD	**220**	VDD	**112**	VSS	**256**	DQS5_t
5	DQ0	**149**	VSS	**41**	DQS12_c/ TDQS12_c	**185**	DQS3_c	**77**	VTT	**221**	VTT	**113**	DQ46	**257**	VSS
6	VSS	**150**	DQ1	**42**	VSS	**186**	DQS3_t	**78**	EVENT_n	**222**	PARITY	**114**	VSS	**258**	DQ47
7	DQS9_t/ TDQS9_t	**151**	VSS	**43**	DQ30	**187**	VSS	**79**	A0	**223**	VDD	**115**	DQ42	**259**	VSS
8	DQS09_c/ TDQS9_c	**152**	DQS0_c	**44**	VSS	**188**	DQ31	**80**	VDD	**224**	BA1	**116**	VSS	**260**	DQ43
9	VSS	**153**	DQS0_t	**45**	DQ26	**189**	VSS	**81**	BA0	**225**	A10/AP	**117**	DQ52	**261**	VSS
10	DQ6	**154**	VSS	**46**	VSS	**190**	DQ27	**82**	RAS_n /A16	**226**	VDD	**118**	VSS	**262**	DQ53
11	VSS	**155**	DQ7	**47**	CB4	**191**	VSS	**83**	VDD	**227**	RFU	**119**	DQ48	**263**	VSS
12	DQ2	**156**	VSS	**48**	VSS	**192**	CB5	**84**	CS0_n	**228**	WE_n/ A14	**120**	VSS	**264**	DQ49
13	VSS	**157**	DQ3	**49**	CB0	**193**	VSS	**85**	VDD	**229**	VDD	**121**	DQS15_t/ TDQS15_t	**265**	VSS
14	DQ12	**158**	VSS	**50**	VSS	**194**	CB1	**86**	CAS_n/ A15	**230**	NC	**122**	DQS15_c/ TDQS15_c	**266**	DQS6_c
15	VSS	**159**	DQ13	**51**	TDQS17_t/ TDQS17_t	**195**	VSS	**87**	ODT0	**231**	VDD	**123**	VSS	**267**	DQS6_t
16	DQ8	**160**	VSS	**52**	DQS17_c/ TDQS17_c	**196**	DQS8_c	**88**	VDD	**232**	A13	**124**	DQ54	**268**	VSS
17	VSS	**161**	DQ9	**53**	VSS	**197**	DQS8_t	**89**	CS1_n	**233**	VDD	**125**	VSS	**269**	DQ55
18	DQS10_t/ TDQS10_t	**162**	VSS	**54**	CB6	**198**	VSS	**90**	VDD	**234**	A17	**126**	DQ50	**270**	VSS
19	DQS10_c/ TDQS10_c	**163**	DQS1_c	**55**	VSS	**199**	CB7	**91**	ODT1	**235**	NC/C2	**127**	VSS	**271**	DQ51
20	VSS	**164**	DQS1_t	**56**	CB2	**200**	VSS	**92**	VDD	**236**	VDD	**128**	DQ60	**272**	VSS
21	DQ14	**165**	VSS	**57**	VSS	**201**	CB3	**93**	CS2_n/C0,NC	**237**	CS3_n C1,NC	**129**	VSS	**273**	DQ61
22	VSS	**166**	DQ15	**58**	RESET_n	**202**	VSS	**94**	VSS	**238**	SA2	**130**	DQ56	**274**	VSS
23	DQ10	**167**	VSS	**59**	VDD	**203**	CKE1	**95**	DQ36	**239**	VSS	**131**	VSS	**275**	DQ57
24	VSS	**168**	DQ11	**60**	CKE0	**204**	VDD	**96**	VSS	**240**	DQ37	**132**	DQS16_t/ TDQS16_t	**276**	VSS
25	DQ20	**169**	VSS	**61**	VDD	**205**	RFU	**97**	DQ32	**241**	VSS	**133**	DQS16_c /TDQS16_c	**277**	DQS7_c
26	VSS	**170**	DQ21	**62**	ACT_n	**206**	VDD	**98**	VSS	**242**	DQ33	**134**	VSS	**278**	DQS7_t
27	DQ16	**171**	VSS	**63**	BG0	**207**	BG1	**99**	DQS13_t/ TDQ13_t	**243**	VSS	**135**	DQ62	**279**	VSS
28	VSS	**172**	DQ17	**64**	VDD	**208**	ALERT_n	**100**	DQS13_c/ TDQS13_c	**244**	DQS4_c	**136**	VSS	**280**	DQ63
29	DQS11_t/ TDQS11_t	**173**	VSS	**65**	A12/BC_n	**209**	VDD	**101**	VSS	**245**	DQS4_t	**137**	DQ58	**281**	VSS
30	DQS11_c/ TDQS11_c	**174**	DQS2_c	**66**	A9	**210**	A11	**102**	DQ38	**246**	VSS	**138**	VSS	**282**	DQ59
31	VSS	**175**	DQS2_t	**67**	VDD	**211**	A7	**103**	VSS	**247**	DQ39	**139**	SA0	**283**	VSS
32	DQ22	**176**	VSS	**68**	A8	**212**	VDD	**104**	DQ34	**248**	VSS	**140**	SA1	**284**	VDDSPD
33	VSS	**177**	DQ23	**69**	A6	**213**	A5	**105**	VSS	**249**	DQ35	**141**	SCL	**285**	SDA
34	DQ18	**178**	VSS	**70**	VDD	**214**	A4	**106**	DQ44	**250**	VSS	**142**	VPP	**286**	VPP
35	VSS	**179**	DQ19	**71**	A3	**215**	VDD	**107**	VSS	**251**	DQ45	**143**	VPP	**287**	VPP
36	DQ28	**180**	VSS	**72**	A1	**216**	A2	**108**	DQ40	**252**	VSS	**144**	RFU	**288**	VPP

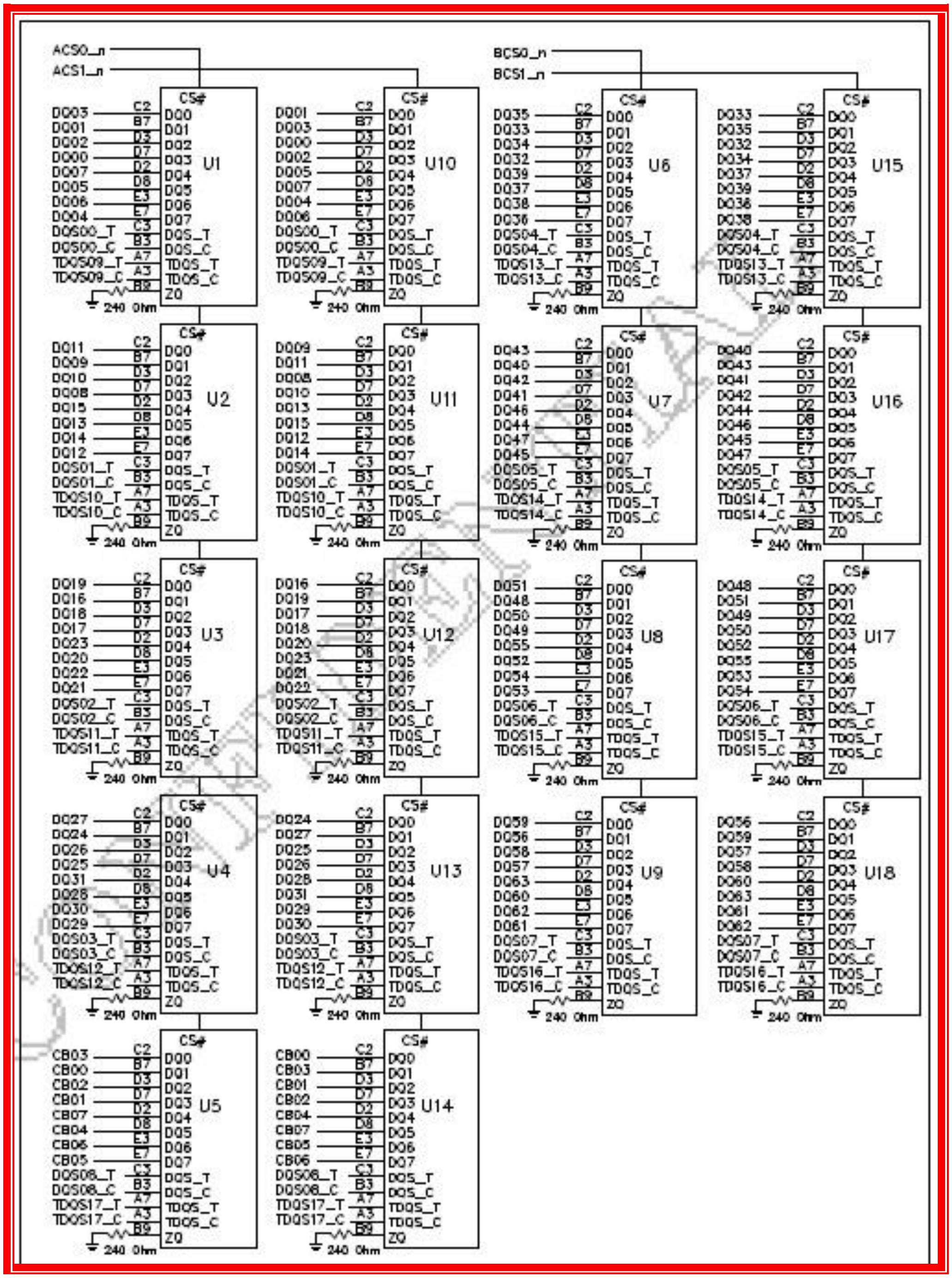
Note:
1. NC = No Connect, RFU = Reserved for Future Use
2. Address A17 is only valid for 16 Gb x4 based SDRAMs.
3. RAS_n is a multiplexed function with A16.
4. CAS_n is a multiplexed function with A15.
5. WE_n is a multiplexed function with A14.

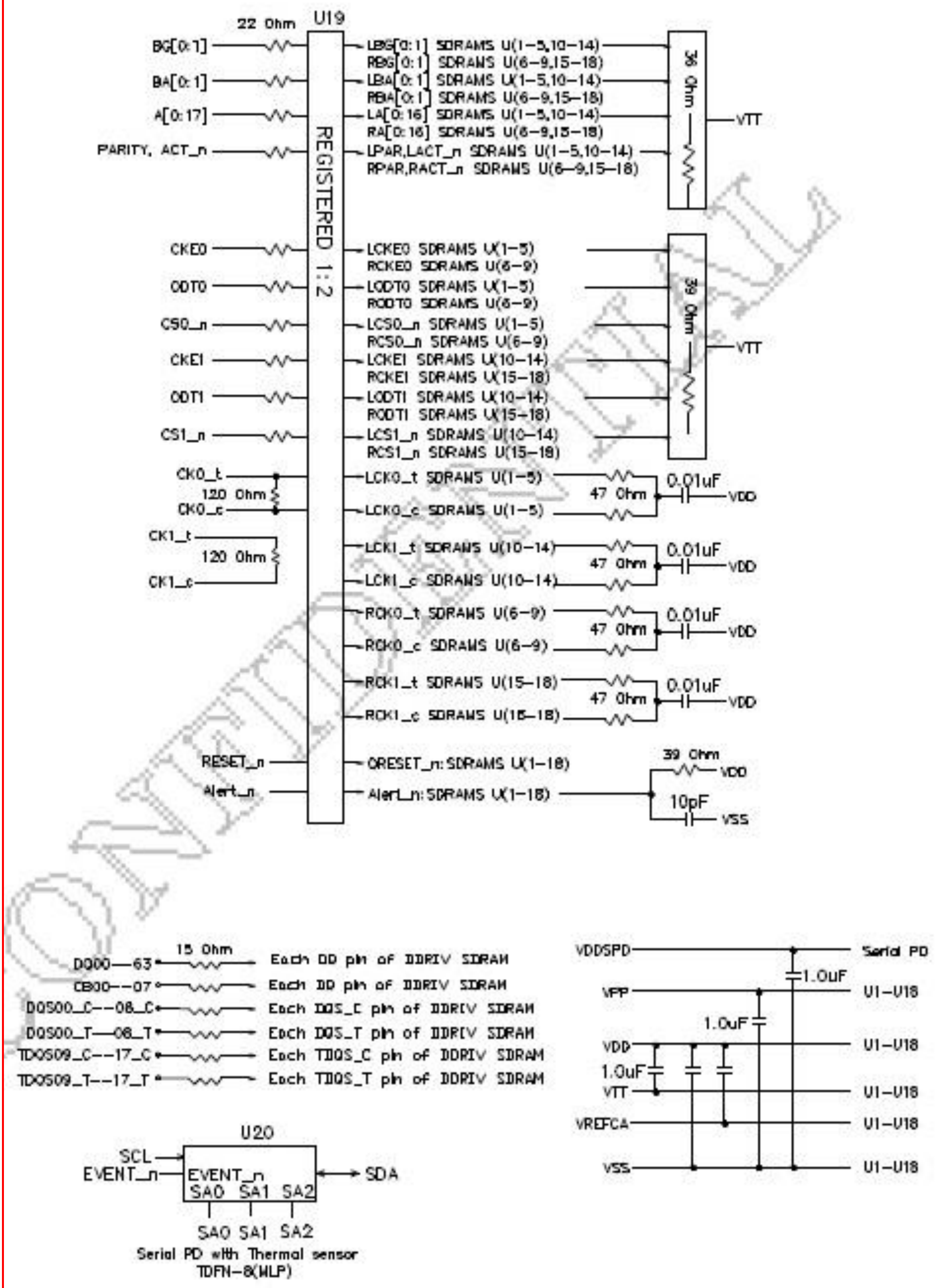
Ordering Information

DDR4 RDIMM

Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M4R0-AGS1BCRG	16GB	PC4-2133	2Gx72	18	2	Y

5. Block Diagram




22 Ohm
U19
BG[0:1]
BA[0:1]
A[0:17]
PARITY, ACT_n
REGISTERED 1:2
LBG[0:1] SDRAMS U(1–5,10–14)
RBG[0:1] SDRAMS U(6–9,15–18)
LBA[0:1] SDRAMS U(1–5,10–14)
RBA[0:1] SDRAMS U(6–9,15–18)
LA[0:16] SDRAMS U(1–5,10–14)
RA[0:16] SDRAMS U(6–9,15–18)
LPAR,LACT_n SDRAMS U(1–5,10–14)
RPAR,RACT_n SDRAMS U(6–9,15–18)
36 Ohm
VTT
CKE0
ODT0
CS0_n
CKE1
ODT1
CS1_n
LCKE0 SDRAMS U(1–5)
RCKE0 SDRAMS U(6–9)
LODT0 SDRAMS U(1–5)
RODT0 SDRAMS U(6–9)
LCS0_n SDRAMS U(1–5)
RCS0_n SDRAMS U(6–9)
LCKE1 SDRAMS U(10–14)
RCKE1 SDRAMS U(15–18)
LODT1 SDRAMS U(10–14)
RODT1 SDRAMS U(15–18)
LCS1_n SDRAMS U(10–14)
RCS1_n SDRAMS U(15–18)
39 Ohm
VTT
CK0_t
120 Ohm
CK0_c
CK1_t
120 Ohm
CK1_c
LCK0_t SDRAMS U(1–5)
LCK0_c SDRAMS U(1–5)
47 Ohm
0.01uF
VDD
LCK1_t SDRAMS U(10–14)
LCK1_c SDRAMS U(10–14)
47 Ohm
0.01uF
VDD
RCK0_t SDRAMS U(6–9)
RCK0_c SDRAMS U(6–9)
47 Ohm
0.01uF
VDD
RCK1_t SDRAMS U(15–18)
RCK1_c SDRAMS U(15–18)
47 Ohm
0.01uF
VDD
RESET_n
Alert_n
QRESET_n:SDRAMS U(1–18)
Alert_n:SDRAMS U(1–18)
39 Ohm
VDD
10pF
VSS
15 Ohm
DQ00—63
CB00—07
DQS00_C—08_C
DQS00_T—08_T
TDQS09_C—17_C
TDQS09_T—17_T
Each DQ pin of DDRIV SDRAM
Each DQ pin of DDRIV SDRAM
Each DQS_C pin of DDRIV SDRAM
Each DQS_T pin of DDRIV SDRAM
Each TDQS_C pin of DDRIV SDRAM
Each TDQS_T pin of DDRIV SDRAM
VDDSPD
Serial PD
1.0uF
VPP
U1–U18
1.0uF
VDD
U1–U18
1.0uF
VTT
U1–U18
VREFCA
U1–U18
VSS
U1–U18
U20
SCL
EVENT_n
EVENT_n
SA0 SA1 SA2
SDA
SA0 SA1 SA2
Serial PD with Thermal sensor
TDFN-8(WLP)

6. IDD Specification Parameter

(IDD values are for full operating range of Voltage and Temperature)

Symbol	Proposed Conditions	Value	Units
IDD0	Operating One Bank Active-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT and PRE; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling; Data IO: VDDQ; DM_n:stable at 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2;ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	558	mA
IDD0A	Operating One Bank Active-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD0	576	mA
IDD1	Operating One Bank Active-Read-Precharge Current (AL=0)CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: Highbetween ACT, RD and PRE; Command, Address, Bank Group Address, Bank Address Inputs, Data IO: partially toggling; DM_n: stableat 1; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	792	mA
IDD1A	Operating One Bank Active-Read-Precharge Current (AL=CL-1) AL = CL-1, Other conditions: see IDD1	846	mA
IDD2N	Precharge Standby Current (AL=0)CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command,Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banksclosed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	396	mA
IDD2NA	Precharge Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD2N	450	mA
IDD2NT	Precharge Standby ODT Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VSSQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: toggling according ; Pattern Details: Refer to Component Datasheet for detail pattern	450	mA
IDD2NL	Precharge Standby Current with CAL enabled Same definition like for IDD2N, CAL enabled3	270	mA
IDD2NG	Precharge Standby Current with Gear Down mode enabled Same definition like for IDD2N, Gear Down mode enabled3	396	mA
IDD2ND	Precharge Standby Current with DLL disabled Same definition like for IDD2N, DLL disabled3	360	mA
IDD2N_par	Precharge Standby Current with CA parity enabled Same definition like for IDD2N, CA parity enabled3	414	mA
IDD2P	Precharge Power-Down Current CKE: Low; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL:0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	288	mA
IDD2Q	Precharge Quiet Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	360	mA

IDD3N	Active Standby Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details:Refer to Component Datasheet for detail pattern	648	mA
IDD3NA	Active Standby Current (AL=CL-1) AL = CL-1, Other conditions: see IDD3N	684	mA
IDD3P	Active Power-Down Current CKE: Low; External clock: On; tCK, CL: sRefer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: stable at 1; Command, Address, Bank Group Address, Bank Address Inputs: stable at 0; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0	756	mA
IDD4R	Operating Burst Read Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 82; AL: 0; CS_n: High between RD; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless read data burst with different data between one burst and the next one according ; DM_n: stable at 1; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	1818	mA
IDD4RA	Operating Burst Read Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4R	1890	mA
IDD4RB	Operating Burst Read Current with Read DBI Read DBI enabled3, Other conditions: see IDD4R	1836	mA
IDD4W	Operating Burst Write Current CKE: High; External clock: On; tCK, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between WR; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: seamless write data burst with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at HIGH; Pattern Details: Refer to Component Datasheet for detail pattern	1512	mA
IDD4WA	Operating Burst Write Current (AL=CL-1) AL = CL-1, Other conditions: see IDD4W	1584	mA
IDD4WB	Operating Burst Write Current with Write DBI Write DBI enabled3, Other conditions: see IDD4W	1512	mA
IDD4WC	Operating Burst Write Current with Write CRC Write CRC enabled3, Other conditions: see IDD4W	1332	mA
IDD4W_par	Operating Burst Write Current with CA Parity CA Parity enabled3, Other conditions: see IDD4W	1656	mA
IDD5B	Burst Refresh Current (1X REF) CKE: High; External clock: On; tCK, CL, nRFC: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n: High between REF; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; Data IO: VDDQ; DM_n: stable at 1; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	3582	mA

IDD5F2	Burst Refresh Current (2X REF) tRFC=tRFC_x2, Other conditions: see IDD5B	2484	mA
IDD5F4	Burst Refresh Current (4X REF) tRFC=tRFC_x4, Other conditions: see IDD5B	2088	mA
IDD6N	Self Refresh Current: Normal Temperature Range TCASE: 0 - 85°C; Low Power Array Self Refresh (LP ASR) : Normal4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n: stable at 1; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	414	mA
IDD6E	Self-Refresh Current: Extended Temperature Range) TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Extended4; CKE: Low; External clock: Off; CK_t and CK_c: LOW; CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: 0; CS_n, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	612	mA
IDD6R	Self-Refresh Current: Reduced Temperature Range TCASE: 0 - 45 °C; Low Power Array Self Refresh (LP ASR) : Reduced4; CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 36 on p age 39; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Extended Temperature Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MIDLEVEL	288	mA
IDD6A	Auto Self-Refresh Current TCASE: 0 - 95°C; Low Power Array Self Refresh (LP ASR) : Auto4;CKE: Low; External clock: Off; CK_t and CK_c#: LOW; CL: see Table 36 on p age 39; BL: 81; AL: 0; CS_n#, Command, Address, Bank Group Address, Bank Address, Data IO: High; DM_n:stable at 1; Bank Activity: Auto Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: MID-LEVEL	396	mA
IDD7	Operating Bank Interleave Read Current CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, nRRD, nFAW, CL: Refer to Component Datasheet for detail pattern; BL: 81; AL: CL-1; CS_n: High between ACT and RDA; Command, Address, Bank Group Address, Bank Address Inputs: partially toggling ; DataIO: read data bursts with different data between one burst and the next one ; DM_n: stable at 1; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers2; ODT Signal: stable at 0; Pattern Details: Refer to Component Datasheet for detail pattern	2556	mA
IDD8	Maximum Power Down Current TBD	198	mA

7. Absolute Maximum DC ratings

Symbol	Parameter	Rating	Units	Notes
VDD	Voltage on VDD pin relative to Vss	-0.3 ~ 1.5	V	1,3
VDDQ	Voltage on VDDQ pin relative to Vss	-0.3 ~ 1.5	V	1,3
VPP	Voltage on VPP pin relative to Vss	-0.3 ~ 3.0	V	4
V_{IN}, V_{OUT}	Voltage on any pin except VREFCA to Vss	-0.3 ~ 1.5	V	1
T_{STG}	Storage Temperature	-55 to +100	^{0}C	1,2

NOTE :
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability
2. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3. VDD and VDDQ must be within 300 mV of each other at all times; and VREFCA must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREFCA may be equal to or less than 300 mV
4. VPP must be equal or greater than VDD/VDDQ at all times.

8. AC and DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.14	1.2	1.26	V	1,2,3
V_{DDQ}	Supply Voltage for Output	1.14	1.2	1.26	V	1,2,3
V_{PP}		2.375	2.5	2.75	V	3

NOTE:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. DC bandwidth is limited to 20MHz.

9. Timing Parameters

Clock Timing

Parameter	Symbol	MIN	MAX	Units
Minimum Clock Cycle Time (DLL off mode)	tCK (DLL_OFF)	8	20	ns
Average Clock Period	tCK(avg)	0.938	<1.071	ns
Average high pulse width	tCH(avg)	0.48	0.52	tCK(avg)
Average low pulse width	tCL(avg)	0.48	0.52	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg)min+ tJIT(per)min_tot	tCK(avg)max + tJIT(per)max_tot	tCK(avg)
Absolute clock HIGH pulse width	tCH(abs)	0.45	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.45	-	tCK(avg)
Clock Period Jitter-total	JIT(per)_tot	-47	47	ps
Clock Period Jitter-deterministic	JIT(per)_dj	-23	23	ps
Clock Period Jitter during DLL lock-ing period	tJIT(per, lck)	-38	38	ps
Cycle to Cycle Period Jitter	tJIT(cc)_to-tal	94		ps
Cycle to Cycle Period Jitter deter-ministic	tJIT(cc)_dj	47		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	75		ps
Duty Cycle Jitter	tJIT(duty)	TBD	TBD	ps
Cumulative error across 2 cycles	tERR(2per)	-69	69	ps
Cumulative error across 3 cycles	tERR(3per)	-82	82	ps
Cumulative error across 4 cycles	tERR(4per)	-91	91	ps
Cumulative error across 5 cycles	tERR(5per)	-98	98	ps
Cumulative error across 6 cycles	tERR(6per)	-104	104	ps
Cumulative error across 7 cycles	tERR(7per)	-109	109	ps
Cumulative error across 8 cycles	tERR(8per)	-113	113	ps
Cumulative error across 9 cycles	tERR(9per)	-117	117	ps
Cumulative error across 10 cycles	tERR(10per)	-120	120	ps
Cumulative error across 11 cycles	tERR(11per)	-123	123	ps
Cumulative error across 12 cycles	tERR(12per)	-126	126	ps

Cumulative error across 13 cycles	tERR(13per)	-129	129	ps
Cumulative error across 14 cycles	tERR(14per)	-131	131	ps
Cumulative error across 15 cycles	tERR(15per)	-133	133	ps
Cumulative error across 16 cycles	tERR(16per)	-135	135	ps
Cumulative error across 17 cycles	tERR(17per)	-137	137	ps
Cumulative error across 18 cycles	tERR(18per)	-139	139	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = ((1 + 0.68ln(n)) * tJIT(per)_total min) tERR(nper)max = ((1 + 0.68ln(n)) * tJIT(per)_total max)		ps
Command and Address setup time to CK_t, CK_c referenced to Vih(ac) / Vil(ac) levels	tIS(base)	80	-	ps
Command and Address setup time to CK_t, CK_c referenced to Vref levels	tIS(Vref)	180	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vih(dc) / Vil(dc) levels	tIH(base)	105	-	ps
Command and Address hold time to CK_t, CK_c referenced to Vref levels	tIH(Vref)	180	-	ps
Control and Address Input pulse width for each input	tIPW	460	-	ps

Command and Address Timing

Parameter	Symbol	MIN	MAX	Units
CAS_n to CAS_n command delay for same bank group	tCCD_L	max(5 nCK, 5.625 ns)	-	nCK
CAS_n to CAS_n command delay for different bank group	tCCD_S	4	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(2K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group for 2KB page size	tRRD_S(1K)	Max(4nCK,3.7ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to different bank group	tRRD_S(1/ 2K)	Max(4nCK,3.7ns)	-	nCK

for 1/ 2KB page size				
ACTIVATE to ACTIVATE Command delay to same bank group for 2KB page size	tRRD_L(2K)	Max(4nCK,6.4ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1KB page size	tRRD_L(1K)	Max(4nCK,5.3ns)	-	nCK
ACTIVATE to ACTIVATE Command delay to same bank group for 1/2KB page size	tRRD_L(1/ 2K)	Max(4nCK,5.3ns)	-	nCK
Four activate window for 2KB page size	tFAW_2K	Max(28nCK,30ns)	-	ns
Four activate window for 1KB page size	tFAW_1K	Max(20nCK,21ns)	-	ns
Four activate window for 1/2KB page size	tFAW_1/2K	Max(16nCK,15ns)	-	ns
Delay from start of internal write transaction to internal read com-mand for different bank group	tWTR_S	max(2nCK,2.5ns)	-	
Delay from start of internal write transaction to internal read com-mand for same bank group	tWTR_L	max(4nCK,7.5ns)	-	
Internal READ Command to PRE-CHARGE Command delay	tRTP	max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	ns
Write recovery time when CRC and DM are enabled	tWR_CRC _DM	tWR+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for different bank group with both CRC and DM enabled	tWTR_S_CRC_DM	tWTR_S+max (5nCK,3.75ns)	-	ns
delay from start of internal write transaction to internal read com-mand for same bank group with both CRC and DM enabled	tWTR_L_CRC_DM	tWTR_L+max (5nCK,3.75ns)	-	ns
DLL locking time	tDLLK	768	-	nCK
Mode Register Set command cycle time	tMRD	8	-	nCK

Mode Register Set command up-date delay	tMOD	max(24nCK,15ns)	-	
Multi-Purpose Register Recovery Time	tMPRR	1	-	nCK
Multi Purpose Register Write Re-covery Time	tWR_MPR	tMOD (min) + AL + PL	-	-
Auto precharge write recovery + precharge time	tDAL(min)	Programmed WR + roundup (tRP / tCK(avg))		nCK
DQ0 or DQL0 driven to 0 set-up time to first DQS rising edge	tPDA_S	0.5	-	UI
DQ0 or DQL0 driven to 0 hold time from last DQS fall-ing edge	tPDA_H	0.5	-	UI
CS_n to Command Address Latency				
CS_n to Command Address Laten-cy	tCAL	4	-	nCK
DRAM Data Timing				
DQS_t,DQS_c to DQ skew, per group, per access	tDQSQ	-	0.16	tCK(avg)/2
DQ output hold time from DQS_t,DQS_c	tQH	0.76	-	tCK(avg)/2
Data Valid Window per device: tQH - tDQSQ for a device	tDVWd	0.64	-	UI
Data Valid Window per device, per pin: tQH - tDQSQ each device's out-put	tDVWp	0.69	-	UI
Data Strobe Timing				
DQS_t, DQS_c differential READ Preamble	tRPRE	0.9		tCK
DQS_t, DQS_c differential READ Postamble	tRPST	0.33	TBD	tCK
DQS_t,DQS_c differential output high time	tQSH	0.4	-	tCK
DQS_t,DQS_c differential output low time	tQSL	0.4	-	tCK
DQS_t, DQS_c differential WRITE Preamble	tWPRE	0.9	-	tCK
DQS_t, DQS_c differential WRITE Postamble	tWPST	0.33	TBD	tCK
DQS_t and DQS_c low-impedance time (Referenced from RL-	tLZ(DQS)	-360	180	ps

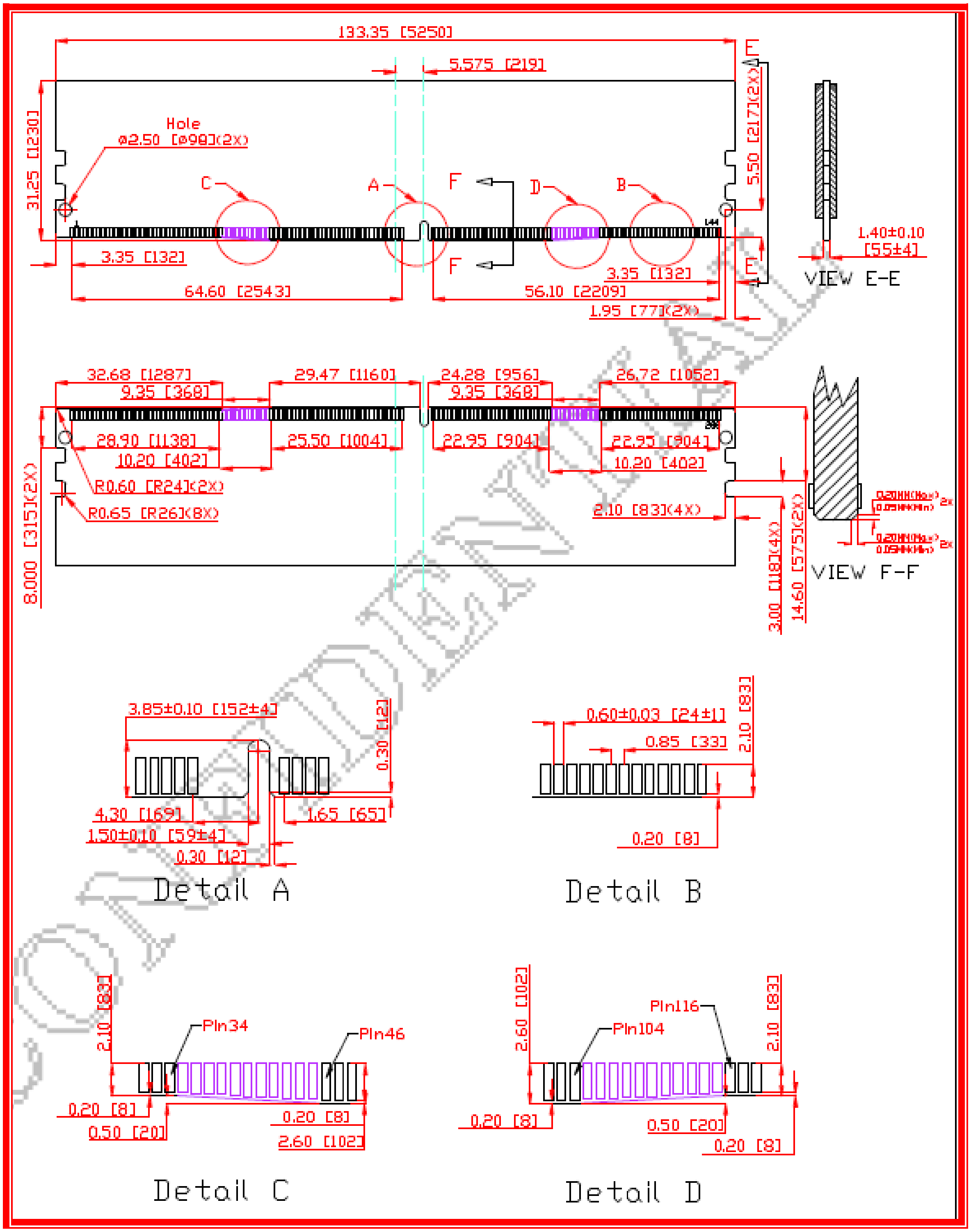
1)				
DQS_t and DQS_c high-impedance time (Referenced from RL+BL/2)	tHZ(DQS)	-	180	ps
DQS_t, DQS_c differential input low pulse width	tDQSL	0.46	0.54	tCK
DQS_t, DQS_c differential input high pulse width	tDQSH	0.46	0.54	tCK
DQS_t, DQS_c rising edge to CK_t, CK_c rising edge (1 clock preamble)	tDQSS	-0.27	0.27	tCK
DQS_t, DQS_c falling edge setup time to CK_t, CK_c rising edge	tDSS	0.18	-	tCK
DQS_t, DQS_c falling edge hold time from CK_t, CK_c rising edge	tDSH	0.18	-	tCK
DQS_t, DQS_c rising edge output timing locatino from rising	tDQSCK (DLL On)	-180	180	ps
DQS_t, DQS_c rising edge output variance window per DRAM	tDQSCKI (DLL On)		310	ps
MPSM Timing				
Command path disable delay upon MPSM entry	tMPED	tMOD(min) + tCPDED(min)	-	
Valid clock requirement after MPSM entry	tCKMPE	tMOD(min) + tCPDED(min)	-	
Valid clock requirement before MPSM exit	tCKMPX	tCKSRX(min)		
Exit MPSM to commands not requiring a locked DLL	tXMP	txs(imin)		
Exit MPSM to commands requiring a locked DLL	tXMPDLL	tXMP(min) + tXSDLL(min)		
CS setup time to CKE	tMPX_S	tISmin + tIHmin	-	
Calibration Timing				
Power-up and RESET calibration time	tZQinit	1024	-	nCK
Normal operation Full calibration time	tZQoper	512	-	nCK
Normal operation Short calibration time	tZQCS	128	-	nCK
Reset/Self Refresh Timing				
Exit Reset from CKE	command tXPR	max	-	

HIGH to a valid command		(5nCK,tRFC(min)+10ns)		
Exit Self Refresh to commands not requiring a locked DLL	tXS	tRFC(min)+10ns	-	
SRX to commands not requiring a locked DLL in Self Refresh ABORT	tX-S_ABORT(min)	tRFC4(min)+10ns	-	
Exit Self Refresh to ZQCL,ZQCS and MRS (CL,CWL,WR,RTP and Gear Down)	tXS_FAST (min)	tRFC4(min)+10ns	-	
Exit Self Refresh to commands re-quiring a locked DLL	tXSDLL	tDLLK(min)	-	
Minimum CKE low width for Self re-fresh entry to exit timing	tCKESR	tCKE(min)+1nCK	-	
Minimum CKE low width for Self re-fresh entry to exit timing with CA Parity enabled	tCKESR_ PAR	tCKE(min)+1nCK+PL	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power- Down when CA Parity is enabled	tCKS-RE_PAR	max(5nCK,10ns)+PL	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	
Power Down Timing				
Exit Power Down with DLL on to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	(4nCK,6ns)	-	
CKE minimum pulse width	tCKE	max (3nCK,5ns)	-	
Command pass disable delay	tCPDED	4	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	2	-	nCK

Timing of PRE or PREA command to Power Down entry	tPRPDEN	2	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRP-BC4DEN	WL+2+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAP-BC4DEN	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	2	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	
PDA Timing				
Mode Register Set command cycle time in PDA mode	tMRD_PDA	max(16nCK,10ns)		
Mode Register Set command up-date delay in PDA mode	tMOD_PDA	tMOD		
ODT Timing				
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONAS	1.0	9.0	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFAS	1.0	9.0	ns
RTT dynamic change skew	tADC	0.3	0.7	tCK(avg)
Write Leveling Timing				
First DQS_t/DQS_n rising edge af-ter write leveling mode is pro-grammed	tWLMRD	40	-	nCK
DQS_t/DQS_n delay after write lev-eling mode is programmed	tWLDQSEN	25	-	nCK
Write leveling setup time from rising CK_t,	tWLS	0.13	-	tCK(avg)

CK_c crossing to rising DQS_t/DQS_n crossing				
Write leveling hold time from rising DQS_t/DQS_n crossing to rising CK_t, CK_ crossing	tWLH	0.13	-	tCK(avg)
Write leveling output delay	tWLO	0	9.5	ns
Write leveling output error	tWLOE			ns
CA Parity Timing				
Commands not guaranteed to be executed during this time	tPAR_UN-KNOWN	-	PL	
Delay from errant command to ALERT_n assertion	tPAR_ALER T_ON	-	PL+6ns	
Pulse width of ALERT_n signal when asserted	tPAR_ALER T_PW	64	128	nCK
Time from when Alert is asserted till controller must start providing DES commands in Persistent CA parity mode	tPAR_ALER T_RSP	-	57	nCK
Parity Latency	PL	4		nCK
CRC Error Reporting				
CRC error to ALERT_n latency	tCRC_ALER T	3	13	ns
CRC ALERT_n pulse width	CRC_ALER T_PW	6	10	nCK
tREFI				
tRFC1 (min)	2Gb	160	-	ns
	4Gb	260	-	ns
	8Gb	350	-	ns
	16Gb	TBD	-	ns
tRFC2 (min)	2Gb	110	-	ns
	4Gb	160	-	ns
	8Gb	260	-	ns
	16Gb	TBD	-	ns
tRFC3 (min)	2Gb	90	-	ns
	4Gb	110	-	ns
	8Gb	160	-	ns
	16Gb	TBD	-	ns

10. Physical Dimension



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

11. RoHS Declaration

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宜鼎國際股份有限公司

Innodisk Corporation

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RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement.

二、本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
鉛（Pb）	< 1000 ppm
汞（Hg）	< 1000 ppm
鎘（Cd）	< 100 ppm
六價鉻（Cr 6+）	< 1000 ppm
多溴聯苯（PBBs）	< 1000 ppm
多溴二苯醚（PBDEs）	< 1000 ppm

立保證書人 (Guarantor)

Company name 公司名稱：Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人：Randy Chien 簡川勝

Company Representative Title 公司代表人職稱：Chairman 董事長

Date 日期：2016 / 08 / 04

Revision Log

Rev	Date	Modification
0.1	6th February 2017	Preliminary Edition
1.0	6th February 2017	Official Released
1.1	13rd July 2017	Modified typo