innodisk

The Total Solution For Industrial Flash Storage

Approval Sheet

Customer	
Product Number	**M3M0-4GSSOCPC**
Module speed	**PC3-12800**
Pin	**244 pin**
Cl-tRCD-tRP	**11-11-11**
SDRAM Operating Temp	**0℃~85℃**
Date	**7th December 2014**

Approval by Customer

P/N:

Signature:

Date:

Sales: **Sr. Technical Manager: John Hsieh**

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)	tRC (ns)
		CL=7	CL=9	CL=11				
PC3-12800	**P**	1066	1333	1600	13.125	13.125	13.125	48.125

- JEDEC Standard 244-pin Dual In-Line Memory Module
- Intend for PC3-12800 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt ± 0.075
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- Ultra Low-profile PCB design
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8μs ($T_A \leq +85°C$)
- 16/10/1 Addressing (row/column/rank)-4GB
- SDRAM operating temperature range
  - $0°C \leq T_A \leq +85°C$
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 7,9,11
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- ECC Function
- RoHS Compliant *(Section 12)*

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +65	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	
H_{OPR}	Operating Humidity (relative)	10 to 90	%	
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.
2. Up to 9850 ft.

3. SDRAM Parameters by device density

RTT_Nom Setting	Parameter		4Gb	Units
tRFC	REF command ACT or REF command time		260	ns
tREFI	Average periodic refresh interval	0°C≦ T_{CASE}≦ **85**°C	7.8	µs
		85°C≦ T_{CASE}≦ **95**°C	3.9	µs

4. Ordering Information

ULP DDR3 ECC Mini-DIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M3M0-4GSSOCPC	4GB	PC3-12800	512Mx72	9	1	Y

5. Pin Configurations (Front side/Back side)

X72 Mini-DIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{TT}	41	CB1	82	V_{SS}	123	V_{TT}	163	V_{SS}	204	DQ36
2	V_{REFDQ}	42	V_{SS}	83	DQ32	124	V_{SS}	164	DM8 or TDQS17 **	205	DQ37
3	V_{SS}	43	/DQS8	84	DQ33	125	DQ4	165	NC *or /TDQS17 **	206	V_{SS}
4	DQ0	44	DQS8	85	V_{SS}	126	DQ5	166	V_{SS}	207	DM4 or TDQS13 **
5	DQ1	45	V_{SS}	86	/DQS4	127	V_{SS}	167	CB6	208	NC *or /TDQS13 **
6	V_{SS}	46	CB2	87	DQS4	128	DM0 or TDQS9 **	168	CB7	209	V_{SS}
7	/DQS0	47	CB3	88	V_{SS}	129	NC * or /TDQS9 **	169	V_{SS}	210	DQ38
8	DQS0	48	V_{SS}	89	DQ34	130	V_{SS}	170	NC *	211	DQ39
9	V_{SS}	49	NC *	90	DQ35	131	DQ6	171	NC *	212	V_{SS}
10	DQ2	50	/Reset	91	V_{SS}	132	DQ7	172	NC * or CKE1 **	213	DQ44
11	DQ3	51	CKE0	92	DQ40	133	V_{SS}	173	V_{DD}	214	DQ45
12	V_{SS}	52	V_{DD}	93	DQ41	134	DQ12	174	A15	215	V_{SS}
13	DQ8	53	BA2	94	V_{SS}	135	DQ13	175	A14	216	DM5 or TDQS14**
14	DQ9	54	NC* or Err_Out **	95	/DQS5	136	V_{SS}	176	V_{DD}	217	NC *or /TDQS14**
15	V_{SS}	55	V_{DD}	96	DQS5	137	DM1 or TDQS10 **	177	A12	218	V_{SS}
16	/DQS1	56	A11	97	V_{SS}	138	NC *or /TDQS10 **	178	A9	219	DQ46
17	DQS1	57	A7	98	DQ42	139	V_{SS}	179	V_{DD}	220	DQ47
18	V_{SS}	58	V_{DD}	99	DQ43	140	DQ14	180	A8	221	V_{SS}
19	DQ10	59	A5	100	V_{SS}	141	DQ15	181	A6	222	DQ52
20	DQ11	60	A4	101	DQ48	142	V_{SS}	182	V_{DD}	223	DQ53
21	V_{SS}	61	V_{DD}	102	DQ49	143	DQ20	183	A3	224	V_{SS}
22	DQ16	62	A2	103	V_{SS}	144	DQ21	184	A1	225	DM6 or TDQS15 **
23	DQ17	63	V_{DD}	104	/DQS6	145	V_{SS}	185	V_{DD}	226	NC *or /TDQS15 **
24	V_{SS}	64	CK1 or NA**	105	DQS6	146	DM2 or TDQS11 **	186	CK0	227	V_{SS}
25	/DQS2	65	/CK1 or NA**	106	V_{SS}	147	NC *or /TDQS11 **	187	/CK0	228	DQ54
26	DQS2	66	V_{DD}	107	DQ50	148	V_{SS}	188	V_{DD}	229	DQ55
27	V_{SS}	67	V_{REFCA}	108	DQ51	149	DQ22	189	V_{DD}	230	V_{SS}
28	DQ18	68	V_{DD}	109	V_{SS}	150	DQ23	190	/EVENT	231	DQ60
29	DQ19	69	NC * or Par_in **	110	DQ56	151	V_{SS}	191	A0	232	DQ61
30	V_{SS}	70	V_{DD}	111	DQ57	152	DQ28	192	V_{DD}	233	V_{SS}
31	DQ24	71	A10	112	V_{SS}	153	DQ29	193	BA1	234	DM7 or TDQS16 **
32	DQ25	72	BA0	113	/DQS7	154	V_{SS}	194	V_{DD}	235	NC *or /TDQS16 **
33	V_{SS}	73	V_{DD}	114	DQS7	155	DM3 or TDQS12 **	195	/RAS	236	V_{SS}
34	/DQS3	74	/WE	115	V_{SS}	156	NC *or /TDQS12 **	196	/CS0	237	DQ62
35	DQS3	75	/CAS	116	DQ58	157	V_{SS}	197	V_{DD}	238	DQ63
36	V_{SS}	76	V_{DD}	117	DQ59	158	DQ30	198	ODT0	239	V_{SS}
37	DQ26	77	NC * or /CS1 **	118	V_{SS}	159	DQ31	199	A13	240	V_{DDSPD}
38	DQ27	78	NC * or ODT1 **	119	SA0	160	V_{SS}	200	V_{DD}	241	SA1
39	V_{SS}	79	V_{DD}	120	SCL	161	CB4	201	NC *	242	SDA
40	CB0	80	NC *	121	SA2	162	CB5	202	NC *	243	V_{SS}
		81	NC *	122	V_{TT}			203	V_{SS}	244	V_{TT}

* NC = No Connect
** 2 Ranks MiniDIMM use.
*** Pin might conneceted to NC ball or DRAMs (depanding on density); alternatively may connect to termination resistor

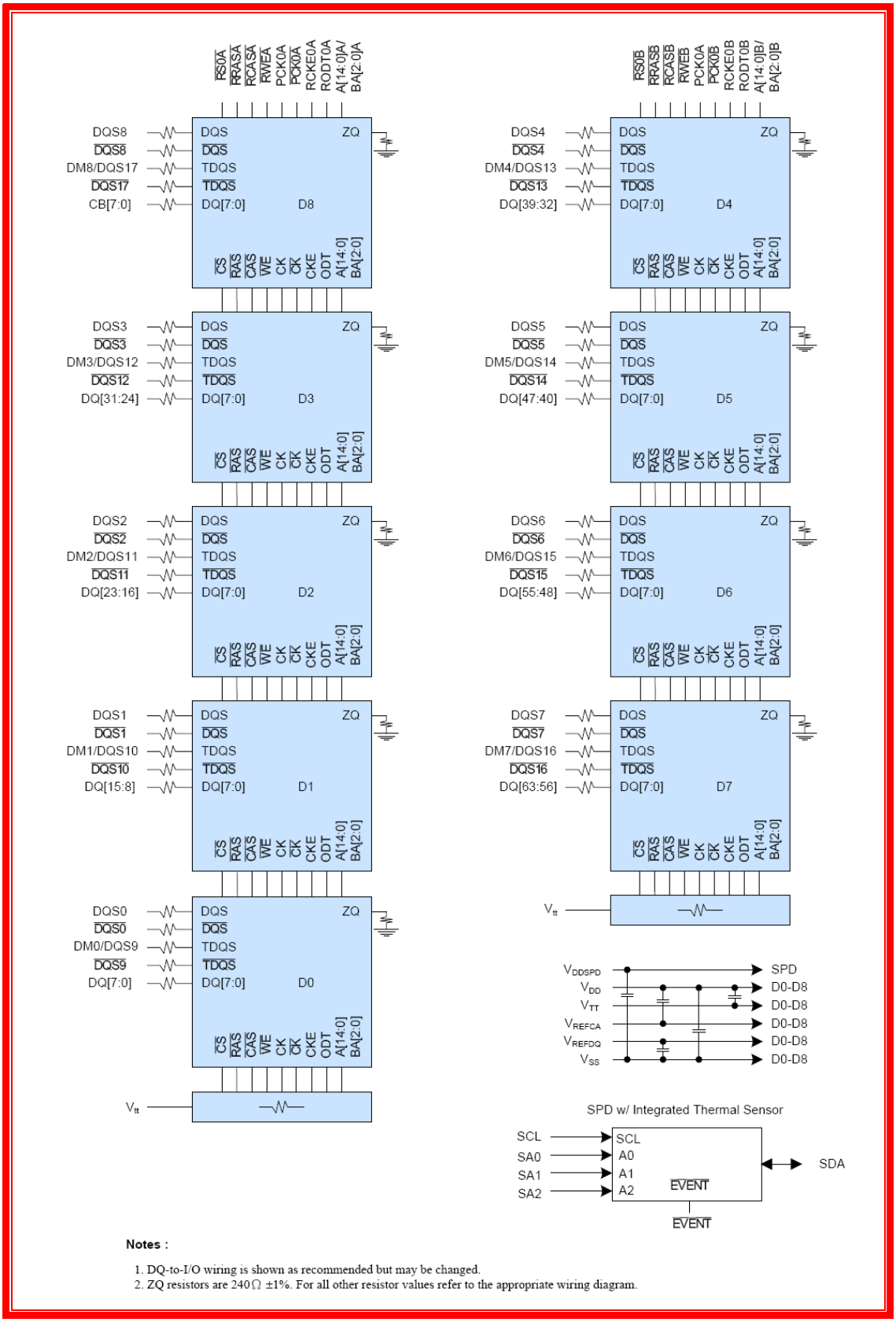
6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	V_{DD}	Power Supply
/WE	SDRAM write enable	V_{DDID}	V_{DD} Identification Flag
/CS0 - /CS1	DIMM Rank Select Lines	V_{DDQ}	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V_{REFDQ}	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V_{REFCA}	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	V_{TT}	SDRAM I/O termination supply.

7. Function Block Diagram:

- (4GB, 1 Rank, 512Mx8 DDR3 SDRAMs)



Notes :

1. DQ-to-I/O wiring is shown as recommended but may be changed.
2. ZQ resistors are 240Ω ±1%. For all other resistor values refer to the appropriate wiring diagram.

8. SDRAM Absolute Maximum Ratings

Symbol	Parameter		Rating	Units	Note
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature		-55 to 100	°C	4,5
V_{IN}, V_{OUT}	Voltage on any pins relative to Vss		-0.4 to +1.975	V	4
V_{DD}	Voltage on VDD supply relative to Vss		-0.4 to +1.975	V	4,6
V_{DDQ}	Voltage on VDDQ supply relative to Vss		-0.4 to +1.975	V	4,6

Note:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM.
For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under
all operating conditions.
3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 ℃ case temperature. Full specifications are supported in this range, but the following additional
conditions apply:
   a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 µs. It is also possible to specify a component with 1X refresh (tREFI to 7.8µs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
   b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.
4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
$V_{IH\ (DC)}$	DC Input High (Logic1) Voltage	V_{REF} + 0.1	-	V_{DD}	V	3
$V_{IL\ (DC)}$	DC Input Low (Logic 0) Voltage	V_{SS}	-	V_{REF} - 0.1	V	3
$V_{IH\ (AC)}$	AC Input High (Logic1) Voltage	V_{REF}+ 0.175	-	-	V	3
$V_{IL\ (AC)}$	AC Input Low (Logic 0) Voltage	-	-	V_{REF} - 0.175	V	3
$V_{REFDQ\ (DC)}$	Reference Voltage for DQ, DM inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
$V_{REFCA\ (DC)}$	Reference Voltage for ADD,CMD inputs	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	4,5
Single Ended AC/DC output Levels						
$V_{OH\ (DC)}$	DC output high measurement level (for IV curve linearity)	-	0.8 x VDDQ	-	V	
$V_{OM\ (DC)}$	DC output mid measurement level (for IV curve linearity)	-	0.5 x VDDQ	-	V	
$V_{OL\ (DC)}$	DC output low measurement level (for IV curve linearity)	-	0.2 x VDDQ	-	V	
$V_{OH\ (AC)}$	AC output high measurement level (for output SR)	-	VTT + 0.1 x VDDQ	-	V	6
$V_{OL\ (AC)}$	AC output low measurement level (for output SR)		VTT - 0.1 x VDDQ	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
V_{IHdiff}	Differential Input high	+0.2	-	Note 9	V	7
V_{ILdiff}	Differential Input logic Low	Note 9	-	-0.2	V	7
$V_{IHdiff(ac)}$	Differential Input high ac	2* ($V_{IH\ (AC)}$-V_{REF})	-	Note 9	V	8
$V_{ILdiff(ac)}$	Differential Input logic Low ac	Note 9	-	2* (V_{REF}-$V_{IL\ (AC)}$)	V	8
Differential AC and DC Output Levels						
$V_{OHdiff(AC)}$	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
$V_{OLdiff(AC)}$	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10

Note:

1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.
4. The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).
5. For reference: approx. VDD/2 +/- 15 mV.
6. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2
7. Used to define a differential signal slew-rate.
8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.
9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.
10. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs.

10. Operating, Standby, and Refresh Currents

- 4GB ECC Mini-DIMM (1 Rank, 512Mx8 DDR3 SDRAMs T_{CASE} = 0 °C ~ 85 °C)

Symbol	Parameter/Condition		PC3-12800	Unit
I DD0	One bank; Active - Precharge		279	mA
I DD1	One bank; Active - Read - Precharge		378	mA
I DD2N	Precharge Standby Current		117	mA
IDD2NT	Precharge Standby ODT Current		135	mA
I DD2P	Precharge Power Down Current	Fast Mode	99	mA
	Precharge Power Down Current	Slow Mode	99	mA
I DD2Q	Pecharge Quiet Standby Current		108	mA
I DD3N	Active Standby Current		207	mA
I DD3P	Active Power-Down Current		99	mA
I DD4R	Operating Current Burst Read		675	mA
I DD4W	Operating Current Burst Write		675	mA
I DD5B	Burst Refresh Current		1800	mA
I DD6	Self-Refresh Current: Normal Temperature Range		135	mA
I DD7	Operating Bank Interleave Read Currentt		1215	mA
I DD8	Reset Current		135	mA

11. Timing Parameters

(T_{CASE} = 0 °C ~ 85 °C; V_{DDQ} = V_{DD} , See AC Characteristics)

Symbol	Parameter	PC3-12800		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.5	3.3	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-70	70	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-60	60	Ps
JIT (CC)	Cycle to Cycle Period Jitter	140		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	120		Ps
TJIT (duty)		-	-	Ps
TERR (2per)	Cumulative error across 2 cycle	-103	103	Ps
TERR (3per)	Cumulative error across 3 cycle	-122	122	Ps
TERR (4per)	Cumulative error across 4 cycle	-136	136	Ps
TERR (5per)	Cumulative error across 5 cycle	-147	147	Ps
TERR (6per)	Cumulative error across 6 cycle	-155	155	Ps
TERR (7per)	Cumulative error across 7 cycle	-163	163	Ps
TERR (8per)	Cumulative error across 3 cycle	-169	169	Ps
TERR (9per)	Cumulative error across 4 cycle	-175	175	Ps
TERR (10per)	Cumulative error across 5 cycle	-180	180	Ps

TERR (11per)	Cumulative error across 6 cycle	-184	184	Ps
TERR (12per)	Cumulative error across 7 cycle	-188	188	Ps
TERR (nper)	Cumulative error across 13~50 cycle	$t_{ERR(nper)min} = (1 + 0.68ln(n)) * t_{JIT(per)min}$ $t_{ERR(nper)max} = (1 + 0.68ln(n)) * t_{JIT(per)max}$		Ps
Data Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDSQ	DQS, DQS# to DQ skew, per group, per access	-	100	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-450	225	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	225	Ps
tDS(base) AC150	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	10	-	Ps
tDH(base) DC 100	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	45	-	Ps
Data Strobe Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps

tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
Command and Address Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK

tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	35	9 tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	40	-	ns
tIS (base) AC175	Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	45		ns
tIH(base) AC150	Command and Address hold time from CK, CK# referenced to Vih(ac) / Vil(ac) levels	170		ps
tIS(base) DC100	Command and Address setup time to CK, CK# referenced to Vih(dc) / Vil(dc) levels	120		ps
Calibration Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tZQinit	Power-up and RESET calibration time	Max. (512nCK, 640ns)	-	nCK
tZQoper	Normal operation Full calibration time	Max. (256nCK, 320ns)	-	nCK
tZQCS	Normal operation Short calibration time	Max. (64nCK, 80ns)	-	nCK

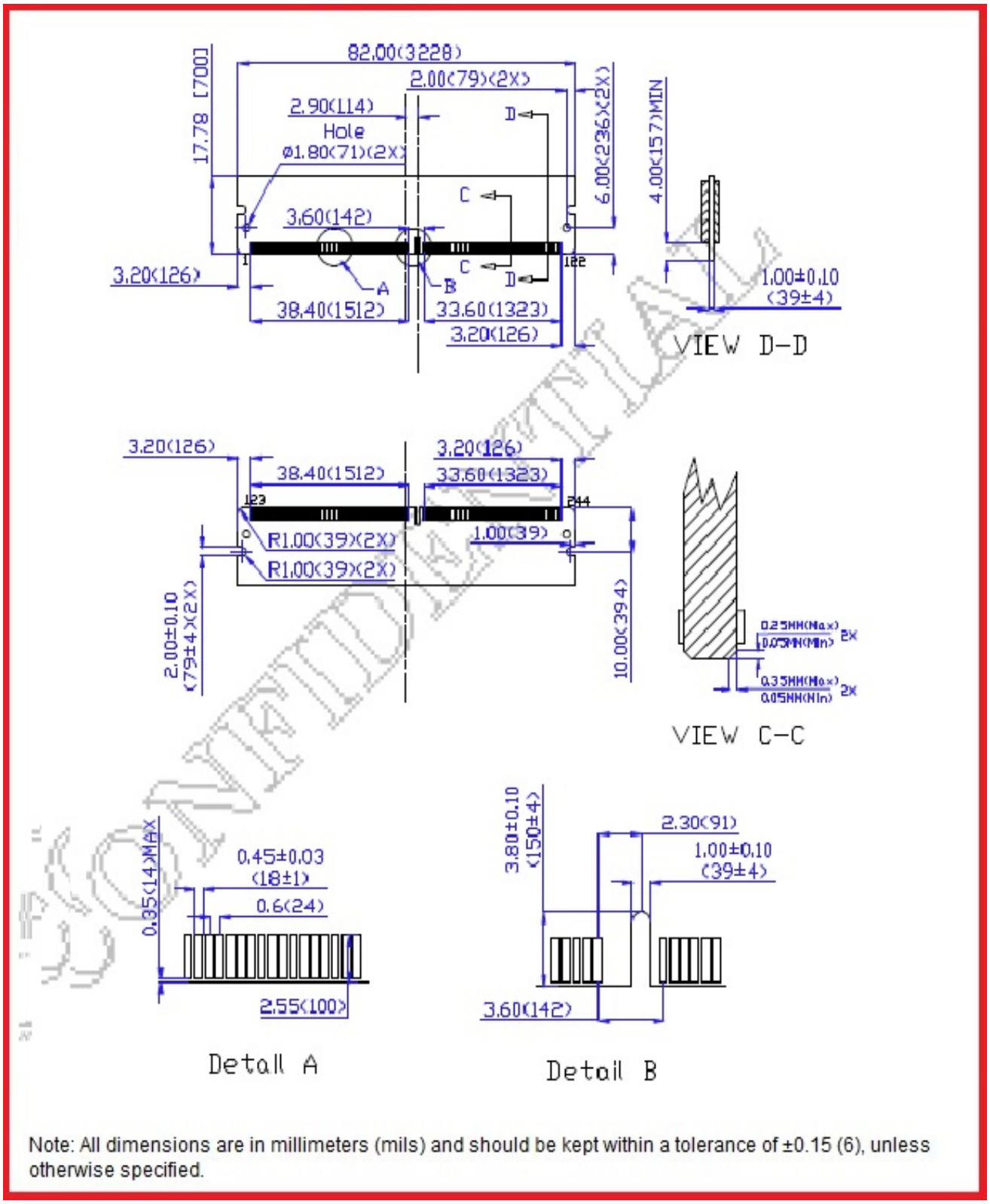
Reset Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK,tRFC(min) +10ns)	-	
Self Refresh Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC(min) +10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE(min) +1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK,10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK,10ns)	-	
Power Down Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK CK, 24ns)	-	

tCKE	CKE minimum pulse width	max(3nCK,5ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCK(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK

tAONPD	Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns
tAON	RTT-turn-on	-225	225	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)

12.PACKAGE DIMENSION

- (4GB, 1 Rank, 512Mx8 DDR3 base Mini-DIMMw/ECC)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

13. RoHS Declaration

Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M3M0-4GSSOCPC complies with the requirement of RoHS directives 2002/95/EC and 2006/122/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	**Limited of RoHS ppm（mg/kg）**
Cd	＜ 100 ppm
Pb	＜ 1000 ppm
Hg	＜ 1000 ppm
Chromium VI（Cr+6）	＜ 1000 ppm
Polybromodiphenyl ether（PBDE）	＜ 1000 ppm
Polybrominated Biphenyls（PBB）	＜ 1000 ppm
Perfluorooctane Sulfonate (PFOS)	Not Contained

Date issued : 2014/01/01

Manufacturer: ：InnoDisk Co., Ltd.
Address：9F, No. 100, Sec.1 Xintai 5th Rd., Xizhi City, Taipei 221, Taiwan

Authorized Signature：

QA Dept. Director – *Ryan Tsai*

Revision Log

Rev	Date	Modification
0.1	7th April 2014	Preliminary Edition
1.0	7th April 2014	Official Released.