innodisk

Total Solution For
Industrial Flash Storage

EDC 1SE

Standard

Customer: _____

Customer Part Number: _____

Innodisk Part Number: _____

Innodisk Model Name: _____

Date: _____

Innodisk Approver	Customer Approver

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REVISION HISTORY

Revision	Description	Date
1.0	Release first version	April, 2014

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1. Product Overview

1.1 Introduction to Embedded Disk Card 1SE

Embedded Disk Card 1SE (EDC1SE) products provide high capacity solid-state flash memory that electrically complies with the Personal Computer Memory Card International Association ATA standard. Innodisk Embedded Disk Card 1SE (EDC1SE) is embedded solid-state data storage systems for industrial work place. Embedded Disk Card 1SE (EDC1SE) features an extremely light weight, reliable, low-profile form factor. Embedded Disk Card 1SE (EDC1SE) supports advanced PIO (0-4), Multi Word DMA (0-2), Ultra DMA (0-4) transfer modes, multi-sector transfers, and LBA addressing.

1.2 Product Models

Embedded Disk Card 1SE (EDC1SE) is available in capacities ranging from 128MB to 4GB, making the upgrade path simple and fast. Available in 40-pin and 44-pin horizontal connector packages, EDC1SE fits into any platform with an IDE connector.

1.3 Features

The Industrial ATA products provide the following system features:

- Capacities: 128MB to 8GB(only for horizontal types)
- Fully compatible with the IDE standard interface, ATA Standard
- Access modes: True IDE Mode
- ECC (Error Correction Code) function: 4 bits/ per 512 byte
- +3.3V/+5V single power supply operation
- Support Auto Stand-by and Sleep Mode.
- Support transfer modes: PIO(0-4), Multiword DMA (0-2) and Ultra DMA(0-4)
- MTBF 3,000,000 hours
- R/W performance:
  - Single Channel: 128MB~2GB
    - ◆ Sustain Read: 20Mbytes/s. (MAX)
    - ◆ Sustain Write: 10Mbytes/s (MAX)
  - Dual Channel
    - 1GB~4GB(vertical type);1GB~8GB(horizontal type)
    - ◆ Sustain Read: 40Mbytes/s. (MAX)
    - ◆ Sustain Write: 20Mbytes/s (MAX)
    - 8GB(horizontal type),
    - ◆ Sustain Read: 40Mbytes/s. (MAX)
    - ◆ Sustain Write: 28Mbytes/s (MAX)

- Operating temperature range:

- Standard Grade: 0°C ~ +70°C
- Industrial Grade: -40°C ~ +85°C

- Storage temperature range: -55°C ~ +95°C

1.4 Pin Assignment

EDC 1SE uses a standard IDE pin-out. See Table 3 for EDC1SE pin assignments.

Table 1: EDC1SE Pin Assignment

Pin No.	Name	Function	Pin No.	Name	Function
1	HRESET	Host Reset	2	GND	Ground
3	HDB[7]	Host Data Bit 7	4	HDB[8]	Host Data Bit 8
5	HDB[6]	Host Data Bit 6	6	HDB[9]	Host Data Bit 9
7	HDB[5]	Host Data Bit 5	8	HDB[10]	Host Data Bit 10
9	HDB[4]	Host Data Bit 4	10	HDB[11]	Host Data Bit 11
11	HDB[3]	Host Data Bit 3	12	HDB[12]	Host Data Bit 12
13	HDB[2]	Host Data Bit 2	14	HDB[13]	Host Data Bit 13
15	HDB[1]	Host Data Bit 1	16	HDB[14]	Host Data Bit 14
17	HDB[0]	Host Data Bit 0	18	HDB[15]	Host Data Bit 15
19	GND	Ground	20	40-pin / VCC[1]	Supply Voltage
				44pin / KEY[1]	Key-pin
21	DMARQ	DMA Request	22	GND	Ground
23	HIOW[3]	Host I/O Write	24	GND	Ground
	STOP[4]	Stop Ultra DMA burst			
25	HIOR[3]	Host I/O Read	26	GND	Ground
	HDMARDY[4]	Ultra DMA ready			
	HSTROBE[4]	Ultra DMA data strobe			
27	IORDY[3]	I/O Ready	28	CSEL	Master/Slave Select (Switch used)
	DDMARDY[4]	Ultra DMA ready			
	DSTROBE[4]	Ultra DMA data strobe			
29	DMACK	DMA Acknowledge	30	GND	Ground
31	INTRQ	Interrupt Request	32	IOCS16	CS I/O 16-Bit
33	HAB[1]	Host Address Bit 1	34	PDIAG	Passed Diagnostic
Pin No.	Name	Function	Pin No.	Name	Function
35	HAB[0]	Host Address Bit 0	36	HAB[2]	Host Address Bit 2
37	CS0	Chip Select 0	38	CS1	Chip Select 1
39	DASP	Drive Active	40	GND	Ground
41[2]	VCC	Supply Voltage	42[2]	VCC	Supply Voltage
43[2]	GND	Ground	44[2]	NC	Not Connected

1. In the 40-pin version, this pin is defined as VCC to reduce the need for an external power connector. In the 44-pin version, this pin is defined as KEY, according to the ATA standard.
2. The 40-pin version does not contain pins 41-44.
   NC = These pins are not connected internally.
3. Signal usage in PIO & Multiword DMA mode.
4. Signal usage in Ultra DMA mode.

1.5 Pin Description

Table 4 describes the pin descriptions for EDC1SE

Table 2: EDC1SE Pin Description

Pin Name	Pin No.	Description	I/O
Host side pins			
HRESET-	1	Host reset signal, High: Reset.	I
CS0-	37	Chip select CS0	I
CS1-	38	Chip select CS1	I
INTRQ	31	Host interrupt signal.	O
HIOR-[3]	25	I/O read strobe signal.	I
HDMARDY-[4]		DMA ready during Ultra DMA data in burst	
HSTROBE[4]		Data strobe during Ultra DMA data out burst	
HIOW-[3]	23	I/O write strobe signal.	I
STOP[4]		Stop during Ultra DMA data bursts	
IOCS16-	32	Asserted in 16-bit access.	O
IORDY[3]	27	I/O Ready Signal	O
DDMARDY-[4]		DMA ready during Ultra DMA data out burst	
DSTROBE[4]		Data strobe during Ultra DMA data in burst	
HDB[15:0]	18, 16, 14, 12, 10, 8, 6, 4, 3, 5, 7, 9, 11, 13, 15, 17	Host data bus	I/O
HAB[2:0]	33, 35, 36	Host Address bus	I/O
CSEL-	28	Master/Slave select signal (cable select signal). Low: Device operates as a master, High: Device operates as a slave. Switch used.	I
DASP-	39	Used as an input port to check in the master mode to see if the slave is present or not, and as an output port to check in the slave mode to see if the slave for the master is present or not.	I/O
PDIAG-	34	Used as an input port to evaluate the result of slave diagnosis in the master mode, and as an output port to return the result of diagnosis to the master.	I/O
DMARQ	21	DMA Request.	O
DMACK-	29	DMA Acknowledge.	I
Power and Ground			
VCC	20[1], 41[2], 42[2]	Connect to VCC	VCC
GND	2, 19, 22, 24, 26, 30, 40, 43[2]	Connect to GND.	GND
Other pins			
NC	44[2]	Not used. Please do not connect.	N/A

1. In the 40-pin version, this pin is defined as VCC to reduce the need for an external power connector. In the 44-pin version, this pin is defined as KEY, according to the ATA standard.
2. The 40-pin version does not contain pins 41-44.
   NC = These pins are not connected internally.
3. Signal usage in PIO & Multiword DMA mode.
4. Signal usage in Ultra DMA mode.

2 Theory of operation

2.1 Overview

Figure 1 shows EDC1SE operation from the system level, including the major hardware blocks.

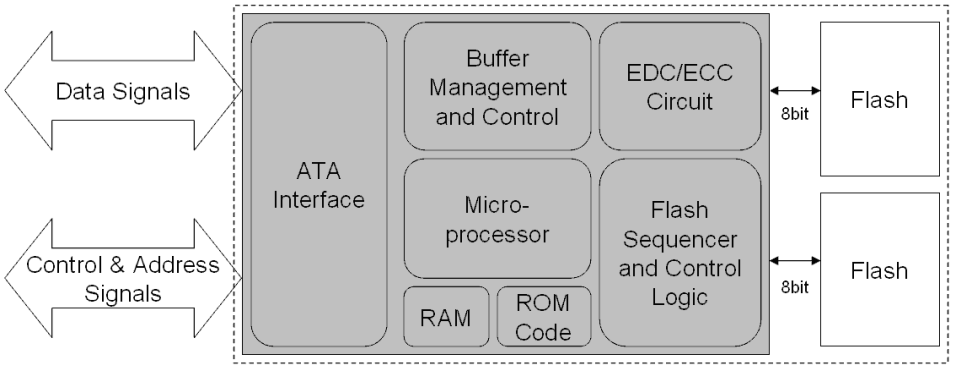


Figure 1: EDC1SE Block Diagram

EDC1SE integrates an IDE controller and flash devices. Communication with the host occurs through the host interface, using the standard ATA protocol. Communication with the flash device(s) occurs through the flash interface.

2.2 Controller

The controller is equipped with 16KB of internal memory that is used for storing code and data. The internal memory can also be used as an intermediate memory for storing data blocks during a wear-leveling procedure. An 8KB internal boot ROM includes basic routines for accessing the flash memories and for loading the main code into the internal memory.

2.3 Error Detection and Correction

Highly sophisticated Error Correction Code algorithms are implemented. The ECC unit consists of the Parity Unit (parity-byte generation) and the Syndrome Unit (syndrome-byte computation). This unit implements a algorithm that can correct 4 bits per 512 bytes in an ECC block. Code-byte generation during write operations, as well as error detection during read operation, is implemented on the fly without any speed penalties.

2.4 Wear-Leveling

Flash memory can be erased a limited number of times. This number is called the ***erase cycle limit*** or ***write endurance limit*** and is defined by the flash array vendor. The erase cycle limit applies to each individual erase block in the flash device.

EDC1SE uses a wear-leveling algorithm to ensure that consecutive writes of a specific sector are not written physically to the same page in the flash. This spreads flash media usage evenly across all pages, thereby maximizing flash lifetime.

3. Installation Requirements

3.1 EDC1SE Pin Directions

From figure 2 to figure 5 are shown for the EDC1SE 40pin and 44pin pin directions.

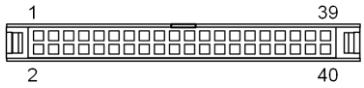


Figure 2: 40-pin Connector Layout (Female)

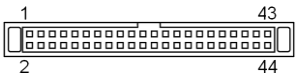


Figure 3: 44-pin Connector Layout (Female)

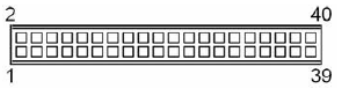


Figure 4: 40-pin Connect Layout (Male)

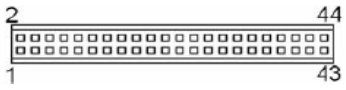


Figure 5: 44-pin Connector Layout (Male)

3.2 Electrical Connections for EDC1SE

EDC1SE can be connected to the host by placing it directly on the on-board socket. If a cable is used, it should be no longer than 20 inches (457mm), and should be aligned as follows:

- For 40-pin EDC1SE:

  Pin 1 of the cable must be aligned with pin 1 of the EDC1SE connector.

  Pin 40 of the cable must be aligned with pin 40 of the EDC1SE connector.

- For 44-pin EDC1SE:

  Pin 1 of the cable must be aligned with pin 1 of the EDC1SE connector.

  Pin 44 of the cable must be aligned with pin 44 of the EDC1SE connector.

The 40-pin EDC1SE version has a separate connector for the power supply, to which a power supply cable can be connected. In addition, pin 20 can also be used for power supply connections. Please refer to the pin

description for further details.

3.3 Installing EDC1SE in a Two-Drive Configuration (Master/Slave)

If EDC1SE is being installed as an additional IDE drive using the same IDE I/O port, Switch S1 in “M” position will be the master, whereas in “S” position it becomes the slave.

4. Power Management

EDC1SE supports the following two operation modes:

Sleep Mode: Internal clock is halted (for EDC1SE, the standby mode defined in the ATA specification is the same as this mode)

Active Mode: Internal clock operates normally (for EDC1SE, the idle mode defined in the ATA specification is the same as this mode)

5. Specifications

5.1 CE, FCC and RoHS Compatibility

◆ *CE and FCC Compatibility*

EDC1SE conforms to CE and FCC requirements.

◆ RoHS Compliance

EDC1SE is fully compliant with RoHS directive.

5.2 Environmental Specifications

5.2.1 Temperature Ranges

Operating Temperature Range:

- Standard Grade: 0°C to +70°C
- Industrial Grade: -40°C to +85°C

Storage Temperature Range: -55°C to +95°C

5.2.2 Humidity

Relative Humidity: 10-95%, non-condensing

5.2.3 Shock and Vibration

Table 3: Shock/Vibration Testing for EDC1SE

Reliability	Test Conditions	Reference Standards
Vibration	7 Hz to 2K Hz, 5G, 3 axes	IEC 68-2-6
Mechanical Shock	Duration: 10ms, 50G, 3 axes	IEC 68-2-27

5.2.4 Mean Time between Failures (MTBF)

Table 4 summarizes the MTBF prediction results for various EDC1SE configurations. The analysis was performed using a RAM Commander™ failure rate prediction.

- **Failure Rate**: The total number of failures within an item population, divided by the total number of life units expended by that population, during a particular measurement interval under stated condition.
- **Mean Time between Failures (MTBF)**: A basic measure of reliability for repairable items: The mean number of life units during which all parts of the item perform within their specified limits, during a particular measurement interval under stated conditions.

Table 4: EDC1SE MTBF

Product	Condition	MTBF (Hours)
40-pin	Telcordia SR-332 GB, 25°C	> 3,000,000
44-pin		> 3,000,000

5.3 Mechanical Dimensions

5.3.1 Vertical type

40pin Vertical (DE0H- XXXD41XXXXX) tolerance±0.3

Mechanical Dimension: 60.2/27.3/6.4 mm±0.3(W/T/H)

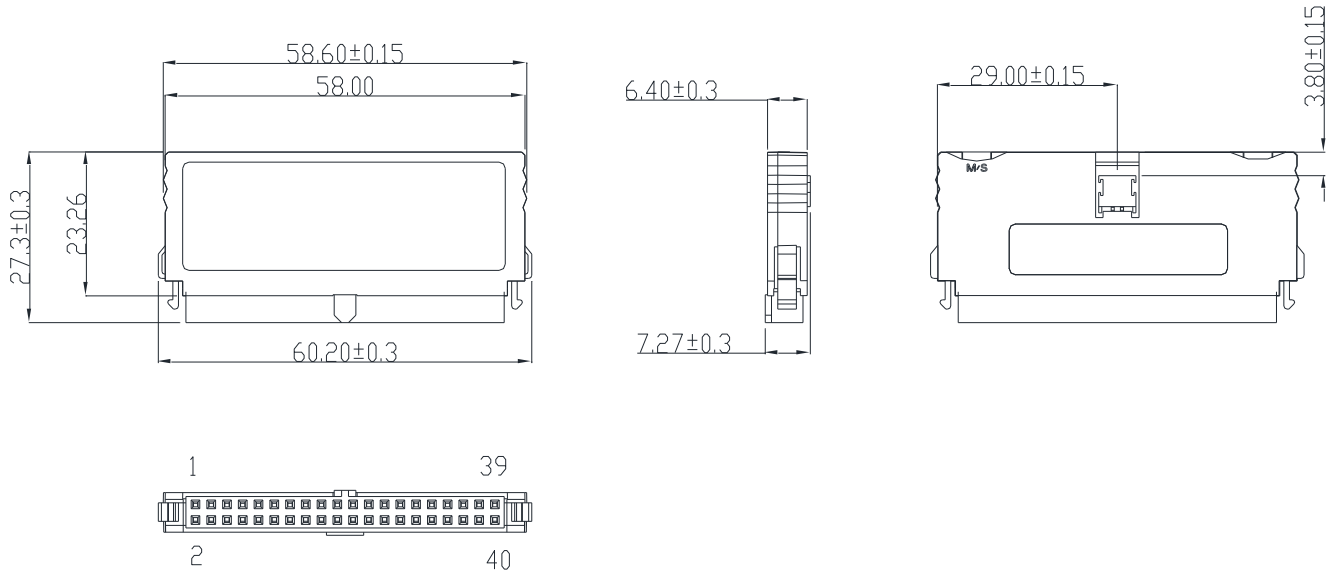


Figure 6: Mechanical Dimension of EDC1SE 40-pin

5.3.2 Horizontal type

40pin Horizontal (DE0PA- XXXD41XXXXX) tolerance±0.3

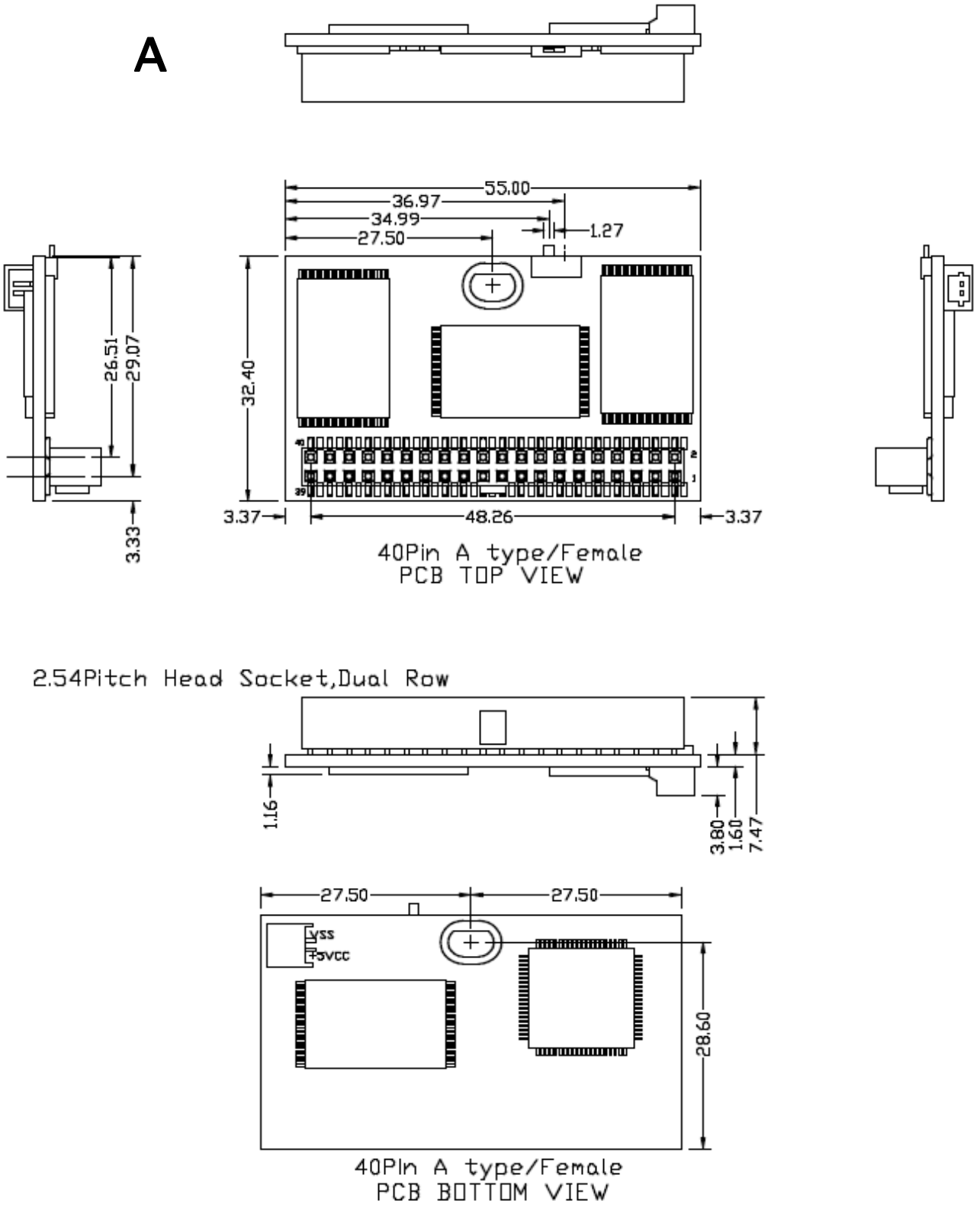


Figure 7: Mechanical Dimension of EDC1SE 40-pin (Horizontal Female Type A)

40pin Horizontal (DE0PB- XXXD41XXXXX) tolerance±0.3

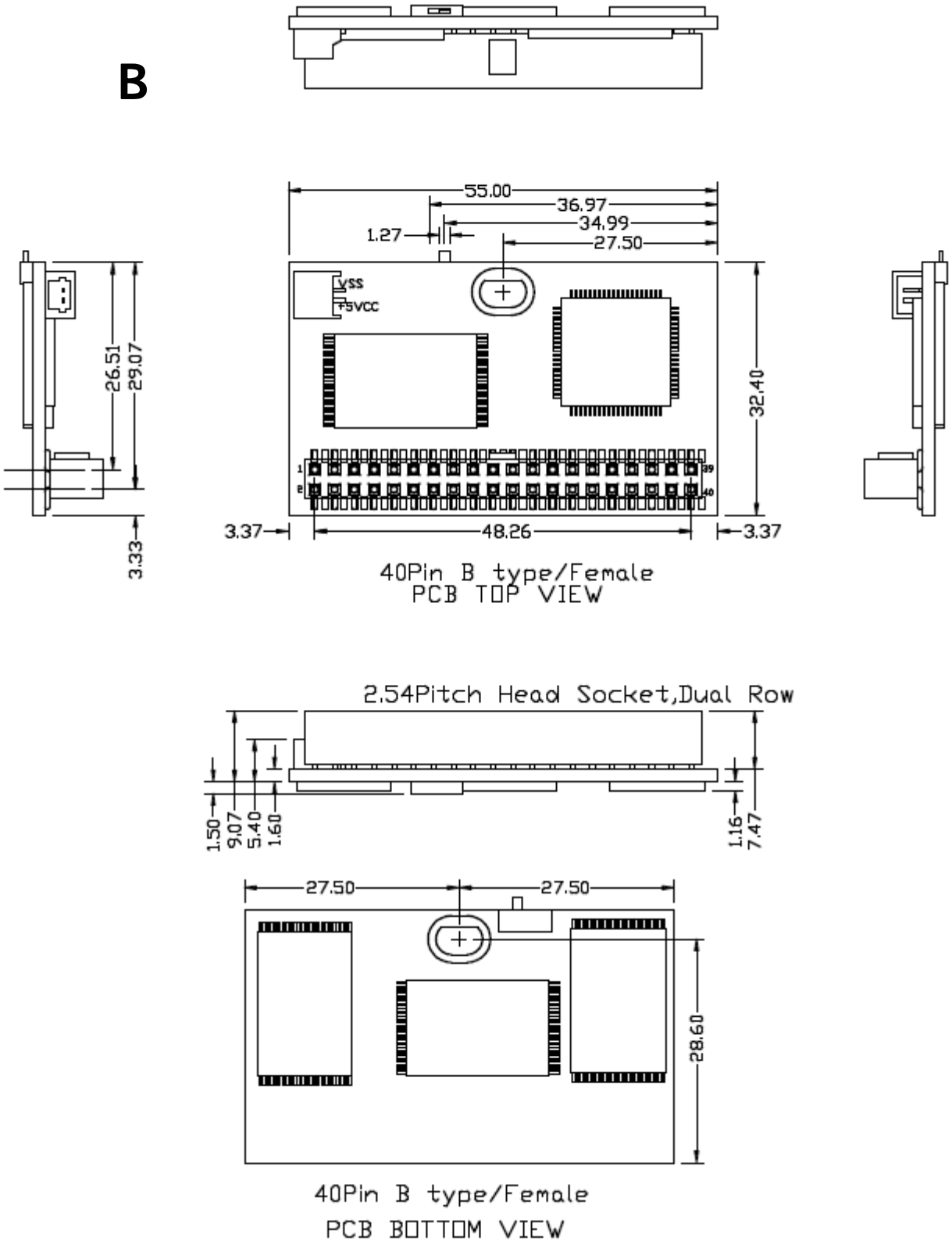


Figure 8: Mechanical Dimension of EDC1SE 40-pin(Horizontal Female Type B)

40pin Horizontal (DE0PC- XXXD41XXXXX) tolerance±0.3

C

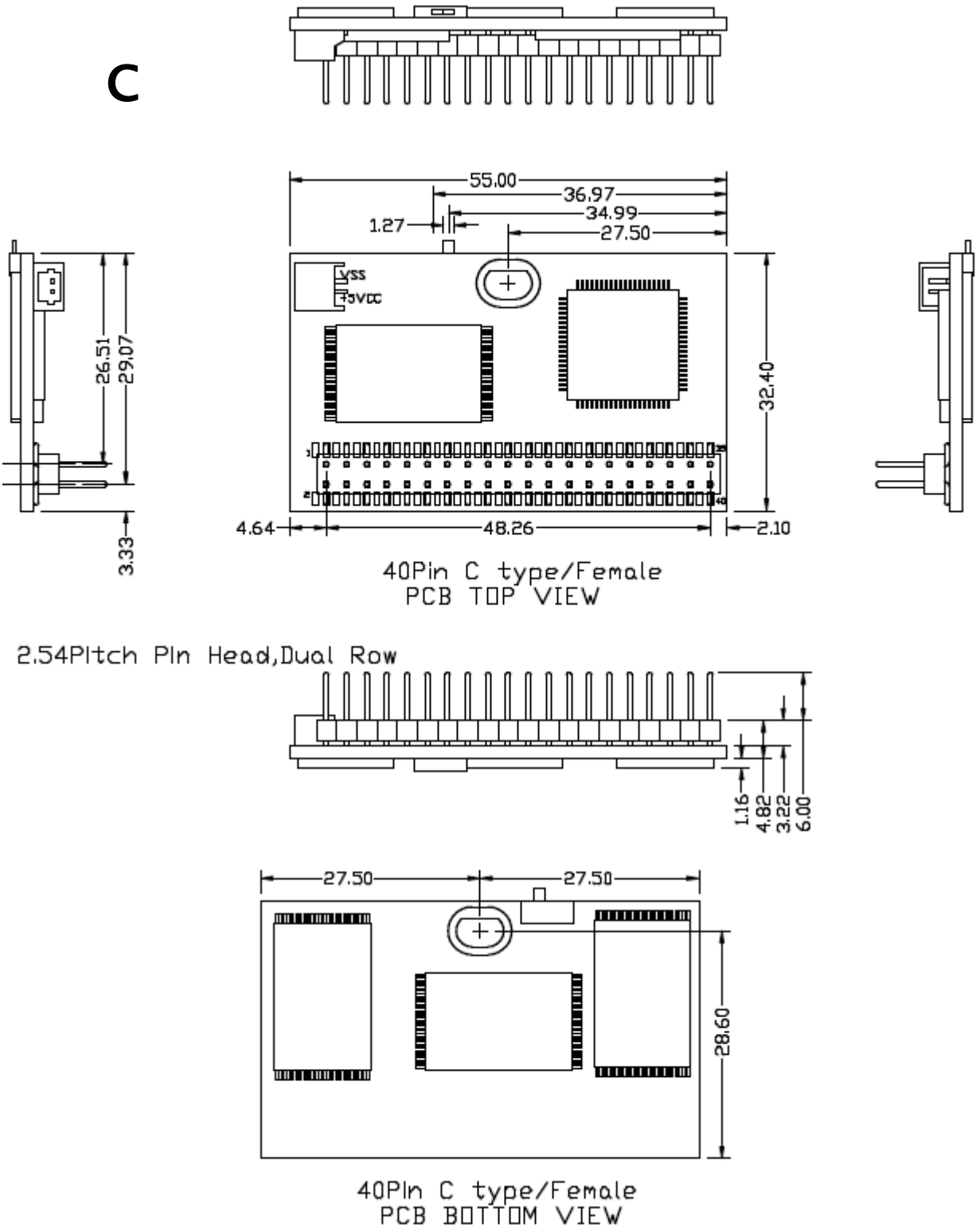


Figure 9: Mechanical Dimension of EDC1SE 40-pin(Horizontal Male Type C)

40pin Horizontal (DE0PD- XXXD41XXXXX) tolerance±0.3

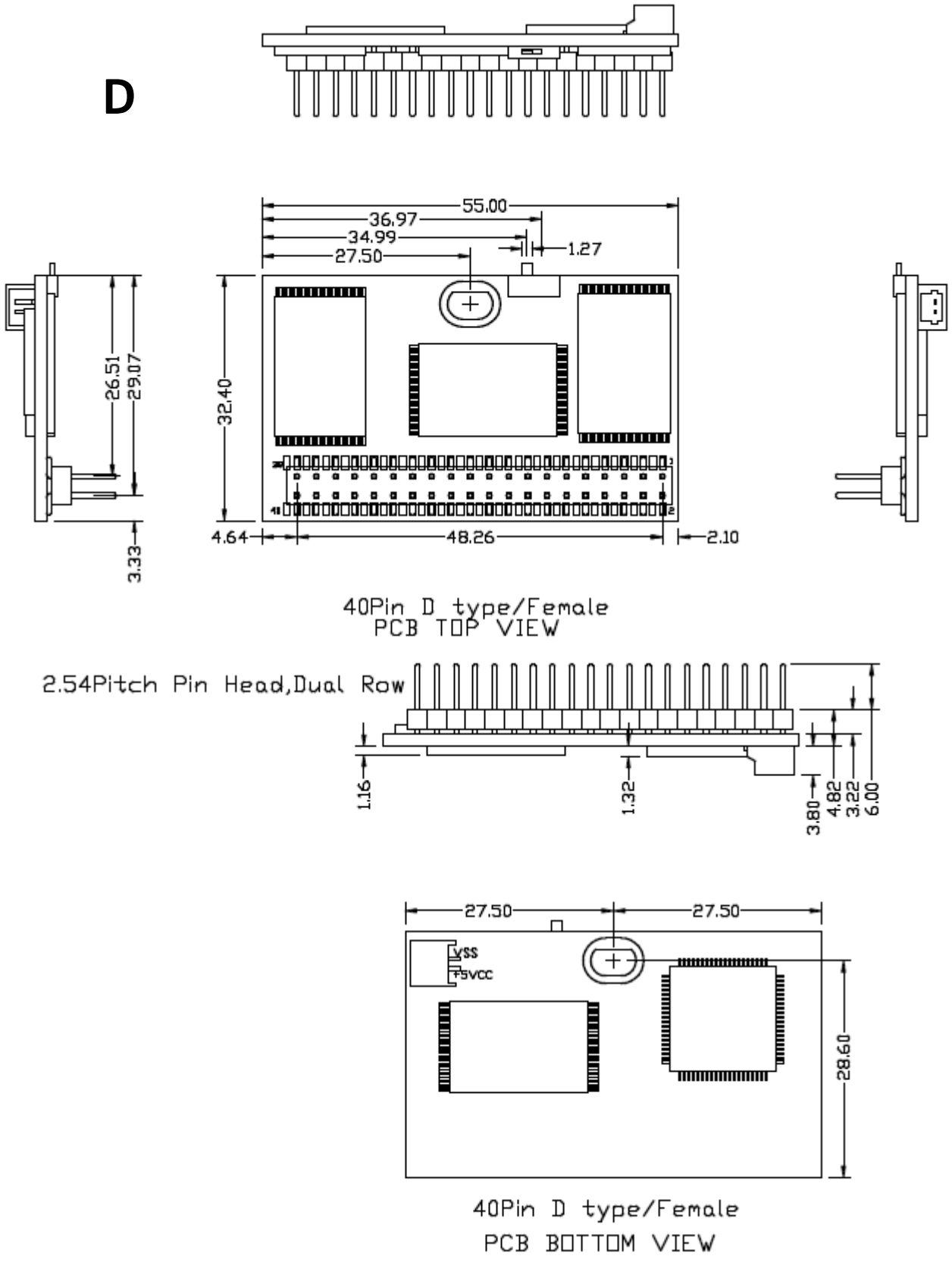


Figure 10: Mechanical Dimension of EDC1SE 40-pin(Horizontal Male Type D)

40pin Horizontal (DE0PE- XXXD41XXXXX) tolerance±0.3

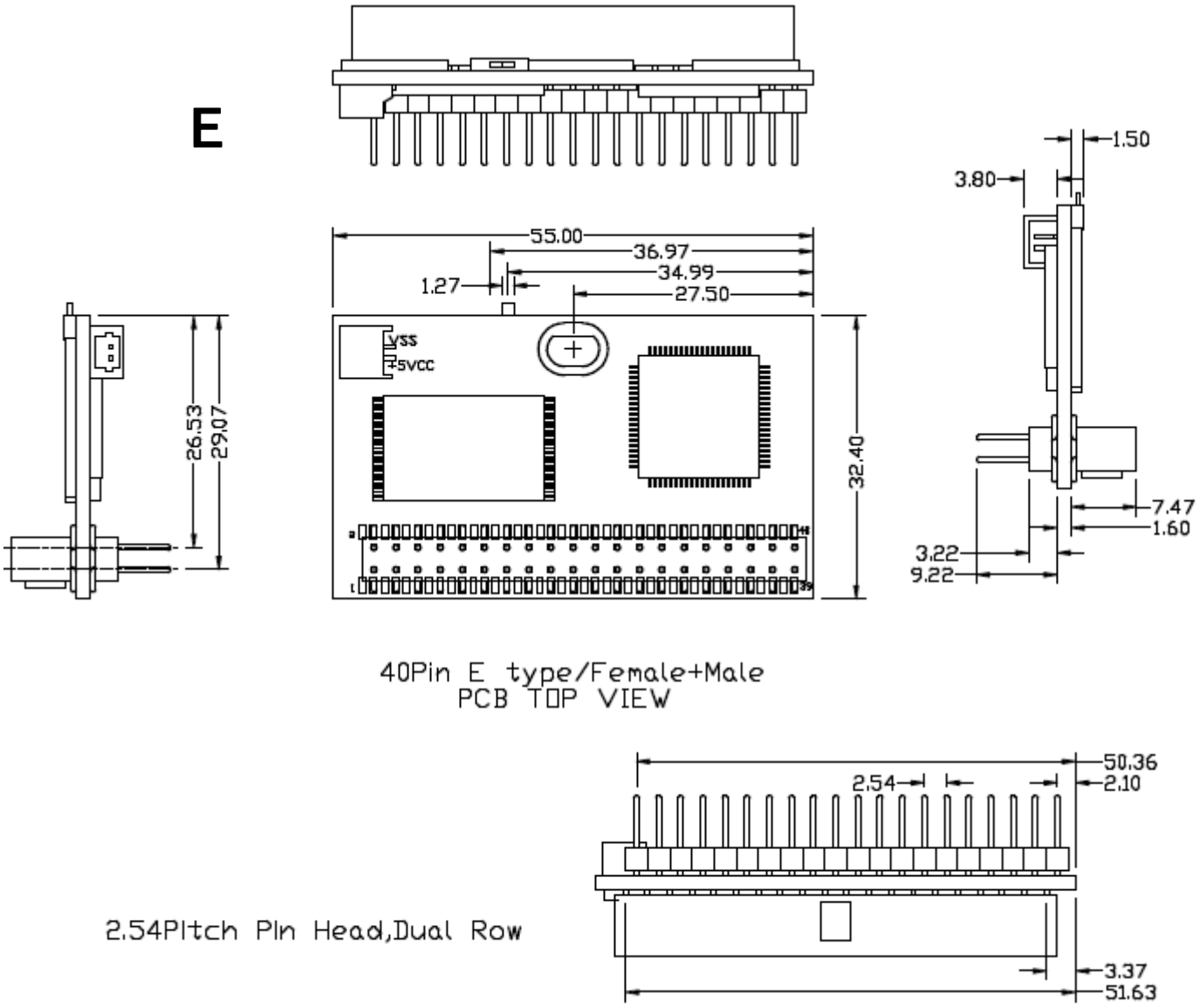


Figure 11: Mechanical Dimension of EDC1SE 40-pin(Horizontal Female/Male Type E)

40pin Horizontal (DE0PF- XXXD41XXXXX) tolerance±0.3

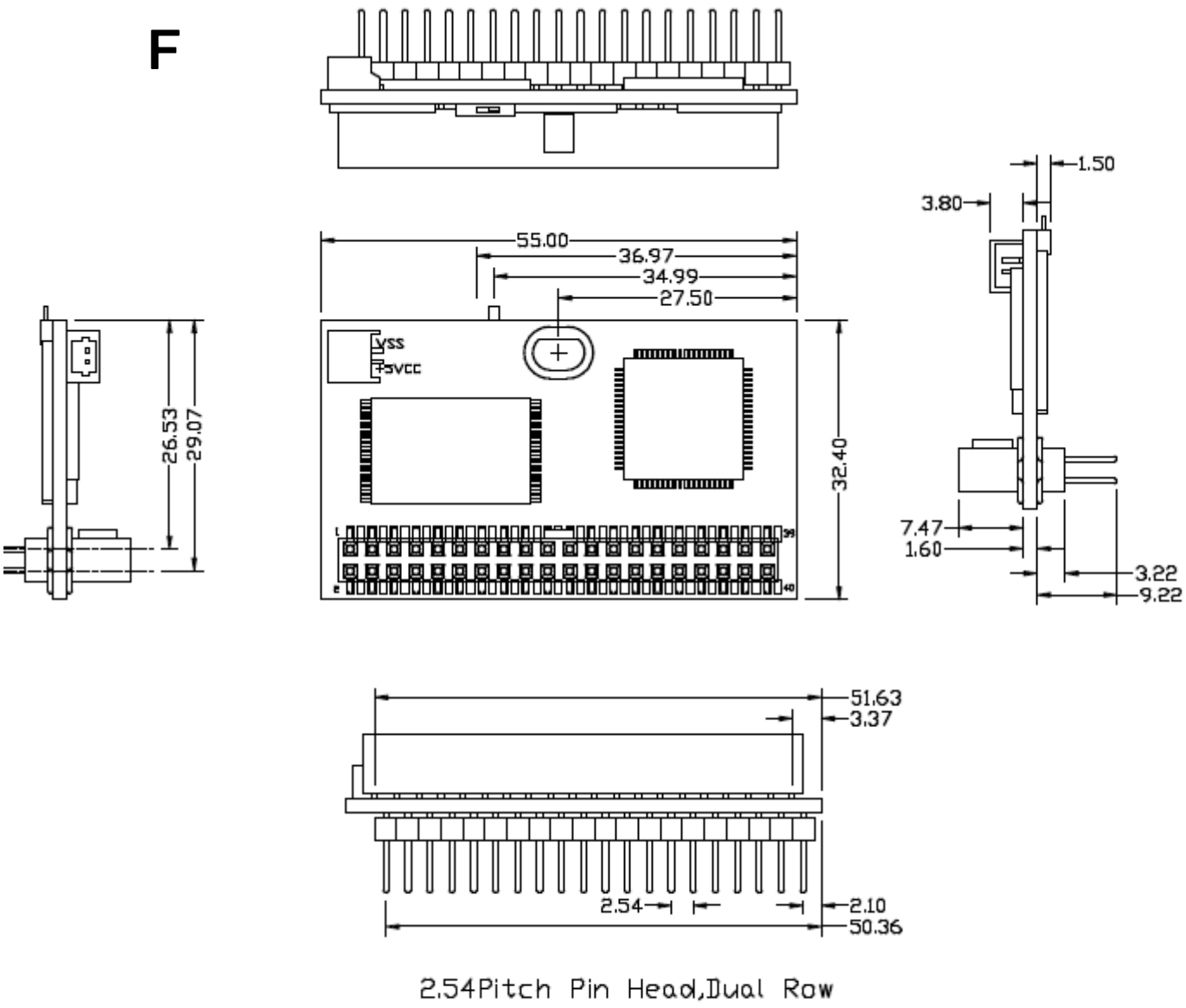


Figure 12: Mechanical Dimension of EDC1SE 40-pin(Horizontal Male/Female Type F)

44-pin

44pin Vertical (DE4H- XXXD41XXXXX) tolerance±0.3

Mechanical Dimension: 50.3/27.3/5.8 mm ± 0.3mm(W/T/H)

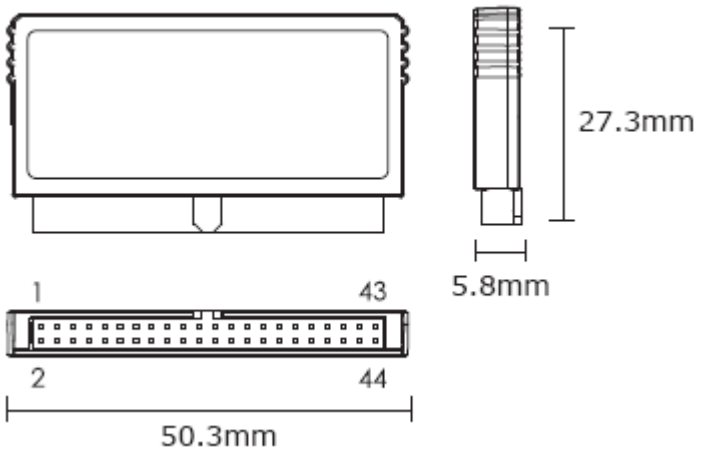
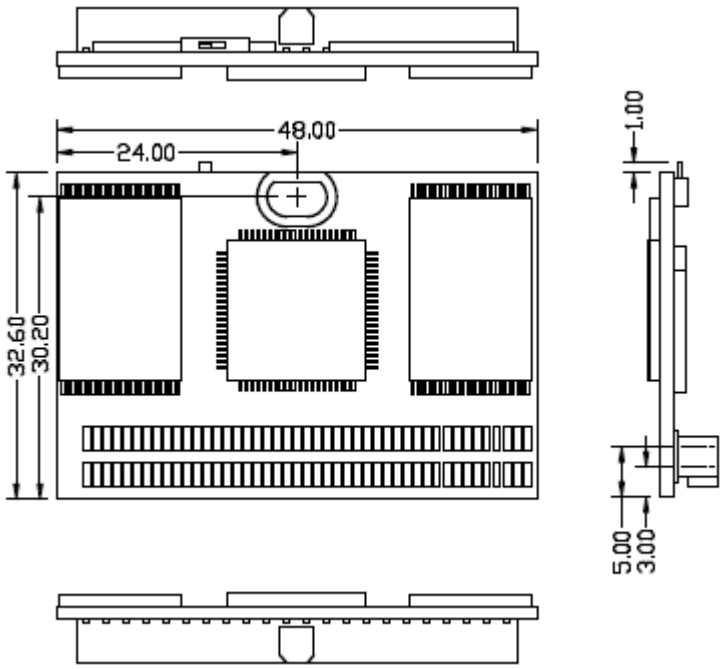


Figure 13: Mechanical Dimension of EDC1SE 44-pin (Vertical Version)

44pin Horizontal (DE4PA- XXXD41XXXXX) tolerance±0.3

A



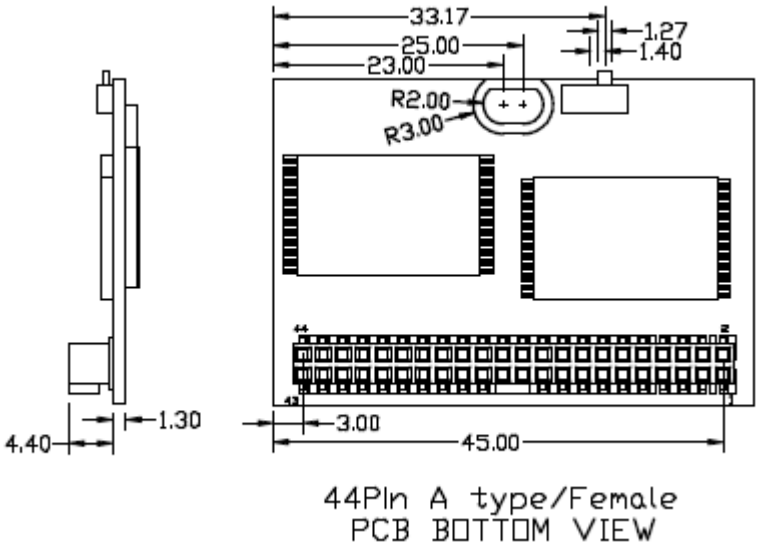
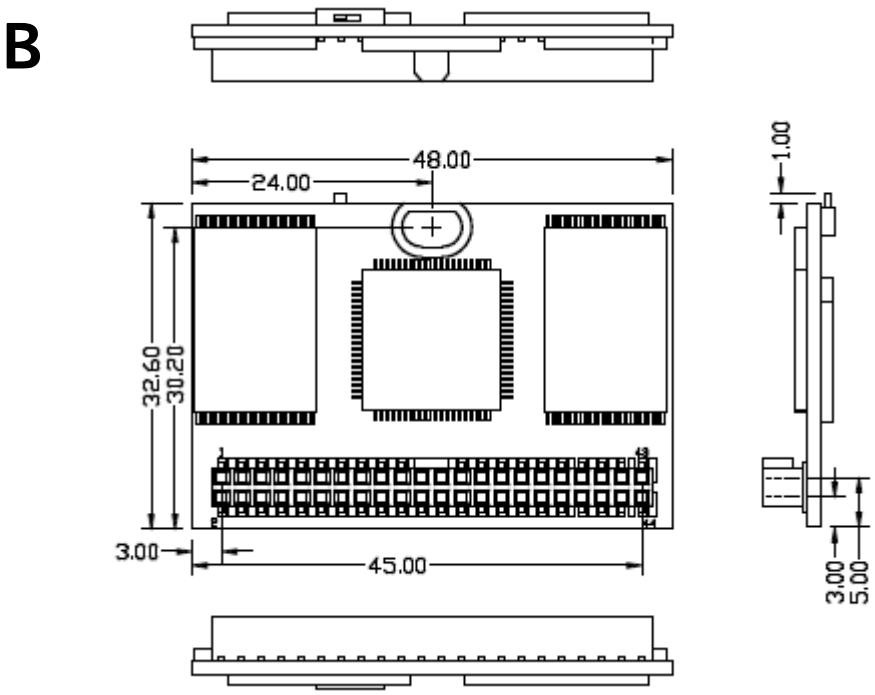


Figure 14: Mechanical Dimension of EDC1SE 44-pin (Horizontal Female Type A)

44pin Horizontal (DE4PB- XXXD41XXXXX) tolerance±0.3



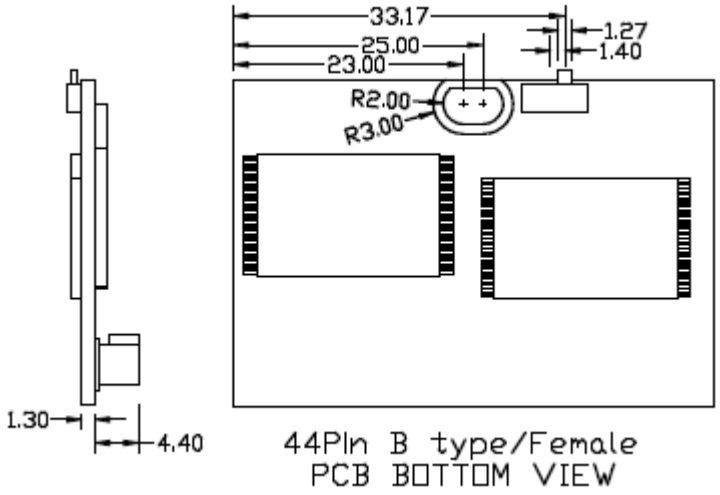
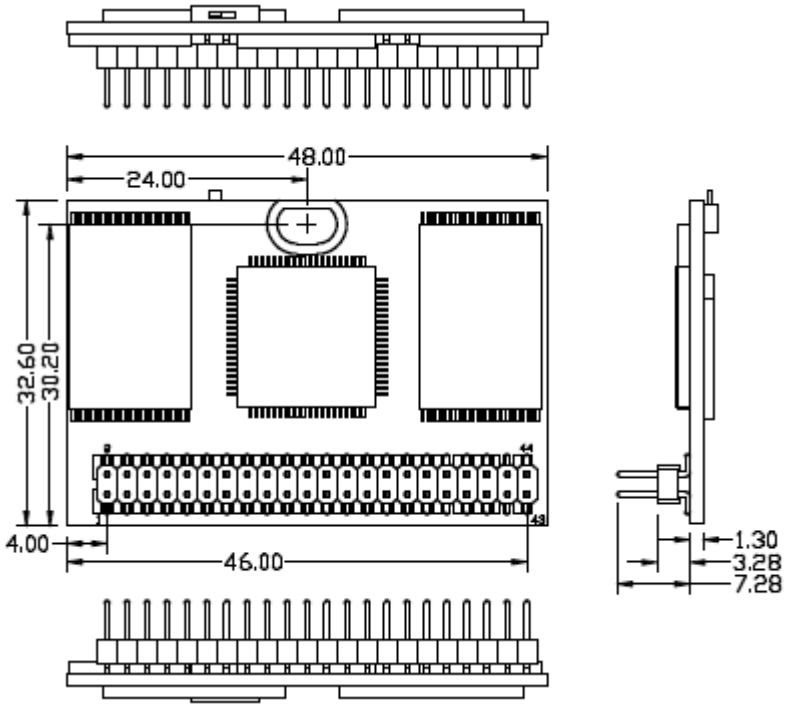


Figure 15: Mechanical Dimension of EDC1SE 44-pin (Horizontal Female Type B)

44pin Horizontal (DE4PC- XXXD41XXXXX) tolerance±0.3

C



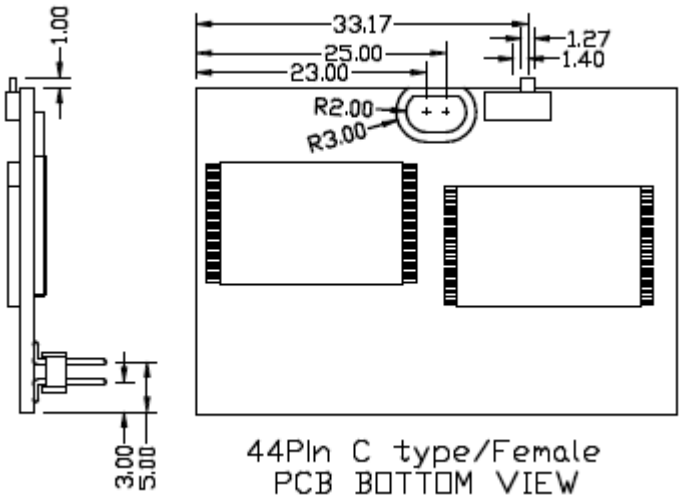
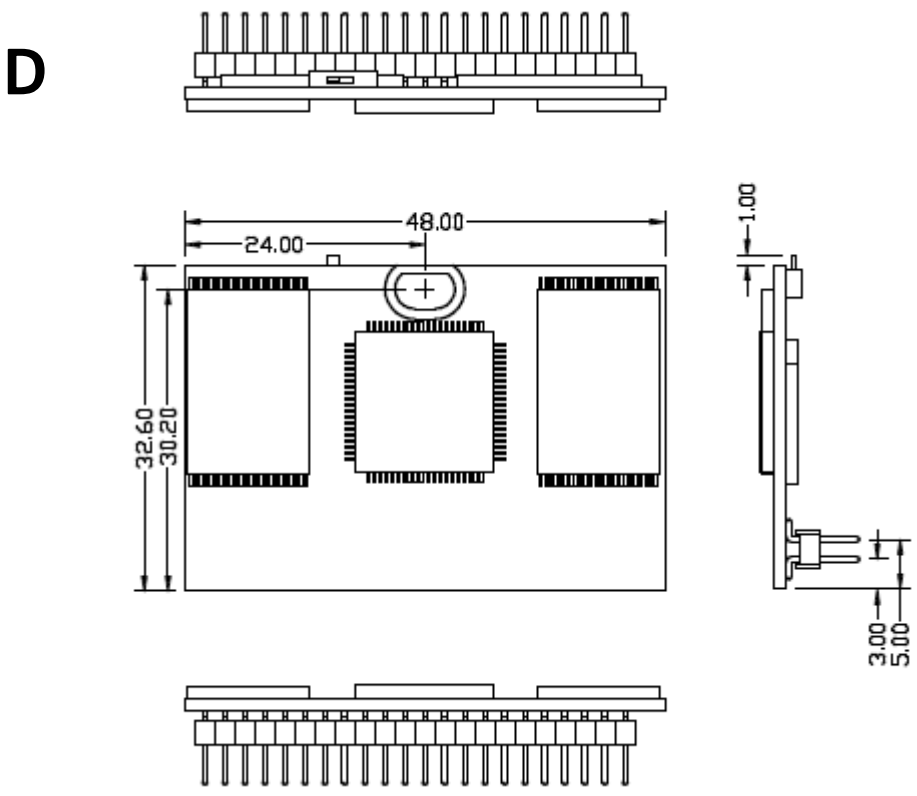


Figure 16: Mechanical Dimension of EDC1SE 44-pin (Horizontal Male Type C)

44pin Horizontal (DE4PD- XXXD41XXXXX) tolerance±0.3



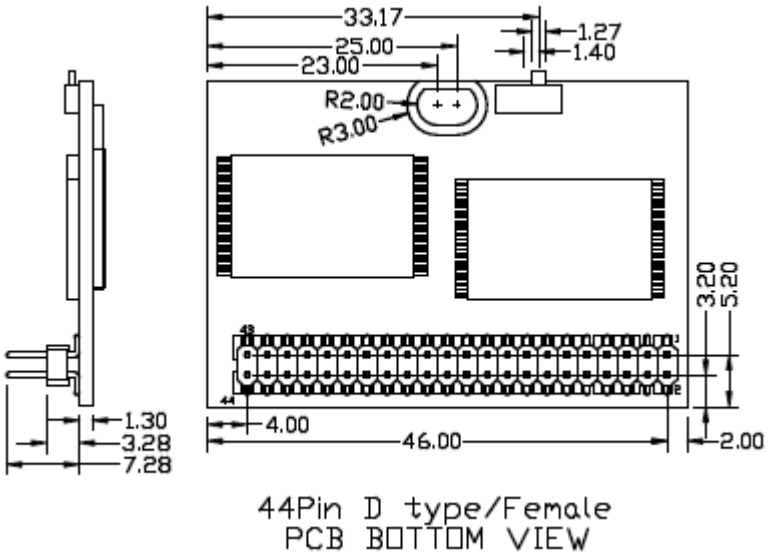
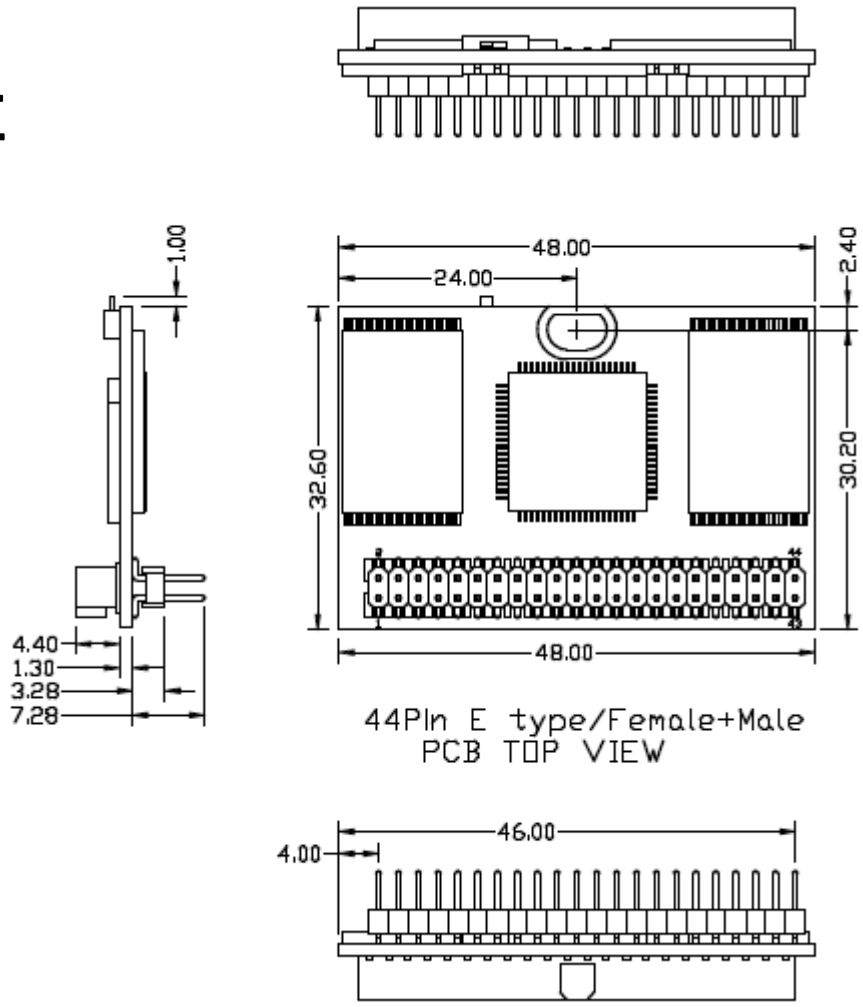


Figure 17: Mechanical Dimension of EDC1SE 44-pin (Horizontal Male Type D)

44pin Horizontal (DE4PE- XXXD41XXXXX) tolerance±0.3

E



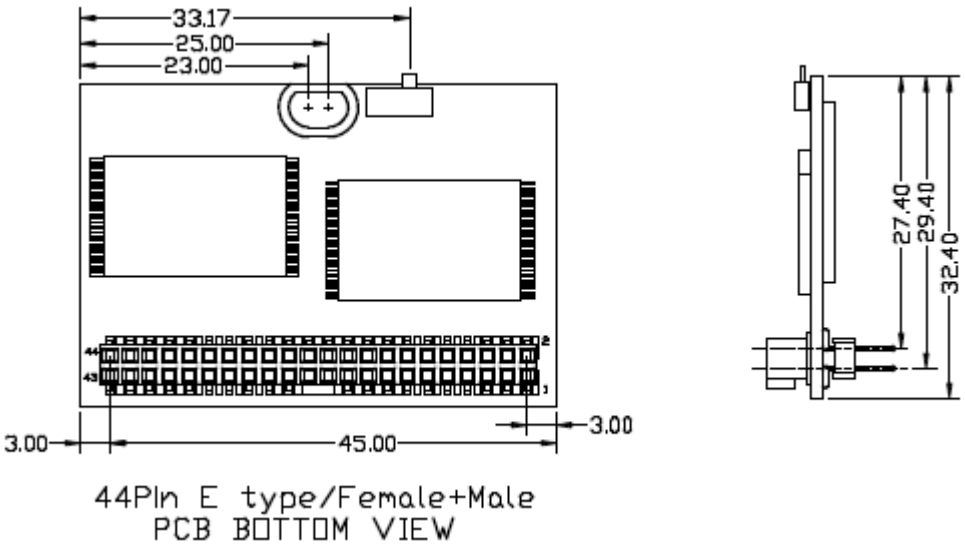
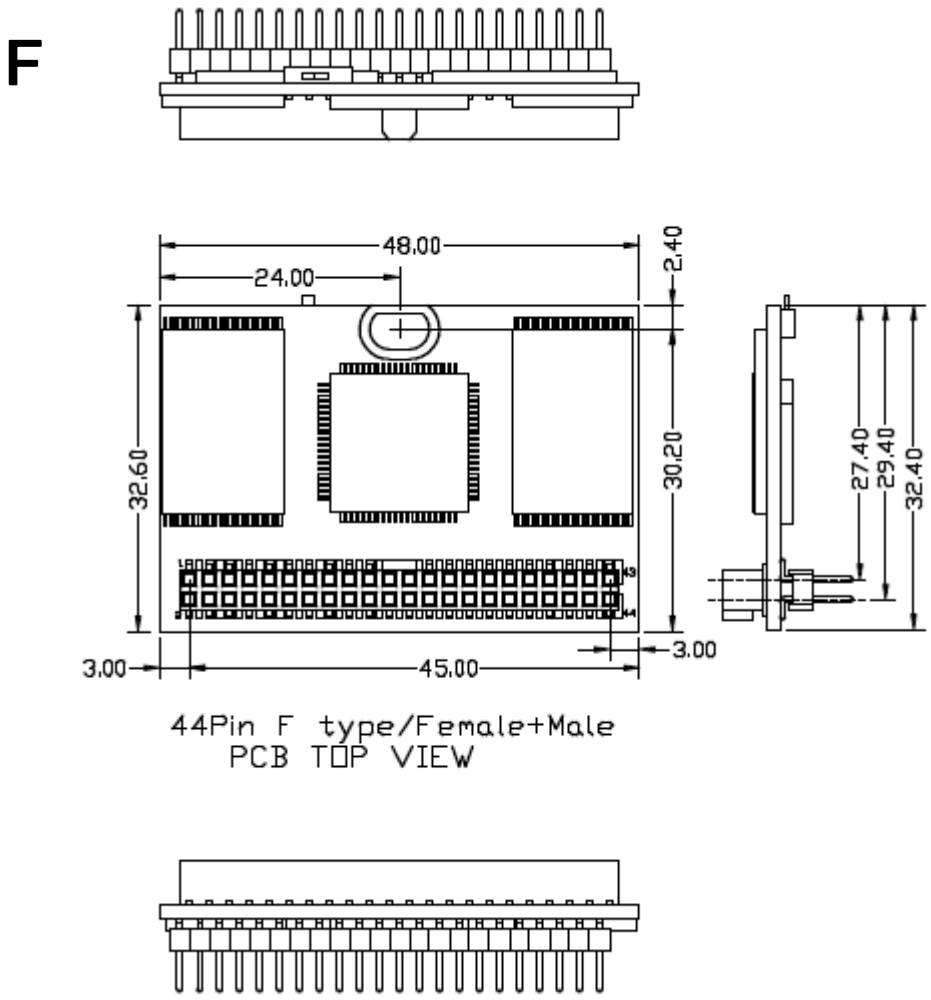


Figure 18: Mechanical Dimension of EDC1SE 44-pin (Horizontal Female/Male Type E)

44pin Horizontal (DE4PF-XXXD41XXXXX) tolerance±0.3



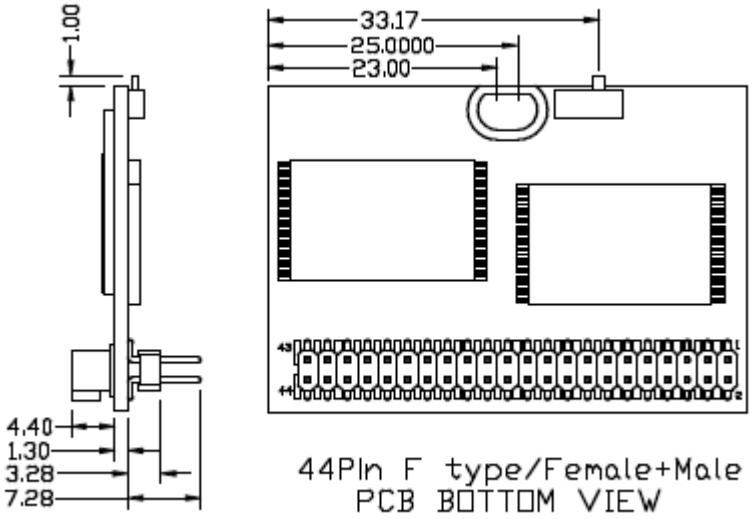


Figure 19: Mechanical Dimension of EDC1SE 44-pin (Horizontal Male/Female Type F)

5.4 Electrical Specifications

5.4.1 Absolute Maximum Ratings

Item	Symbol	Rating	Unit
Input voltage	V_{IN}	+5 DC ± 0.5	V
		+3.3 DC ± 0.3	

5.4.2 DC Characteristic

Table 5: EDC1SE DC Characteristic

Item	Symbol	Value			Unit
		Min	Standard	Max	
Power Supply	VCCH	4.5	5.0	5.5	V
Power Supply	VCCF	3.0	3.3	3.6	V
Input low voltage	V_{IL}	-0.3		0.8	V
Input high voltage	V_{IH}	2.0		Vcc+0.3	V
Output low voltage	V_{OL}			0.45 (at 4mA)	V
Output high voltage	V_{OH}	2.4 (at 1mA)			V
Operating CurrentV Sleep Mode Operation	Icc			 1.4 140	 mA mA
Input Leakage Current	ILI			±10	uA
Output leakage current	L_{LO}			±10	μA
Input/output Capacitance	$C_{I/O}$			10	pF

5.5 Timing Specifications

5.5.1 PIO Mode

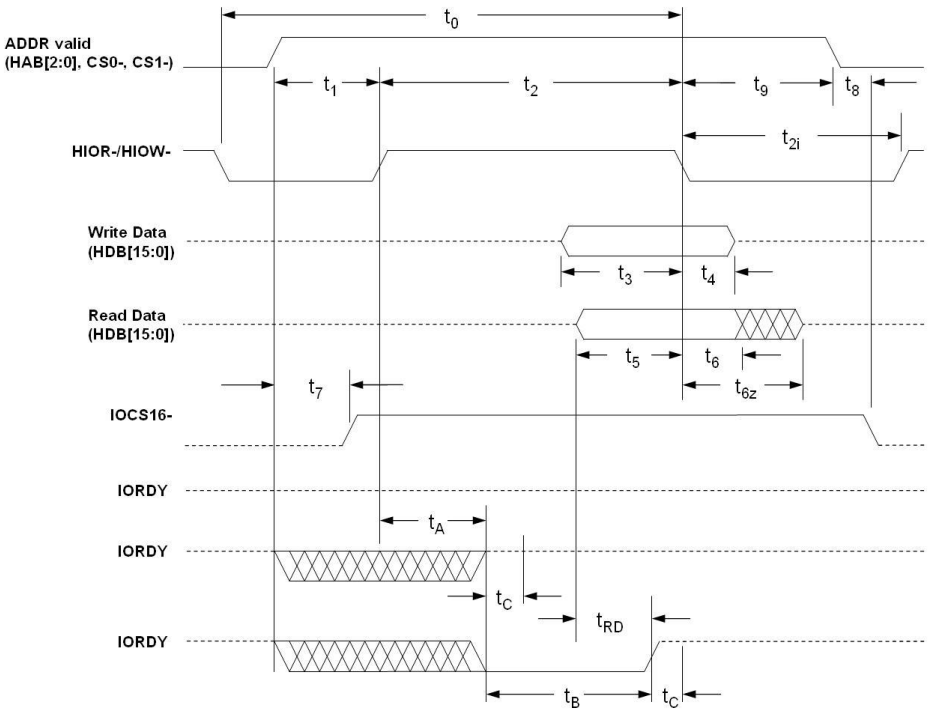


Figure 20: Read/Write Timing Diagram, PIO Mode

Table 6: Read/Write Timing Specifications, PIO Mode 0-4

PIO timing parameters		Mode 0	Mode 1	Mode 2	Mode 3	Mode 4
t_0	Cycle time (min.)	600	383	240	180	120
t_1	Address valid to HIOR-/HIOW- setup (min.)	70	50	30	30	25
t_2	HIOR-/HIOW- 16-bit (min.)	165	125	100	80	70
t_2	HIOR-/HIOW- Register 8-bit (min.)	290	290	290	80	70
t_{2i}	HIOR-/HIOW- recovery time (min.)	-	-	-	70	25
t_3	HIOW- data setup (min.)	60	45	30	30	20
t_4	HIOW- data hold (min.)	30	20	15	10	10
t_5	HIOR- data setup (min.)	50	35	20	20	20
t_6	HIOR- data hold (min.)	5	5	5	5	5
t_{6z}	HIOR- data tri-state (max.)	30	30	30	30	30
t_7	Address valid to IOCS16- assertion (max.)	90	50	40	n/a	n/a
t_8	Address valid to IOCS16- released (max.)	60	45	30	n/a	n/a
t_9	HIOR-/HIOW- to address valid hold	20	15	10	10	10
t_{RD}	Read data valid to IORDY active (min.)	0	0	0	0	0
t_A	IORDY setup time	35	35	35	35	35
t_B	IORDY pulse width (max.)	1250	1250	1250	1250	1250
t_C	IORDY assertion to release (max.)	5	5	5	5	5

5.5.2 Multiword DMA

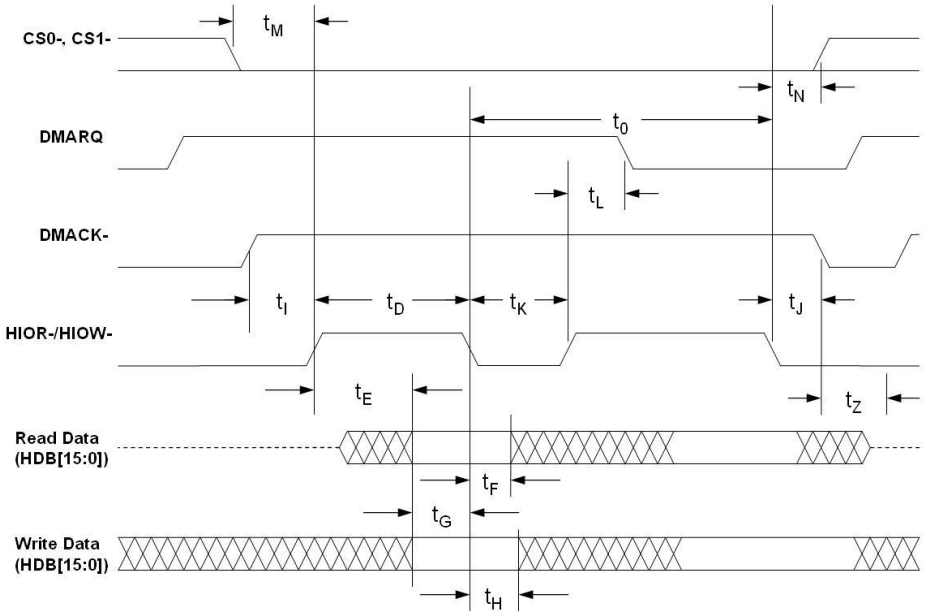


Figure 21: Read/Write Timing Diagram, Multiword DMA Mode

Table 7: Read/Write Timing Specifications, Multiword DMA Mode 0-2

Multiword DMA timing parameters		Mode 0	Mode 1	Mode 2
t_0	Cycle time (min.)	480	150	120
t_D	HIOR-/HIOW- assertion width (min.)	215	80	70
t_E	HIOR- data access (max.)	150	60	50
t_F	HIOR- data hold (min.)	5	5	5
t_G	HIOR-/HIOW- data setup (min.)	100	30	20
t_H	HIOW- data hold (min.)	20	15	10
t_I	DMACK to HIOR-/HIOW- setup (min.)	0	0	0
t_J	HIOR-/HIOW- to DMACK hold (min.)	20	5	5
t_{KR}	HIOR- negated width (min.)	50	50	25
t_{KW}	HIOW- negated width (min.)	215	50	25
t_{LR}	HIOR- to DMARQ delay (max.)	120	40	35
t_{LW}	HIOW- to DMARQ delay (max.)	40	40	35
t_M	CS1-, CS0- valid to HIOR-/HIOW-	50	30	25
t_N	CS1-, CS0- hold	15	10	10
t_Z	DMACK-	20	25	25

5.5.3 Ultra DMA mode

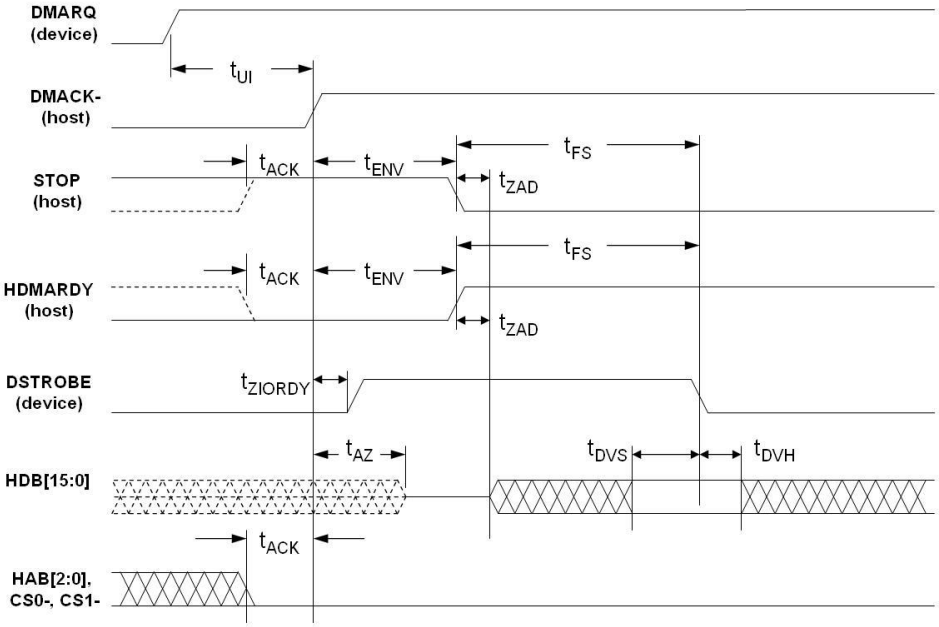


Figure 22: Ultra DMA Mode Data-in Burst Initiation Timing Diagram

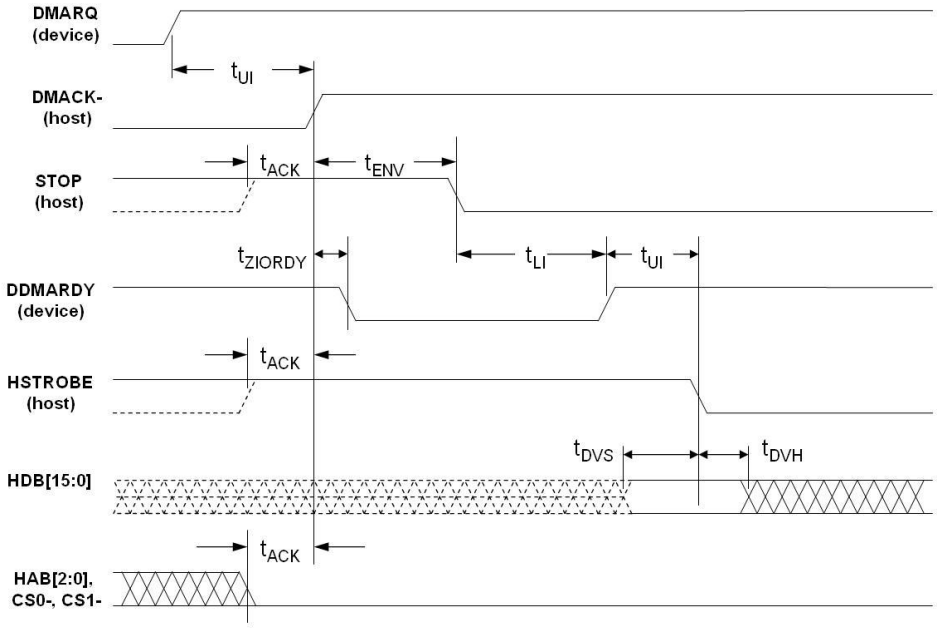


Figure 23: Ultra DMA Mode Data-out Burst Initiation Timing Diagram

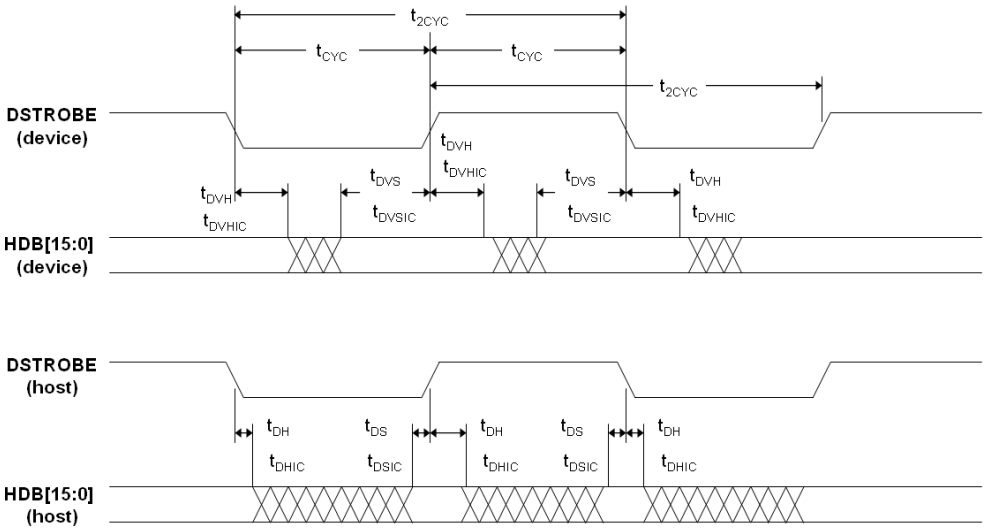


Figure 24: Sustained Ultra DMA Mode Data-in Burst Timing Diagram

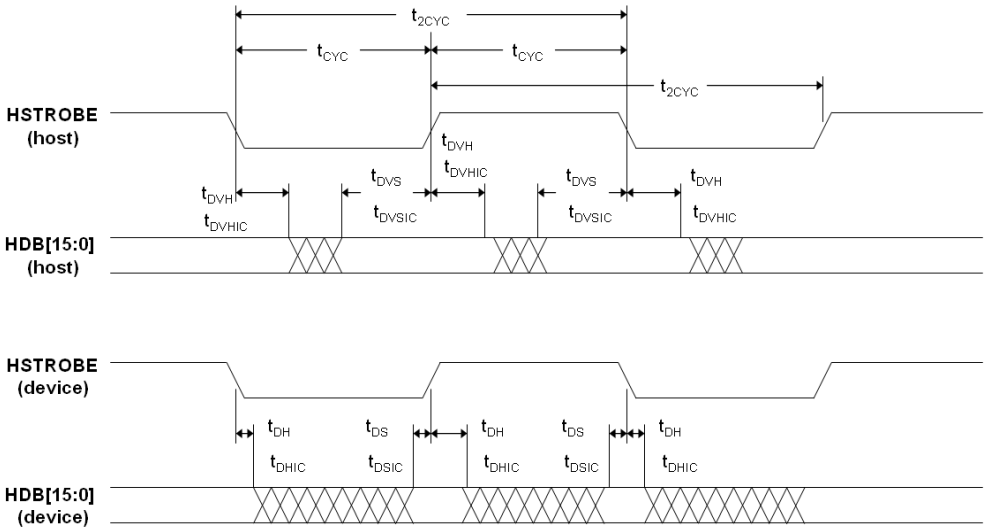


Figure 25: Sustained Ultra DMA Mode Data-out Burst Timing Diagram

Table 8: Timing Diagram, Ultra DMA Mode 0-4

Ultra DMA timing parameters		Mode 0		Mode 1		Mode 2		Mode 3		Mode 4	
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.
t_{2CYC}	Typical sustained average two cycle time	240	-	160	-	120	-	90	-	60	-
t_{CYC}	Cycle time allowing for asymmetry and clock variations (from STROBE edge to STROBE edge)	112	-	73	-	54	-	39	-	25	-
t_{2CYC}	Two cycle time allowing for clock variations (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)	230	-	153	-	115	-	86	-	57	-
t_{DS}	Data setup time (at recipient)	15	-	10	-	7	-	7	-	5	-
t_{DH}	Data hold time (at recipient)	5	-	5	-	5	-	5	-	5	-
t_{DVS}	Data valid setup time at sender (from data bus being valid until STROBE edge)	70	-	48	-	31	-	20	-	6.7	-

t_{DVH}	Data valid hold time at sender (from STROBE edge until data may become invalid)	6.2	-	6.2	-	6.2	-	6.2	-	6.2	-
t_{FS}	First STROBE time (for device to first negate DSTROBE from STOP during a data in burst)	-	230	-	200	-	170	-	130	-	120
t_{LI}	Limited interlock time	0	150	0	150	0	150	0	100	0	100
t_{MLI}	Interlock time with minimum	20	-	20	-	20	-	20	-	20	-
t_{UI}	Unlimited interlock time	0	-	0	-	0	-	0	-	0	-
t_{AZ}	Maximum time allowed for output drivers to release (from being asserted or negated)	-	10	-	10	-	10	-	10	-	10
t_{ZAH}	Minimum delay time required for output drivers to assert or negate (from released state)	20	-	20	-	20	-	20	-	20	-
t_{ZAD}		0	-	0	-	0	-	0	-	0	-
t_{ENV}	Envelope time (from DMACK- to STOP and HDMARDY- during data out burst initiation)	20	70	20	70	20	70	20	55	20	55
t_{RFS}	Ready-to-final-STROBE time (no STROBE edges shall be sent this long after negation of DMARDY-)	-	75	-	70	-	60	-	60	-	60
t_{RP}	Ready-to-pause time (time that recipient shall wait to initiate pause after negating DMARDY-)	160	-	125	-	100	-	100	-	100	-
t_{IORDYZ}	Pull-up time before allowing IORDY to be released	-	20	-	20	-	20	-	20	-	20
t_{ZIORDY}	Minimum time device shall wait before driving IORDY	0	-	0	-	0	-	0	-	0	-
t_{ACK}	Setup and hold times for DMACK- (before assertion or negation)	20	-	20	-	20	-	20	-	20	-
t_{SS}	Time from STROBE edge to negation of DMARQ or assertion of STOP (when sender terminates a burst)	50		50	-	50	-	20	-	20	-

5.5.4 Hardware Reset(Only for Memory Card mode and I/O Card Mode)

Table 9: Timing Diagram, Hardware Reset

	Item	Min.	Max.	Normal	Unit
t_{SU}(RESET)	Reset Setup Time	20	-	-	ms
t_{REC}(VCC)	-CE Recover Time	1	-	-	us
t_{PR}	VCC rising up time	0.1	100	-	ms
t_{PF}	VCC falling down time	3	300	-	ms
t_{W}(RESET)	Reset pulse width	10	-	-	ms
t_{H}(Hi-ZRESET)		0	-	-	
t_{S}(Hi-ZRESET)		0	-	-	

Hardware Reset Timing

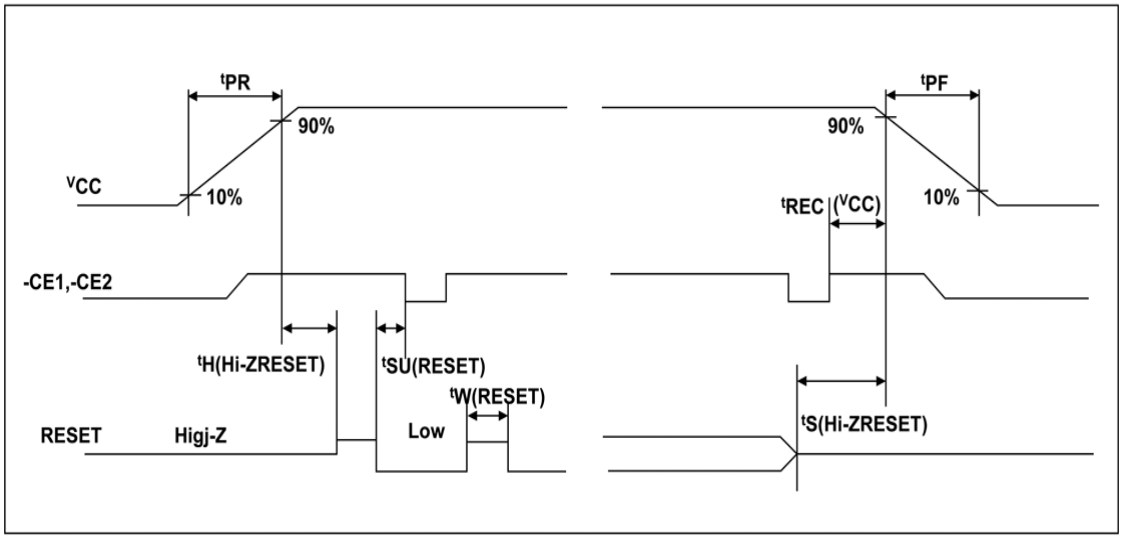


Figure 26 Timing Diagram, Hardware Reset

5.5.5 Power On Reset

When the VCC power reaches to 2.7V, the disk drive will be reset.

Table 10: Timing Diagram, Power On Reset

	Item	Min.	Max.	Normal	Unit	Note
t_{SU}(RESET)	-CE Setup Time	20	-	-	ms	
t_{PR}	-VCC Rising Up Time	0.1	100	-	ms	

Power on Reset Timing

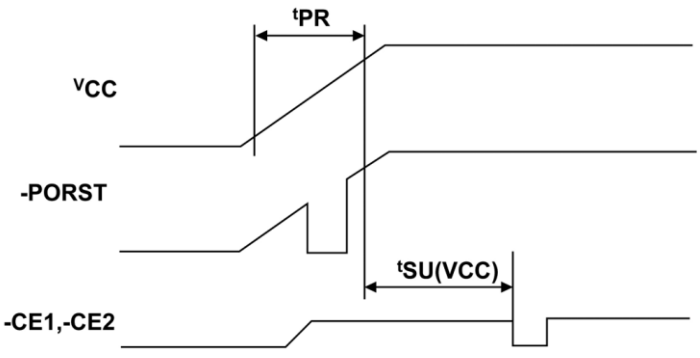


Figure 27 Timing Diagram, Power On Reset

6. Supported ATA Commands

EDC1SE supports the commands listed in Table 13.

Table 11: IDE Commands

Class	Command	Code	FR	SC	SN	CY	DH	LBA
1	Check Power Mode	98H or E5H	-	-	-	-	D	-
1	Execute Device Diagnostic	90H	-	-	-	-	D	-
1	Erase Sector(s)	C0H	-	Y	Y	Y	Y	Y
2	Format Track	50H	-	Y	-	Y	Y	Y
1	Identify Device	ECH	-	-	-	-	D	-
1	Idle	97H or E3H	-	Y	-	-	D	-
1	Idle immediate	95H or E1H	-	-	-	-	D	-
1	Initialize Device Parameters	91H	-	Y	-	-	Y	-
1	Read Buffer	E4H	-	-	-	-	D	-
1	Read DMA	C8H	-	Y	Y	Y	Y	Y
1	Read Long Sector	22H or 23H	-	-	Y	Y	Y	Y
1	Read Sector(s)	20H or 21H	-	Y	Y	Y	Y	Y
1	Read Verify Sector(s)	40H or se41H	-	Y	Y	Y	Y	Y
1	Recalibrate	1XH	-	-	-	-	D	-
1	Request Sense	03H	-	-	-	-	D	-
1	Seek	7XH	-	-	Y	Y	Y	Y
1	Set Features	EFH	Y	-	-	-	D	-
1	Set Sleep Mode	99H or E6H	-	-	-	-	D	-
1	Standby	96H or E2H	-	-	-	-	D	-
1	Standby Immediate	94H or E0H	-	-	-	-	D	-
2	Write Buffer	E8H	-	-	-	-	D	-
2	Write DMA	CAH	-	Y	Y	Y	Y	Y
2	Write Sector(s)	30H or 31H	-	Y	Y	Y	Y	Y
2	Write Sector(s) without Erase	38H	-	Y	Y	Y	Y	Y

6.1 Check power mode – 98H or E5H

Table 12: Check power mode command information

Register	7	6	5	4	3	2	1	0
Command(7)	98h or E5h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command checks the power mode:

If the EDC Storage is in, going to, or recovering from the sleep mode, the EDC Storage Card sets BSY, sets the Sector Count Register to 00h, clears BSY and generates an interrupt. If the EDC Storage Card is in idle mode, the EDC Storage Card sets BSY, sets the Sector Count Register to FFh, clears BSY and generates an interrupt.

6.2 Execute Device Diagnostic – 90H

Table 13: Execute device diagnostic command information

Register	7	6	5	4	3	2	1	0
Command(7)	90h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command performs the internal diagnostic tests implemented by the EDC Storage Card. When the diagnostic command is issued in a PCMCIA configuration mode, this command runs only on the EDC Storage Card that is addressed by the Drive/Head register. This is because PCMCIA card interface does not allow for direct inter-drive communication (such as the ATA PDIAG and DASP signals). When the diagnostic command is issued in the True IDE Mode, the Drive bit is ignored and the diagnostic command is executed by both the Master and the Slave with the Master responding with status for both devices. The Diagnostic codes are shown in Table 14. Diagnostic Codes are returned in the Error Register at the end of the command.

Table 14: Execute device diagnostic codes

Code	Error Type
01h	No Error Detected
02h	Formatter Device Error
03h	Sector Buffer Error
04h	ECC Circuitry Error
05h	Controller Microprocessor Error
8Xh	Slave Error in True IDE Mode

6.3 Erase Sector – C0H

Table 15: Erase sector command information

Register	7	6	5	4	3	2	1	0
Command(7)	C0h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command is used to pre-erase and condition data sectors in advance of a Write without Erase or Write Multiple without Erase command. There is no data transfer associated with this command but a Write Fault error status can occur.

6.4 Format Track – 50H

Table 16: Format track command information

Register	7	6	5	4	3	2	1	0
Command(7)	50h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	X (LBA 7-0)							
Sector Count(2)	Count(LBA mode only)							
Feature(1)	X							

This command writes the desired head and cylinder of the selected drive with a vendor unique data pattern (typically FFh or 00h). To remain host backward compatible, the EDC Storage Card expects a sector buffer of data from the host to follow the command with the same protocol as the Write Sector(s) command although the information in the buffer is not used by the EDC Storage Card. If LBA=1 then the number of sectors to format is taken from

the Sec Cnt register (0=256). The use of this command is not recommended.

6.5 Identify Device – ECH

Table 17: Identify device command information

Register	7	6	5	4	3	2	1	0
Command(7)	ECh							
C/D/H(6)	X	X	X	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Identify Device command enables the host to receive parameter information from the EDC Storage Card. This command has the same protocol as the Read Sector(s) command. The parameter words in the buffer have the arrangement and meanings defined in Table 20. All reserved bits or words are zero. Hosts should not depend in Obsolete words in Identify Device containing 0. Table 21 specifies each filed in the data returned by the Identify Device Command. In Table 20, X indicates a numeric nibble vale specific to the card and aaaa indicates an ASCII string specific to the particular drive.

Table 18: Identify device command for data returned information

Word	Description	Value
0	General Configuration Bit 15 0=ATA device Bit 14:8 Retired Bit 7:6 Obsolete Bit 5:3 Retired Bit 2 Response incomplete Bit 1 Retired Bit 0 reserved	045Ah
1	Number of logical cylinders	XXXXh
2	Specific configuration	0000h
3	Number of logical heads	16
4-5	Retired	0000h
6	Number of logical sectors per logical track	63
7-8	Number of sectors per card	XXXXh
9	Retired	0000h
10-19	Serial number in 20 ASCII	aaa
20-21	Retired	0002h 0002h

22	Obsolete	0004h
23-26	Firmware revision in 8 ASCII	aaaa
27-46	Model number in 40 ASCII	aaaa
47	15-8: 80 7-0: 00h Reserved 01h-FFh: Maximum number of sectors that shall be transferred per DRQ data block on READ/WRITE Multiple commands	8002h
48	Trusted Computing feature set options 15 shall be cleared to zero 14 shall be set to one 13:1 Reserved for the Trusted Computing Group 0 0 = Trusted Computing feature set is not supported	0000h
49	Capabilities 15-14: Reserved for the IDENTIFY PACKET DEVICE command. 13: 1=Standby timer values as specified in this standard are supported 0:Standby timer values shall be managed by the device 12: Reserved for the IDENTIFY PACKET DEVICE command 11: 1=IORDY supported 0=IORDY may be disabled 10 1: IORDY may be disabled 9 1=LBA supported 8 1=DMA supported. 7-0 Retired	0F00h
50	Capabilities 15: Shell be cleared to zero 14: Shall be set to one 13:2 Reserved 1 Obsolete 0 0	0000h
51	PIO data transfer cycle timing mode	0200h
52	Obsolete	0000h
53	15 Free-fall control Sensitivity 00h: Vendor's recommended setting 7:3 Reserved 2: 1=the fields reported in word 88 are valid 1: 1=the fields reported in words (70:64) are valid 0: Obsolete	0007h

54	Number of current logical cylinders	XXXXh
55	Number of current logical heads	XXXXh
56	Number of current logical sectors per logical track	XXXXh
57-58	Current capacity in sectors	XXXXh
59	15:9 Reserved 8 0:Multiple sector setting is invalid 7:0 Current setting for number of logical sectors that shall be transferred per DRQ data block on READ/WRITE Multi commands	0102h
60-61	Total number of user address sectors(DWord)	XXXXXXXXh
62	Obsolete	0000h
63	Multi-word DMA transfer(Not support)	0007h
64	15-8 Reserved 7-0 PIO modes supported	0003h
65	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds In PCMCIA mode this value shall be 0h	0078h
66	Manufacturer's recommended Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds In PCMCIA mode this value shall be 0h	0078h
67	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds	0078h
68	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds	0078h
69-74	Reserved	0000h
75	No DMA QUEUED command supports	0000h
76	Serial ATA Capabilities 15:11 Reserved for Serial ATA 10 1= Supports Phy Event Counters 9 1= Supports receipt of host initiated power management Requests 8 0= No Support native Command Queuing 7:3 Reserved for future SATA signaling speed grades 2 1=Supports SATA Gen2 Signaling Speed (3.0Gb/s) 1 1=Support SATA Gen1 Signaling Speed (1.5Gb/s) 0 Shall be cleared to zero	0000h
77	Reserved for Serial ATA	0000h
78	Serial ATA features supported	0000h

	15:7 Reserved for Serial ATA 6 0=Device not supports Software Settings Preservation 5 Reserved for Serial ATA 4 0= Device not supports in-order data delivery 3 0= Device not supports initiating power management 2 0= Device not supports DMA Setup auto-activation 1 0= Device not supports non-zero buffer offsets 0 Shall be cleared to zero	
79	Serial ATA feature enabled 15:7 Reserved for Serial ATA 6 0=Software Settings Preservation not enabled 5 0=Reserved for Serial ATA 4 0= In-order data delivery not enabled 3 0= Device initiated power management not enabled 2 0= DMA setup auto-activation not enabled 1 0= Non-zero buffer offsets not enabled 0 Shall be cleared to zero	0000h
80-81	ATA Version support (ATA8-ACS)	0020 0000h
82	Command and feature sets supported 15 0 = Obsolete 14 0 = NOP Command not supported 13 0 = READ BUFFER Command not supported 12 0 = WRITE BUFFER Command not supported 11 0 = Obsolete 10 0 = Host Protected Area Feature Set not supported 9 0 = DEVICE RESET Command not supported 8 0 = SERVICE Interrupt not supported 7 0 = RELEASE Interrupt not supported 6 1 = Look-ahead supported 5 1 = Write Cache supported 4 0 = indicate that the PACKET feature set is not supported 3 1 = mandatory Power Management Feature Set supported 2 0 = Obsolete 1 0 = Security Mode Feature Set not supported 0 1 = SMART Feature Set supported	700Ah
83	Command and feature sets supported 15 Shall be cleared to zero 14 Shall be set to one 13 0 = FLUSH CACHE EXT Command not supported	5004h

	12 1 = mandatory FLUSH CACHE Command supported 11 0 = Device Configuration Overlay feature set not supported 10 0 = 48-Bit Address feature set not supported 9 0 = Automatic Acoustic Management feature set not supported 8 0 = SET MAX security extension not supported 7 0 = See Address Offset Reserved Area Boot, INCITS TR27:2001 6 0 = SET FEATURES subcommand not required to spin-up after power-up 5 0 = Power-Up in Standby feature set supported 4 0 = Removable Media Status Notification feature set not supported 3 0 = Advanced Power Management feature set not supported 2 0 = CFA feature set not supported 1 0 = READ/WRITE DMA QUEUED not supported 0 1 = DOWNLOAD MICROCODE Command supported	
84	Command Set/Feature Supported Extension 15 Shall be cleared to zero 14 Shall be set to one 13-6 Reserved 5 0 = General Purpose Logging feature set not supported 4 reserved 3 0 = Media Card Pass Through Command feature set not supported 2 0 = Media Serial Number not supported 1 0 = SMART self-test not supported 0 1 = SMART Error Logging not supported	1SEh
85	Command and feature sets supported or enabled 15 0 = Obsolete 14 0 = NOP Command not enabled 13 0 = READ BUFFER Command not enabled 12 0 = WRITE BUFFER Command not enabled 11 Obsolete 10 0 = Host Protected Area feature set not enabled 9 0 = DEVICE RESET Command not enabled 8 0 = SERVICE Interrupt not enabled 7 0 = RELEASE Interrupt not enabled	7008

	6 0 = Look-ahead not enabled 5 0 = Write Cache not enabled 4 Shall be cleared to zero to indicate that the PACKET Command feature set is not supported. 3 1 = Power Management Feature Set enabled 2 0 = Removable Media feature set not enabled 1 0 = Security Mode Feature Set not enabled 0 0 = SMART Feature Set not enabled	
86	Command set/feature enabled 15-14 0 = Reserved 13 0 = FLUSH CACHE EXT Command not supported 12 1 = FLUSH CACHE Command supported 11 0 = Device Configuration Overlay not supported 10 0 = 48-Bit Address features set not supported 9 0 = Automatic Acoustic Management feature set not enabled 8 0 = SET MAX security extension not enabled by SET MAX SETPASSWORD 7 0 = Reserved 6 0 = SET FEATURES subcommand required to spin-up after power-up not enabled 5 0 = Power-Up in Standby feature set not enabled 4 0 = Obsolete 3 1 = Advanced Power Management feature set enabled 2 0 = CFA feature set not supported 1 0 = READ/WRITE DMA QUEUED Command not supported 0 1 = DOWNLOAD MICROCODE Command supported	1004h
87	Command and feature sets supported or enabled 15 Shall be cleared to zero 14 Shall be set to one 13 1 = IDLE IMMEDIATE with UNLOAD FEATURE supported 12 0 = Reserved for Technical Report, INCITS TR-37-2004 11 0 = Reserved for Technical Report, INCITS TR-37-2004 10:9 0 = Obsolete 8 0 = 64-Bit World Wide Name not supported 7 0 = WRITE DMA QUEUED FUA EXT Command not supported 6 0 = WRITE DMA FUA EXT and WRITE MULTIPLE FUA	1SEh

	EXT commands not supported 5 0 = General Purpose Logging feature set not supported 4 0 = Obsolete 3 0 = Media Card Pass Through Command feature set not supported 2 0 = Media Serial Number is not valid 1 0 = SMART Self-Test not supported 0 0 = SMART Error-Logging not supported	
88	Ultra DMA modes 15 Reserved 14 0 = Ultra DMA mode 6 is not supported 13 1= Ultra DMA mode 5 is selected 0= Ultra DMA mode 5 is not selected 12 1= Ultra DMA mode 4 is selected 0= Ultra DMA mode 4 is not selected 11 1= Ultra DMA mode 3 is selected 0= Ultra DMA mode 3 is not selected 10 1= Ultra DMA mode 2 is selected 0= Ultra DMA mode 2 is not selected 9 1= Ultra DMA mode 1 is selected 0= Ultra DMA mode 1 is not selected 8 1= Ultra DMA mode 0 is selected 0= Ultra DMA mode 0 is not selected 7 Reserved 6 0= Ultra DMA mode 6 is not supported 5 1= Ultra DMA mode 5 and below are supported 4 1= Ultra DMA mode 4 and below are supported 3 1= Ultra DMA mode 3 and below are supported 2 1= Ultra DMA mode 2 and below are supported 1 1= Ultra DMA mode 1 and below are supported 0 1= Ultra DMA mode 0 is supported	X01Fh
89	Time required for Normal Erase mode SECURITY ERASE UNIT command	0000h
90	Time required for Enhanced erase mode SECURITY ERASE UNIT command	0000h
91	Current advanced power management level value	0000h
92	Master Password Identifier	0000h
93	Hardware reset result	XXXXh
94	Current automatic acoustic management value 15:8 Vendor's recommended acoustic management value.	0000h

	7:0 Current automatic acoustic management value.	
95-126	Reserved	0000h
127	Obsolete	0000h
128	Security Status 15:9 Reserved 8 Security level 0 = high, 1 = Maximum 7:6 Reserved 5 1= Enhanced security erase supported 4 1= Security count expired 3 0= Security frozen. 2 0 = Security not locked 1 0= Security not enabled 0 0= Security not supported	0000h
129-159	Vendor specific	0000h
160	CFA power mode 1	0000h
161-175	Reserved	0000h
176-205	Current media serial number	0000h
206-254	Reserved	0000h
255	Integrity word 15:8 Check Sum 7:0 Signature	XXXXh

6.6 Idle -97H or E3H

Table 19: Idle command information

Register	7	6	5	4	3	2	1	0
Command(7)	97h or E3h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Timer Count (5 msec increments)							
Feature(1)	X							

This command causes the EDC Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt. If the sector count is non-zero, it is interpreted as a timer count with each count being 5 milliseconds and the automatic power down mode is enabled. If the sector count is zero, the automatic power down mode is disabled. Note that this time base (5 msec.) is different from the ATA specification.

6.7 Idle immediate - 95H or E1H

Table 20: Idle immediate command information

Register	7	6	5	4	3	2	1	0
Command(7)	95h or E1h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the EDC Storage Card to set BSY, enter the IDLE mode, clear BSY and generate an interrupt.

6.8 Initialize Device Parameters - 91H

Table 21: Initialize device parameters command information

Register	7	6	5	4	3	2	1	0
Command(7)	91h							
C/D/H(6)	X	O	X	Drive	Max Head (no. of heads-1)			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Number of sectors							
Feature(1)	X							

This command enables the host to set the number of sectors per track and the number of heads per cylinder. Only the Sector Count and the Card/Device/Head registers are used by this command.

6.10 Read Buffer - E4H

Table 22: Read buffer command information

Register	7	6	5	4	3	2	1	0
Command(7)	E4h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Read Buffer command enables the host to read the current contents of the EDC

Storage Card's sector buffer. This command has the same protocol as the Read Sector(s) command.

6.11 Read Long Sector - 22H or 23H

Table 23: Read long sector command information

Register	7	6	5	4	3	2	1	0
Command(7)	22h or 23h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	X							
Feature(1)	X							

The Read Long command performs similarly to the Read Sector(s) command except that is returns 516 bytes of data instead of 512 bytes. During a Read Long command, the EDC Storage Card does not check the ECC bytes to determine if there consists of 512 bytes of data transferred in word mode followed by 4 bytes of ECC data transferred in byte mode. This command has the same protocol as the Read Sector(s) command. Use of this command is not recommended.

6.12 Read Sector(s) - 20H or 21H

Table 24: Read sector command information

Register	7	6	5	4	3	2	1	0
Command(7)	20h or 21h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command reads from 1 to 256 sectors as specified in the Sector Count Register. A sector count of 0 requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is issued and after each sector of data (except the last one) has buffer, sets DRQ, cleats BSY, and generates an interrupt. The host then reads the 512 bytes of data from the buffer.

At command completion, the Command Block Registers contain the cylinder, head and sector number of the last sector read. If an error occurs, the read terminates at the sector

where the error occurred. The command Block Registers contain the cylinder head, and sector number of the sector 2 where the error occurred. The flawed data is pending in the sector buffer.

6.13 Read Verify Sector(s) - 40H or 41H

Table 25: Read verify sector command information

Register	7	6	5	4	3	2	1	0
Command(7)	40h or 41h							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command is identical to the Read Sectors command, except that DRQ is never set and no data is transferred to the host. When the command is accepted, the EDC Storage Card sets BSY.

When the requested sectors have been verified, the EDC Storage Card clears BSY and generates an interrupt. Upon command completion, the Command Block Registers contain the cylinder, head, and sector number of the last sector verified.
If an error occurs, the Read Verify Command terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The Sector Count Register contains the number of sectors not yet verified.

6.14 Recalibrate - 1XH

Table 26: Recalibrate command information

Register	7	6	5	4	3	2	1	0
Command(7)	1Xh							
C/D/H(6)	1	LBA	1	Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command is effectively a NOP command to the EDC Storage Card and is provided for

compatibility.

Table 27: Identifier and Security Level Bit Interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The lock mode shall be enabled from the next power-on or hardware reset. The Compact Flash Storage Card shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new user password. The lock mode shall be enabled from the next power-on reset or hardware reset. The EDC Storage Card shall then be unlocked by only the User password. The Master password previously set is still stored in the EDC Storage Card shall not be used to unlock the EDC Storage Card.
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed.

6.15 Seek - 7XH

Table 28: Seek command information

Register	7	6	5	4	3	2	1	0
Command(7)	7Xh							
C/D/H(6)	1	LBA	1	Drive	Head (LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	X (LBA 7-0)							
Sector Count(2)	X							
Feature(1)	X							

This command is effectively a NOP command to the EDC Storage Card although it does perform a range check of cylinder and head or LBA address and returns an error if the address is out of range.

6.16 Set Features – EFH

Table 29: Set features command information

Register	7	6	5	4	3	2	1	0
Command(7)	EFh							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	Config							
Feature(1)	Feature							

This command is used by the host to establish or select certain features. If any subcommand input value is not supported or is invalid, the EDC Storage Card shall return command aborted. Table 32 : Feature Supported defines all features that are supported.

Table 30: Feature Supported

Feature	Operation
02h	Enable Write Cache.
03h	Set transfer mode based on value in Sector Counter register.
55h	Disable Read Look Ahead.
66h	Disable Power on Reset (POR) establishment of defaults at Soft reset.
82h	Disable Write cache.
9Ah	Set the host current source capability. Allows tradeoff between current drawn and read/write speed.
AAh	Enable Read Look Ahead.
BBh	4 Bytes of data apply on Read/Write Long commands.
CCh	Enable Power on Reset (POR) establishment of defaults at Soft Reset.

6.17 Set Sleep Mode - 99H or E6H

Table 31: Set sleep mode command information

Register	7	6	5	4	3	2	1	0
Command(7)	99h or E6h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the EDC Storage Card to set BSY, enter the Sleep mode, clear BSY and generate an interrupt. Recovery from sleep mode is accomplished by simply issuing another command (a reset is permitted but not required). Sleep mode is also entered when internal timers expire so the host does not need to issue this command except when it wishes to enter Sleep mode immediately. The default value for the timer is 5 milliseconds.

6.18 Standby - 96H or E2H

Table 32: Standby command information

Register	7	6	5	4	3	2	1	0
Command(7)	96h or E2h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

This command causes the EDC Storage Card to set BSY, enter the Sleep mode, cleat BSY and return interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.19 Standby Immediate - 94H or E0H

Table 33: Standby immediate command information

Register	7	6	5	4	3	2	1	0
Command(7)	94h or E0h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							

Feature(1)	X

This command causes the EDC Storage Card to set BSY, enter the Sleep mode, clear BSY and return the interrupt immediately. Recovery from sleep mode is accomplished by simply issuing another command (a reset is not required).

6.20 Write Buffer - E8H

Table 34: Write buffer command information

Register	7	6	5	4	3	2	1	0
Command(7)	E8h							
C/D/H(6)	X			Drive	X			
Cylinder High(5)	X							
Cylinder Low(4)	X							
Sector Number(3)	X							
Sector Count(2)	X							
Feature(1)	X							

The Write Buffer command enables the host to overwrite contents of the EDC Storage Card's sector buffer with any data pattern desired. This command has the same protocol as the Write Sector(s) command and transfer 512 bytes.

6.21 Write Sector(s) - 30H or 31H

Table 35: Write sector command information

Register	7	6	5	4	3	2	1	0
Command(7)	30h or 31h							
C/D/H(6)	1	LBA	1	Drive	Head(LBA 27-24)			
Cylinder High(5)	Cylinder High (LBA 23-16)							
Cylinder Low(4)	Cylinder Low (LBA 15-8)							
Sector Number(3)	Sector Number (LBA 7-0)							
Sector Count(2)	Sector Count							
Feature(1)	X							

This command writes from 1 to 256 sectors as specified in the Sector Count Register. A sector count of zero requests 256 sectors. The transfer begins at the sector specified in the Sector Number Register. When this command is accepted, the EDC Storage Card sets BST, then sets DRQ and clears BSDY, then waits for the host to fill the sector buffer with the data to be written. No interrupt is generated to start the first host transfer operation. No data should be transferred by the host until BSY has been cleared by the host.

For multiple sectors, after the first sector of data is in the buffer, BSY shall be set and DRQ shall be cleared. After the next buffer is ready for data, BSY is cleared, DRQ is set and an interrupt is generated. When the final sector of data is transferred, BSY is set and DRQ is

cleared. It shall remain in this state until the command is completed at which time BSY is cleared and an interrupt is generated.

If an error occurs during a write of more than one sector, writing terminates at the sector where the error occurs. The Command Block Registers contain the cylinder, head and sector number of the sector where the error occurred. The host may then read the command block to determine what error has occurred, and on which sector.

7. Device Parameters

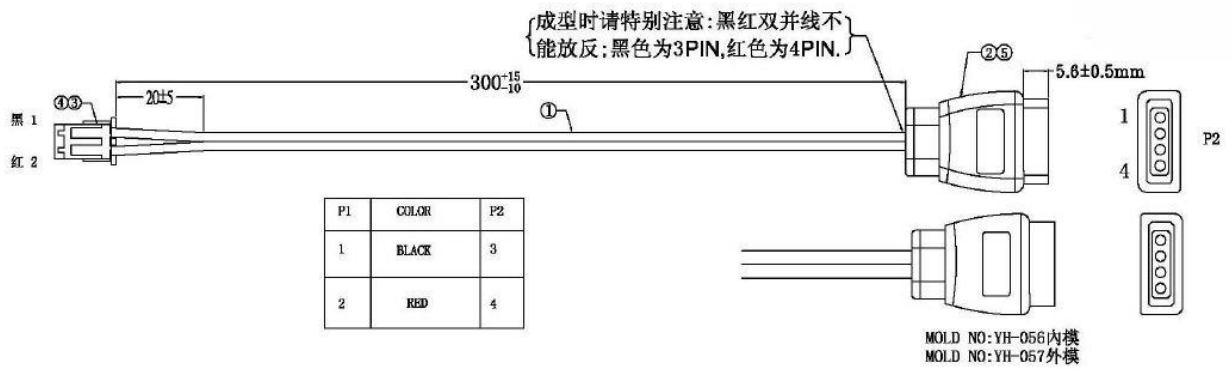
EDC 1SE device parameters listed in Table 36.

Table 36: Device parameters

Capacity	Cylinders	Heads	Sectors	Capacity(MB)	LBA
128MB	480	16	32	120	245760
256MB	984	16	32	246	503808
512MB	1001	16	63	492.68	1009008
1GB	2002	16	63	985.36	2018016
2GB	4003	16	63	1970.23	4035024
4GB	8006	16	63	3940.45	8070048
8GB	16000	16	63	7875	16128000

8. Appendix

Power cable specifications



P1	COLOR	P2
1	BLACK	3
2	RED	4

Figure 28 : EDC 1SE powercable mechanical drawing

9. Innodisk Part Number Rule-

Vertical Type

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18
	D	**E**	**0**	**H**	**-**	**5**	**1**	**2**	**D**	**4**	**1**	**A**	**C**	**X**	**S**	**B**	**-**	**X**
Description	Disk	EDC1SE 40-pin, vertical			-	Capacity			Category			FW version	Operation Temp.	Internal Control	CH	Flash		Customized Code

Definition	
Code 1st (Disk)	**Code 13th (Operation Temperature)**
D : Disk	C：Standard Grade (0 ~ +70 ℃)
Code 2nd ~ 4th (Form Factor)	W：Industrial Grade (-40 ~ +85 ℃)
E0H：40-pin EDC, InnoLite EDC, Vertical	
E4H：44-pin EDC, Vertical	**Code 14th (Internal Control Code)**
	1: 1st PCB version, default setting
Code 6th ~8th (Capacity)	4: Preformat, Fixed Mode + PIO Mode 4
128：128MB	5: Pre-formatted (iCF1SE only) + UltraDMA 4
256：256MB	7: Fixed Mode + PIO Mode 4
512：512MB	8: Fixed Mode + MwDMA Mode 2
01G：1GB	
02G：2GB	**Code 15th (Channel of data transfer)**
04G：4GB	S: Single Channel
	D: Dual Channels
Code 9th ~ 11th (Series)	**Code 16th (Flash)**
D41：EDC 1SE	B: Toshiba SLC
Code 12th (FW version)	**Code 18th**
A: Standard F/W version	Customized code

Horizontal Type

CODE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
	D	**E**	**0**	**P**	**X**	**-**	**5**	**1**	**2**	**D**	**4**	**1**	**A**	**C**	**X**	**S**	**B**	**-**	**X**
Description	Disk	EDC1SE 40-pin,Horzontal				-	Capacity			Category			FW version	Operation Temp.	Internal Control	CH	flash		Customized Code

Definition	
Code 1st (Disk)	**Code 14th (Operation Temperature)**
D : Disk	C：Standard Grade (0 ~ +70 ℃)
Code 2nd ~ 5th (Form Factor)	W：Industrial Grade (-40 ~ +85 ℃)
E0P：40-pin EDC, Horizontal	
E4P：44-pin EDC, Horizontal	**Code 15th (Internal Control Code)**
* code 5th : A/B/C/D/E/F for EDC horizontal type only	1: 1st PCB version, default setting
	4: Preformat, Fixed Mode + PIO Mode 4
Code 7th ~9th (Capacity)	5: Pre-formatted (iCF1SE only) + UltraDMA 4
128：128MB	7: Fixed Mode + PIO Mode 4
256：256MB	8: Fixed Mode + MwDMA Mode 2
512：512MB	
01G：1GB	**Code 16th(Channel of data transfer)**
02G：2GB	S: Single Channel
04G：4GB	D: Dual Channels
08G：8GB	**Code 17th (Flash)**
	B: Toshiba SLC
Code 10th ~ 12th (Series)	**Code 19th**
D41：EDC 1SE	Customized code
Code 13th (FW version)	
A: Standard F/W version	