Approval Sheet

Customer	
Product Number	**M1UF-1GMC2C03-J**
Module speed	**PC-3200**
Pin	**184 pin**
CAS Latency	**CL-3**
Operating Temp	**0 ℃ ~ 70 ℃**
Date	**1st June 2018**

Rev 1.0

The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=2	CL=2.5	CL=3			
PC-3200	**F**	266	333	400	15	15	55

- JEDEC Standard 184-pin Dual In-Line Memory Module
- Intend for 400 MHz applications
- Inputs and Outputs are SSTL-2 compatible
- VDD=VDDQ= 2.6 Volt ± 0.1 (PC-3200)
- Differential clock input
- DLL aligns DQ and DQS transition with CK transition
- Bi-Directional data strobe with one clock cycle
- Built with 512Mb DDR SDRAMs
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Auto & self refresh 7.8μs ($T_A \leq +70°C$)
- SDRAM Operation Temperature
  - $-0°C \leq T_A \leq +70°C$
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 2,2.5, 3
  - Burst Length: 2, 4 or 8
- RoHS Compliant *(Section 12)*

2. Environmental Requirements

DDR UDIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to 55	°C	1
H_{OPR}	Operating Humidity (relative)	10 to 90	%	1
T_{STG}	Storage Temperature	-50 to 100	°C	1
H_{STG}	Storage Humidity (without condensation)	5 to 95	%	1
P_{BAR}	Barometric Pressure (operating & storage)	105 to 69	kPa	1,2

1. Stresses greater than those listed may cause permanent damage to the device. This is a stress rating only, and device functional operation at or above the conditions indicated is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. Up to 9850 ft.
Following JEDEC specifications.

3. Ordering Information

DDR UDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M1UF-1GMC2C03-J	1GB	PC-3200	128M x64	16	2	N/A

4. Pin Assignments and Descriptions

Front				Back			
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	48	A0	93	VSS	140	NC
2	DQ0	49	NC	94	DQ4	141	A10
3	VSS	50	VSS	95	DQ5	142	NC
4	DQ1	51	NC	96	VDDQ	143	VDDQ
5	DQS0	52	BA1	97	DM0/DQS9	144	NC
6	DQ2	Key		98	DQ6	Key	
7	VDD	53	DQ32	99	DQ7	145	VSS
8	DQ3	54	VDDQ	100	VSS	146	DQ36
9	NC,A15	55	DQ33	101	NC	147	DQ37
10	NC	56	DQS4	102	NC,TEST	148	VDDQ
11	VSS	57	DQ34	103	A13	149	DM4/DQS13
12	DQ8	58	VSS	104	VDDQ	150	DQ38
13	DQ9	59	BA0	105	DQ12	151	DQ39
14	DQS1	60	DQ35	106	DQ13	152	VSS
15	VDDQ	61	DQ40	107	DM1/DQS10	153	DQ44
16	CK1	62	VDDQ	108	VDD	154	/RAS
17	/CK1	63	/WE	109	DQ14	155	DQ45
18	VSS	64	DQ41	110	DQ15	156	VDDQ
19	DQ10	65	/CAS	111	CKE1	157	/S0
20	DQ11	66	VSS	112	VDDQ	158	/S1
21	CKE0	67	DQS5	113	BA2	159	DM5/DQS14
22	VDDQ	68	DQ42	114	DQ20	160	VSS
23	DQ16	69	DQ43	115	A12	161	DQ46
24	DQ17	70	VDD	116	VSS	162	DQ47
25	DQS2	71	NC,/S2	117	DQ21	163	NC,/S3
26	VSS	72	DQ48	118	A11	164	VDDQ
27	A9	73	DQ49	119	DM2/DQS11	165	DQ52
28	DQ18	74	VSS	120	VDD	166	DQ53
29	A7	75	/CK2	121	DQ22	167	NC,A13
30	VDDQ	76	CK2	122	A8	168	VDD
31	DQ19	77	VDDQ	123	DQ23	169	DM6/DQS15
32	A5	78	DQS6	124	VSS	170	DQ54
33	DQ24	79	DQ50	125	A6	171	DQ55
34	VSS	80	DQ51	126	DQ28	172	VDDQ
35	DQ25	81	VSS	127	DQ29	173	NC,A14
36	DQS3	82	VDDID	128	VDDQ	174	DQ60
37	A4	83	DQ56	129	DM3/DQS12	175	DQ61
38	VDD	84	DQ57	130	A3	176	VSS
39	DQ26	85	VDD	131	DQ30	177	DM7/DQS16
40	DQ27	86	DQS7	132	VSS	178	DQ62
41	A2	87	DQ58	133	DQ31	179	DQ63
42	VSS	88	DQ59	134	NC	180	VDDQ
43	A1	89	VSS	135	NC	181	SA0
44	NC	90	NC	136	VDDQ	182	SA1
45	NC	91	SDA	137	CK0	183	SA2
46	VDD	92	SCL	138	/CK0	184	VDDSPD
47	NC			139	VSS		

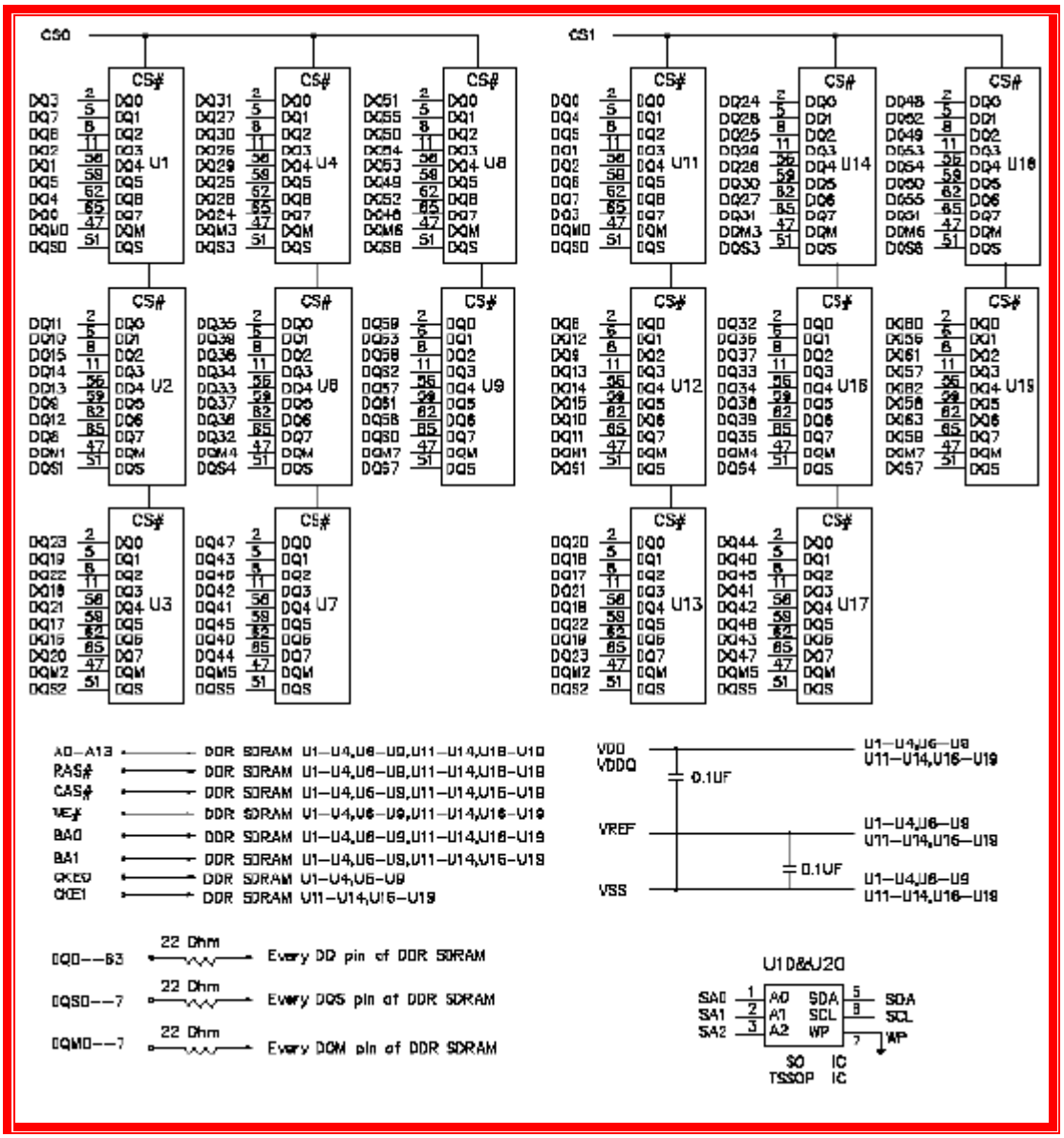
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0–A15	SDRAM address bus	CK0 - CK2	SDRAM clock (positive lines of 3 differential pairs)
BA0–BA1	SDRAM bank select	/CK0 - /CK2	SDRAM clock (negative lines of these three pairs)
DQ0–DQ63	DIMM memory data bus	SCL	I^2C serial bus clock for EEPROM
CB0–CB7	DIMM ECC check bits	SDA	I^2C serial bus data line for EEPROM
/RAS	SDRAM row address strobe	SA0-SA2	I^2C slave address select for EEPROM
/CAS	SDRAM column address strobe	V_{DD}*	SDRAM positive power supply
/WE	SDRAM write enable	$V_{DD}Q$*	SDRAM I/O Driver positive power supply
/S0 - /S1	SDRAM chip select lines (Phys. banks 0 and 1)	V_{REF}	SDRAM I/O reference supply
CKE0–CKE1	SDRAM clock enable lines	V_{SS}	Power supply return (ground)
DQS0–DQS8	SDRAM low data strobes	V_{DDSPD}	Serial EEPROM positive power supply (2.5 Volts to 3.3 Volts)--VDDSPD is not connected to VDD or VDDQ
DM(0-8),DQS(9-17)	SDRAM low data masks/high data strobes (x4, 2 Phys. banks)	NC	Spare pins (no connect)
VDDID	VDD identification flag	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
*The V_{DD} and $V_{DD}Q$ pins are tied common to a single power-plane on these designs.			

6. Function Block Diagram:

- (1GB, 2 Ranks, 64Mx8 DDR SDRAM base UDIMM)



7. SDRAM Absolute Maximum Ratings

Symbol	Parameter	Min.	Max.	Units
T_{STG}	Storage Temperature	-55	150	°C
V_{INPUT}	Voltage input pins relative to Vss	-1.0	3.6	V
V_{IO}	Voltage on I/O pins relative to Vss	-0.5	VDDQ+0.5	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0	3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-1.0	3.6	V
I_{OS}	Output short Circuit Current		50	mA

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. AC & DC Operating Conditions

AC Input Operating Conditions

Symbol	Parameter	Value		Units	Notes
		Min	Max		
V_{IH} (AC)	Input High (Logic1) Voltage	V_{REF} + 0.31	-	V	1
V_{IL} (AC)	Input Low (Logic0) Voltage	-	V_{REF} - 0.31	V	1
V_{ID} (AC)	Input differential Voltage: CK, /CK	0.7	V_{DDQ} + 0.6	V	2
V_{IX} (AC)	Input crossing point Voltage: CK, /CK	0.5* V_{DDQ} - 0.2	0.5* V_{DDQ} + 0.2	V	3
$V_{REF(AC)}$	I/O reference voltage	0.49*V_{DDQ}	0.51*V_{DDQ}	V	4

Note:

1. VIH overshoot: VIH,max = VDDQ + 1.5V for a pulse width 3ns, and the pulse width can not be greater than 1/3 of the cycle rate. VIL undershoot: VIL,min = –1.5V for a pulse width 3ns, and the pulse width can not be greater than 1/3 of the cycle rate.
2. VID is the magnitude of the difference between the input level on CK and the input level on CK#.
3. The value of VIX and VMP is expected to equal VDDQ/2 of the transmitting device and must track variations in the DC level of the same.
4. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on VREF may not exceed ±2% of the DC value. Thus, from VDDQ/2, VREF is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest VREF bypass capacitor.

DC Electrical Characteristics and Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Units	Notes
V_{DD}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	1
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	1
V_{DDQ}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	1
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	1
$V_{IH\ (DC)}$	Input High (Logic1) Voltage	VREF + 0.15	-	VDD + 0.3	V	2
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage	-0.3	-	VREF - 0.15	V	2
V_{TT}	Termination Voltage	VREF-0.04		VREF+0.04	V	3
I_I	Input leakage current:	-2		2	uA	
V_{REF}	I/O Reference Voltage	0.49VDDQ	0.5VDDQ	0.51VDDQ	V	4
$V_{IN(DC)}$	Input Voltage Level: CK, /CK	-0.3	-	VDDQ + 0.3	V	4
$V_{ID(DC)}$	Input Differential Voltage: CK, /CK	0.36	-	VDDQ + 0.6	V	4,5

Note:

1. VDD and VDDQ must track each other.
2. To maintain a valid level, the transitioning edge of the input must:
   Sustain a constant slew rate from the current AC level through to the target AC level, VIL(AC) or VIH(AC).
   Reach at least the target AC level.
   After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).
3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, it is expected to be set equal to VREF, and it must track variations in the DC level of VREF.
4. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on VREF may not exceed ±2% of the DC value. Thus, from VDDQ/2, VREF is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest VREF bypass capacitor.
5. VID is the magnitude of the difference between the input level on CK and the input level on CK#.

9. Operating, Standby, and Refresh Currents

- 1GB UDIMM (2 Rank, 64Mx8 DDR SDRAMs)

Symbol	Parameter/Condition	PC-3200	Unit
I DD0	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	1200	mA
I DD1	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	1360	mA
I DD2P	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	80	mA
I DD2F	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle.VIN=VREF for DQ, DQS and DM	368	mA
I DD3P	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	288	mA
I DD3N	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge;tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	640	mA
I DD4R	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	1920	mA
I DD4W	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	1920	mA
I DD5	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	1920	mA
I DD6	CKE=<0.2V; External clock on; tCK=tCK(min)	80	mA
I DD7	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	3680	mA

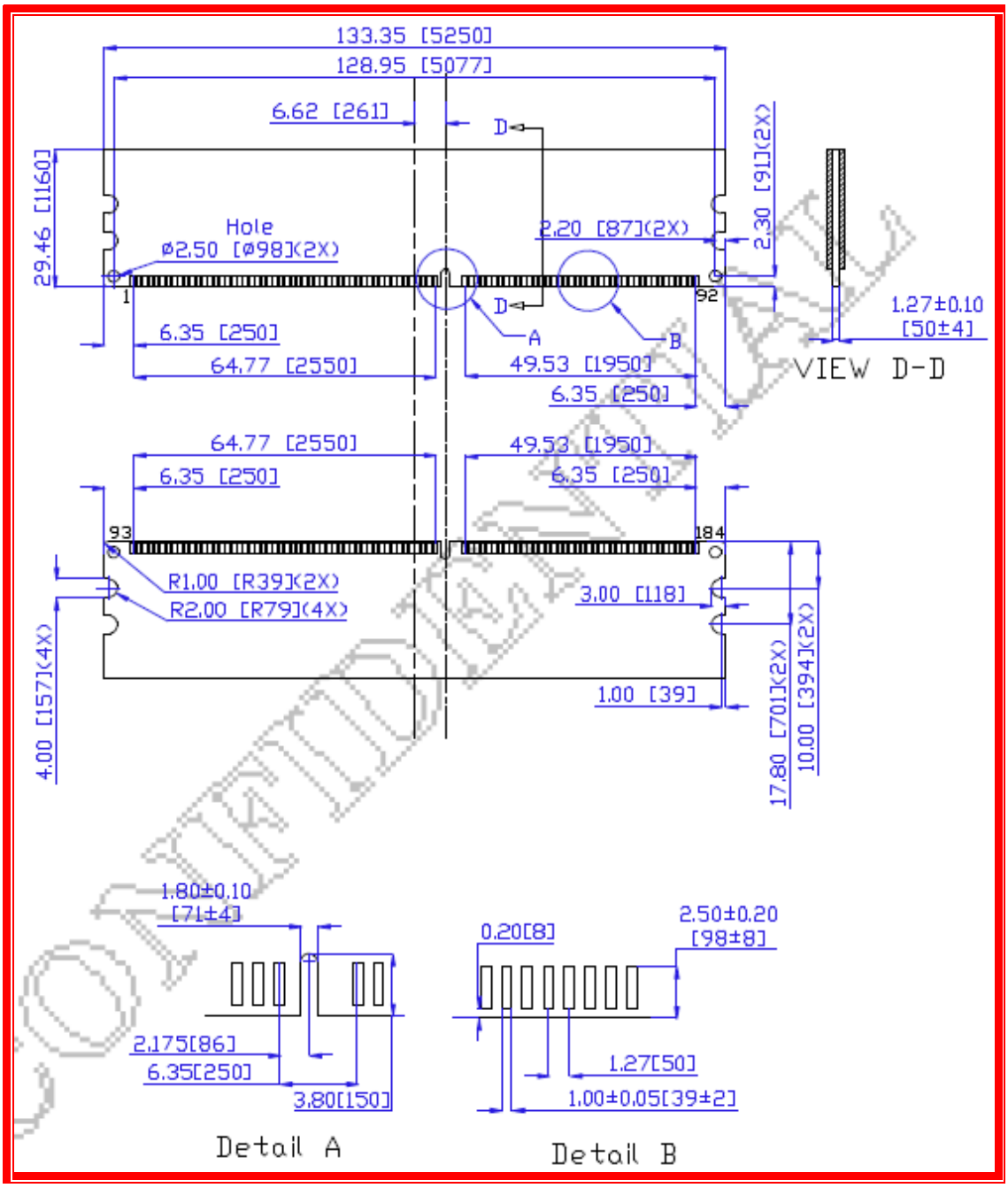
10. AC Timing Specifications

Symbol	Parameter	PC2-3200		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.7	0.7	ns
tDQSCK	DQS output access time from CK/CK#	-0.60	0.60	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	min (tCL,tCH)	-	ns
tCK	Clock Cycle Time	5	7.5	ns
tDS	DQ and DM input setup time(differential data strobe)	0.4	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.4	-	ns
tIPW	Input pulse width	2.2	-	ns
tDIPW	DQ and DM input pulse width (each input)	1.75	-	ns
tHZ	Data-out high-impedance time from CK/CK	-	0.7	ns
tLZ	Data-out Low-Z window from CK/CK#	-0.7	-	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.4	ns
tQHS	Data hold Skew Factor	-	0.5	ns
tQH	Data output hold time from DQS	tHP –tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	0.72	1.28	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.2	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.2	-	tCK
tMRD	Mode register set command cycle time	10	-	ns
tWPST	Write postamble	0.4	0.6	tCK
tWPRE	Write preamble	0.25		tCK
tIH	Address and control input hold time	0.6	-	ns
tIS	Address and control input setup time	0.6	-	ns

t_{RPRE}	Read preamble	0.9	1.1	t_{CK}
t_{RPST}	Read postamble	0.4	0.6	t_{CK}
t_{RRD}	Active bank A to Active bank B command	10	-	ns
t_{REFI}	Average Periodic Refresh Interval	-	7.8	µs
t_{WR}	Write recovery time without Auto-Precharge	15		ns
t_{WTR}	Internal write to read command delay	2	-	t_{CK}
t_{XSNR}	Exit self refresh to a Non-read command	70	-	ns
t_{XSRD}	Exit self refresh to a Read command	200	-	t_{CK}

11. PACKAGE DIMENSION

- (1GB, 2 Ranks, 64Mx8 DDR SDRAMs)



Note: All dimensions are in millimeters and should be kept within a tolerance of ±0.15, unless otherwise specified.

12. RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯 (DEHP)	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯 (BBP)	< 1000 ppm
鄰苯二甲酸二丁酯 (DBP)	< 1000 ppm
鄰苯二甲酸二異丁酯 (DIBP)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2017 / 01 / 18

13. Revision Log

Rev	Date	Modification
0.1	1st June 2018	Preliminary Edition
1.0	1st June 2018	Official Released.