AEx-9XXAP(H)

15”, 15.6”, 19”, and 21.5” Full IP66 Stainless Steel Designed with M12 waterproof connector of Panel PC Series.

User Manual

Release Date	Revision
Mar. 2022	V2.0

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Revision History

Reversion	Date	Description
0.1	2017/11/24	For Preliminary Release
1.0	2018/01/02	Official version
1.1	2018/03/27	Modify power pin defined
1.2	2018/05/16	Modify power pin description
1.3	2018/06/22	Add Warning
1.4	2018/10/12	Revise specification wording
1.5	2019/08/16	Modify MB Information
1.6	2020/10/16	Modify 1.2 Spec data
1.7	2021/06/24	Add IECEX/ATEX Standards in P5
1.8	2021/10/28	Add pin define information in 1.2
1.9	2022/01/20	Modify ATEX Standards and Notice, Certification information
2.0	2022/03/11	Add UKCA LOGO and Standards

Warning!_____

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, it may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Electric Shock Hazard – Do not operate the machine with its back cover removed. There are dangerous high voltages inside.

If you need to connect or reconnect M12 cables, please make sure turning off the power before all the replacement procedures and must in normal environment, Recommend use ATEx certificated IO cables.

Disclaimer

This information in this document is subject to change without notice. In no event shall Aplex Technology Inc. be liable for damages of any kind, whether incidental or consequential, arising from either the use or misuse of information in this document or in any related materials.

ATEX Instruction Guide

SAFETY INSTRUCTIONS

Read these instructions carefully, and look at the equipment to become familiar with the device before trying to install, operate, or maintain it. The following special messages may appear throughout this documentation or on the equipment to warn of potential hazards or to call attention to information that clarifies or simplifies a procedure.

This is the safety alert symbol. It is used to alert you to potential personal injury hazards. Obey all safety messages that follow this symbol to avoid possible injury or death.

PLEASE NOTE

Electrical equipment should be installed, operated, serviced, and maintained only by qualified personnel. No responsibility is assumed by Digital Electronics Corporation for any consequences arising out of the use of this material. A qualified person is one who has skills and knowledge related to the construction and operation of electrical equipment and its installation, and has received safety training to recognize and avoid the hazards involved.

SCOPE

This present document applies when AEx-9XXAP(H) Series bears  marking. They are supplied only with DC 9~36 V. This documentation has to be kept and always refer to those instructions for installation, operation, maintenance or evolution of your system.

Permitted zones of application

Refer to the section titled "Markings" to get information about the permitted zones of protection and the types of protection.

- AEx-9XXAP(H) Series is installed in zones 2 hazardous areas must be certified and bear the  marking.
- Ensure with the marking that the terminals are compatible with the conditions permitted for the hazardous area at the site where it is being used.

Notice

1. **Under certain extreme circumstances, the label may generate an ignition-capable level of electrostatic charge. Therefore the equipment shall not be installed in a location where the external conditions are conducive to the build-up of electrostatic charge on the label. In addition, the label shall only be cleaned with a damp cloth.**

2. **Warning – in locations where high external humidity and internal temperature variations (e.g. frequent on-off cycles) may cause condensation inside the equipment, the interior should be periodically inspected.**

3. **When the device is mounted in a hazardous area, connection and disconnection of external connectors while live is only permitted if the potentially explosive atmosphere is shown to be absent.**

4. **The "9-36" Vdc rated supply shall be protected such that transients are limited to a maximum of 119 V; no such protection is required for the signal lines.**

5. **Equipotential bonding facilities on the outside of enclosure are assessed as providing effective connection of a conductor with a cross-sectional area of at least 4 mm2, 10AWG, 600V wire**

6. **The equipment is suitable for use in class I, division 2, groups A, B, C, D, Class II, Division2, Group F,G, T135℃, Class III OR non-hazardous locations only.**

7. **Warning- Do not use USB while the circuit is live unless the area is known to be non-hazardous.**

8. **Electrostatic charging hazard - Clean only with a damp cloth.**

Markings

Markings applied to the AEx-9XXAP(H) Series Graphic Operator Interface, are as follows:

AEx-9XXAP(H) Series
Ex ec ic IIC T4 Gc **CID2, CIID2, CIII, IP66** **Ex tc IIIC T135°C Dc** **Power Input Voltage: DC 9~36V** WARNING: Read instruction manual before installation and use.

Below designated standards were certified with conform the relevant regulations:

New standards		
 II 3GD Ex ec ic IIC T4 Gc Ex tc IIIC T135°C Dc		
IECEx	ATEX	UKCA
IEC 60079-0:2017	EN 60079-0:2018	BS 60079-0:2018
IEC 60079-11:2011	EN 60079-11:2012	BS 60079-11:2012
IEC 60079-7:2015 +AMD1:2017	EN 60079-7:2015/A1:2018	BS 60079-7:2015/A1:2018
IEC 60079-31:2013	EN 60079-31:2014	BS 60079-31:2014

Table of Contents

Chapter 1 Getting Started

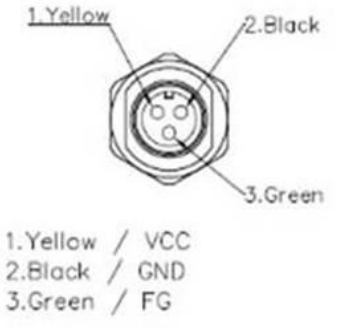
1.1 Features

- Intel® 6th generation core i5/i3 Processors
- Full flat bezel and fanless design

- Full IP66 grade with M12 waterproof connector
- Wide range DC 9~36V power input
- Projective capacitive touch supports
- 316 Stainless steel design
- Various of IO applications
- Support Panel/VESA mount
- ATEX Zone2/22, IECEx and C1D2/C2D2/C3/UKCA Certified

1.2 Specifications

<table>
<tr><th></th><th>AEx-915AP(H)</th><th>AEx-916AP</th><th>AEx-919AP(H)</th><th>AEx-921AP</th></tr>
<tr><td colspan="5">System</td></tr>
<tr><td>CPU</td><td colspan="4">Onboard Intel® 6th generation core i5-6300U/i3-6100U</td></tr>
<tr><td>Chipset</td><td colspan="4">SoC</td></tr>
<tr><td>Memory</td><td colspan="4">1 x 260-pin SO-DIMM DDR4 2133MHz, up to 16GB</td></tr>
<tr><td colspan="5">Outside IO Port</td></tr>
<tr><td>USB</td><td colspan="2">1 x M12 for USB 2.0 with waterproof cover and chain
<table>
<tr><th>CN1</th><th>Pin Define</th></tr>
<tr><td>1</td><td>USB1 5V</td></tr>
<tr><td>3</td><td>D1-</td></tr>
<tr><td>4</td><td>D1+</td></tr>
<tr><td>7</td><td>GND</td></tr>
<tr><td>2</td><td>USB2 5V</td></tr>
<tr><td>5</td><td>D2-</td></tr>
<tr><td>6</td><td>D2+</td></tr>
<tr><td>8</td><td>GND</td></tr>
</table></td><td colspan="2"> 
</td></tr>
<tr><td>Serial/Parallel</td><td colspan="2">1 x M12 for RS-232/422/485, Default RS-232
<table>
<tr><th>CN1</th><th>RS-232/422/485</th><th>CN2</th></tr>
<tr><td>1</td><td>DCD / 422R+</td><td>1</td></tr>
<tr><td>2</td><td>RXD / 422R-</td><td>2</td></tr>
<tr><td>3</td><td>TXD / 422T- / 485-</td><td>3</td></tr>
<tr><td>4</td><td>DTR / 422T+ / 485+</td><td>4</td></tr>
<tr><td>5</td><td>GND</td><td>5</td></tr>
<tr><td>6</td><td>DSR</td><td>6</td></tr>
<tr><td>7</td><td>RTS</td><td>7</td></tr>
<tr><td>8</td><td>CTS</td><td>8</td></tr>
</table></td><td colspan="2"> 
</td></tr>
</table>

<table>
<tr><td>LAN</td><td>1 x M12 8-pinfor LAN with waterproof cover and chain
<table><tr><td></td><td>Pin Define</td></tr><tr><td>1</td><td>LAN1_0+</td></tr><tr><td>2</td><td>LAN1_0-</td></tr><tr><td>3</td><td>LAN1_1+</td></tr><tr><td>4</td><td>LAN1_1-</td></tr><tr><td>5</td><td>LAN1_2+</td></tr><tr><td>6</td><td>LAN1_2-</td></tr><tr><td>7</td><td>LAN1_3+</td></tr><tr><td>8</td><td>LAN1_3-</td></tr></table></td><td> 
</td></tr>
<tr><td>Power</td><td>1 x DC power input (9~36V) by M12 connector
<table><tr><td></td><td>Pin Define</td></tr><tr><td>1</td><td>VCC (Yellow)</td></tr><tr><td>2</td><td>GND (Black)</td></tr><tr><td>4</td><td>FG (Green)</td></tr></table></td><td> 
</td></tr>
<tr><td>Ohers</td><td colspan="2">1 x Power Switch on the rear</td></tr>
<tr><td colspan="3">IO Port</td></tr>
<tr><td>USB</td><td colspan="2">1 x M12 for 2 x USB2.0 with waterproof cover and chain</td></tr>
<tr><td>Serial/Parallel</td><td colspan="2">1 x M12 for COM1— RS-232(RS-422/485 for option) with waterproof cover and chain</td></tr>
<tr><td>LAN</td><td colspan="2">2 x M12 for LAN with waterproof cover and chain</td></tr>
<tr><td>Power</td><td colspan="2">1 x M12 for DC power input with waterproof cover and chain</td></tr>
<tr><td>VGA</td><td colspan="2">1 x M12 for VGA with waterproof cover and chain</td></tr>
<tr><td colspan="3">Expansion</td></tr>
<tr><td>Expansion slot</td><td colspan="2">1 x Mini PCIe full size slot</td></tr>
<tr><td colspan="3">Storage Space</td></tr>
<tr><td>Storage</td><td colspan="2">1 x 2.5” SATA HDD or SSD space
1 x mSATA slot</td></tr>
<tr><td colspan="3">Display</td></tr>
</table>

Display type	15” color TFT LCD		15.6” color TFT LCD	19” color TFT LCD		21.5” color TFT LCD
Max. Resolution	1024 x 768		1920 x 1080	1280 x 1024		1920 x 1080
Max. Color	16.2M	262K	16.7M	16.7M		16.7M
Luminance (cd/m^2)	450	1000	400	350	1000	300

Contrast Ratio	800: 1		700: 1	1000: 1	3000: 1
Viewing Angle	160(H) / 150(V)		160(H) / 140(V)	170(H) / 160(V)	178(H) / 178(V)
Backlight Lifetime	70,000hrs	50,000hrs	50,000 hrs	70,000 hrs	50,000 hrs
Touch Screen					
Type	Project Capacitive Touch				
Interface	USB				
Light Transmission	Over 90%				
Power					
Power Input	DC 9~36V				
Power Consumption	MAX: 21W		MAX: 27W	MAX: 24W	MAX: 37W
Mechanical					
Construction	316 Stainless Steel Chassis				
Mounting	VESA Mount 100 x100 (default) Panel Mount (option)				
Dimension (mm)	399 x 324 x 70		440 x 290 x 75	470 x 388.6 x 75	571 x 362 x 75.1
Net Weight (Kg)	9.6		10	13.2	13.4	12.6
Environmental					
Operating temperature	-20~60°C				
Storage temperature	-30~70°C				
Humidity	10 to 95% @ 40°C, non- condensing				
Altitude limit for application	Under 2000m				
Overvoltage category	CAT II				
Pollution degree	2				
Certification	CE / FCC Class A IECEx Certification: Ex ec ic IIC T4 Gc Ex tc IIIC T135°C Dc ATEX Certification: Ⓔx II 3 GD Certification: Class I, Division2, Group A,B,C,D,T4 Class II, Division2, Group F,G, T135℃ Class III ANSI/ISA 12.12.01-2013 CSA Std.C22.2 No213-1987 CSAE 22UKEX 1073X				

IP level	Total IP66 6 sides
Operating System Support	
OS Support	Windows Embedded Standard 7 Windows Embedded 8.1 Windows 10 IOT Enterprise LTSB 2016

1.3 Dimensions

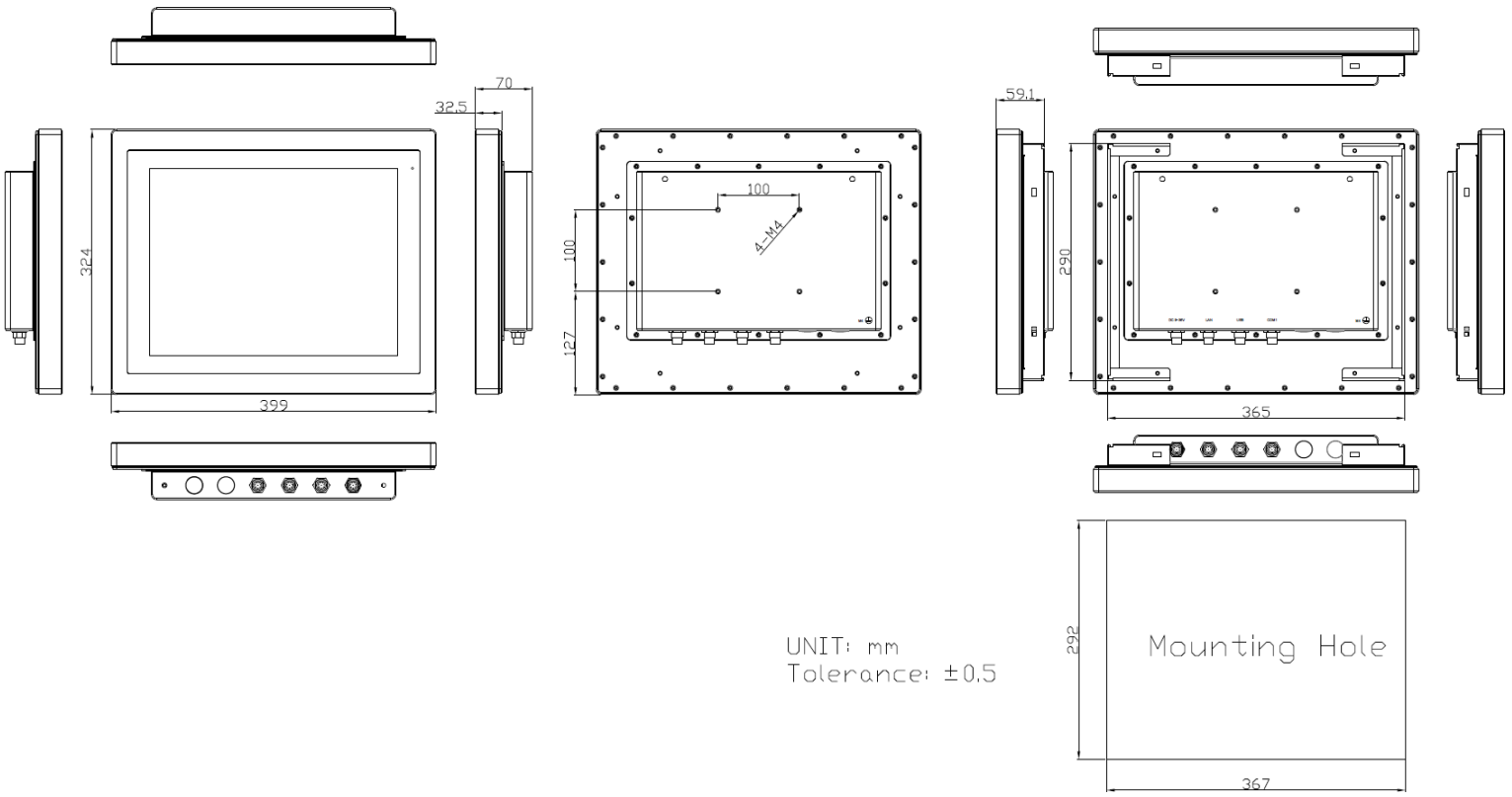


Figure 1.1: Dimensions of AEx-915AP(H)

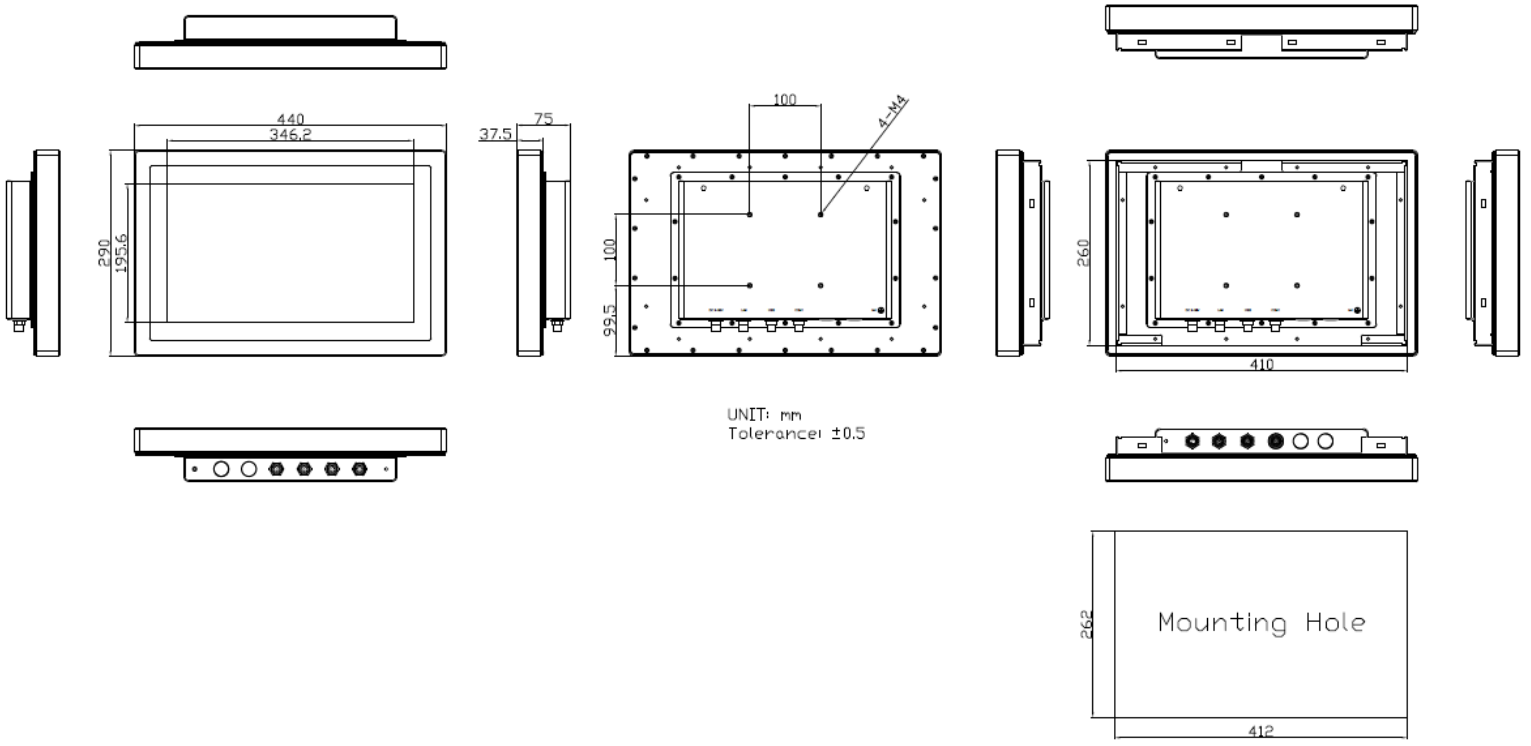


Figure 1.2: Dimensions of AEx-916AP

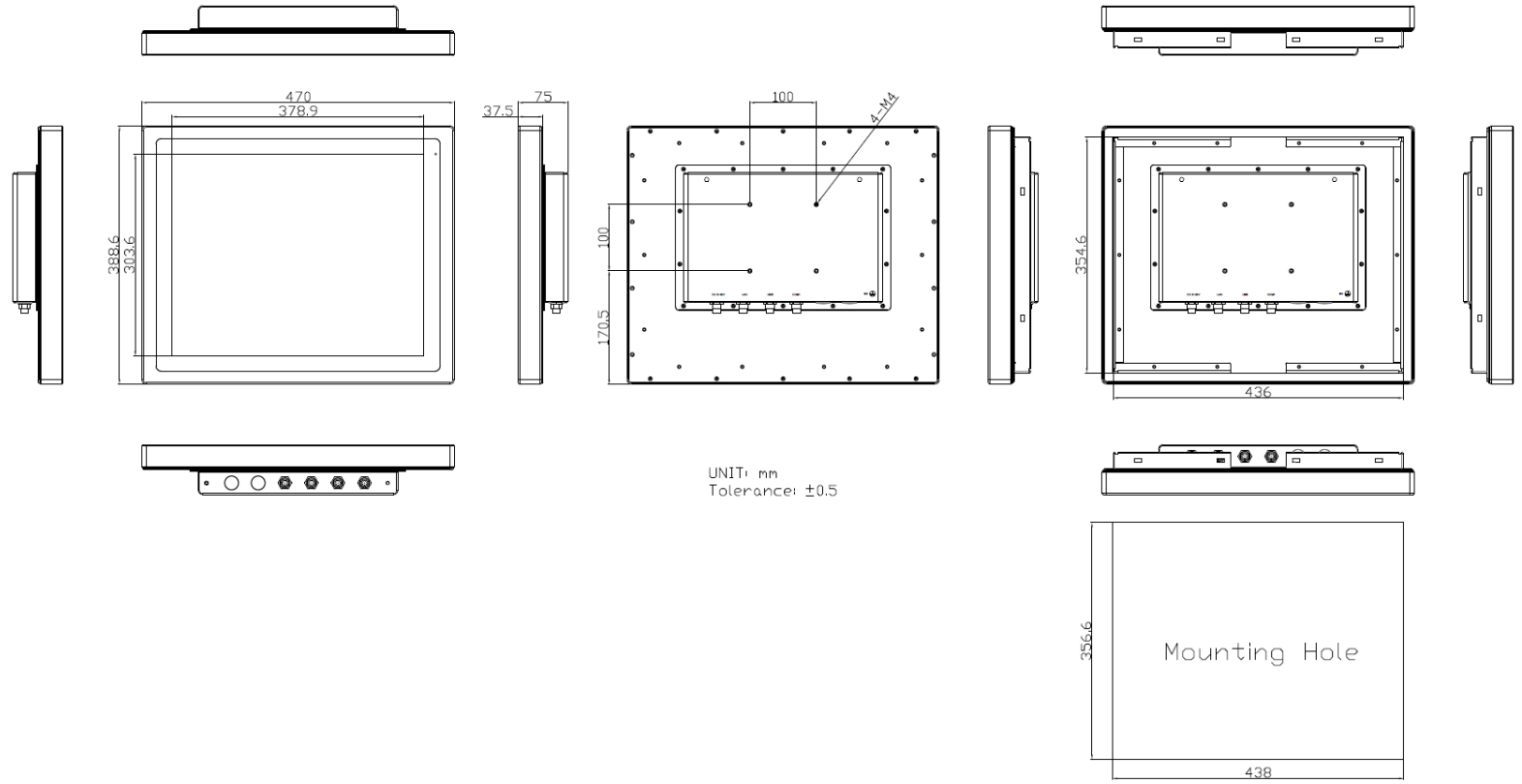


Figure 1.3: Dimensions of AEx-919AP(H)

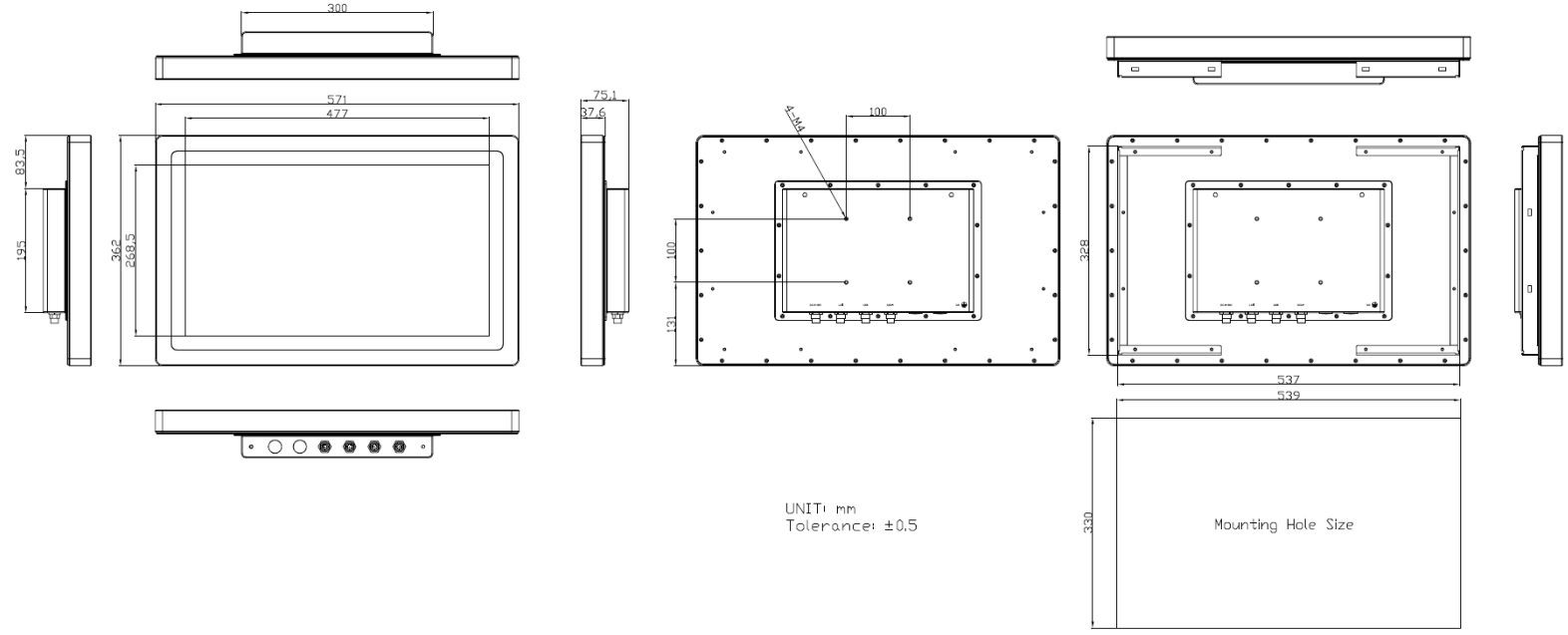


Figure 1.4: Dimensions of AEx-921AP

1.4 Brief Description of AEx-9XXAP(H) Series

AEx-9XXAP(H) are panel PC series models for ATEX certification, which comes with full waterproof with IP66 level designed. It is powered by Intel 6th generation core i5/i3 processor and supports 1 x so-dimm DDR4 up to 16GB. It comes with a 15”, 15.6”, 19”, and 21.5” color TFT display. This model are designed by full waterproof connector with 1x USB2.0 (support 2x USB2.0 function), 1x LAN, 1x COM and 1x VGA for standard I/O port, but also can be replaced by USB2.0/3.0 or RS-232. The model supports wide range DC 9~36V power input and can be panel mounted and VESA mounted. AEx-9XXAP(H) series has more outstanding features, thus you can use it in some difficult environment and give the best in monitoring and control applications.

Figure 1.5: Front View of AEx-9XXAP(H) Series

Figure 1.6: Rear View of AEx-9XXAP(H) Series

1.5 VESA Mounting

The AEx-9XXAP(H) series is designed to be VESA mounted as shown in Picture. Just carefully place the unit through the hole and tighten the given screws from the rear to secure the mounting.

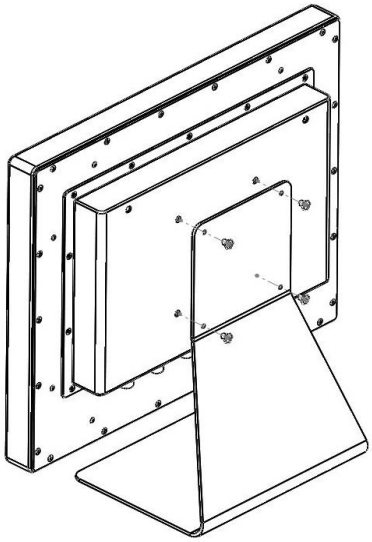


Figure 1.7: AEx-9XXAP(H) Series VESA Mounting

1.6 Panel Mounting

There are six holes located along the four sides of the panel PC. Insert the clamp from the four sides and tighten them with the nuts provided.

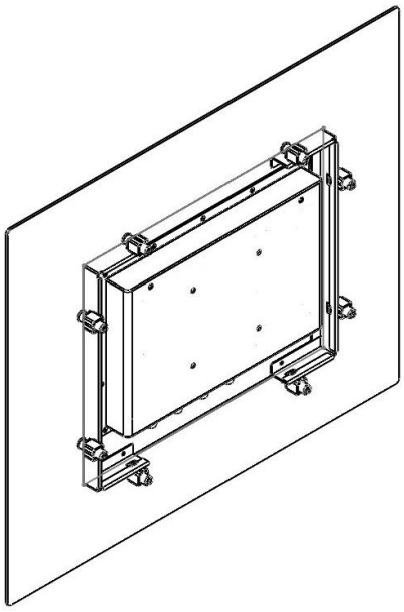


Figure 1.8: AEx-9XXAP(H) Series Panel Mounting

Chapter 2 Hardware

2.1 Motherboard Introduction

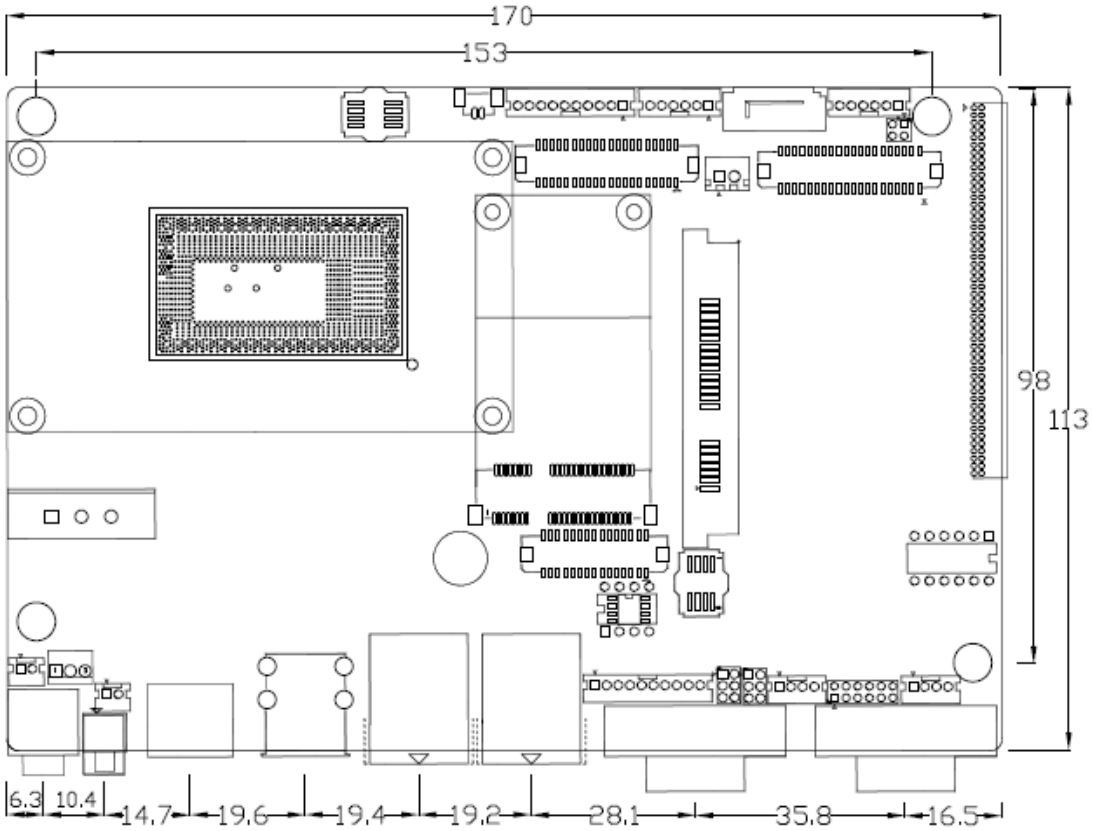
SBC-7114 is a 4" industrial motherboard developed on the basis of Intel Skylake-U/Kabylake-U Processor, which provides abundant peripheral interfaces to meet the needs of different customers. Also, it features dual GbE ports, 6-COM ports and one mSATA configuration, one HDMI port, one LVDS interface. To satisfy the special needs of high-end customers, CN1 and CN2 and CN3 richer extension functions. The product is widely used in various sectors of industrial control.

2.2 Specifications

Specifications	
Board Size	170mm x 113mm
CPU Support	Intel® Core™ i3-6100U /2.30GHz (onboard) Intel® Core™ /i5-6300U /2.40 up to 3.00GHz (option) Intel® Core™ /i7-6600U /2.60 up to 3.40GHz (option)
Chipset	SOC
Memory Support	1x SO-DIMM (260pins), up to 16GB DDR4 2133MHz FSB
Graphics	Intel® HD Graphics 520
Display Mode	1 x HDMI 1.4Port 1 x LVDS (18/24-bit dual LVDS) 1 x DP Signal Port (DF13-40P)
Support Resolution	Up to 4096 x 2304 for HDMI Up to 1920 x 1200 for LVDS (PS8625) Up to 4096 x 2304 for DP1
Dual Display	HDMI + LVDS HDMI + DP1 (option) LVDS + DP1 (option) HDMI + LVDS + DP1 (option)
Super I/O	Nuvoton NCT6106D
BIOS	AMI/UEFI
Storage	1 x SATAIII Connector (7P) 1 x SATAIII Connector (7P+15P)

	1 x MSATA Connector (option)
Ethernet	2 x PCIe Gbe LAN by Intel I210-AT
USB	2 x USB 3.0 (type A)stack ports (USB3) (USB3.0:USB3-1/USB3-2,USB2.0:USB1/USB2) 4 x USB 2.0 Pin header for CN3 (USB3/USB4/USB8/USB9) 2 x USB 3.0/USB2.0 Pin header for CN3 (PCIe 1x or USB3.0, option) 1 x USB 2.0 Pin header for CN2 (USB5) 1 x USB 2.0 Pin header for CN1 (USB7 or Touch, option) 1 x USB 2.0 Pin header for EDP1 (USB7 or Touch, option) 1 x USB 2.0 for MPCIE1 (USB6)
Serial	1 x RS232/RS422/RS485 port, DB9 connector for external (COM1) Pin 9 w/5V/12V/Ring select 1 x RS232 port, DB9 connector for external (COM2) Pin 9 w/5V/12V/Ring select 2 x UART for CN3 (COM3,COM4) 1 x RS422/485 header for CN2 (NCT6106D /COM5) 1 x RS422/485 header for CN2 (NCT6106D /COM6)
Digital I/O	8-bit digital I/O by Pin header (CN2) 4-bit digital Input 4-bit digital Output 4-bit digital I/O by Pin header (CN3) 2-bit digital Input 2-bit digital Output
Battery	Support CR2477 Li battery by 2-pin header (BAT3/CMOS)
Smart battery	1 x Smart battery Support 3 Serial Li battery by 10-pin header (BAT2)
Audio	Support Audio via Realtek ALC269Q HD audio codec Support Line-out by JACK (LINE_OUT1) Support Line-in, Line-out, MIC by 2x6-pin header(AUDIO2) Support a stereo Class-D Speaker Amplifier with 2 watt per channel output power, by 1x4-pin header (SPK1)
Expansion Bus	1 x mini-PCI-express slot (MPCIE or MSATA, Default： MSATA) 1 x PCI-express for CN3 2 x PCI-express for CN3（PCIe 1x or USB3.0, Default： PCIe 1x)
Touch Ctrl	1 x Touch ctrl header for TCH1（USB10）

Power Management	Wide Range DC9V~36V input 1 x 3-pin power input connector
Switches and LED Indicators	1 x Power on/off switch (BT1/BT2/CN2/CN3) 1 x Reset (CN2) 1 x HDD LED status (CN2) 1 x Power LED status (CN1) 1 x Buzzer
External I/O port	2 x COM Ports (COM1/COM2) 2 x USB 3.0 Ports (stack) 2 x RJ45 GbE LAN Ports 1 x HDMI Port 1 x Audio Jack (Line out)
TPM	Infineon's Trusted Platform Module (TPM2.0, option) *Note: Only support Windows 10 IoT*
Temperature	Operating: -20℃ to 70℃ Storage: -40℃ to 85℃
Humidity	10% - 90%, non-condensing, operating
Power Consumption	12V/3A(Intel i3-6100U 2.30 GHz Processor with 16GB DDR4/HDD)
EMI/EMS	Meet CE/FCC class A



(units :mm)

Figure 2.1: Motherboard Dimensions

2.3 Jumpers and Connectors Location

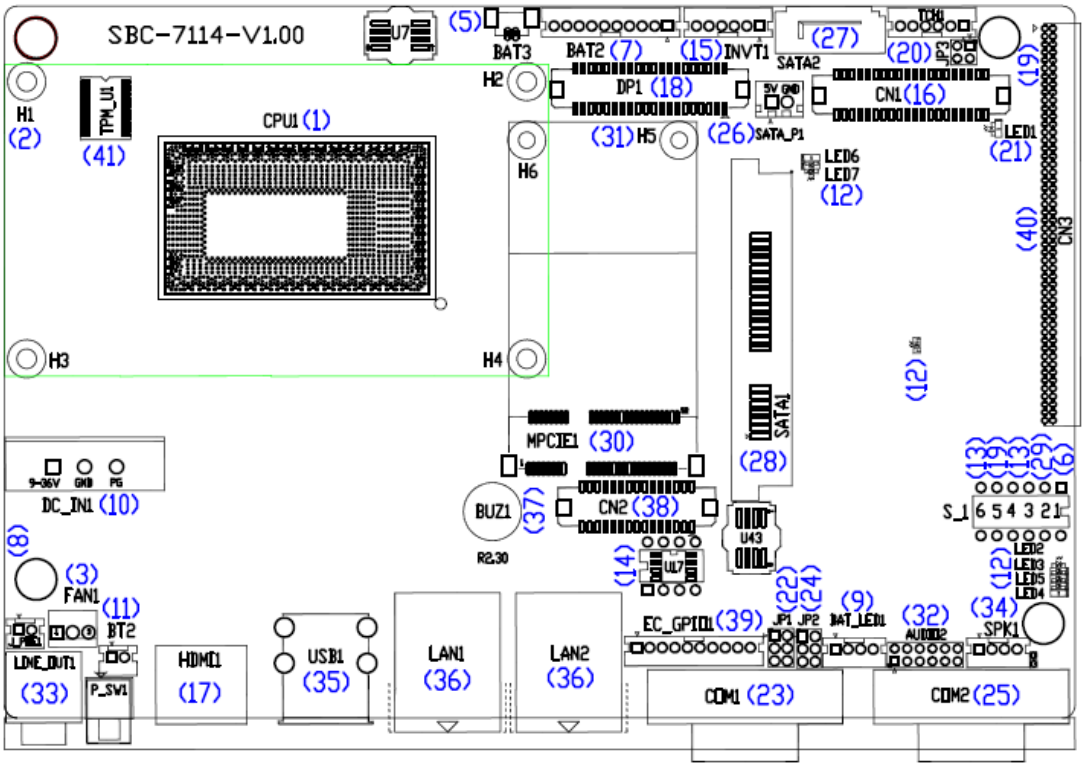


Figure 2.2: Jumpers and Connectors Location- Board Top

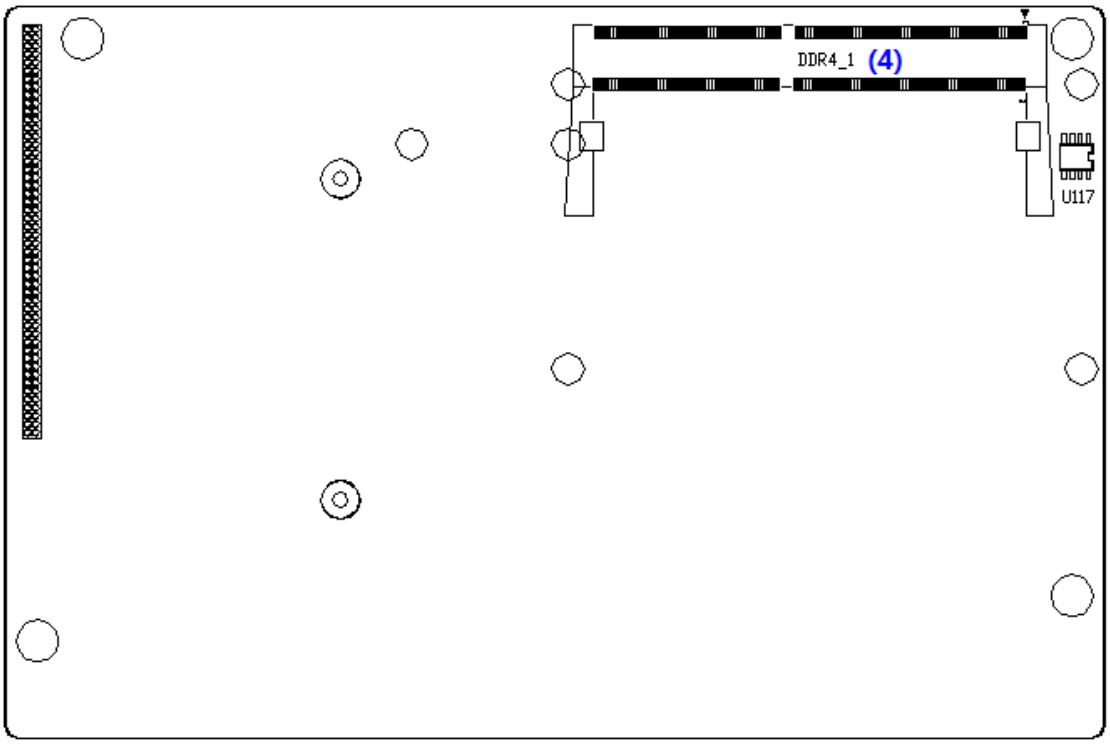


Figure 2.3: Jumpers and Connectors Location- Board Bottom

2.4 Jumpers Setting and Connectors

1. CPU1:

(FCBGA1356), onboard Intel Skylake-U/ Kabylake-U processors.

Model	Processor					
	Number	PBF	Cores/ Threads	TDP	Embedded	Remarks
SBC-7114-I3-6100U	I3-6100U	2.30GHz	2 / 4	15W	●	
SBC-7114-I3-6100UP	I3-6100U	2.30GHz	2 / 4	15W	●	option
SBC-7114-I5-6300U	I5-6300U	2.4 up to 3.0GHz	2 / 4	15W 25W	●	option
SBC-7114-I5-6300UP	I5-6300U	2.4 up to 3.0GHz	2 / 4	15W 25W	●	option
SBC-7114-I7-6600U	I7-6600U	2.6 up to 3.4GHz	2 / 4	15W 25W	●	option
SBC-7114-I7-6600UP	I7-6600U	2.6 up to 3.4GHz	2 / 4	15W 25W	●	option

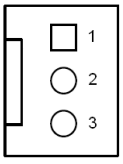
2. H1/H2/H3/H4 (option**):**

CPU1 Heat Sink Screw holes, four screw holes for Intel Skylake-U/Kabylake-U Processors.

Heat Sink assembles.

3. FAN1:

(2.54mm Pitch 1x3 Pin Header), Fan connector, cooling fans can be connected directly for use. You may set the rotation condition of cooling fan in menu of BIOS CMOS Setup.



Pin#	Signal Name
1	Ground

2	VCC
3	Rotation detection

Note:

Output power of cooling fan must be limited under 5W.

4. DDR4_1:

(SO-DIMM 260Pin socket), DDR4 memory socket, the socket is located at the top of the board and supports 260Pin 1.2V DDR4 2133MHz FSB SO-DIMM memory module up to 16GB.

Model	DDR4 Memory Types (FSB)
SBC-7114-I3-6100U/P	2133 MHz
SBC-7114-I5-6300U/P	2133 MHz
SBC-7114-I7-6600U/P	2133 MHz

5. BAT3 :

(1.25mm Pitch 1x2 Wafer Pin Header, SMD) 3.0V Li battery is embedded to provide power for CMOS. CMOS clear operation will permanently reset old BIOS settings to factory defaults.

Pin#	Signal Name
Pin1	Ground
PIN2	VBAT

Procedures of CMOS clear:

a) Turn off the system and unplug the power cord from the power outlet.

b) Remove the Lithium battery connection from BAT3 for 10 seconds, and then connect it.

c) Power on the system again.

d) When entering the POST screen, press the <ESC> or <DEL> key to enter CMOS Setup Utility to load optimal defaults.

e) After the above operations, save changes and exit BIOS Setup.

6. S_1 (PIN1):

(Switch), ATX Power and Auto Power on jumper setting**.**

S-1(Switch)	Mode
Pin1（Off）	ATX Power
Pin1（On）	**Auto Power on (Default)**

7. BAT2:

(2.0mm Pitch 1x10 Wafer Pin Header), smart battery Interface.

Pin#	Signal Name
Pin1	VCC_BAT1
Pin2	VCC_BAT1
Pin3	VCC_BAT1
Pin4	SMB_DAT_SW
Pin5	SMB_CLK_SW
Pin6	BAT1_TEMP
Pin7	Ground
Pin8	Ground
Pin9	Ground
Pin10	SET_BAT1_ON

Function	Specifications
Nominal voltage (3S1P)	11.1~12.6V
Charge voltage	12.6V
Charge current	0.5C

8. J_POE1:

(2.0mm Pitch 1x2 Wafer Pin Header),POE or DCIN input setting.

J_POE1 (Jumper)	DC_IN1	BAT2
Pin1-Pin2(open,**Default**)	●	-
Pin1-Pin2（Close）	-	●

9. BAT_LED1:

(2.0mm Pitch 1x4 Wafer Pin Header),The Charge status indicator for BAT2.

Pin1-Pin3: Charge LED status.

Pin2-Pin3: Discharge LED status.

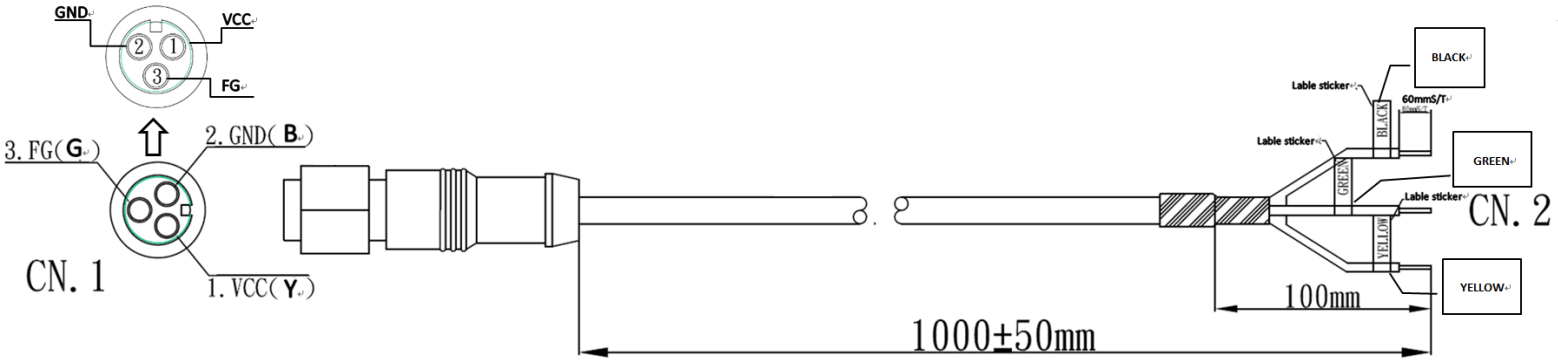
Pin4-Pin3: This is reserved for LVDS MCU IC reset.

Pin#	Signal Name
Pin1	BAT1_LED+
Pin2	BAT1_LED-
Pin3	Ground
Pin4	SBW_TDIO_RST (option)

10. DC_IN1:

(5.08mm Pitch 1x3 Pin Connector),DC 9V~36V System power input connector.

Pin#	Power Input
Pin1	DC_IN+ (DC+9V~36V)
Pin2	DC_IN- (Ground)
Pin3	FG



Model	DC_IN1
SBC-7114-I3-6100U	180°Connector
SBC-7114-I5-6300U	180°Connector
SBC-7114-I7-6600U	180°Connector
SBC-7114-I3-6100UP	45°Connector
SBC-7114-I5-6300UP	45°Connector
SBC-7114-I7-6600UP	45°Connector

Connector	Power input
DC_IN1 (Default)	DC_IN1
BAT2（option）	BAT2
DC_IN1 + BAT2（option）	DC_IN1

11. P_SW1/BT1, BT2：

Power on/off button (2.0mm Pitch 1x2 Wafer Pin Header)

They are used to connect power switch button. The two pins are disconnected under normal condition. You may short them temporarily to realize system startup & shutdown or awaken the system from sleep state. P_SW1 or BT1 need to be selected before manufacturing.

P_SW1 or BT1	Function
BT1(1x2Pin connect)	Default
P_SW1(Button)	Option
BT2	**Function**
BT2(1x2Pin connect)	Default

12. LED2/LED3/LED4/LED5/LED6/LED7/LED8:

LED2: LED STATUS. Green LED for 3P3V_ALLS_EC Power status.

LED3: LED STATUS. Green LED for 3P3V_S5 Power status.

LED4: LED STATUS. Green LED for Motherboard Standby Power Good status.

LED5: LED STATUS. Reserve.

LED6: LED STATUS. Green LED for charge status.

LED7: LED STATUS. Green LED for charge Complete status.

LED8: LED STATUS. Green LED for charge Power Good status.

13. S_1 (PIN3/PIN4/PIN6):

(Switch), LVDS jumper setting**.**

S-1(Switch)	Function (CN1)
Pin3（ON）	Single channel LVDS
Pin3（OFF）	**Dual channel LVDS (Default)**
Pin4（ON）	**8/24 bit (Default)**
Pin4（OFF）	6/18 bit
SEL-LCD-EDID （U17 or OPC-547 U2/U3）	
Pin6（**ON**）	Onboard EDID
Pin6（**OFF**）	Panel EDID

14. U17:

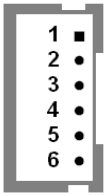
AT24C02-DIP8,The EEPROM IC（U17）is the set of LVDS resolution.

If you need other resolution settings, please upgrade U17 data.

Model	LVDS resolution
SBC-7114-I3-6100U SBC-7114-I5-6300U SBC-7114-I7-6600U	1280*1024 (Default)
	800*480（option）
	800*600（option）
	1024*768（option）
	1920*1080（option）
	……

15. INVT1:

(2.0mm Pitch 1x6 wafer Pin Header), Backlight control connector for LVDS.



Pin#	Signal Name
1	+DC12V_S0
2	+DC12V_S0
3	Ground
4	Ground
5	BKLT_EN_OUT
6	BKLT_CTRL

16. CN1:

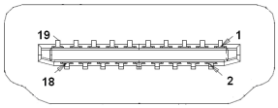
(1.25mm Pitch 2x20 Connector, DF13-40P),For 18⁄24-bit LVDS output connector, fully supported by Parad PS8625(DP to LVDS), the interface features dual channel 24-bit output. Low Voltage Differential Signaling, A high speed, low power data transmission standard used for display connections to LCD panels.

Function	Signal Name	Pin#		Signal Name	Function
LVDS	12V_S0	2	1	12V_S0	LVDS
	BKLT_EN_OUT	4	3	BKLT_CTRL	
	Ground	6	5	Ground	
	LVDS_VDD5	8	7	LVDS_VDD5	
	LVDS_VDD3	10	9	LVDS_VDD3	
	Ground	12	11	Ground	
	LA_D0_P	14	13	LA_D0_N	
	LA_D1_P	16	15	LA_D1_N	
	LA_D2_P	18	17	LA_D2_N	
	LA_D3_P	20	19	LA_D3_N	
	LA_CLKP	22	21	LA_CLKN	
	LB_D0_P	24	23	LB_D0_N	
	LB_D1_P	26	25	LB_D1_N	
	LB_D2_P	28	27	LB_D2_N	
	LB_D3_P	30	29	LB_D3_N	

	LB_CLKP	32	31	LB_CLKN	
USB7 (option)	Ground	34	33	LCD_EDID_SEN	
	USB7_P	36	35	USB7_N	
	5V_S5_USB	38	37	LVDS1_DDC_DATA	
Power LED	PWR_LED+	40	39	LVDS1_DDC_CLK	Power LED

17. HDMI1:

(HDMI 19P Connector), HDMI 1.4 Port, High Definition Multimedia Interface connector.



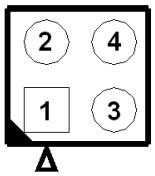
18. DP1 (option**):**

(1.25mm Pitch 2x20 Connector, DF13-40P), For DP Signal output connector. It can connect to TB-540A, a DP to VGA board.

Function	Signal Name	Pin#		Signal Name	Function
DP	12V_S0_EDP	2	1	12V_S0_EDP	DP
	12V_S0_EDP	4	3	12V_S0_EDP	
	Ground	6	5	Ground	
	5V_S0	8	7	5V_S0	
	3P3V_S0	10	9	3P3V_S0	
	CPU_CFG4	12	11	Ground	
	NC	14	13	DDI1_TX1_N	
	NC	16	15	DDI1_TX1_P	
	NC	18	17	Ground	
	DDI1_TX2_N	20	19	DDI1_TX0_N	
	DDI1_TX2_P	22	21	DDI1_TX0_P	
	Ground	24	23	Ground	
	DDI1_TX3_N	26	25	DDI1_AUX_N	
	DDI1_TX3_P	28	27	DDI1_AUX_P	
	NC	30	29	I2C1_SCL	I2C
	EDP_HP_CN	32	31	I2C1_SDA	
	Ground	34	33	Ground	USB7 (option)
USB7 (option)	USB7_P	36	35	USB7_N	
	5V_S5_USB	38	37	5V_S5_USB	
Power LED	PWR_LED+	40	39	Ground	Power LED

19. JP3/S_1(PIN5):

(2.0mm Pitch 2x2 wafer Pin Header), touch jumper setting**.**



JP3	Touch(TCH1)
Open 3-4**(default)**	Enable
Close 3-4(option)	Disable
Open 1-2**(default)**	-

Priority Order：			
Touch Function	JP3(3-4)	S_1(Pin5)	EC_GPIO
TCH1(Enable)	Short	-	-
TCH1(Disable)	Open	ON	-
TCH1(Enable)	Open	OFF	1（Default）
TCH1(Disable)	Open	OFF	0

20. TCH1:

(2.0mm Pitch 1x6 wafer Pin Header), internal touch controller connector.

Pin#	Signal Name
1	SENSE
2	X+
3	X-
4	Y+
5	Y-
6	GND_EARCH

21. LED1:

LED1: LED STATUS. Green LED for touch power status.

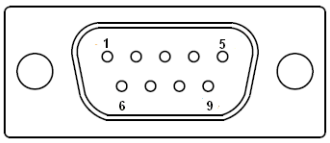
22. JP1:

(2.0mm Pitch 2x3 Pin Header), COM1 jumper setting, pin 1~6 are used to select signal out of pin 9 of COM1 port.

JP1 Pin#	Function
Close 1-2	**COM1 RI (Ring Indicator) (default)**
Close 3-4	COM1 Pin9:DC+5V (option)
Close 5-6	COM1 Pin9:DC+12V (option)

23. COM1:

(Type DB9M),Rear serial port, standard DB9 Male serial port is provided to make a direct connection to serial devices. COM1 port is controlled by pins No.1~6 of JP1, select output Signal RI or 5V or 12V, for details, please refer to description of JP1 and S_232 and S_422 setting.



RS232 (Default):	
Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	**JP1 select Setting (RI/5V/12V)**
BIOS Setup： Advanced/NCT6106D Super IO Configuration/F75111 COM1 Configuration【RS-232】	

RS422 (option):	
Pin#	Signal Name
1	422_TX-
2	422_TX+
3	422_RX+

4	422_RX-
5	Ground
6	NC
7	NC
8	NC
9	NC
BIOS Setup： Advanced/NCT6106D Super IO Configuration/F75111 COM1 Configuration【RS-422】	

RS485 (option):	
Pin#	Signal Name
1	485-
2	485+
3	NC
4	NC
5	Ground
6	NC
7	NC
8	NC
9	NC
BIOS Setup： Advanced/NCT6106D Super IO Configuration/F75111 COM1 Configuration【RS-485】	

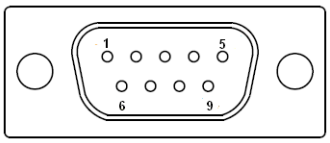
24. JP2:

(2.0mm Pitch 2x3 Pin Header),COM2 jumper setting, pin 1~6 are used to select signal out of pin 9 of COM2 port.

JP2 Pin#	Function
Close 1-2	**COM2 RI (Ring Indicator) (default)**
Close 3-4	COM2 Pin9：DC+5V (option)
Close 5-6	COM2 Pin9：DC+12V (option)

25. COM2:

(Type DB9M),Rear serial port, standard DB9 Male serial port is provided to make a direct connection to serial devices.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	**JP2 select Setting (RI/5V/12V)**

26. SATA_P1:

(2.5mm Pitch 1x2 box Pin Header), One onboard 5V output connector are reserved to provide power for SATA devices.

Pin#	Signal Name
1	5V_S0(+DC5V output)
2	Ground

Note:

Output current of the connector must not be above 1A.

27. SATA2:

(SATA 7Pin), SATA Connectors, one SATA connector are provided; with transfer speed up to 6.0Gb/s.

28. SATA1:

(SATA 7Pin+15Pin), SATA Connectors, one SATA connector are provided; with transfer speed up to 6.0Gb/s.

29. S_1 (PIN2):

(Switch), MSATA Signal and PCIE Signal jumper setting for MPCIE1.

S-1 (Switch)	MPCIE1
Pin2 (Off)	MSATA Signal (Default)
Pin2 (On)	PCIE Signal (option)

30. MPCIE1:

(50.95mmx30mm Socket 52Pin), mSATA socket, it is located at the top, it supports mini PCIe devices with LPCbus and SMbus and mSATA signal.**B2 mSATA bus** for flash disk signal.

Function	Support
Mini SATA	●(Default, S_1 setting)
Mini PCie	○ (option, S_1 setting)
LPC bus	●
SMbus	●
USB2.0（USB6）	●

31. H5/H6:

MPCIE1 SCREW HOLES, H5 and H6 for mini PCIE card (30mmx50.95mm) assemble.

32. AUDIO2:

(2.0mm Pitch 2X6 Pin Header), Front Audio, An onboard Realtek ALC269Q codec is used to provide high-quality audio I/O ports. Line Out can be connected to a headphone or amplifier. Line In is used for the connection of external audio source via a Line in cable. MIC is the port for microphone input audio.

Signal Name	Pin#	Pin#	Signal Name
+5V_F_AUDIO	1	2	GND_AUD
LINE-OUT-L	3	4	LINE-OUT-R
FRONT_JD	5	6	LINE_IN_JD
LINE-IN-L	7	8	LINE-IN-R
MIC-IN-L	9	10	MIC-IN-R
GND_AUD	11	12	MIC1_JD

33. LINE_OUT:

(Diameter 3.5mm Jack), HD Audio port, An onboard Realtek ALC269-VB codec is used to provide high quality audio I/O ports. Line Out can be connected to a headphone or amplifier.

Line out

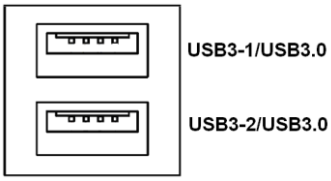
34. SPK1:

(2.0mm Pitch 1x4 Wafer Pin Header), support a stereo Class-D Speaker Amplifier with 2 watt per channel output power

Pin#	Signal Name
1	SPK_OUTL_P
2	SPK_OUTL_N
3	SPK_OUTR_N
4	SPK_OUTR_P

35. USB1:

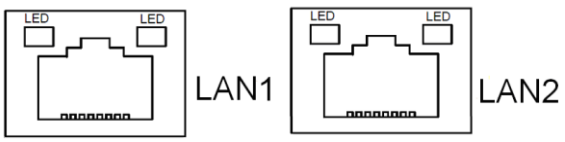
USB3-1/USB3-2：(Double stack USB type A), Rear USB connector, it provides up to two USB3.0 ports, High-speed USB 2.0 allows data transfers up to 480 Mb/s, USB 3.0 allows data transfers up to 5.0Gb/s ,support USB full-speed and low-speed signaling.



Each USB Type A Receptacle (2 Ports) Current limited value is 2.0A.
If the external USB device current exceeds 1.5A, please separate connectors into different Receptacle.

36. LAN1/LAN2:

LAN1/LAN2: (RJ45 Connector), Rear LAN port, Two standard 10/100/1000M RJ-45 Ethernet ports are provided. Use Intel 82574L chipset, LINK LED (green) and ACTIVE LED (green) respectively located at the left-hand and right-hand side of the Ethernet port indicate the activity and transmission state of LAN.



37. BUZ1:

Onboard buzzer.

38. CN2:

(DF13-30P Connector), For expand output connector, It provides eight GPIOs, two RS422 or RS485, one USB2.0, one Power on/off, one Reset.

Function	Signal Name	Pin#		Signal Name	Function
5V	5V_S5	2	1	5V_S5	5V
6106_GPIO41	GPIO_IN2	4	3	GPIO_IN1	6106_GPIO40
6106_GPIO43	GPIO_IN4	6	5	GPIO_IN3	6106_GPIO42
6106_GPIO45	GPIO_OUT2	8	7	GPIO_OUT1	6106_GPIO44
6106_GPIO47	GPIO_OUT4	10	9	GPIO_OUT3	6106_GPIO46
	Ground	12	11	Ground	
485 or 422 (COM5)	485+_422TX5+	14	13	485-_422TX5-	485 or 422 (COM5)
	422_RX5+	16	15	422_RX5-	
485 or 422 (COM6)	485+_422TX6+	18	17	485-_422TX6-	485 or 422 (COM6)
	422_RX6+	20	19	422_RX6-	
5V	5V_S0	22	21	HDD_LED+	HDD LED
USB2.0	5V_USB5	24	23	5V_USB5	USB2.0
	USB5_P	26	25	USB5_N	
	Ground	28	27	FP_RST-	RESET
Power auto on	PWRBTN_ON	30	29	Ground	
COM5 BIOS Setup： Advanced/NCT6106D Super IO Configuration/ COM5 Configuration【RS-422】 Advanced/NCT6106D Super IO Configuration/ COM5 Configuration【RS-485】 COM6 BIOS Setup： Advanced/NCT6106D Super IO Configuration/ COM5 Configuration【RS-422】 Advanced/NCT6106D Super IO Configuration/ COM5 Configuration【RS-485】					

39. EC_GPIO1：

(2.0mm Pitch 1X10 Pin Header),For expand connector ,It provides eight GPIO.

Pin#	Signal Name	GPIO Name
1	Ground	Ground
2	GPA0_ONOFF	EC_GPA0
3	GPA1_SPK	EC_GPA1
4	GPE6_BKLT	EC_GPE6
5	GPE0_BKLT+	EC_GPE0

6	GPH3_SPK+	EC_GPH3
7	BKLT_CTRL_PWR	BKLT_CTRL_PWR
8	ADC6_BKLT_CTRL	EC_ADC6
9	ADC7_RSV	EC_ADC7
10	3.3V_ALLS_EC	3.3V_ALLS_EC

40. CN3:

(1.27mm Pitch 2X50 Female Header),For expand output connector, it provides four GPIO, two USB 2.0, two PS/2 for keyboard and mouse (no support currently), two uart, one PCIex1, one SMbus, two PCIex1 or USB3.0, two USB 2.0, connects to the TB-528 riser Card.

Function	Signal Name	Pin#		Signal Name	Function
	5V_S5_USB	2	1	5V_S5_USB	
	5V_S5_USB	4	3	5V_S5_USB	
	USB3489_OC	6	5	PS_ON_ALL-	
USB4	USB4_N	8	7	USB4_P	USB4
USB3	USB3_N	10	9	USB3_P	USB3
	Ground	12	11	Ground	
Not support	PS2_MSCLK	14	13	PS2_MSDATA	Not Support
	PS2_KBCLK	16	15	PS2_KBDATA	
COM4 (UART)	COM4_RI	18	17	COM4_DCD-	COM4 (UART)
	COM4_TXD	20	19	COM4_RXD	
	COM4_DTR	22	21	COM4_RTS-	
	COM4_DSR	24	23	COM4_CTS-	
	Ground	26	25	Ground	
COM3 (UART)	COM3_RI	28	27	COM3_DCD-	COM3 (UART)
	COM3_TXD	30	29	COM3_RXD	
	COM3_DTR	32	31	COM3_RTS-	
	COM3_DSR	34	33	COM3_CTS-	
GPPC20	PCH_GPPC20	36	35	PCH_GPPC22	GPPC22
GPPC21	PCH_GPPC21	38	37	PCH_GPPC23	GPPC23
	Ground	40	39	Ground	
PCIE4	PCIE4_TX_N0	42	41	PE4_TX_P0	PCIE4
	PCIE4_RX_N0	44	43	PE4_RX_P0	
	Ground	46	45	Ground	
	CLK_100M_PE4_N	48	47	CLK_100M_PE4_P	

	PCIE4_WAKE_N	50	49	PLT_RST_BUF2-	
SMBUS	SMB_CLK_S5	52	51	SMB_DATA_S5	SMBUS
PCIE	CLKREQ_PE1-	54	53	Ground	
	3P3V_S5	56	55	PWRBTN_ON-	Power Auto on
	3P3V_S5	58	57	3P3V_S5	
12V	12V_S0	60	59	12V_S0	12V
12V	12V_S0	62	61	12V_S0	12V
PCIE3	Ground	64	63	Ground	PCIE3
	PE3_TX_N0	66	65	PE3_TX_P0	
	PE3_RX_N0	68	67	PE3_RX_P0	
	Ground	70	69	Ground	
	CLK_100M_PE0_N	72	71	CLK_100M_PE0_P	
	CLKREQ_PE0-	74	73	CLKREQ_PE5-	PCIE5 or USB3.0
PCIE5 or USB3.0	Ground	76	75	Ground	
	CLK_100M_PE5_N	78	77	CLK_100M_PE5_P	
	USB5PE1_TX_N	80	79	USB5PE1_TX_P	
	USB5PE1_RX_N	82	81	USB5PE1_RX_P	
PCIE6 or USB3.0	Ground	84	83	Ground	PCIE6 or USB3.0
	USB6PE2_TX_N	86	85	USB6PE2_TX_P	
	USB6PE2_RX_N	88	87	USB6PE2_RX_P	
	CLK_100M_XDP_N	80	89	CLK_100M_XDP_P	
USB2.0	Ground	92	91	Ground	USB2.0
	USB8_N	94	93	USB8_P	
	USB9_N	96	95	USB9_P	
	5V_S5	98	97	5V_S5	
	3P3V_S5	100	99	3P3V_S5	

41. TPM-U1（option）：

Infineon's Trusted Platform Module (TPM2.0) SLB 9665 is a fully standard compliant TPM based on the latest Trusted Computing Group (TCG) specification 2.0.

Note: Only supports WINDOWS 10 IoT

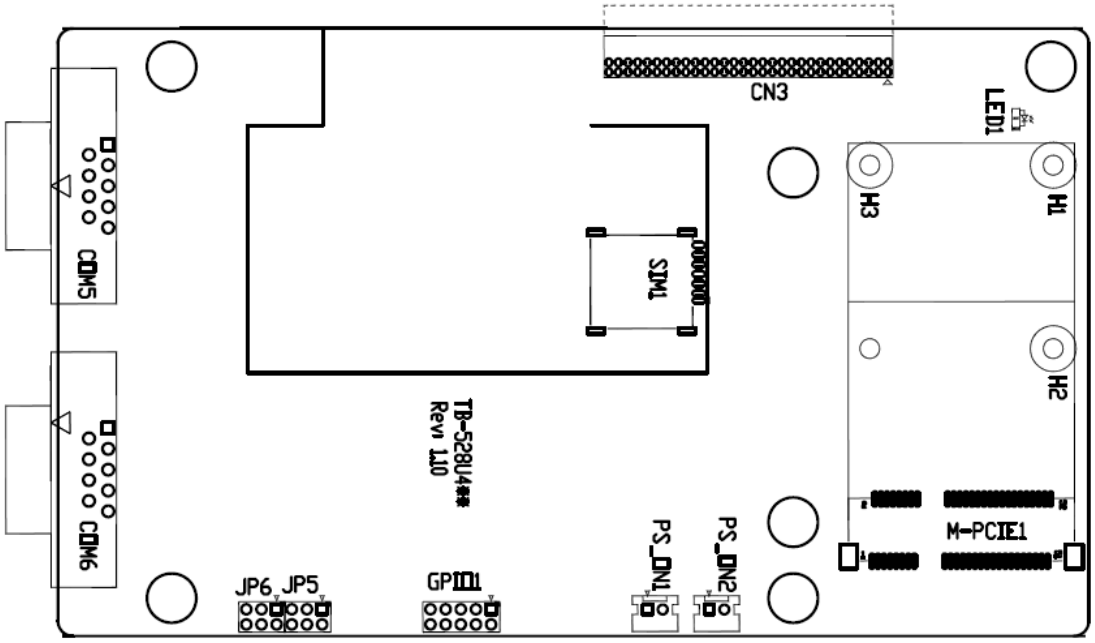
TPM_U1	SLB 9665 TT2.0
MODEL	TPM Function
SBC-7114-XXX R2.30	●

SBC-7114-XXX R2.20	X
SBC-7114-XXX R1XX	X

42. TB-528C2ME1（option）：

SBC-7114 Riser Card, TB-528C2ME1 CN3 connect to SBC-7114 CN3 pin Header.

TB-528C2ME1 Top：



CN3：

(1.27mm Pitch 2X30 Pin Header),connect to SBC-7114 CN3 pin Header.

M-PCIE1：

(Socket 52Pin), mini PCIe socket, it is located at the top, it supports mini PCIe devices with **USB2.0(USB3)**, Smbus, SIM and PCIe signal. MPCIe card size is 30x30mm or 30x50.95mm.

Signal Name	Function support
PCIe 1X	Yes
USB2.0 (USB2)	Yes
SMBus	Yes
SIM	Yes

H1/H2:

MPCIE1 SCREW HOLES, H2 for mini PCIE card (30mmx30mm) assemble. H1 for mini PCIE card (30mmx50.95mm) assemble.

LED1：

Mini PCIe devices' LED Status.

SIM1：

(SIM Socket 6 Pin), Support SIM Card devices.

GPIO1：

(2.0mm Pitch 2x5 Pin Header),General-purpose input/output port, it provides a group of self-programming interfaces to customers for flexible use.

Signal Name	Pin#	Pin#	Signal Name
Ground	1	2	NC
NC	3	4	SMB_DATA_R
SMB_CLK_R	5	6	PCH-GPIO56
PCH -GPIO57	7	8	PCH -GPIO59
PCH -GPIO58	9	10	+5V

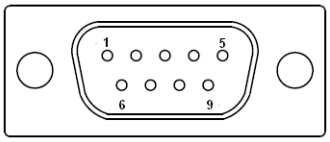
JP5：

(2.0mm Pitch 2x3 Pin Header),COM5 setting jumper, pin 1~6 are used to select signal out of pin 9 of COM5 port.

JP5 Pin#	Function
Close 1-2	**RI (Ring Indicator) (default)**
Close 3-4	COM5 Pin9=+5V (option)
Close 5-6	COM5 Pin9=+12V (option)

COM5(SBC-7114/COM3)：

(Type DB9), serial port, standard DB9 serial port is provided to make a direct connection to serial devices. COM5 port is controlled by pins No.1~6 of **JP5**, select output Signal RI or 5V or 12v. For details, please refer to description of JP3.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground

6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	JP5 Setting: **Pin1-2 : RI (**Ring Indicator**)** **(default)** Pin3-4 : 5V Standby power **(**option**)** Pin5-6:12V Standby power (option)

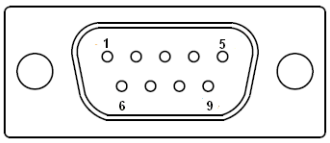
JP6：

(2.0mm Pitch 2x3 Pin Header),COM6 setting jumper, pin 1~6 are used to select signal out of pin 9 of COM6 port.

JP6 Pin#	Function
Close 1-2	**RI (Ring Indicator) (default)**
Close 3-4	COM6 Pin9=+5V (option)
Close 5-6	COM6 Pin9=+12V (option)

COM6(SBC-7114/COM4)：

(Type DB9), serial port, standard DB9 serial port is provided to make a direct connection to serial devices. COM6 port is controlled by pins No.1~6 of **JP6**, select output Signal RI or 5V or 12v. For details, please refer to description of JP6.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	JP6 Setting: **Pin1-2 : RI (**Ring Indicator**)** **(default)**

	Pin3-4 : 5V Standby power **(**option**)** Pin5-6:12V Standby power (option)

PS_ON1:

(2.0mm Pitch 1x2 Pin Wafer), ATX Power and Auto Power on jumper setting.

PS_ON	Mode
Close 1-2	**Auto Power on (Default)**
Open 1-2	ATX Power

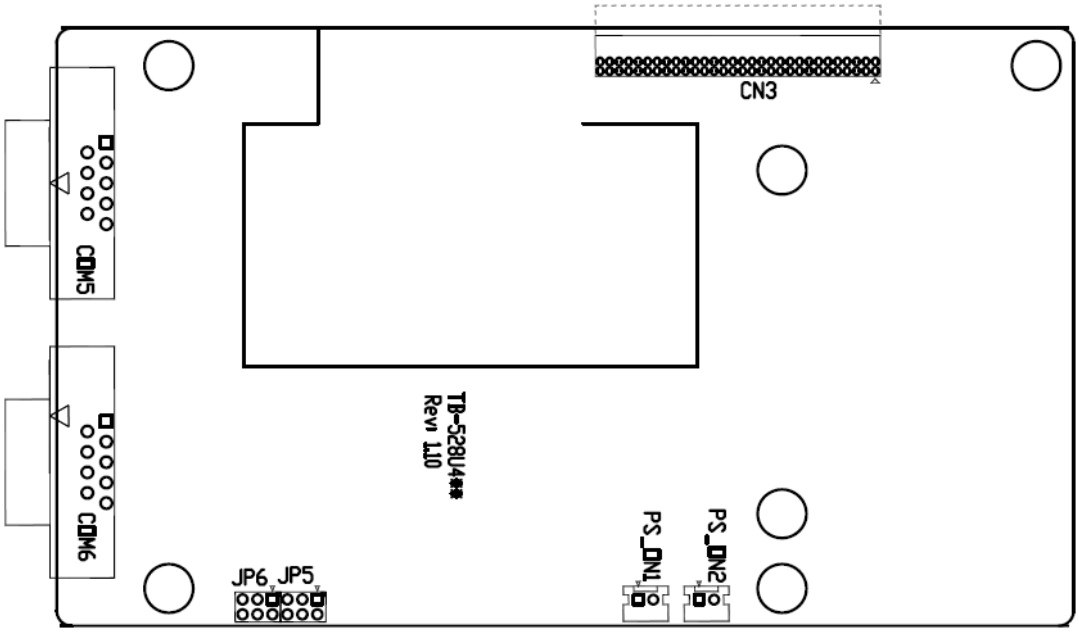
PS_ON2 (option):

(2.0mm Pitch 1x2 Pin Wafer).

43. TB-528C2 R1.10（option）:

SBC-7114 Riser Card,TB-528C2 CN3 connect to SBC-7114 CN3 pin Header.

TB-528C2 Top：



CN3：

(1.27mm Pitch 2X30 Pin Header),connect to SBC-7114 CN3 pin Header.

JP5：

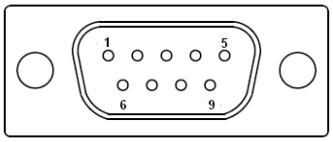
(2.0mm Pitch 2x3 Pin Header),COM5 setting jumper, pin 1~6 are used to select signal out of pin 9 of COM5 port.

JP5 Pin#	Function

Close 1-2	RI (Ring Indicator) (default)
Close 3-4	COM5 Pin9：+5V (option)
Close 5-6	COM5 Pin9：+12V (option)

COM5(SBC-7114/COM3)：

(Type DB9),serial port, standard DB9 serial port is provided to make a direct connection to serial devices. COM5 port is controlled by pins No.1~6 of **JP5**, select output Signal RI or 5V or 12v. For details, please refer to description of JP3.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	JP5 Setting: **Pin1-2 : RI (**Ring Indicator**) (default)** Pin3-4 : 5V Standby power **(**option**)** Pin5-6:12V Standby power (option)

JP6：

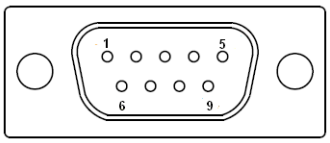
(2.0mm Pitch 2x3 Pin Header), COM6 setting jumper, pin 1~6 are used to select signal out of pin 9 of COM6 port.

JP6 Pin#	Function
Close 1-2	**RI (Ring Indicator) (default)**
Close 3-4	COM6 Pin9：+5V (option)
Close 5-6	COM6 Pin9：+12V (option)

COM6(SBC-7114/COM4)：

(Type DB9), serial port, standard DB9 serial port is provided to make a direct connection to serial devices. COM6 port is controlled by pins No.1~6 of **JP6**,

select output Signal RI or 5V or 12v. For details, please refer to description of JP6.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	JP6 Setting: **Pin1-2 : RI (**Ring Indicator**)** **(default)** Pin3-4 : 5V Standby power **(**option**)** Pin5-6:12V Standby power (option)

PS_ON1:

(2.0mm Pitch 1x2 Pin Wafer), ATX Power and Auto Power on jumper setting.

PS_ON	Mode
Close 1-2	**Auto Power on (Default)**
Open 1-2	ATX Power

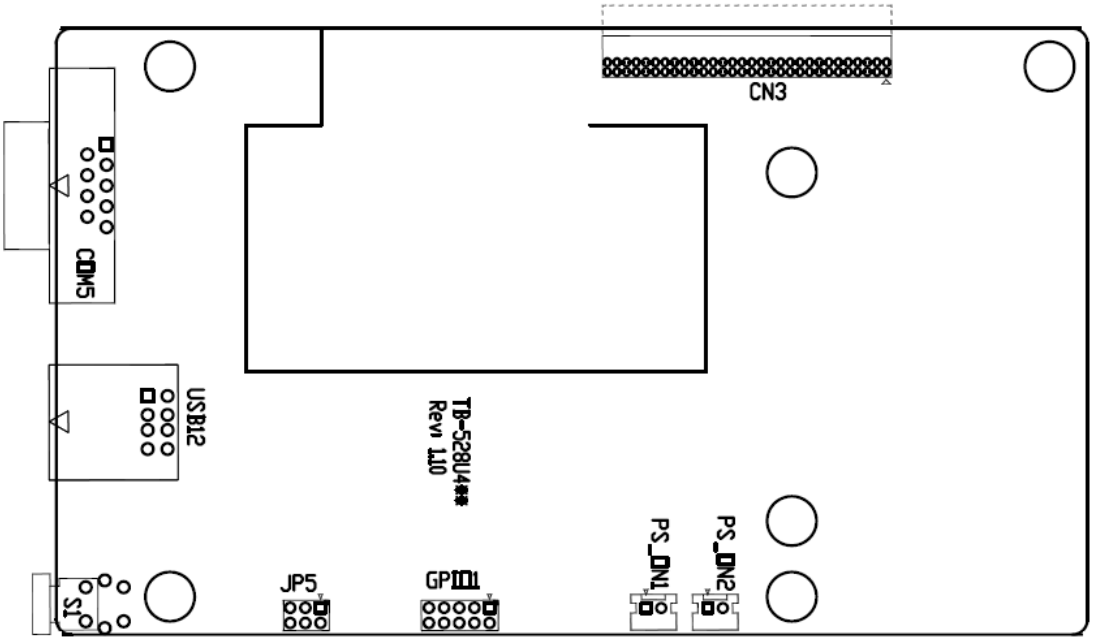
PS_ON2 (option):

(2.0mm Pitch 1x2 Pin Wafer).

44. TB-528C1U2P1/TB-528C1U2 R1.10（option）:

SBC-7114 Riser Card, TB-528C1U2P1 CN3 connects to SBC-7114 CN3 pin Header.

TB-528C1U2P1 Top：



CN3：

(1.27mm Pitch 2X30 Pin Header),connect to SBC-7114 CN3 pin Header.

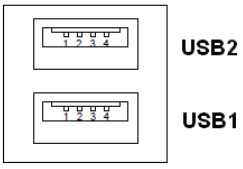
GPIO1：

(2.0mm Pitch 2x5 Pin Header), General-purpose input/output port, it provides a group of self-programming interfaces to customers for flexible use.

Signal Name	Pin#	Pin#	Signal Name
Ground	1	2	GPIO_OUT1
GPIO_OUT2	3	4	SMB_DATA_R
SMB_CLK_R	5	6	GPIO_IN1
GPIO_IN2	7	8	GPIO_IN3
GPIO_IN4	9	10	+5V

USB12 (USB-HUB):

(Double stack USB type A), Rear USB connector, it provides up to 2 USB 2.0 ports, speed up to 480Mb/s.



Note:

Before connection, make sure that pinout of the USB cable is in accordance with that of the said tables. Any inconformity may cause system down and even hardware damages.

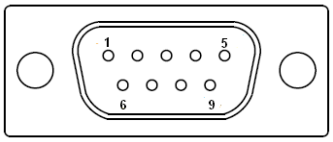
JP5：

(2.0mm Pitch 2x3 Pin Header), COM5 setting jumper, pin 1~6 are used to select signal out of pin 9 of COM5 port.

JP5 Pin#	Function
Close 1-2	**RI (Ring Indicator) (default)**
Close 3-4	COM5 Pin9：+5V (option)
Close 5-6	COM5 Pin9：+12V (option)

COM5(SBC-7114/COM3)：

(Type DB9), serial port, standard DB9 serial port is provided to make a direct connection to serial devices. COM5 port is controlled by pins No.1~6 of **JP5**, select output Signal RI or 5V or 12v. For details, please refer to description of JP3.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	JP5 Setting: **Pin1-2 : RI (**Ring Indicator**) (default)** Pin3-4 : 5V Standby power **(**option**)** Pin5-6:12V Standby power (option)

PS_ON1：

(2.0mm Pitch 1X2 Pin Wafer), ATX Power and Auto Power on jumper setting**.**

PS_ON	Mode
Close 1-2	**Auto Power on (Default)**
Open 1-2	ATX Power

PS_ON2（option）：

(2.0mm Pitch 1X2 Pin Wafer).

S1：

PWR BT: POWER on/off Button, They are used to connect power switch button. The two pins are disconnected under normal condition. You may short them temporarily to realize system startup & shutdown or awaken the system from sleep state.

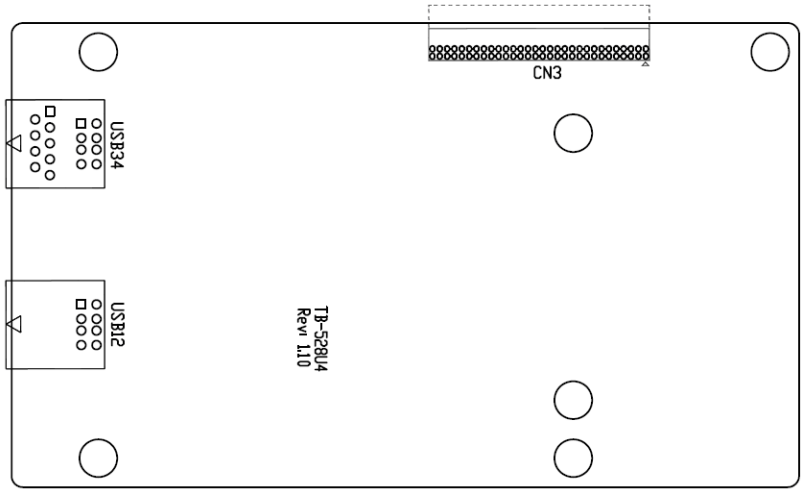
PWR LED: POWER LED status.

S1	Model
Yes	TB-528C1U2P1
No	TB-528C1U2

45. TB-528U4 R1.10（option）：

SBC-7114 Riser Card, TB-528U4 CN3 connects to SBC-7114 CN3 pin Header.

TB-528U4 Top：

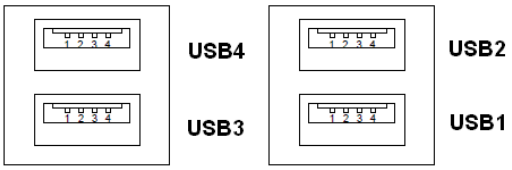


CN3：

(1.27mm Pitch 2X30 Pin Header),connect to SBC-7114 CN3 pin Header.

USB12/USB34 (USB-HUB)：

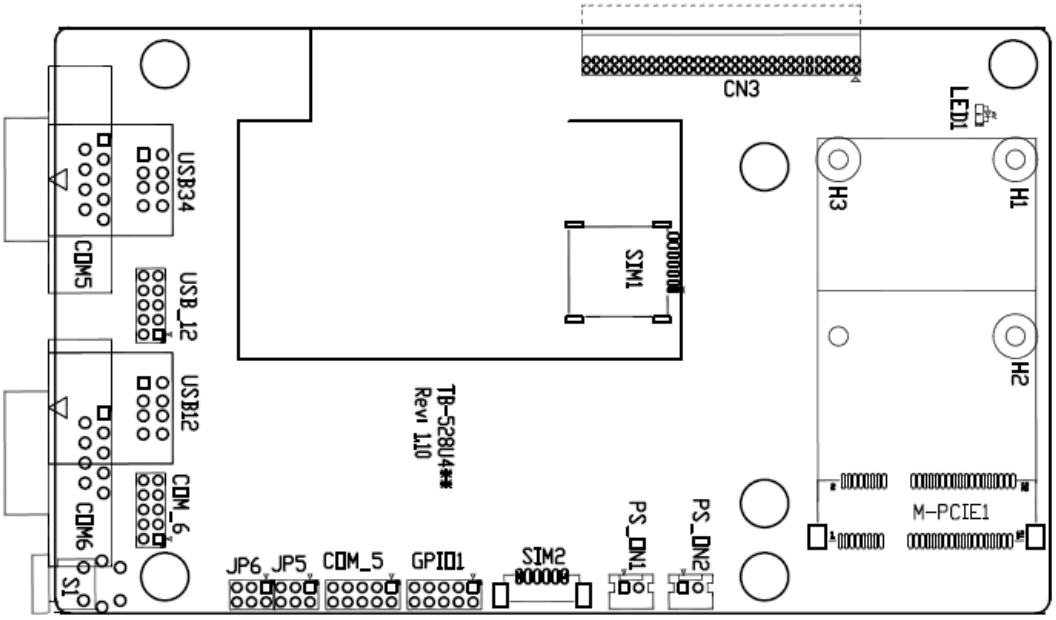
(Double stack USB type A), Rear USB connector, it provides up to 4 USB 2.0 ports, speed up to 480Mb/s.



46. TB-528U4C2ME1P1（option）：

SBC-7114 Riser Card, TB-528U4C2ME1P1 CN3 connects to SBC-7114 CN3 pin Header.

TB-528U4C2ME1P1 Top：



CN3：

(1.27mm Pitch 2X30 Pin Header),connect to SBC-7114 CN3 pin Header.

M-PCIE1：

(Socket 52Pin), mini PCIe socket, it is located at the top, it supports mini PCIe devices with USB2.0 (USB3), SMbus, SIM and PCIe signal. MPCIe card size is 30x30mm or 30x50.95mm.

Signal Name	Function support
PCIe 1x	●
USB2.0 (USB2)	●
SMbus	●
SIM	●

H1/H2：

MPCIE1 SCREW HOLES, H2 for mini PCIE card (30x30mm) assemble. H1 for mini PCIE card (30x50.95mm) assemble.

LED1：

Mini PCIe devices LED status.

SIM1:

(Nano SIM Socket 6 Pin), Support SIM Card devices.

SIM2 (option):

(1.25mm Pitch 1x6 Pin Wafer), Support SIM Card devices.

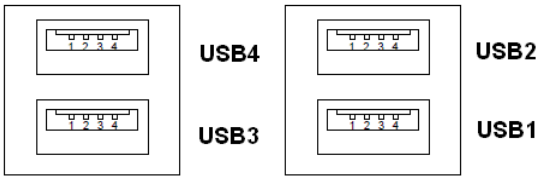
GPIO1:

(2.0mm Pitch 2x5 Pin Header), General-purpose input/output port, it provides a group of self-programming interfaces to customers for flexible use.

Signal Name	Pin#	Pin#	Signal Name
Ground	1	2	GPIO_OUT1
GPIO_OUT2	3	4	SMB_DATA_R
SMB_CLK_R	5	6	GPIO_IN1
GPIO_IN2	7	8	GPIO_IN3
GPIO_IN4	9	10	+5V

USB12/USB34 (USB-HUB):

(Double stack USB type A), Rear USB connector, it provides up to 4 USB 2.0 ports, speed up to 480Mb/s.



USB_12 (option):

(2.0mm Pitch 2x5 Pin Header), Front USB connector, it provides two USB port via a dedicated USB cable, speed up to 480Mb/s.

Signal Name	Pin#	Pin#	Signal Name
5V_USB12	1	2	5V_USB12

E_USB1_N	3	4	E_USB2_N
E_USB1_P	5	6	E_USB2_P
Ground	7	8	Ground
NC	9	10	Ground

Note:

Before connection, make sure that pin out of the USB cable is in accordance with that of the said tables. Any inconformity may cause system down and even hardware damages.

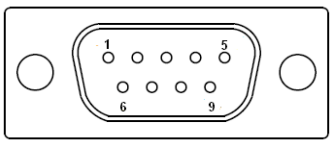
JP5:

(2.0mm Pitch 2x3 Pin Header), COM5 setting jumper, pin 1~6 are used to select signal out of pin9 of COM5 port.

JP5 Pin#	Function
Close 1-2	**RI (Ring Indicator) (default)**
Close 3-4	COM5 Pin9=+5V (option)
Close 5-6	COM5 Pin9=+12V (option)

COM5 (SBC-7114/COM3, option):

(Type DB9), serial port, standard DB9 serial port is provided to make a direct connection to serial devices. COM5 port is controlled by pins No.1~6 of **JP5**, select output Signal RI or 5V or 12v. For details, please refer to description of JP3.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	JP5 Setting: **Pin1-2 : RI (**Ring Indicator**) (default)**

	Pin3-4 : 5V Standby power **(**option**)** Pin5-6:12V Standby power (option)

COM5 (SBC-7114/COM3):

(2.0mm Pitch 2x5 Pin Header), COM5 port, up to one standard RS232 port is provided. They can be used directly via COM cable connection.

Signal Name	Pin#	Pin#	Signal Name
DCD	1	2	RXD
TXD	3	4	DTR
Ground	5	6	DSR
RTS	7	8	CTS
JP6 Setting: RI/5V/12V	9	10	NC

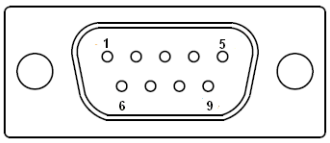
JP6：

(2.0mm Pitch 2x3 Pin Header), COM6 setting jumper, pin 1~6 are used to select signal out of pin 9 of COM6 port.

JP6 Pin#	Function
Close 1-2	**RI (Ring Indicator) (default)**
Close 3-4	COM6 Pin9：+5V (option)
Close 5-6	COM6 Pin9：+12V (option)

COM6(SBC-7114/COM4)：

(Type DB9), serial port, standard DB9 serial port is provided to make a direct connection to serial devices. COM6 port is controlled by pins No.1~6 of **JP6**, select output Signal RI or 5V or 12v. For details, please refer to description of JP6.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)

5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	JP6 Setting: **Pin1-2 : RI (**Ring Indicator**)** **(default)** Pin3-4 : 5V Standby power **(**option**)** Pin5-6:12V Standby power (option)

COM6 (SBC-7114/COM4):

(2.0mm Pitch 2x5 Pin Header), COM6 port, up to one standard RS232 port is provided. They can be used directly via COM cable connection.

Signal Name	Pin#	Pin#	Signal Name
DCD	1	2	RXD
TXD	3	4	DTR
Ground	5	6	DSR
RTS	7	8	CTS
JP6 Setting: RI/5V/12V	9	10	NC

PS_ON1：

(2.0mm Pitch 1X2 Pin Wafer), ATX Power and Auto Power on jumper setting**.**

PS_ON	Mode
Close 1-2	**Auto Power on (Default)**
Open 1-2	ATX Power

PS_ON2（option）：

(2.0mm Pitch 1X2 Pin Wafer).

S1：

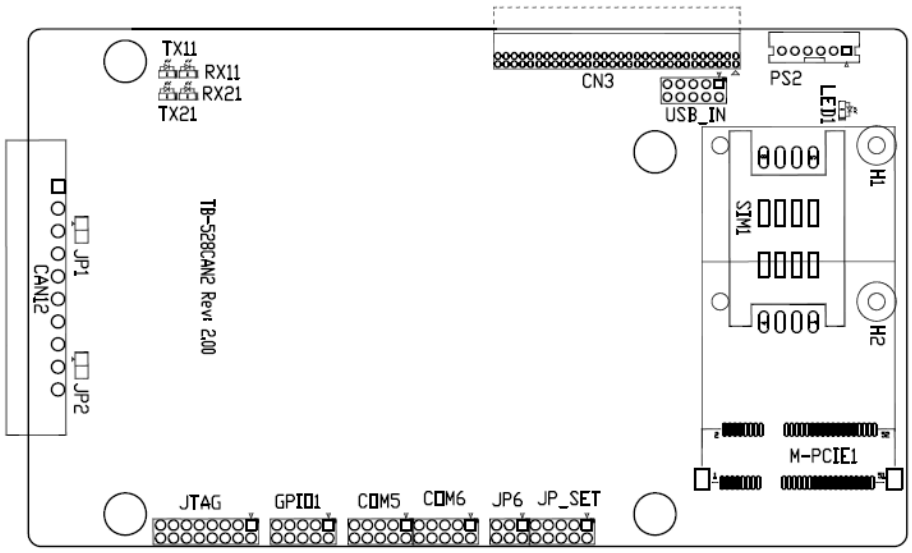
PWR BT: POWER on/off Button, They are used to connect power switch button. The two pins are disconnected under normal condition. You may short them temporarily to realize system startup & shutdown or awaken the system from sleep state.

PWR LED: POWER LED status.

47. TB-528CAN2 R2.00（option）：

SBC-7114 Riser Card, TB-528CAN2 CN3 connects to SBC-7114 CN3 pin Header. It provides two CAN-bus interface.

TB-528CAN2 Top：



CN3：

(1.27mm Pitch 2X30 Pin Header),connect to SBC-7114 CN3 pin Header.

M-PCIE1：

(Socket 52Pin), mini PCIe socket, it is located at the top, it supports mini PCIe devices with SMbus, USB 2.0, SIM and PCIe signal. MPCIe card size is 30x30mm or 30x50.95mm.

Signal Name	Function Support
PCIe 1x	Yes
USB 2.0 (USB2)	Yes
SMbus	Yes
SIM	Yes

H1/H2 :

MPCIE1 SCREW HOLES, H2 for mini PCIE card (30x30mm) assemble. H1 for mini PCIE card (30x50.95mm) assemble.

LED1 :

Mini PCIe devices LED status.

SIM1 (option) :

(SIM Socket 6Pin), support SIM Card devices.

PS2 :

(2.0mm Pitch 1x6 Pin Wafer), PS/2 keyboard and mouse port, the port can be connected to PS/2 keyboard or mouse via a dedicated cable for direct use.

Pin#	Signal Name
1	KBDATA
2	MSDATA
3	Ground
4	+5V
5	KBCLK
6	MSCLK

USB_IN (option) :

(2.0mm Pitch 2x5 Pin Header), front USB connector, it provides two USB port via a dedicated USB cable, speed up to 480Mb/s.

Signal Name	Pin#	Pin#	Signal Name
5V_USB34	1	2	5V_USB34
NC (USB4_N)	3	4	NC (USB3_N)
NC (USB4_P)	5	6	NC (USB3_P)
Ground	7	8	Ground
NC	9	10	Ground

 Note :

Before connection, make sure that pin out of the USB cable is in accordance with that of the said tables. Any inconformity may cause system down and even hardware damages.

JP_SET (option):

(2.0mm Pitch 2x5 Pin Header).

Signal Name	Pin#	Pin#	Signal Name
3P3V_S5_USB	1	2	3P3V_S5
3P3V_S5_USB	3	4	3P3V_S5
3P3V_S5_USB	5	6	3P3V_S5
PSON_ATX	7	8	Ground
PSON_ATX	9	10	Ground

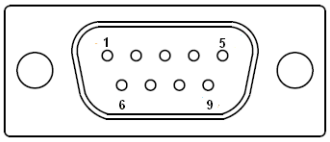
JP6：

(2.0mm Pitch 2x3 Pin Header), COM6 setting jumper, pin 1~6 are used to select signal out of pin 9 of COM6 port.

JP6 Pin#	Function
Close 1-2	**RI (Ring Indicator) (default)**
Close 3-4	COM6 Pin9：+5V (option)
Close 5-6	COM6 Pin9：+12V (option)

COM6(SBC-7114/COM4)：

(Type DB9), serial port, standard DB9 serial port is provided to make a direct connection to serial devices. COM6 port is controlled by pins No.1~6 of **JP6**, select output Signal RI or 5V or 12v. For details, please refer to description of JP6.



Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	JP6 Setting: **Pin1-2 : RI (**Ring Indicator**) (default)** Pin3-4 : 5V Standby power **(**option**)** Pin5-6:12V Standby power (option)

COM6 (SBC-7114/COM4):

(2.0mm Pitch 2x5 Pin Header), COM6 port, up to one standard RS232 port is provided. They can be used directly via COM cable connection.

Signal Name	Pin#	Pin#	Signal Name
DCD	1	2	RXD
TXD	3	4	DTR
Ground	5	6	DSR
RTS	7	8	CTS
JP6 Setting: RI/5V/12V	9	10	NC

COM5 (SBC-7114/COM3):

(2.0mm Pitch 2x5 Pin Header), COM5 port, up to one standard RS232 port is provided. They can be used directly via COM cable connection.

Signal Name	Pin#	Pin#	Signal Name
DCD	1	2	RXD
TXD	3	4	DTR
Ground	5	6	DSR
RTS	7	8	CTS
JP6 Setting: RI/5V/12V	9	10	NC

GPIO1:

(2.0mm Pitch 2x5 Pin Header), General-purpose input/output port, it provides a group of self-programming interfaces to customers for flexible use.

Signal Name	Pin#	Pin#	Signal Name
Ground	1	2	NC
NC	3	4	SMB_DATA_R
SMB_CLK_R	5	6	PCH-GPIO56
PCH-GPIO57	7	8	PCH-GPIO59
PCH-GPIO58	9	10	+5V

JTAG:

(2.0mm Pitch 2x5 Pin Header), Reserve.

JP1:

(2.0mm Pitch 1x2 Pin Header), Reserve.

JP2:

(2.0mm Pitch 1x2 Pin Header), Reserve.

CAN1/CAN2:

(3.5mm Pitch 1x10 Pin connector), it provides two CAN-bus interfaces.

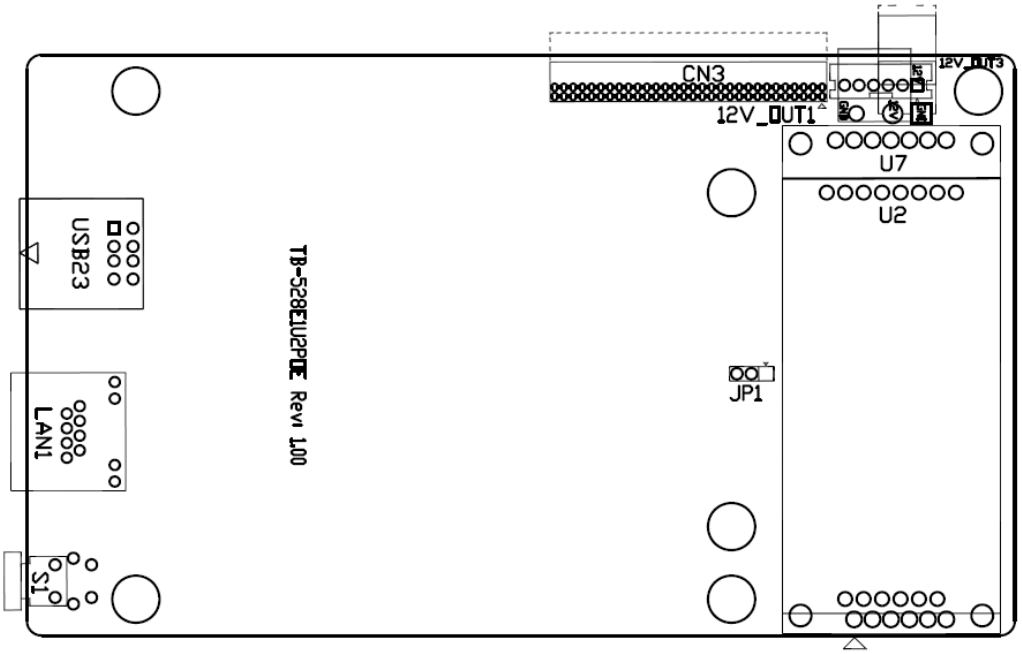
Pin#	Channel	Signal Name	Function
1	CAN2	CANL2	CAN bus Signal L
2		R2-	Terminal resistor R-(internally connected to CANL2)
3		FG	Shield cable (FG)
4		R2+	Terminal resistor R+(internally connected to CANH2)
5		CANH2	CAN bus Signal H
6	CAN1	CANL1	CAN bus Signal L
7		R1-	Terminal resistor R-(internally connected to CANL1)
8		FG	Shield cable (FG)
9		R1+	Terminal resistor R+(internally connected to CANH1)
10		CANH1	CAN bus Signal H

[See TB-528CAN2 Manual]

48. TB-528E1U2POE（option）:

SBC-7114 Riser Card,TB-528E1U2POE CN3 connect to SBC-7114 CN3 pin Header, TB-528E1U2POE 12V_OUT1 connect to SBC-7114 BAT2.

TB-528E1U2POE Top：

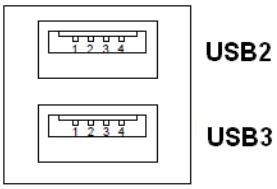


CN3：

(1.27mm Pitch 2X30 Pin Header),connect to SBC-7114 CN3 pin Header.

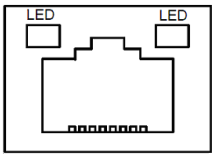
USB23(SBC-7114 USB3/USB4)：

(Double stack USB type A), Rear USB connector, it provides up to 2 USB2.0 ports, speed up to 480Mb/s.



LAN1：

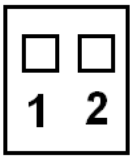
(RJ45 Connector), Rear LAN port, one standard 10/100/1000M RJ-45 Ethernet ports are provided. Use Intel 82574L chipset, LINK LED (green) and ACTIVE LED (green) respectively located at the left-hand and right-hand side of the Ethernet port indicate the activity and transmission state of LAN.



PSE Function support	
PSE output Voltage	44-DC 57V

12V_OUT1：

(3.96mm Pitch 1x2 Pin Header), POE DC12V Output.



Pin#	Output Voltage
1	12V_POE
2	Ground

POE: The Ag5510 input complies with the IEEE802.3at specification. When the inputs are connected to a Power Sourcing Equipment (PSE), they will

automatically present a Powered Device (PD) signature to the PSE (when requested). The equipment will then recognize that a PD is connected to that line and supply power.

Model	U7	Maximum Output Power	SBC-7114
TB-528E1UPOE	AG5510	40W	●

12V_OUT3（option）：

(2.0mm Pitch 1x6 Pin Header), Reserve.

12V_OUT1（option）：

(3.96mm Pitch 1x2 Pin Header), Reserve.

JP3（option）：

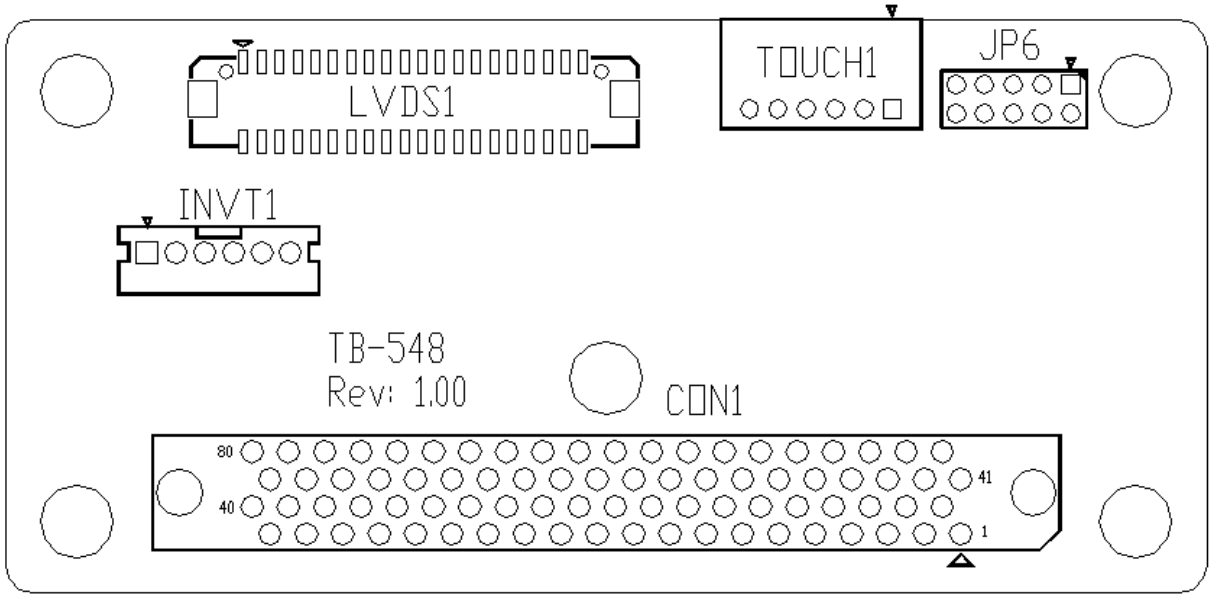
2.0mm Pitch 1x3 Pin Header), Reserve.

S1（option）：Reserve.

49. TB-548 R1.00 (option):

SBC-7114 Riser Card, TB-548 LVDS1 connect to SBC-7115 CN1 DF13-40P, TB-548 INVT1 connects to SBC-7114 INVT1, TB-548 TOUCH1 connect to SBC-7114 TCH1, TB-548 CON1 connect to TB-547 CON1.

TB-548 Top:



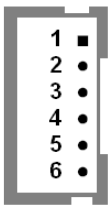
LVDS1:

(1.25mm Pitch 2x20 Connector, DF13-40P).

Function	Signal Name	Pin#		Signal Name	Function
LVDS	12V_S0	2	1	12V_S0	LVDS
	BKLT_EN_OUT	4	3	BKLT_CTRL	
	Ground	6	5	Ground	
	LVDS_VDD5	8	7	LVDS_VDD5	
	LVDS_VDD3	10	9	LVDS_VDD3	
	Ground	12	11	Ground	
	LA_D0_P	14	13	LA_D0_N	
	LA_D1_P	16	15	LA_D1_N	
	LA_D2_P	18	17	LA_D2_N	
	LA_D3_P	20	19	LA_D3_N	
	LA_CLKP	22	21	LA_CLKN	
	LB_D0_P	24	23	LB_D0_N	
	LB_D1_P	26	25	LB_D1_N	
	LB_D2_P	28	27	LB_D2_N	
	LB_D3_P	30	29	LB_D3_N	
	LB_CLKP	32	31	LB_CLKN	
USB7 (option)	Ground	34	33	SEL_LCD_EDID	
	USB7_P	36	35	USB7_N	
	5V_S5_USB	38	37	LVDS1_DDC_DATA	
Power LED	PWR_LED+	40	39	LVDS1_DDC_CLK	

INVT1:

(2.0mm Pitch 1x6 wafer Pin Header), Backlight control connector for LVDS.



Pin#	Signal Name
1	+DC12V_S0
2	+DC12V_S0
3	Ground
4	Ground
5	BKLT_EN_OUT
6	BKLT_CTRL

TOUCH1:

(2.0mm Pitch 1x6 wafer Pin Header), internal Touch controller connector.

Pin#	Signal Name
1	SENSE
2	X+
3	X-
4	Y+
5	Y-
6	GND_EARCH

JP6 (option):

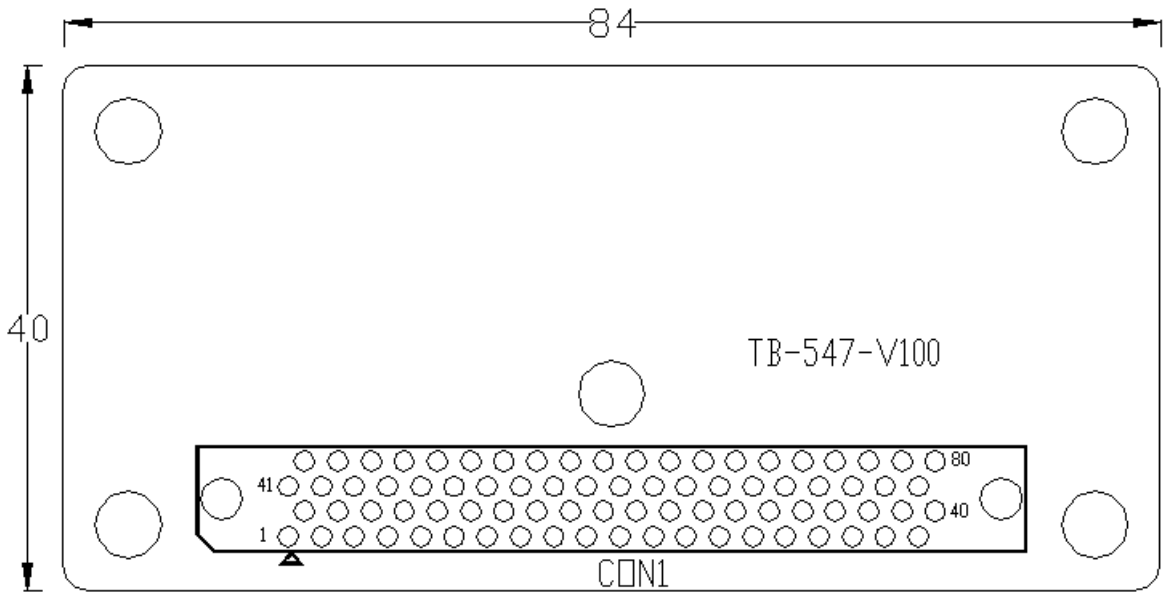
(2.0mm Pitch 2x5 Pin Header), LVDS EDID setting jumper.

JP6 Pin#	*Function (CN1)*
Close 1-2	*Single channel LVDS*
Open 1-2	*Dual channel LVDS*
Close 3-4	*8/24 bit*
Open 3-4	*6/18 bit*
SEL-LCD-EDID:	
Close 5-6	*Onboard EDID*
Open 5-6	*Panel EDID*
All open (JP6)	**Default**

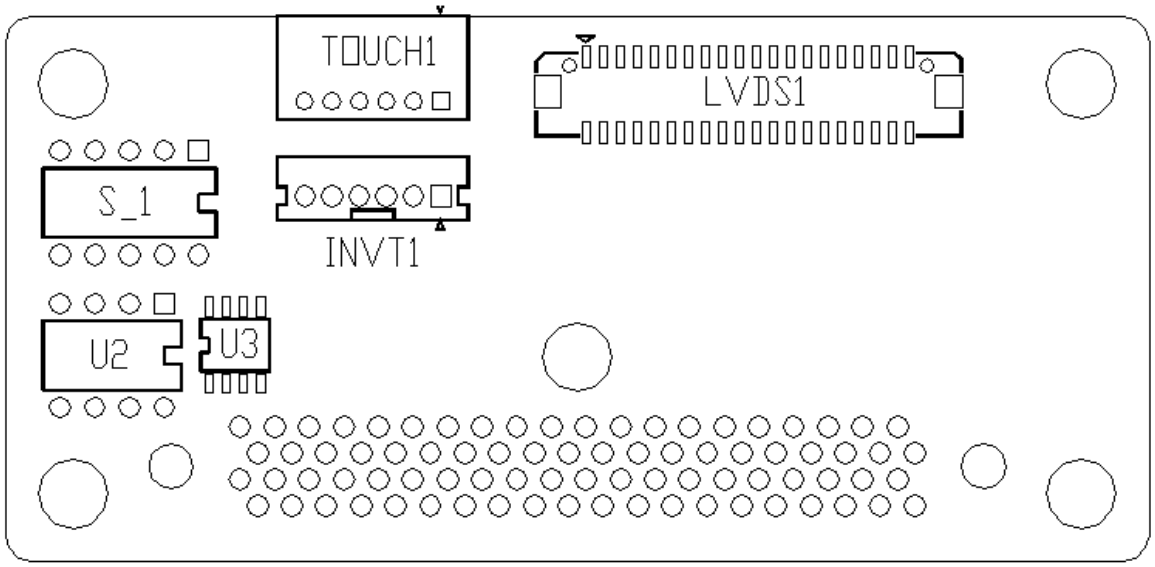
50. TB-547 R1.20 (option):

TB-548 Riser Card, TB-547 LVDS connect to LVDS Panel, TB-547 INVT1 connect to LVDS Panel, TB-547 TOUCH1 connect to TOUCH Panel, TB-547 CON1 OPS connect to TB-548 CON1.

TB-547 Top:



TB-547 Bottom:



LVDS1:

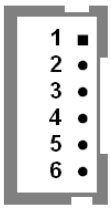
(1.25mm Pitch 2x20 Connector, DF13-40P).

Function	Signal Name	Pin#		Signal Name	Function
LVDS	12V_S0	2	1	12V_S0	LVDS
	BKLT_EN_OUT	4	3	BKLT_CTRL	
	Ground	6	5	Ground	
	LVDS_VDD5	8	7	LVDS_VDD5	
	LVDS_VDD3	10	9	LVDS_VDD3	
	Ground	12	11	Ground	
	LA_D0_P	14	13	LA_D0_N	
	LA_D1_P	16	15	LA_D1_N	

	LA_D2_P	18	17	LA_D2_N	
	LA_D3_P	20	19	LA_D3_N	
	LA_CLKP	22	21	LA_CLKN	
	LB_D0_P	24	23	LB_D0_N	
	LB_D1_P	26	25	LB_D1_N	
	LB_D2_P	28	27	LB_D2_N	
	LB_D3_P	30	29	LB_D3_N	
	LB_CLKP	32	31	LB_CLKN	
USB7 (option)	Ground	34	33	Ground	
	USB7_P	36	35	USB7_N	
	5V_S5_USB	38	37	5V_S5_USB	
Power LED	PWR_LED+	40	39	Ground	

INVT1:

(2.0mm Pitch 1x6 wafer Pin Header), Backlight control connector for LVDS.



Pin#	Signal Name
1	+DC12V_S0
2	+DC12V_S0
3	Ground
4	Ground
5	BKLT_EN_OUT
6	BKLT_CTRL

TOUCH1:

(2.0mm Pitch 1x6 wafer Pin Header), internal Touch controller connector.

Pin#	Signal Name
1	SENSE
2	X+
3	X-
4	Y+
5	Y-
6	GND_EARCH

S_1 (PIN3):

(Switch), LVDS EDID setting jumper.

S_1 (Switch)	Function (LVDS)
Pin1 (ON)	Single channel LVDS
Pin1 (OFF)	Dual channel LVDS
Pin2 (ON)	8/24 bit
Pin2 (OFF)	6/18 bit
SEL-LCD-EDID (SBC-7114 U17 or OPC-547 U2/U3)	
Pin3 **(ON)**	Panel EDID
Pin3 **(OFF)**	Onboard EDID
Pin4	-
Pin5	-
This setting can only select SBC-7114 R2.XX S_1 or TB-547 S_1.	

U3:

AT24C02, The EEPROM IC (U3) is the set of LVDS resolution.

If you need other resolution settings, please upgrade U3 data.

LVDS Resolution	800*480 (option)
	800*600 (option)
	1024*768 (option)
	1280*1024 (option)
	1920*1080 (option)
	……..

Chapter 3 BIOS Setup

3.1 Operations after POST Screen

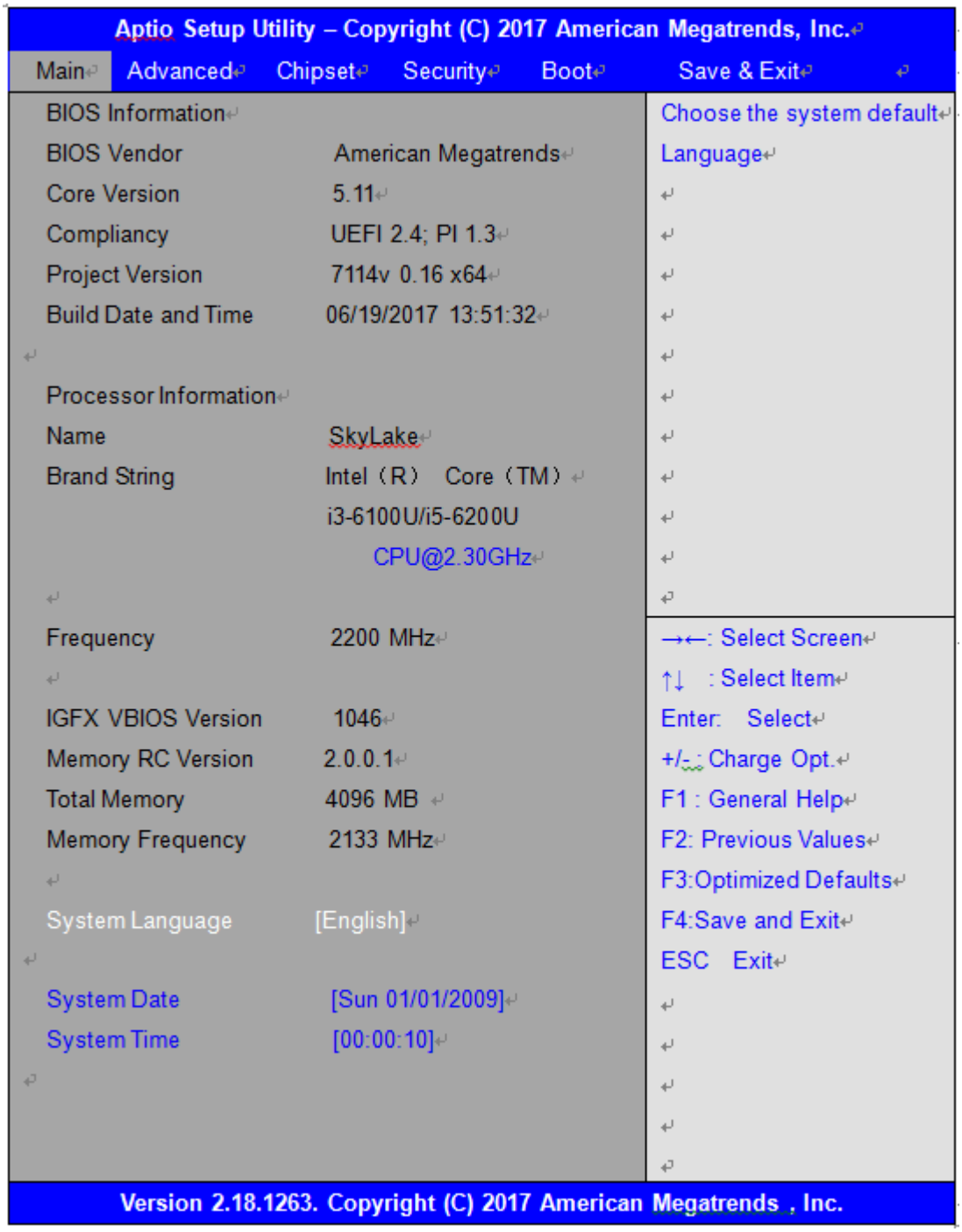
After CMOS discharge or BIOS flashing operation, press [Delete] key to enter CMOS Setup.

After optimizing and exiting CMOS Setup

3.2 BIOS Setup Utility

Press [Delete] key to enter BIOS Setup utility during POST, and then a main menu containing system summary information will appear.

3.3 Main Settings



System Time:

Set the system time, the time format is:

Hour : 0 to 23

Minute : 0 to 59

Second : 0 to 59

System Date:

Set the system date, the date format is:

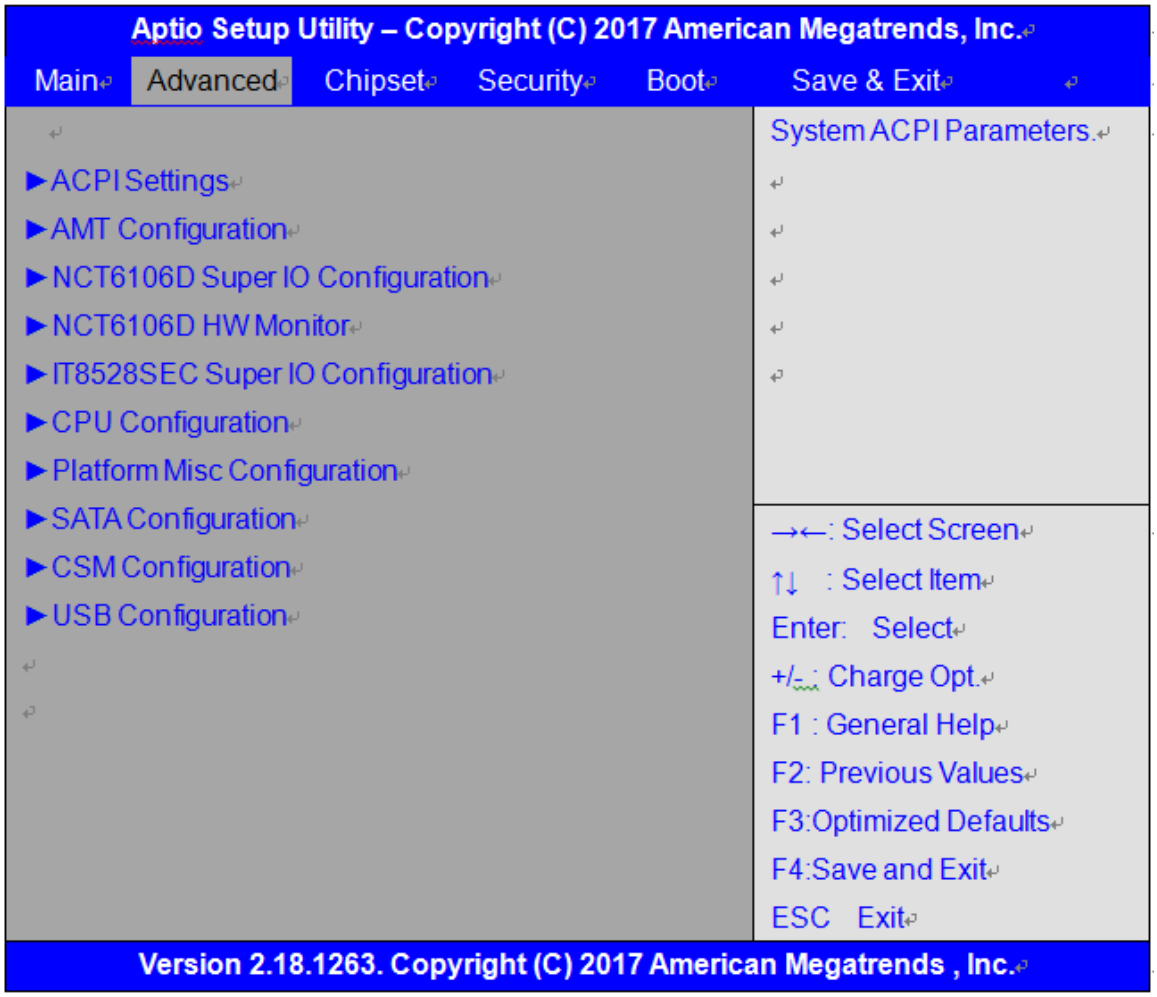
Day: Note that the 'Day' automatically changes when you set the date.

Month: 01 to 12

Date: 01 to 31

Year: 1998 to 2099

3.4 Advanced Settings



3.4.1 ACPI Settings

Enable ACPI Auto Configuration:

[Disabled]

[Enabled]

Enable Hibernation:

[Enabled]

[Disabled]

ACPI Sleep State:

[S3 (Suspend to RAM)]

[Suspend Disabled]

Lock Legacy Resources:

[Disabled]

[Enabled]

S3 Video Repost:

[Disabled]

[Enabled]

ACPI Low Power S0 Idle:

[Disabled]

[Enabled]

3.4.2 AMT Configuration

Intel AMT	[Disabled]
BIOS Hotkey Pressed	[Disabled]
MEBx Selection Screen	[Disabled]
Hide Un-Configure ME Configuration Prompt	[Disabled]
MEBx Debug Message Output	[Disabled]
Un-Configure ME	[Disabled]
Amt Wait Timer	0
ASF	[Enabled]
Activate Remote Assistance Process	[Disabled]
USB Provisioning of AMT	[Enabled]
PET Progress	[Enabled]
AMT CIRA Timeout	0
WatchDog	[Disabled]
OS Timer	0
BIOS Timer	0

3.4.3 NCT6106D Super IO Configuration

Super IO Chip	NCT6106D
Serial Port 1 Configuration	
Serial port	**[Enabled]**
	[Disabled]
Device Settings	IO=3F8h； IRQ=4；

Change Settings	**[Auto]**
F75111 COM1 Config	
	[RS-232 Mode]
	[RS-485 Mode]
	[RS-422 Mode]
Serial Port 2 Configuration	
Serial port	**[Enabled]**
	[Disabled]
Device Settings	IO=2F8h； IRQ=3；
Change Settings	**[Auto]**
Serial Port 3 Configuration	
Serial port	**[Enabled]**
	[Disabled]
Device Settings	IO=3E8h； IRQ=7；
Change Settings	**[Auto]**
Serial Port 4 Configuration	
Serial port	**[Enabled]**
	[Disabled]
Device Settings	IO=2E8h； IRQ=7；
Change Settings	**[Auto]**
Serial Port 5 Configuration	
Serial port	**[Enabled]**
	[Disabled]
Device Settings	IO=2F0h； IRQ=7；
Change Settings	**[Auto]**
COM5 Config	**[RS-485 Mode]**
	[RS-422 Mode]
Serial Port 6 Configuration	
Serial port	**[Enabled]**
	[Disabled]
Device Settings	IO=2E0h； IRQ=7 ；

Change Settings	**[Auto]**
COM6 Config	**[RS-485 Mode]**
	[RS-422 Mode]
Power Failure	**[Power OFF]**
	[Power ON]
	[Last state]

3.4.4 NCT6106D HW Monitor

Pc Health Status

CPU Temperature	：38
CPU Fan Speed	：N/A
VCORE	：+0.872V
12V	：+11.864V
5V	：+5.299V
VCC3V	：+3.472V

3.4.5 IT8528SEC Super IO Configuration

EC VERSION	7114E005
Super IO Chip	IT8528SEC

3.4.6 CPU Configuration

Intel® Core™ i5-6200U CPU @ 2.30GHz

CPU Signature	406E3
Microcode Patch	9E
Max CPU Speed	2300 MHz
Mix CPU Speed	400MHz
CPU Speed	2200 MHz
Processor Cores	2
Hyper Threading Technology	Supported
Intel VT-X Technology	Supported
Intel SMX Technology	Not Supported
64-bit	Supported
EIST Technology	Supported
CPU C3 state	Supported
CPU C6 state	Supported
CPU C7 state	Supported
CPU C8 state	Supported

CPU C9 state	Supported
CPU C10 state	Supported
L1 Date Cache	32KB x 2
L1 Code Cache	32KB x 2
L2 Cache	256 KB x 2
L3 Cache	3 MB
L4 Cache	Not Present
Hyper-threading	[Enabled]
Active Processor Cores	[All]
Overclocking lock	[Disabled]
Intel Virtualization Technology	[Enabled]
Hardware Prefetcher	[Enabled]
Adjacent Cache Line Prefetch	[Enabled]
CPU AES	[Enabled]
Boot performance mode	[Max Non-Turbo Performance]
Intel(R) Speed Shift Technology	[Enabled]
Intel(R) SpeedStep(tm)	[Enabled]
Turbo Mode	[Enabled]
Package Power Limit MSR Lock	[Disabled]
1-Core Ratio Limit Override	0
2-Core Ratio Limit Override	0
Configurable TDP Boot Mode	[Nominal]
Configurable TDP Lock	[Disabled]
CTDP BIOS control	[Disabled]
Platform PL1 Enable	[Disabled]
Platform PL2 Enable	[Disabled]
CPU C states	[Enabled]
Enhanced C-states	[Enabled]
C-State Auto Demotion	[C1 and C3]
C-State Un- Demotion	[C1 and C3]
Package C state demotion	[Enabled]
Package C state undemotion	[Enabled]
CState Pre-Wake	[Enabled]
Package C State limit	[AUTO]
CFG lock	[Enabled]
►Power Limit 3 Settings	
Power Limit 3 Override	[Disabled]

► **Power Limit 4 Settings**

Power Limit 4 Override	[Disabled]

► **CPU Thermal Configuration**

CPU DTS	[Disabled]
TCC Activation Offset	0
ACPI 3.0 T-States	[Disabled]
Debug Interface	[Disabled]
Debug Interface Lock	[Enabled]
SW Guard Extensions(SGX)	[Software Controlled]
Select Owner EPOCH input type	[No Change In Owner EPOCHS]
PRMRR Size	[AUTO]

3.4.7 Platform Misc Configuration

Native PCIE Enable	[Enabled]
Native ASPM	[Auto]
BDAT ACPI Table Support	[Disabled]
Intel Ready Mode Technology	[Disabled]
ACPI Debug	[Disabled]
PTID Support	[Enabled]
PECI Access Method	[Direct I/O]
Firmware Configuration	[Test]
ZpODD Support	[Disabled]
PCI Delay Optimization	[Disabled]

► **DPTF Configuration**

DPTF	[Enabled]

► **Platform Setting**

Pmic Vcc IO Level	[Disabled]
Pmic Vddq Level	[Disabled]

Power Sharing Manager	[Disabled]
Select Camera	[IVCAM]
Enable 3D Camera DFU device	[Disabled]
Wireless device	[Disabled]
WRDS Package	
WiFi SAR	[Disabled]
HID Event Filter Driver	[Disabled]
Enable Wireless Charge Support	[Disabled]
Enable FFU Support	[Disabled]

3.4.8 SATA Configuration

SATA Controller(S)	[Enabled]
SATA Mode	[AHCI]
SATA Test Mode	[Disabled]
►Software Feature Mask SATA Controller	
Aggressive LPM Support	[Enabled]
SATA Controller Speed	[Default]
Serial ATA Port 0	Empty
Software Preserve	Unknown
Port 0	[Enabled]
Hot Plug	[Disabled]
External SATA	[Disabled]
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
Device Sleep	[Disabled]
SATA DEVSLEP Idle Timeout Config	[Disabled]
Serial ATA Port 1	Empty
Software Preserve	Unknown
Port 1	[Enabled]
Hot Plug	[Disabled]
External SATA	[Disabled]
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]

Device Sleep	[Disabled]
SATA DEVSLEP Idle Timeout Config	[Disabled]
Serial ATA Port 2	Empty
Software Preserve	Unknown
Port 2	[Enabled]
Hot Plug	[Disabled]
External SATA	[Disabled]
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
Device Sleep	[Disabled]
SATA DEVSLEP Idle Timeout Config	[Disabled]
Serial ATA Port 3	Empty
Software Preserve	Unknown
Port 3	[Enabled]
Hot Plug	[Disabled]
External SATA	[Disabled]
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
Device Sleep	[Disabled]
SATA DEVSLEP Idle Timeout Config	[Disabled]
Serial ATA Port 4	Empty
Software Preserve	Unknown
Port 4	[Enabled]
Hot Plug	[Disabled]
External SATA	[Disabled]
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
Device Sleep	[Disabled]
SATA DEVSLEP Idle Timeout Config	[Disabled]
Serial ATA Port 5	Empty
Software Preserve	Unknown

Port 5	[Enabled]
Hot Plug	[Disabled]
External SATA	[Disabled]
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
Device Sleep	[Disabled]
SATA DEVSLEP Idle Timeout Config	[Disabled]

3.4.9 CSM Configuration

Compatibility Support Module Configuration

CSM Support	[Enabled]
CSM16 Module Version	07.79
GateA20 Active	[Upon Request]
Option ROM Messages	[Force BIOS]
INT19 Trap Response	[Immediate]
Boot option filter	[UEFI and Legacy]
Option ROM execution	
Network	[Do not launch]
Storage	[UEFI]
Video	[Legacy]
Other PCI devices	[UEFI]

3.4.10 USB Configuration

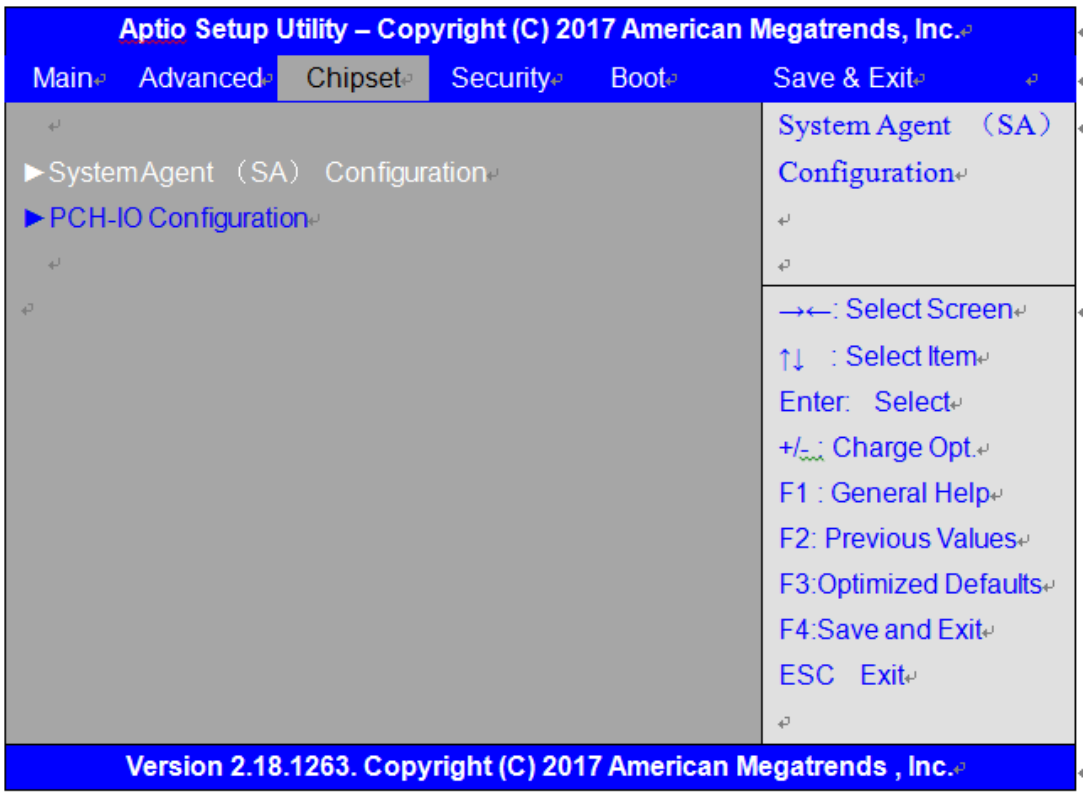
USB Module Version	16
USB Controllers:	1XHCI
USB Devices:	1 Keyboard,1 Mouse
Legacy USB Support	[Enabled]

XHCI Hand-off	[Enabled]
USB Mass Storage Driver Support	[Enabled]
Port 60/64 Emulation	[Disabled]

USB Hardware delays and time-outs:

USB transfer time-out	[20 sec]
Device reset time-out	[20 sec]
Device power-up delay	[Auto]

3.5 Chipset Settings



3.5.1 System Agent （SA） Configuration

System Agent Bridge Name	Skylake
SA PCIe Code Version	2.0.0.0
VT-d	Supported

VT-d	[Enabled]
Primary IGFX Boot Display	[VBIOS Deafault]
Secondary IGFX Boot Display	[Disabled]
Active LFP	[eDP Port-A]
Panel Color Depth	[18 Bit]

LCD Backlight Control	[PWM Normal by BIOS]
BIOS Control Backlight Level	[Level7]
►Graphics Configuration	
IGFX VBIOS Version	1046
Graphics Turbo IMON Current	31
Skip Scanning of External Gfx Card	[Disabled]
Primary Display	[Auto]
Primary PEG	[Auto]
Primary PCIE	[Auto]
Internal Graphics	[Auto]
GTT Size	[8MB]
Aperture Size	[256MB]
DVMT Pre-Allocated	[32M]
DVMT Total Gfx Mem	[256M]
Gfx Low Power Mode	[Enabled]
VDD Enable	[Enabled]
PM Support	[Enabled]
PAVP Enable	[Enabled]
Cdynmax Clamping Enable	[Enabled]
Cd Clock Frequency	[675MHz]
►Intel® Ultrabook Event Support	
IUER Slate Enable	[Disabled]
IUER Dock Enable	[Disabled]
IUER Button Enable	[Disabled]
►DMI/OPI Configuration	
DMI Vc1 Control	[Disabled]
DMI Vcm Control	[Enabled]
►Memory Configuration	
Memory RC Version	2.0.0.1
Memory Frequency	2133MHz
Total Memory	4096MB
VDD	1200
DIMM#0	4096MB
DIMM#1	Not Present
DIMM#2	Not Present
DIMM#3	Not Present

Memory Timings(tCL-tRCD-tRP-tRAS)	15-36
MRC ULT Safe Conifg	[Disabled]
Maximum Memory Frequency	[Auto]
HOB Buffer Size	[Auto]
ECC Support	[Enabled]
Max TOLUD	[Dynamic]
LCD Backlight Mode	[PWM]
Backlight Control	[PWM Normal by BIOS]
BIOS Control Backlight Level	[Level 7]
SA GV	[Enabled]
SA GV Low Freq	[MRC default]
Energy Performance Gain	[Disabled]
EPG DIMM Idd3N	26
EPG DIMM Idd3P	11
Retrain on Fast fall	[Enabled]
Enable RH Prevention	[Enabled]
Row Hammer Solution	[Hardware RHP]
RH Activation Probability	[1/2^11]
Exit On Failure(MRC)	[Enabled]
MC Lock	[Enabled]
Probeless Trace	[Disabled]
Enable/Disable IED(Intel Enhanced Debug)	[Disabled]
Ch Hash Support	[Enabled]
Ch Hash Mask	12488
Ch Hash Interleaved Bit	[BIT8]
VC1 Read Metering	[Enabled]
VC1 RdMeter Time Window	800
VC1 RdMeter Threshold	280
Strong Weak Leaker	7
Memory Scrambler	[Enabled]
Channel A DIMM Control	[Enable both DIMMS]
Channel B DIMM Control	[Enable both DIMMS]
Force Single Rank	[Disabled]
Memory Remap	[Enabled]
Time Measure	[Disabled]
Lpddr Mem WL Set	[Set B]
EV Loader	[Disabled]

EV Loader Delay [Enabled]

Fast Boot [Enabled]

DLL Weak Lock Support [Enabled]

►**Memory Thermal Configuration**

►**Memory Power and Thermal Throttling**

DDR PowerDown and idle counter [BIOS]

For LPDDR Only:DDR PowerDown and idle counter [BIOS]

REFRESH_2X_MODE [Disabled]

LPDDR Thermal Sensor [Enabled]

SelfRefresh Enable [Enabled]

SelfRefresh IdleTimer 512

Throttler CKEMin Defeature [Enabled]

Throttler CKEMin Timer 48

For LPDDR Only:Throttler CKEMin Defeature Enabled]

For LPDDR Only:Throttler CKEMin Timer 64

Pwr Down Idle Timer 0

►**Dram Power Idle Timer**

Use user provided power weights, scale factor, and channel power floor values [Disabled]

Energy Scale factor 4

Idle Energy Ch0Dimm0 10

PowerDown Energy Ch0Dimm0 6

Activate Energy Ch0Dimm0 172

Read Energy Ch0Dimm0 212

Write Energy Ch0Dimm0 221

Idle Energy Ch0Dimm1 10

PowerDown Energy Ch0Dimm1 6

Activate Energy Ch0Dimm1 172

Read Energy Ch0Dimm1 212

Write Energy Ch0Dimm1 221

Idle Energy Ch1Dimm0 10

PowerDown Energy Ch1Dimm0 6

Activate Energy Ch1Dimm0	172
Read Energy Ch1Dimm0	212
Write Energy Ch1Dimm0	221
Idle Energy Ch1Dimm0	10
PowerDown Energy Ch1Dimm0	6
Activate Energy Ch1Dimm0	172
Read Energy Ch1Dimm0	212
Write Energy Ch1Dimm0	221
Idle Energy Ch1Dimm1	10
PowerDown Energy Ch1Dimm1	6
Activate Energy Ch1Dimm1	172
Read Energy Ch1Dimm1	212
Write Energy Ch1Dimm1	221

►Memory Thermal Reporting

Lock Thermal: Management Registers	[Enabled]
Memory Thermal Reporting	
Extern Therm Status	[Disabled]
Closed Loop Therm Manage	[Disabled]
Open Loop Therm Manage	[Disabled]
Thermal Threhold Settings	
Warm Threshold Ch0 Dimm0	255
Warm Threshold Ch0 Dimm1	255
Hot Threshold Ch0 Dimm0	255
Hot Threshold Ch0 Dimm1	255
Warm Threshold Ch1 Dimm0	255
Warm Threshold Ch1 Dimm1	255
Hot Threshold Ch1 Dimm0	255
Hot Threshold Ch1 Dimm1	255
Thermal Throttle Budget Settings	
Warm Budget Ch0 Dimm0	255

Warm Budget Ch0 Dimm1	255
Hot Budget Ch0 Dimm0	255
Hot Budget Ch0 Dimm1	255
Warm Budget Ch1 Dimm0	255
Warm Budget Ch1 Dimm1	255
Hot Budget Ch1 Dimm0	255
Hot Budget Ch1 Dimm1	255

►Memory RAPL

Rapl Power Floor Ch0	0
Rapl Power Floor Ch1	0
RAPL PL Lock	[Disabled]
RAPL PL 1 enable	[Disabled]
RAPL PL 1 Power	0
RAPL PL 1 WindowX	0
RAPL PL 1 WindowY	0
RAPL PL 1 enable	[Disabled]
RAPL PL 1 Power	0
RAPL PL 1 WindowX	0
RAPL PL 1 WindowY	0
Memory Thermal Management	[Disabled]

►Memory Training Algorithms

Early Command Training	[Disabled]
SenseAmp Offset Training	[Enabled]
Early ReadMPR Timing Centering 2D	[Enabled]
Read MPR Training	[Enabled]
Receive Enable Training	[Enabled]
Jedec Write Leveling	[Enabled]
Early Write Time Centering 2D	[Enabled]
Early Read Time Centering 2D	[Enabled]
Write Timing Centering 1D	[Enabled]
Write Voltage Centering 1D	[Enabled]
Read Timing Centering 1D	[Enabled]
Dimm ODT Training*	[Enabled]
Max RTT_WR	[ODT Off]

DIMM RON Training*	[Enabled]
Write Drive Strength/Equalization 2D*	[Disabled]
Write Slew Rate Training*	[Enabled]
Read ODT Training*	[Enabled]
Read Equalization Training*	[Enabled]
Read Amplifier Training*	[Enabled]
Write Timing Centering 2D	[Enabled]
Read Timing Centering 2D	[Enabled]
Command Voltage Centering	[Enabled]
Write Voltage Centering	[Enabled]
Read Voltage Centering 2D	[Enabled]
Late Command Training	[Enabled]
Round Trip Latency	[Enabled]
Turn Around Timing Training	[Enabled]
Rank Margin Tool	[Disabled]
Memory Test	[Disabled]
DIMM SPD Alias Test	[Enabled]
Receive Enable Centering 1D	[Enabled]
Retrain Margin Check	[Enabled]
Command Power Training	[Disabled]

►GT-Power Management Control

GT Info	GT2
RC6(Render Standby)	**[Enabled]**

3.5.2 PCH-IO Configuration

Intel PCH RC Version	2.0.0.0
Intel PCH SKU Name	PCH-LP Mobile(U) Premium SKU
Intel PCH REV ID	21/C1

►PCI Express Configuration

PCI Express Clock Gating	[Enabled]
DMI Link ASPM Control	[Enabled]
Port8xh Decode	[Disabled]
Peer Memory Write Enable	[Disabled]

Compliance Test Mode	[Disabled]
PCIe-USB Glitch W/A	[Disabled]
PCIe function swap	[Enabled]
►PCI Express Gen3 Eq Lanes	
Override SW EQ Settings	[Disabled]
►PCI Express Root Port 1	
PCI Express Root Port 1	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	

PCIE1 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►PCI Express Root Port 2

PCI Express Root Port 2	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]

PCH PCIe CLKREQ# Configuration

PCIE2 CLKREQ Mapping Override	[Default]

Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]
►PCI Express Root Port 3	
PCI Express Root Port 3	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE3 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►PCI Express Root Port 4

PCI Express Root Port 4	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE4 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►PCI Express Root Port 5

PCI Express Root Port 5	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE5 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►PCI Express Root Port 6

PCI Express Root Port 6	[Enabled]
Topology	[Unknown]

ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE6 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►PCI Express Root Port 7

PCI Express Root Port 7	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]

L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE7 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►PCI Express Root Port 8

PCI Express Root Port 8	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]

Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE8 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►PCI Express Root Port 9

PCI Express Root Port 9	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]

UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE9 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]
►PCI Express Root Port 10	
PCI Express Root Port 10	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7

ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE10 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►PCI Express Root Port 11

PCI Express Root Port 11	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]

URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE11 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►PCI Express Root Port 12

PCI Express Root Port 12	[Enabled]
Topology	[Unknown]
ASPM Support	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]

FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Non-Compliance Device	[Disabled]
Extra Bus Reserved	0
Reserved Memory	10
Prefetchable Memory	10
Reserved I/O	4
PCIE Cp	2
PCIE Cm	6
PCIE LTR	[Enabled]
PCIE LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE12 CLKREQ Mapping Override	[Default]
Snoop Latency Ocerride	[Auto]
Non Snoop Latency Ocerride	[Auto]

►USB Configuration

USB Precondition	[Disabled]
XHCI Disable Compliance Mode	[FALSE]
xDCI Support	[Disabled]
USB Port Disable Override	[Disabled]

►BIOS Security Configuration

RTC Lock	[Enabled]
BIOS Lock	[Disabled]

►HD Audio Configuration

HD Audio	[Autio]
Audio DSP	[Disabled]

HDA-Link Codec Select [Platform Onboard]
iDisplay Audio Disconnect [Disabled]
PME Enable [Disabled]

►HD Audio Advanced Configuration

HD Audio Subsystem Advanced Configuration Settings
I/O Buffer Control:
I/O Buffer Ownership [HD-Audio Link]
I/O Buffer Voltage Select [3.3V]
Statically Switchable BCLK Clock
Frequency Configuration:
HD Audio Link Frequency [24MHz]
iDisplay Link Frequency [96MHz]

►HD Audio DSP Features Configuration

HD Audio Subsystem Features Configuration(ACPI)

Audio DSP NHLT Endpoints:
Configuration:
DMIC [4 Mic Array]
Bluetooth [Disabled]
I2S [Disabled]
Audio DSP Feature Support:
WoV(Wake on Voice) [Disabled]
Bluetooth Sideband [Disabled]
BT Intel HFP [Disabled]
BT Intel A2DP [Disabled]
Codec based VAD [Disabled]
DSP based Speech.Pre-Peocessing Disabled [Disabled]

Voice Activity Detection [Intel Wake on Voice]

Audio DSP Pre/Post-Processing
Module Support:
Waves [Disabled]
DTS [Disabled]
IntelSst Speech [Disabled]
Dolby [Disabled]

ForteMedia SAMSoft	[Disabled]
Intel WoV	[Disabled]
Sound Research IP	[Disabled]
Conexant Pre-Process	[Disabled]
Conexant Smart Amp	[Disabled]
Custom Module 'Alpha'	[Disabled]
Custom Module 'Beta'	[Disabled]
Custom Module 'Gamma'	[Disabled]
►Serial IO Configuration	
Touch Panel	[SPI Touch]
BT/UART Mux Select	[UART Signal]
I2C0 Controller	[Disabled]
I2C1 Controller	[Disabled]
I2C2 Controller	[Disabled]
I2C3 Controller	[Disabled]
I2C4 Controller	[Disabled]
I2C5 Controller	[Disabled]
SPI0 Controller	[Disabled]
SPI1 Controller	[Disabled]
UART0 Controller	[Disabled]
UART1 Controller	[Disabled]
UART2 Controller	[Disabled]
GPIO Controller	[Enabled]
►Serial IO GPIO Settings	
GPIO IRQ Route	[IRQ14]
WITT/MITT Test Device	[Disabled]
UART Test Device	[Disabled]
Addtional Serial IO devices	[Disabled]
►SerialIO timing parameters	
SerialIO timing parameters	[Disabled]
►SkyCam Configuration	
SkyCam CIO2 Device	[Disabled]
Control Logic 0	[Disabled]
Control Logic 1	[Disabled]

Control Logic 2	[Disabled]
Control Logic 3	[Disabled]
Link0	[Disabled]
Link1	[Disabled]
Link2	[Disabled]
Link3	[Disabled]
PORT-A HS-RXEN/TEM-EN Override	[Disabled]
PORT-B HS-RXEN/TEM-EN Override	[Disabled]
PORT-C HS-RXEN/TEM-EN Override	[Disabled]
PORT-D HS-RXEN/TEM-EN Override	[Disabled]
PORT-A CTLE	[Enabled]
PORT-B CTLE	[Enabled]
PORT-C/D CTLE	[Enabled]
PORT-A CTLE CAP Value	e
PORT-A CTLE RES Value	d
PORT-B CTLE CAP Value	e
PORT-B CTLE RES Value	d
PORT-C/D CTLE CAP Value	e
PORT-C/D CTLE RES Value	d
PORT-A TRIM	[Enabled]
PORT-B TRIM	[Enabled]
PORT-C TRIM	[Enabled]
PORT-D TRIM	[Enabled]
PORT-A Data Trim Value	bbbb
PORT-B Data Trim Value	bbbb
PORT-C/D Data Trim Value	cccc
PORT-A Clk Trim Value	a
PORT-B Clk Trim Value	a
PORT-C Clk Trim Value	9
PORT-D Clk Trim Value	a

►SCS Configuration

eMMC 5.0 Controller	[Enabled]
eMMC 5.0 HS400 Mode	[Enabled]
Driver Strength	[33 Ohm]
SDCard 3.0 Controller	[Disabled]

►ISH Configuration

ISH Controller	[Disabled]
PDT Unlock Message	[Disabled]

►TraceHub Configuration Menu

TraceHub Enabled Mode	[Disabled]
MemRegion 0 Buffer Size	[1MB]
MemRegion 1 Buffer Size	[1MB]

►Pch Thermal Throttling Control

Thermal Throttling Level	[Suggested Setting]
DMI Thermal Setting	[Suggested Setting]
SATA Thermal Setting	[Suggested Setting]

►SB Porting Configuration

SATA RAID ROM	[Legacy ROM]
DCI enable(HDCIEN)	[Disabled]
DCI Auto Detect Enabled	[Enabled]
Debug Port Selection	[Legacy UART]
GNSS	[Disabled]
PCH LAN Controller	[Enabled]
LAN PHY Drives LAN_WAKE#	[Disabled]
Sensor Hub Type	[None]
DeepSx Power Policies	[Disabled]
LAN Wake From DeepSx	[Enabled]
Wake on LAN	[Enabled]
SLP_LAN# Low on DC Power	[Enabled]
K1 off	[Enabled]
Wake on WLAN Enable	[Disabled]
Disable DSX ACPRESENT PullDown	[Disabled]
CLKRUN# Logic	[Enabled]
Serial IRQ Mode	[Continuous]
Port 61h Bit-4 Emulation	[Enabled]
High Precision Timer	[Enabled]
State After G3	[S5 State]
Port 80h Redirection	[LPC Bus]
Enhance Port 80h LPC Decoding	[Enabled]
Compatible Revision ID	[Disabled]

PCH Cross Throttling	[Enabled]
Disable Energy Reporting	[Disabled]
Capsule Reset Type	[Capsule S3 Resume]
Pcie Pll SSC	[Auto]
IOAPIC 24-119 Entries	[Enabled]
Unlock PCH P2SB	[Disabled]
PMC READ DISABLE	[Enabled]

3.6 Security Settings

3.6.1 Administrator Password

3.6.2 User Password

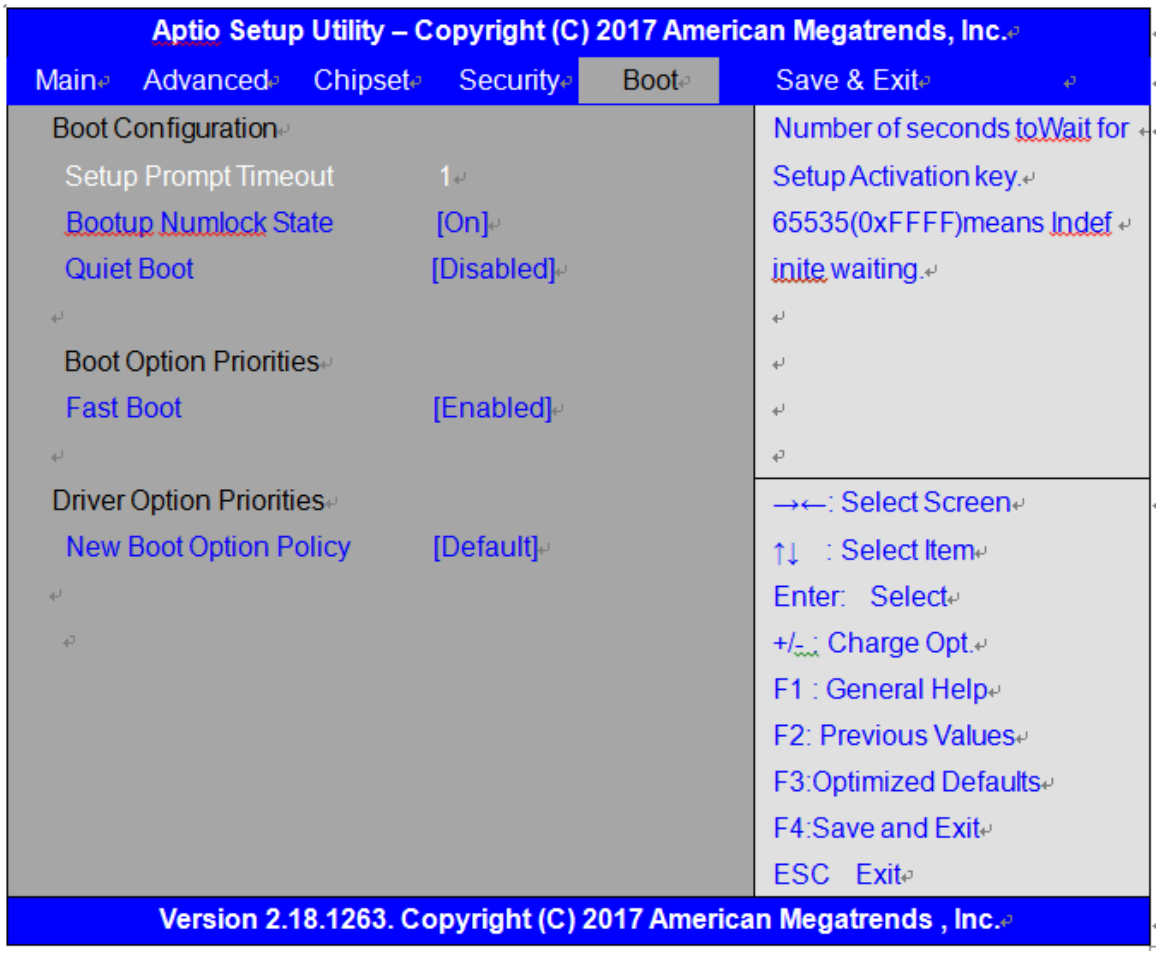
Type the password with up to 20 characters and then press ≺Enter≻ key. This will clear all previously typed CMOS passwords. You will be requested to confirm the password. Type the password again and press ≺Enter≻ key. You may press ≺Esc≻ key to abandon password entry operation.

To clear the password, just press ≺Enter≻ key when password input window pops up. A confirmation message will be shown on the screen as to whether the password will be disabled. You will have direct access to BIOS setup without typing any password after system reboot once the password is disabled.

Once the password feature is used, you will be requested to type the password each time you enter BIOS setup. This will prevent unauthorized persons from changing your system configurations.

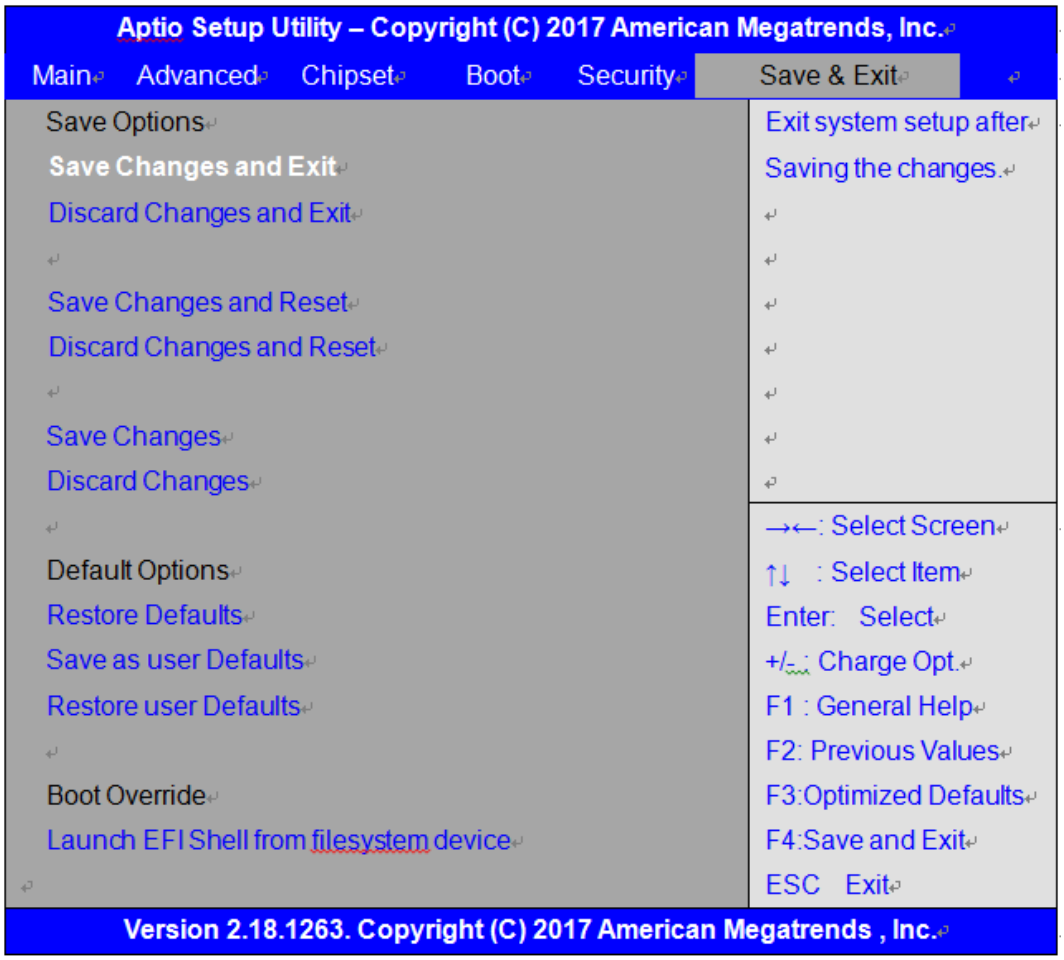
Also, the feature is capable of requesting users to enter the password prior to system boot to control unauthorized access to your computer. Users may enable the feature in Security Option of Advanced BIOS Features. If Security Option is set to System, you will be requested to enter the password before system boot and when entering BIOS setup; if Security Option is set to Setup, you will be requested for password for entering BIOS setup.

3.7 Boot Settings



Setup Prompt Timeout	1
Bootup Numlock State	[On]
Quiet Boot	[Disabled]
Boot Option Priorities	
Fast Boot	[Disabled]
Driver Option Priorities	
New Boot Option Policy	[Default]

3.8 Save & Exit Settings



Save Changes and Exit

Save & Exit Setup save Configuration and exit ?

[Yes]

[No]

Discard Changes and Ext

Exit Without Saving Quit without saving?

[Yes]

[No]

Save Changes and Reset

Reset the system affer Saving The changes?

[Yes]

[No]

Discard Changes and Reset

Reset system setup without Saving any changes?

[Yes]

[No]

Save Changes

Save Setup done so far to any of the setup options?

[Yes]

[No]

Discard Changes

Discard Changes done so far to any of the setup options?

[Yes]

[No]

Restore Defaults

Restore /Load Defaults values for all the setup options?

[Yes]

[No]

Save as user Defaults

Save the changes done so far as User Defaults?

[Yes]

[No]

Restore user Defaults

Restore the User Defaults to all the setup options?

[Yes]

[No]

Boot Override

Launch EFI Shell from filesystem device

WARNING Not Found

[ok]

Chapter 4 Installation of Drivers

This chapter describes the installation procedures for software and drivers under the windows 8.1 & 10. The software and drivers are included with the motherboard. The contents include **Intel H170 , Graphics 530 chipset driver, Audio driver, IntelR management engine interface, and DPTF Driver Installation instructions are given below.**

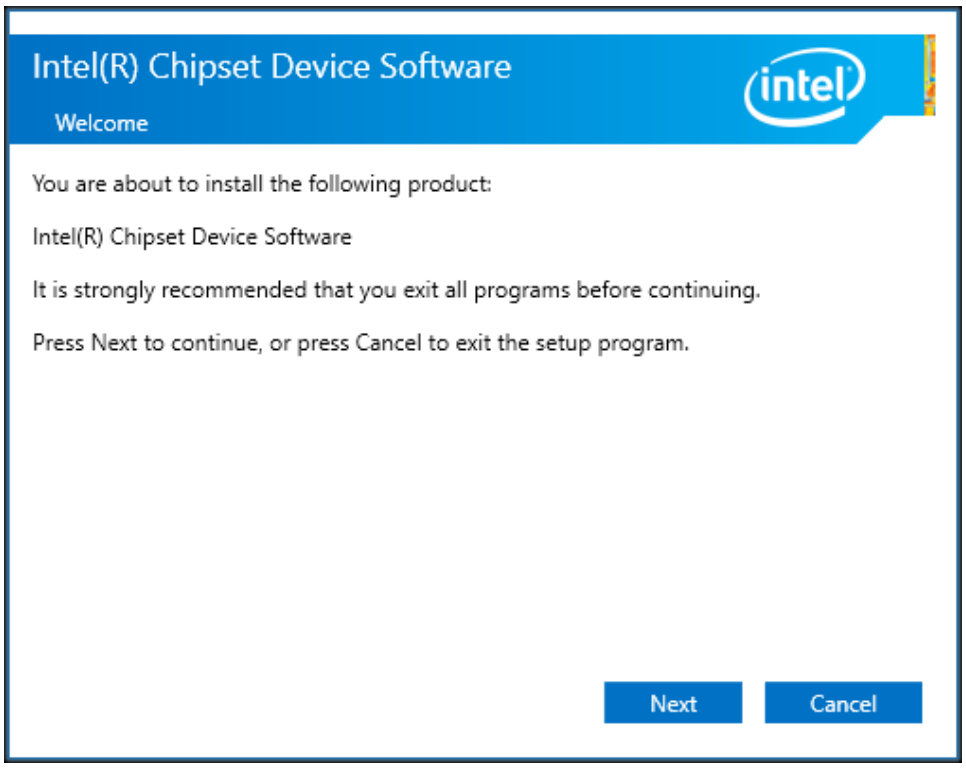
Important Note:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the installation of drivers.

4.1 Intel H170 Chipset

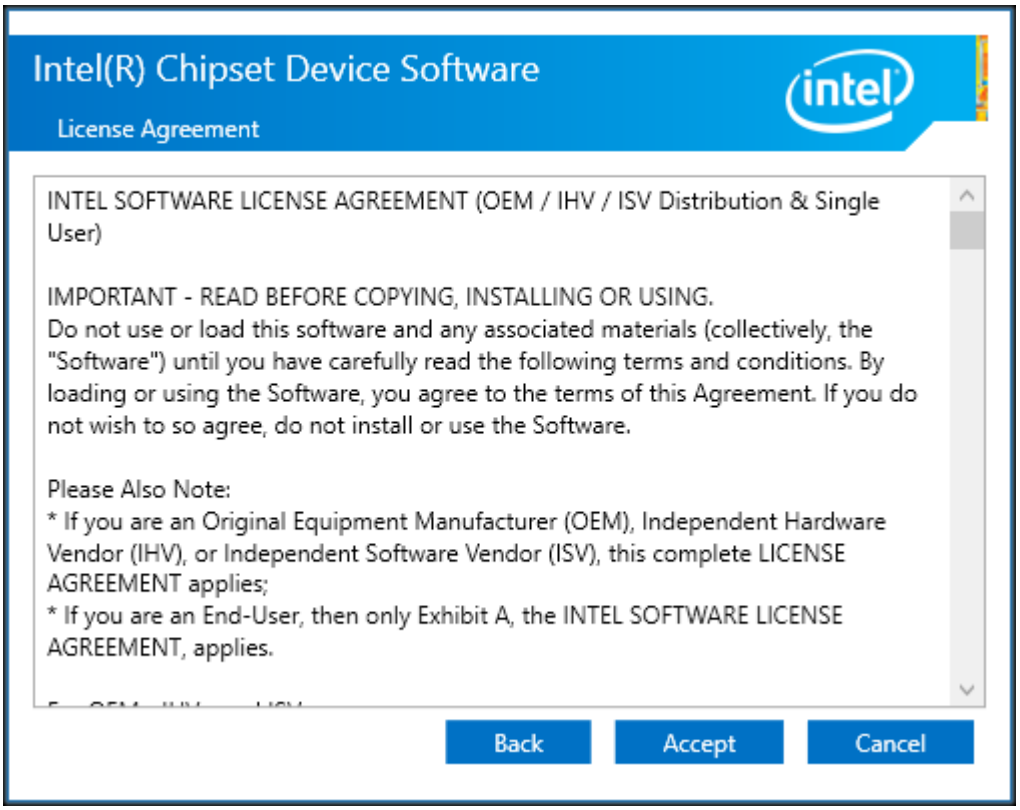
To install the Intel H170 chipset driver, please follow the steps below.

Step 1. Select **Intel H170 Chipset** from the list

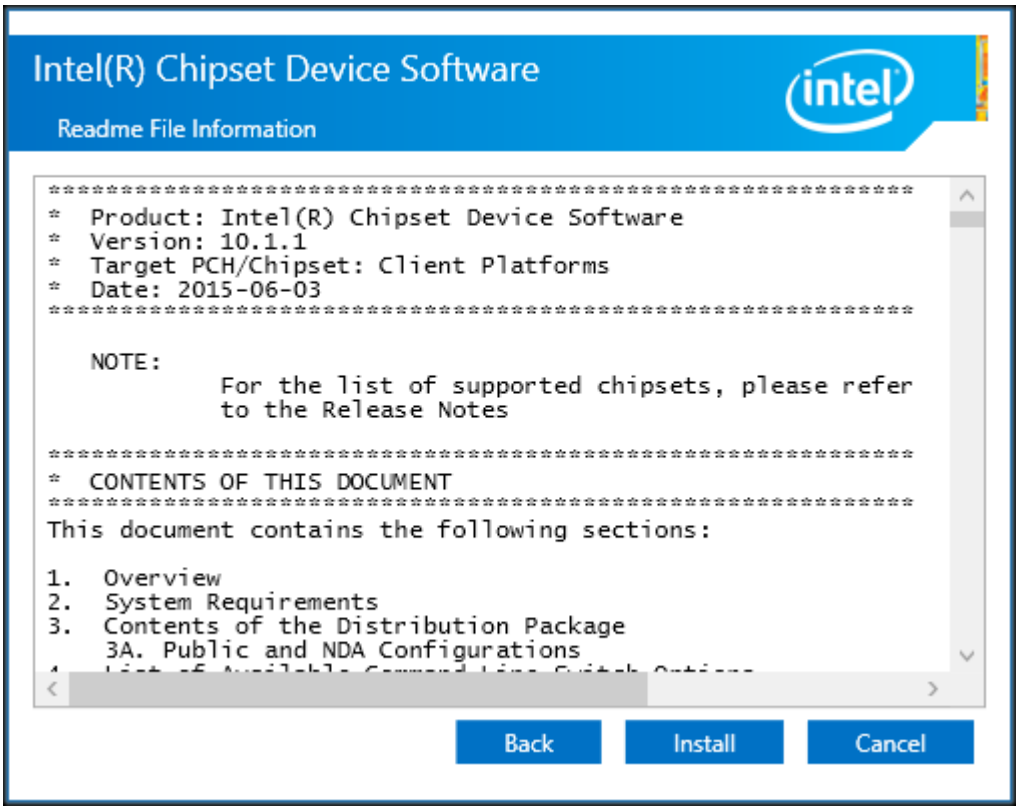
Step 2. Here is welcome page. Please make sure you save and exit all programs before install**.** Click **Next.**



Step 3. Read the license agreement. Click **Accept** to accept all of the terms of the license agreement.



Step 4. Click **Install** to begin the installation.



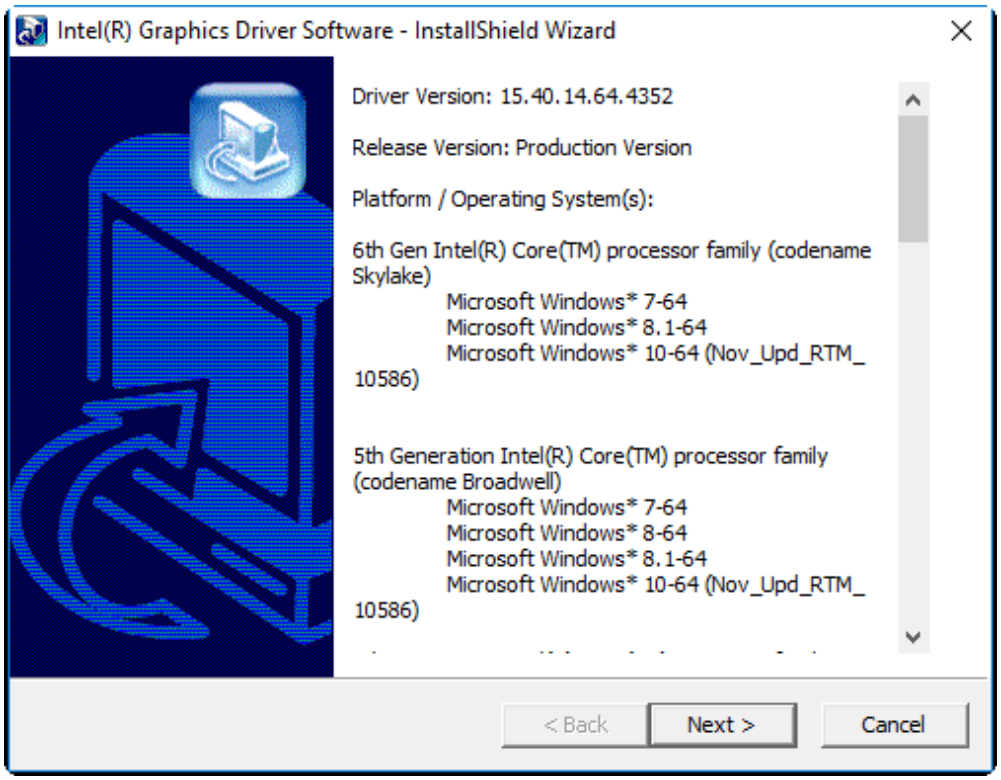
Step 5. Select **Restart Now** to reboot your computer for the changes to take effect.

4.2 Intel® HD Graphics 530 Chipset

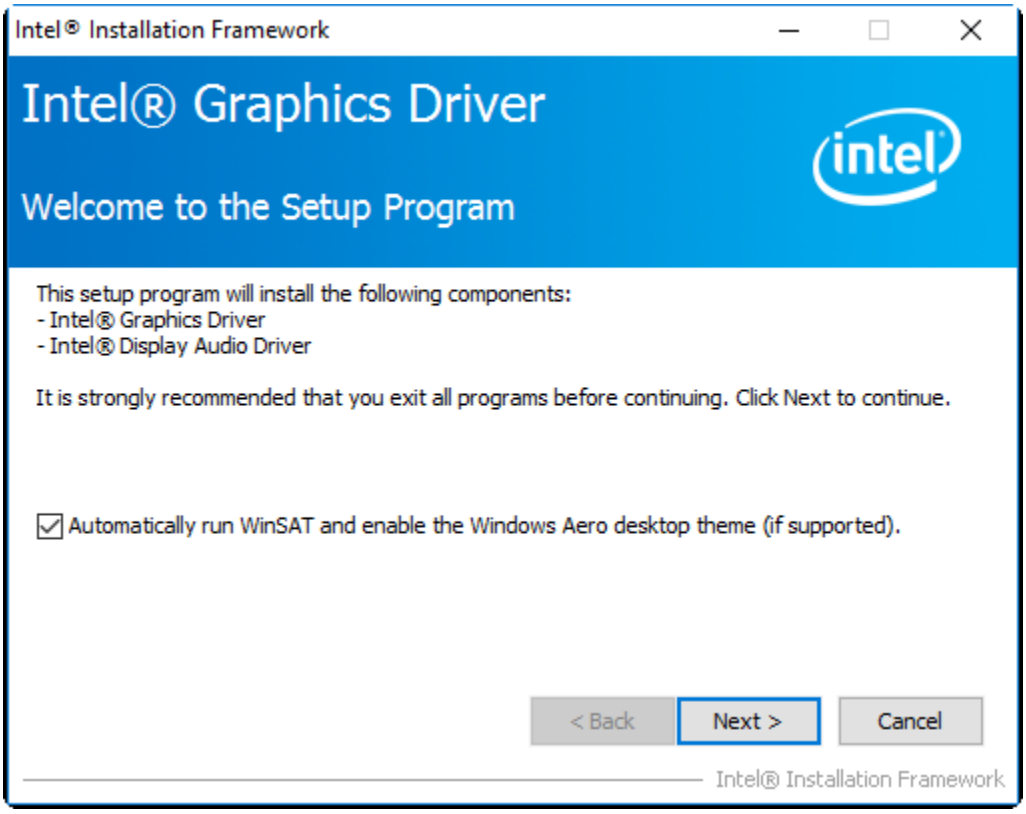
To install the Intel® HD Graphics 530 Chipset, please follow the steps below.

Step 1. Select **Intel® HD Graphics 530 Chipset** from the list**.**

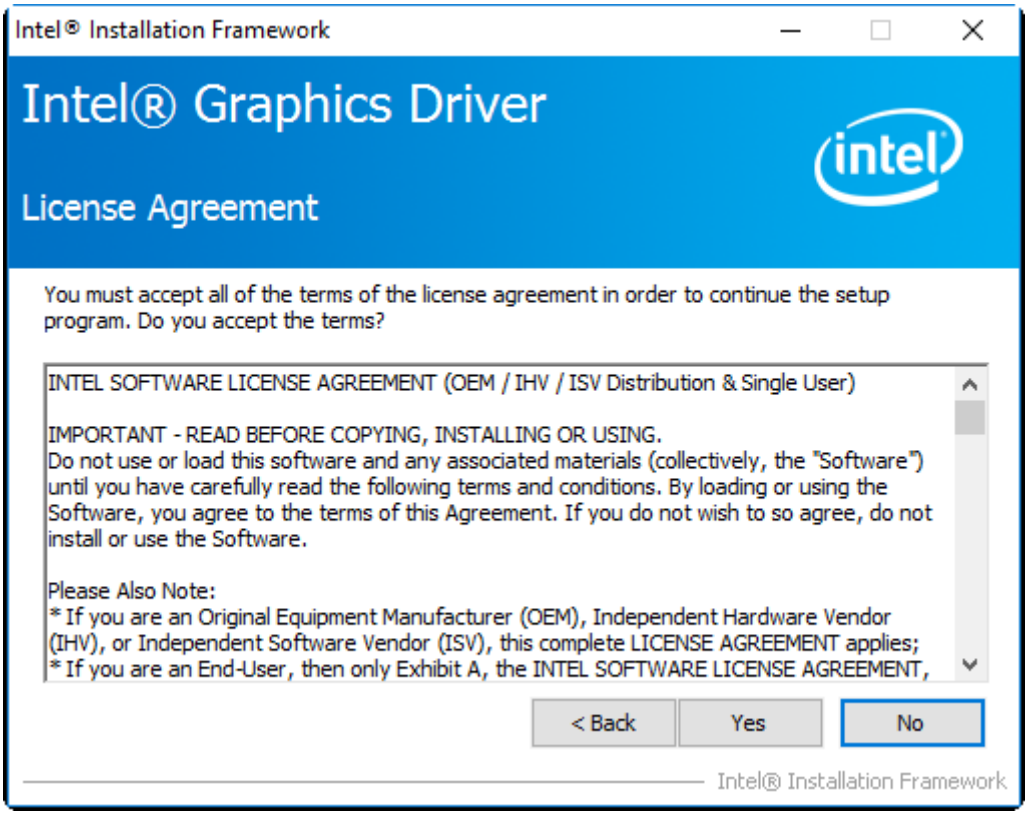
Step 2. . Click **Next.**



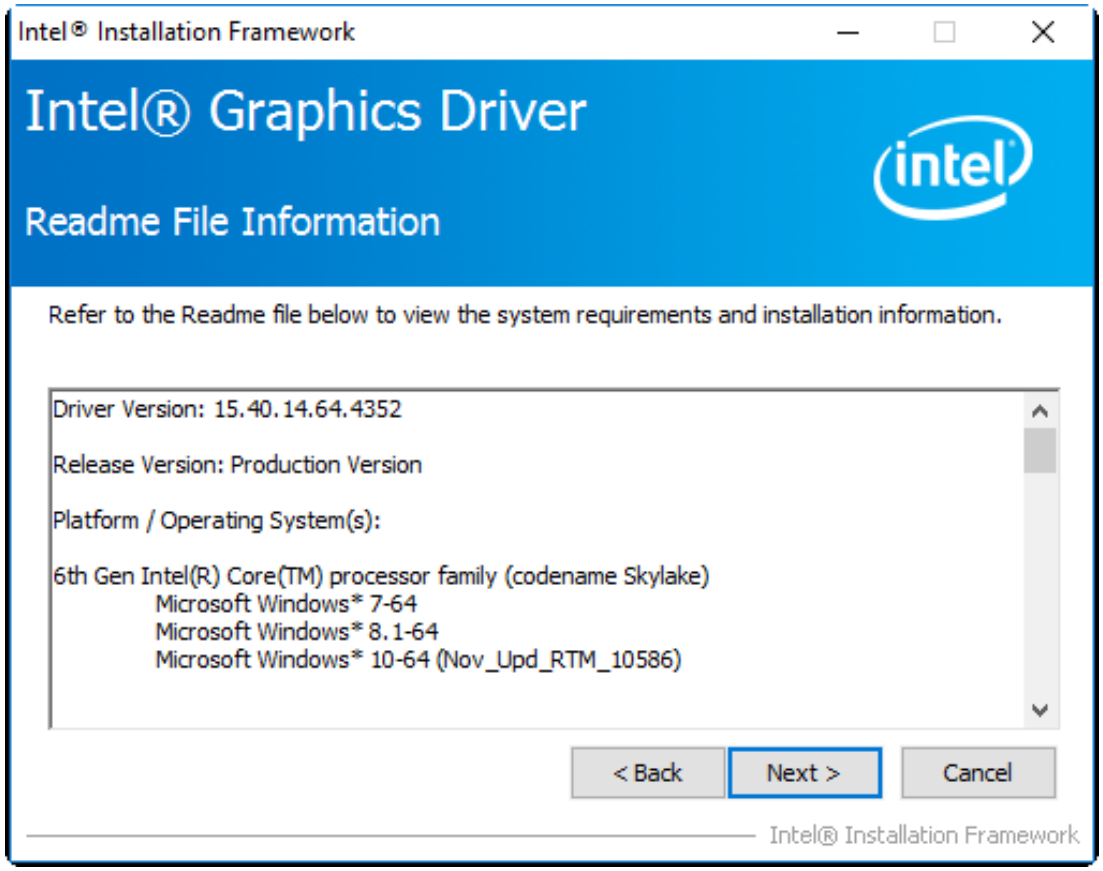
Step 3. Choose **automatically run** function and Click **Next** to setup program.



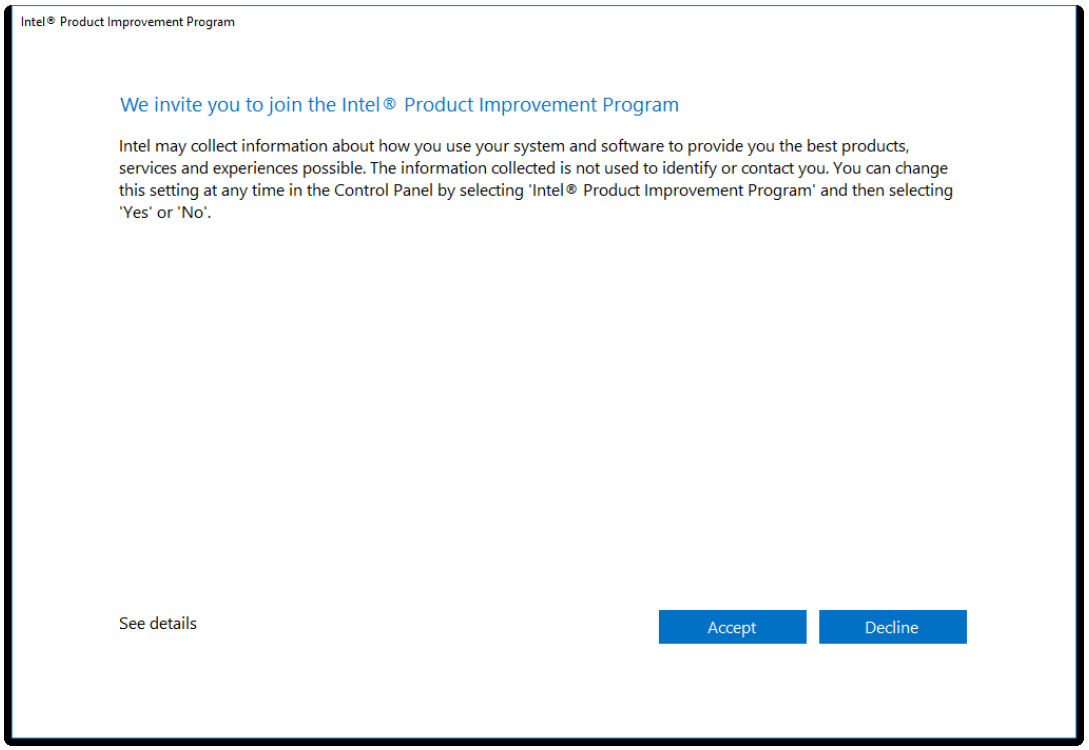
Step 4. Read the license agreement. Click **Yes** to accept all of the terms of the license agreement.



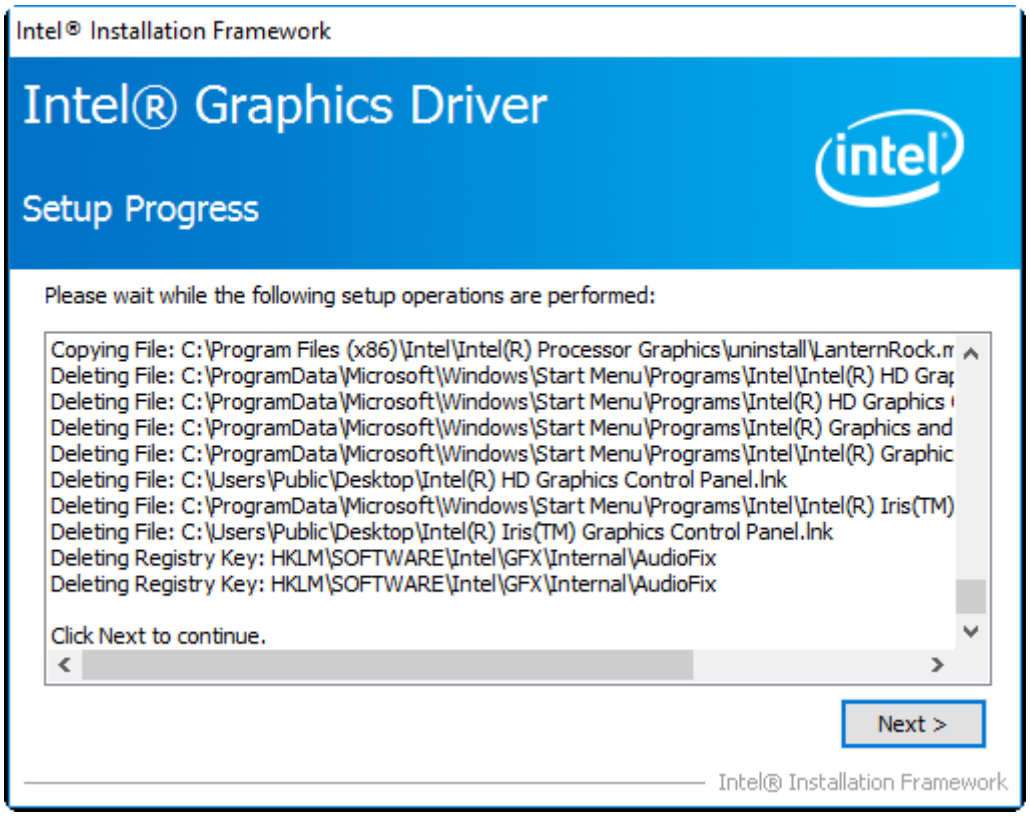
Step 5. Click **Next** to continue.



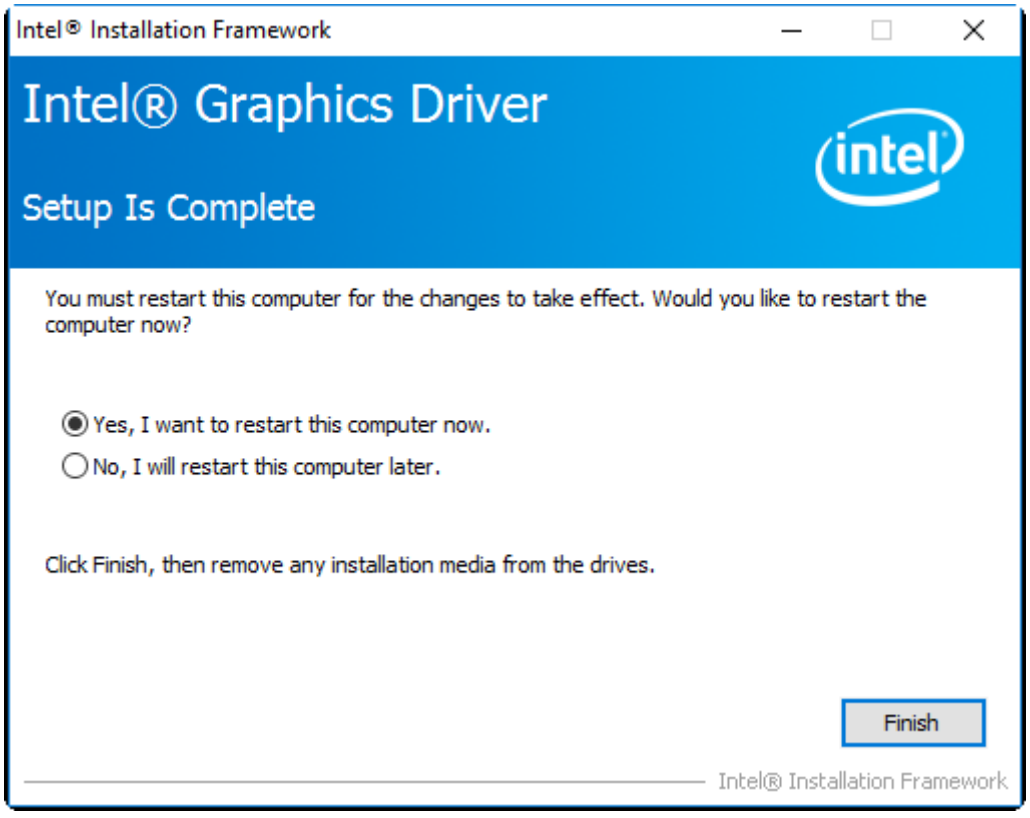
Step 6. Here is Intel product improvement program information, you can choose **Accept** or **Decline** by your option and installation will go to next step.



Step 7. Click **Next** to continue the program.



Step 8. Select **Yes, I want to restart this computer now**. Click **Finish** to complete installation.

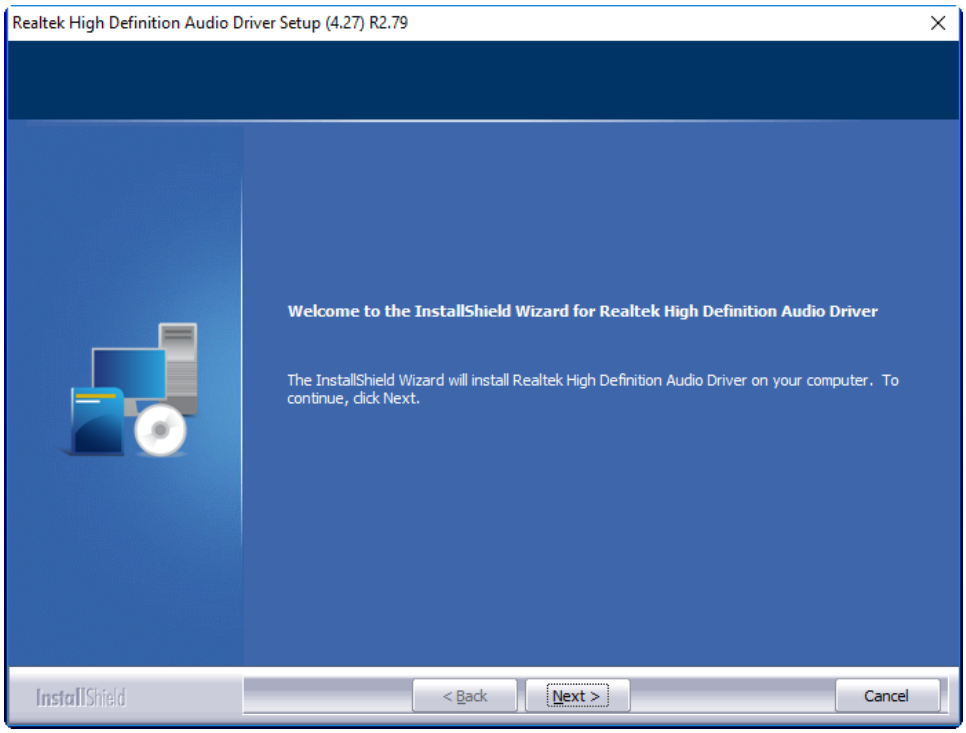


4.3 Realtek ALC662 HD Audio Driver Installation

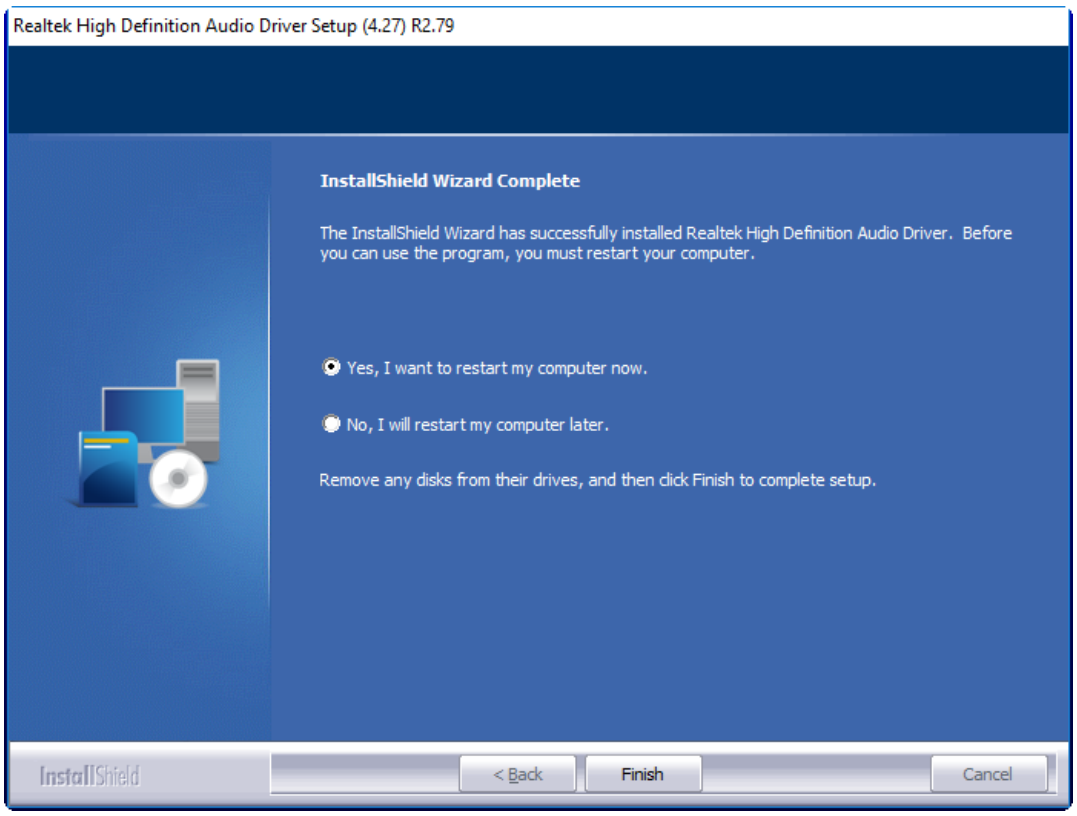
To install the Realtek ALC662 HD Audio Driver, please follow the steps below.

Step 1. Select **Realtek AL662 HD Audio Driver** from the list

Step 2. Click **Next** to continue.



Step 3. Click **Yes, I want to restart my computer now**. Click **Finish** to complete the installation.

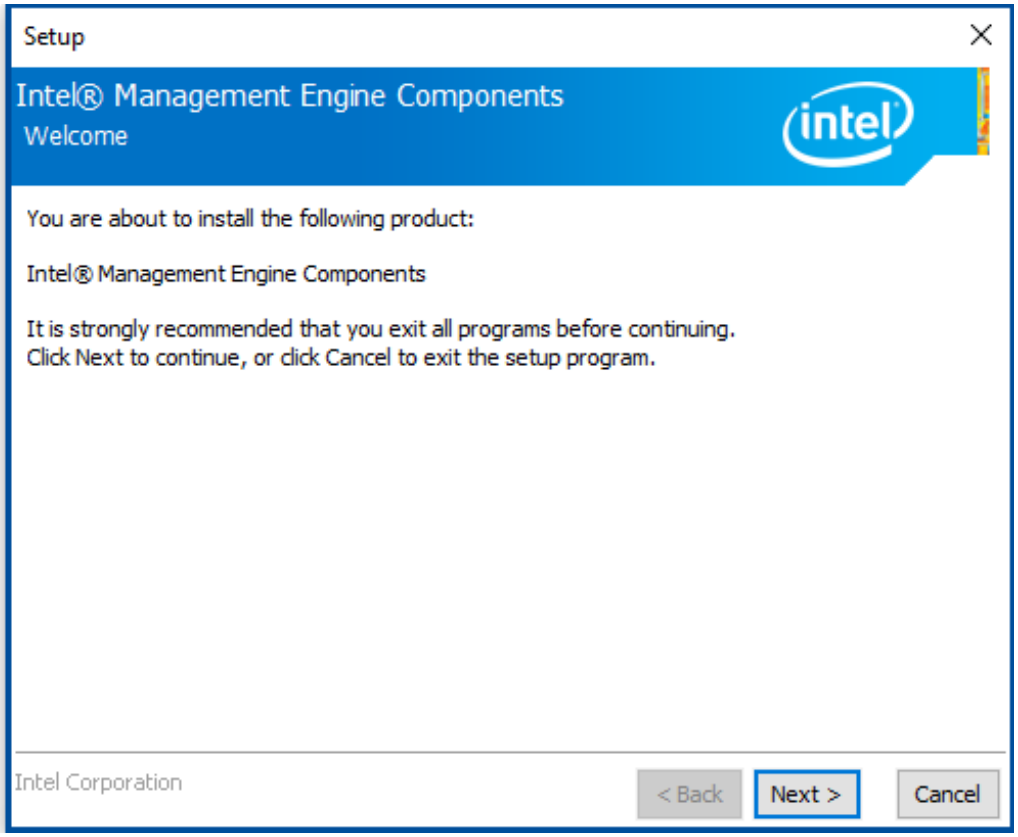


4.4 Intel® Management Engine Interface

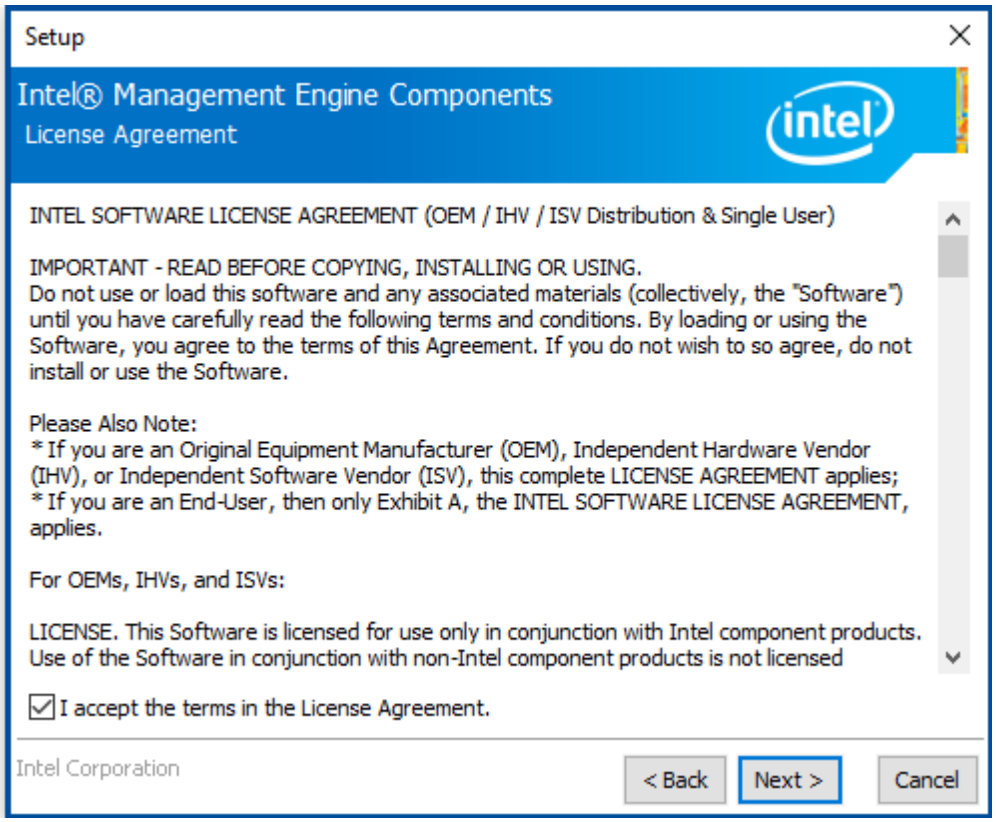
To install the Intel® Management Engine Interface, please follow the steps below.

Step 1. Select **Intel® Management Engine Interface** from the list

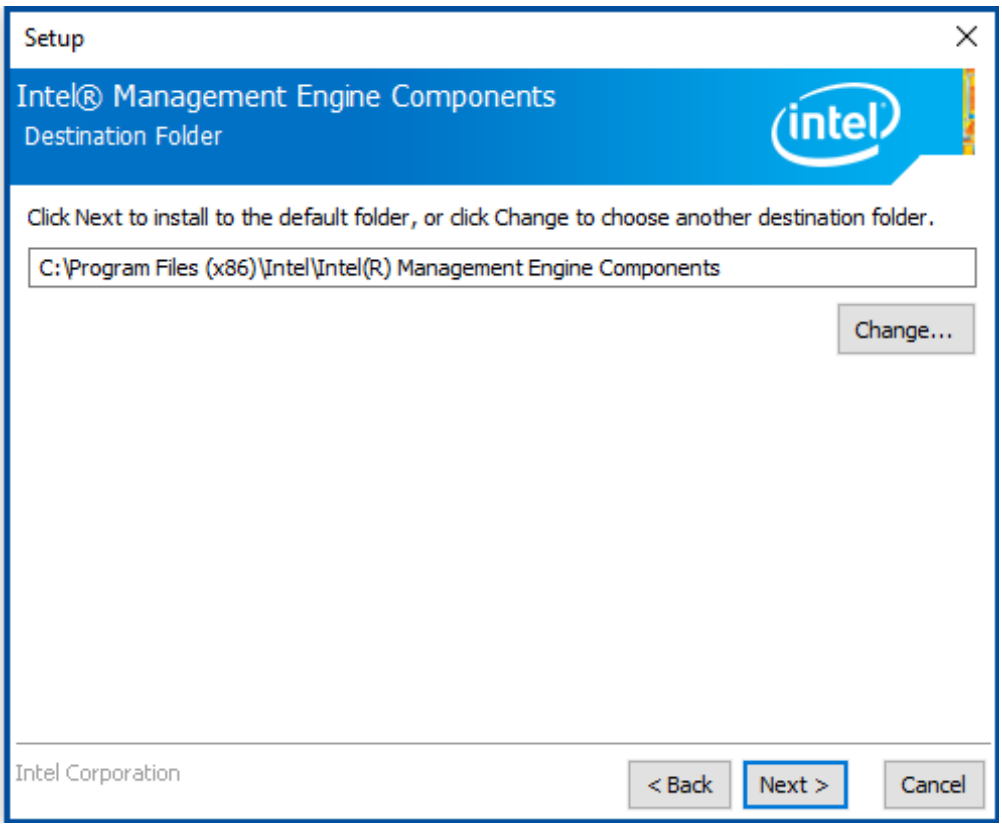
Step 2. Select setup language you need. Click **Next** to continue.



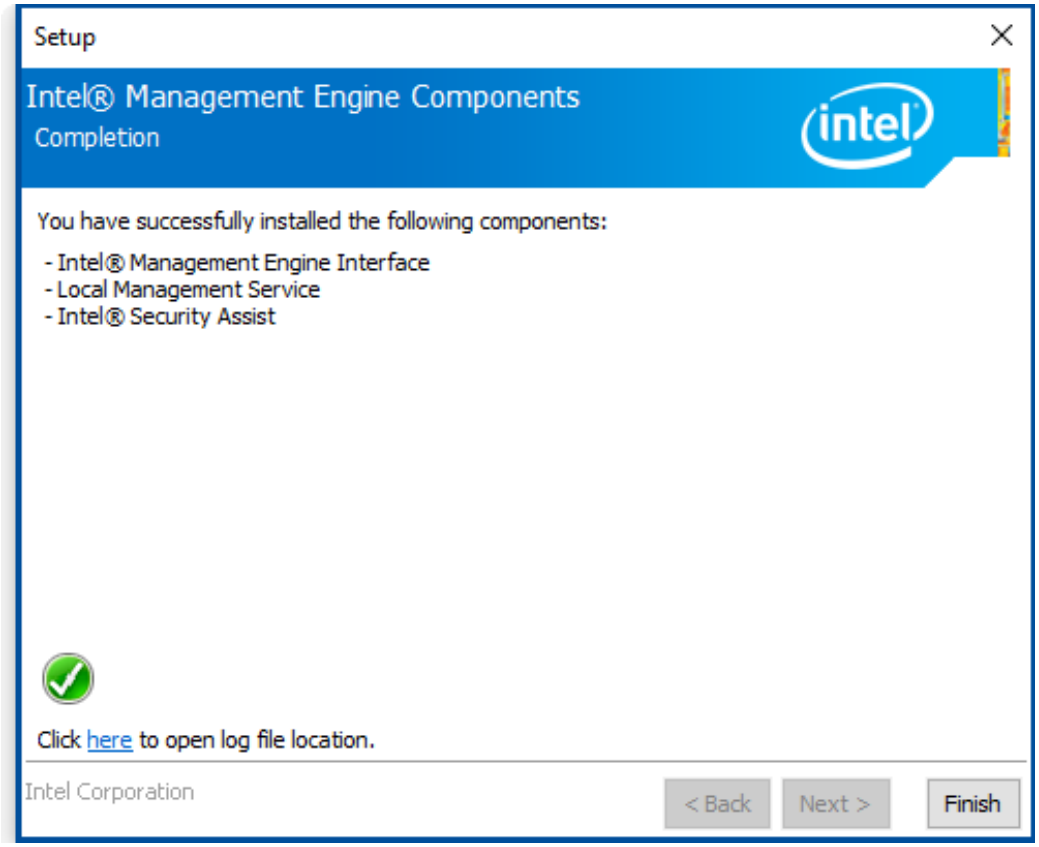
Step 3. Choose **I accept the terms in the License Agreement** and click **Next** to begin the installation.



Step 4. Click **Next** to continue.



Step 5. Click **Finish** to complete the installation.

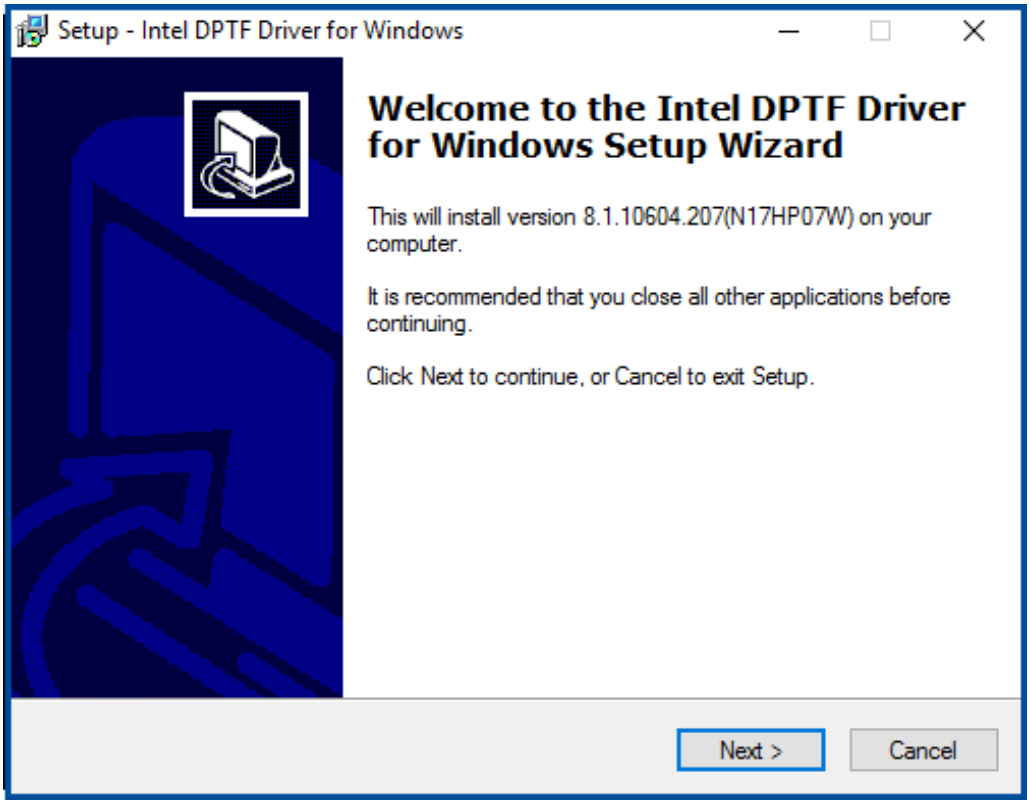


4.5 DPTF Driver

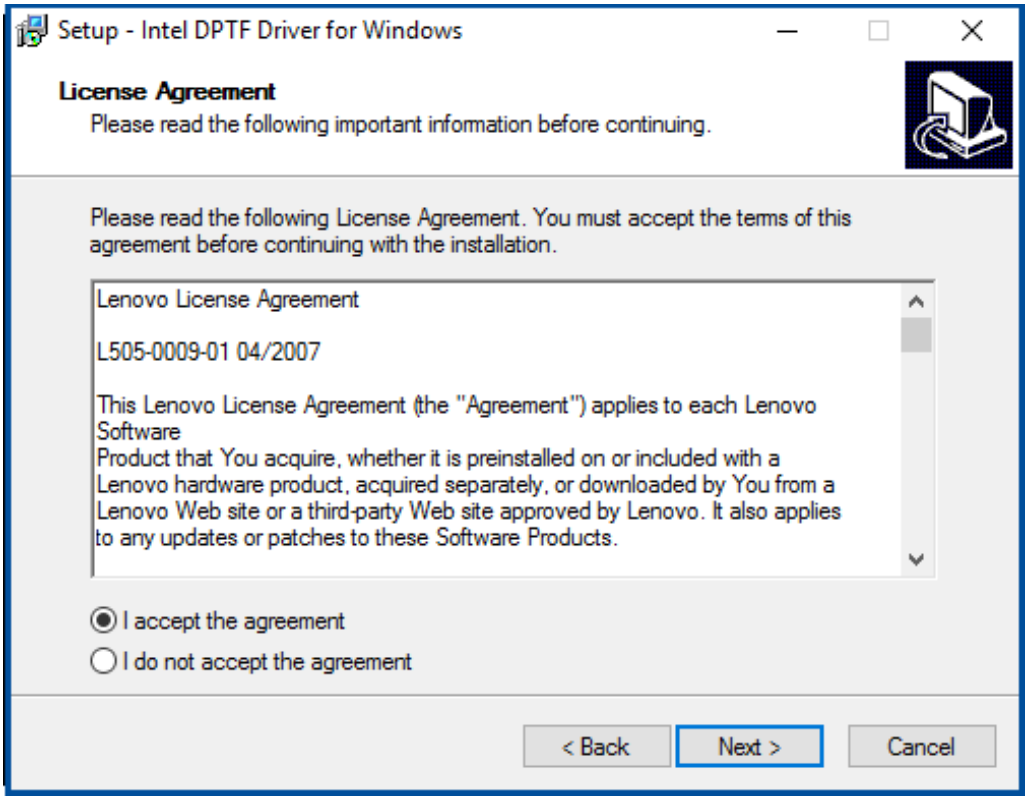
To install the DPTF Driver, please follow the steps below.

Step 1. Select **DPTF Driver** from the list

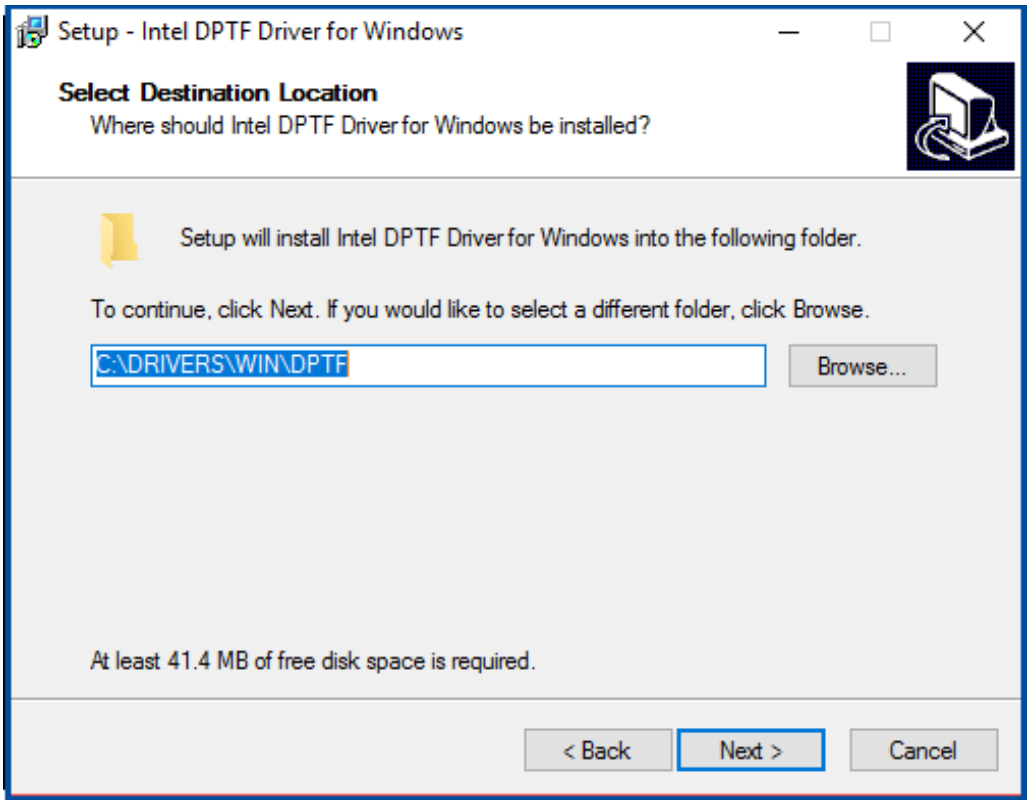
Step 2. Click **Next** to continue.



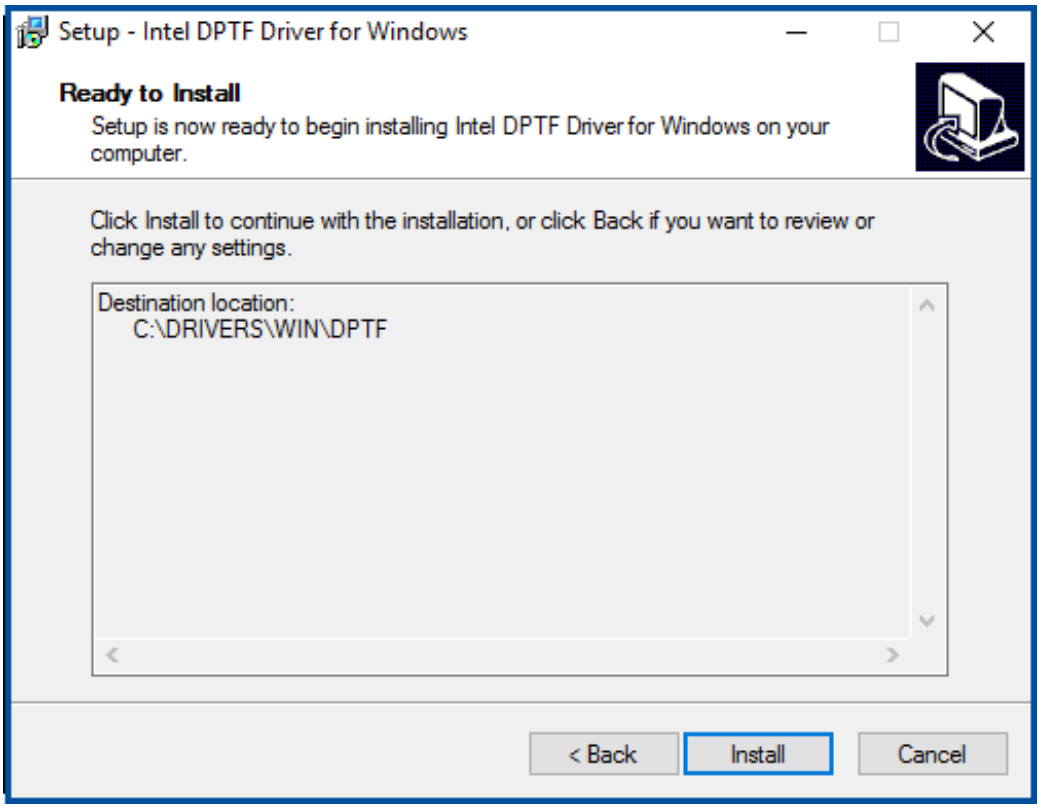
Step 3. Read the license agreement. Choose **Accept** and click **Next** to accept all of the terms of the license agreement.



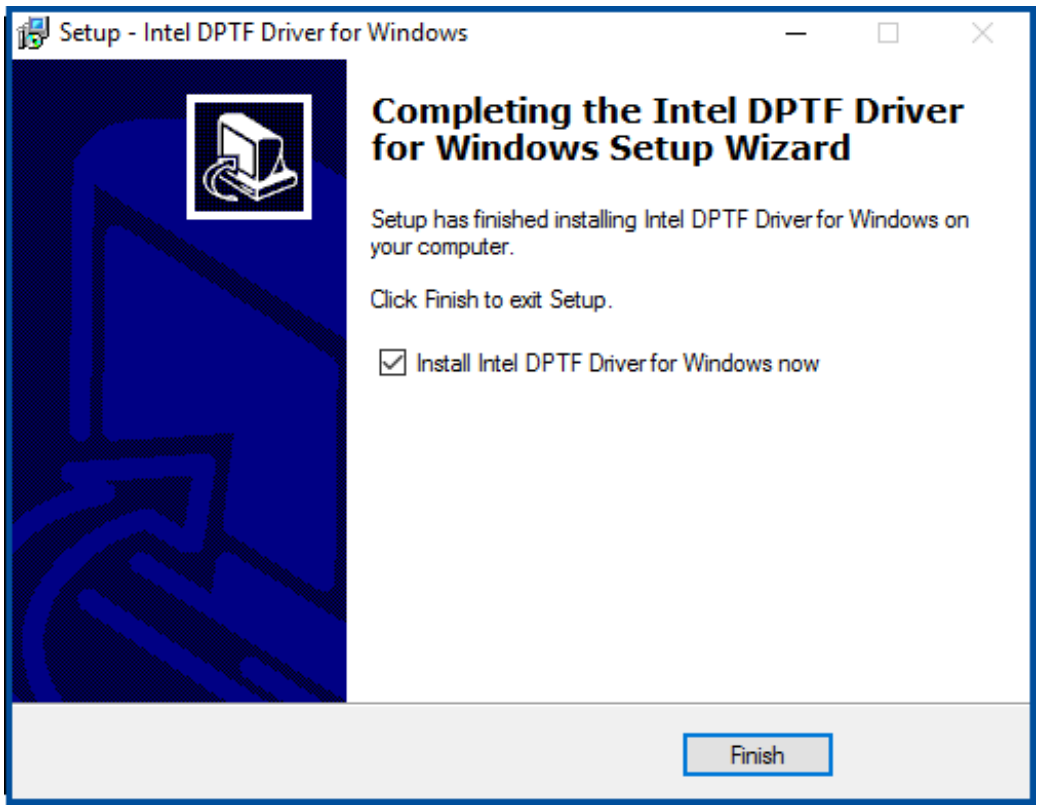
Step 4. Select destination location by your option and click **Next** to continue.



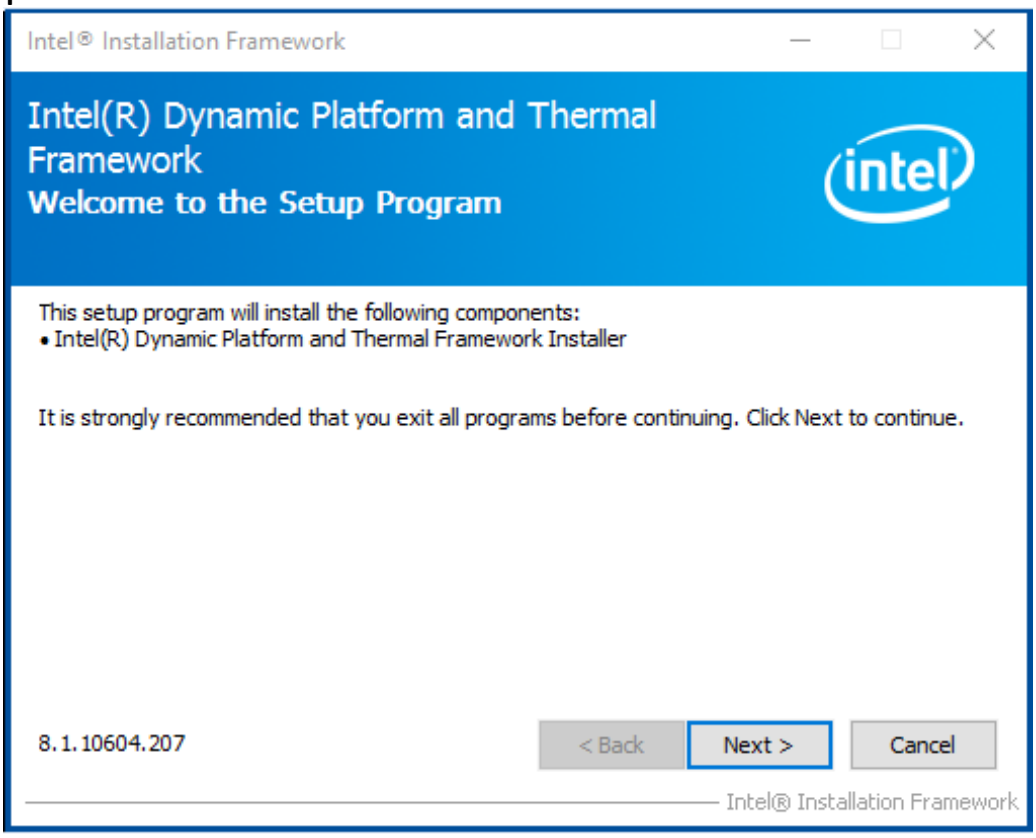
Step 5. Click **Install** to continue the installing.



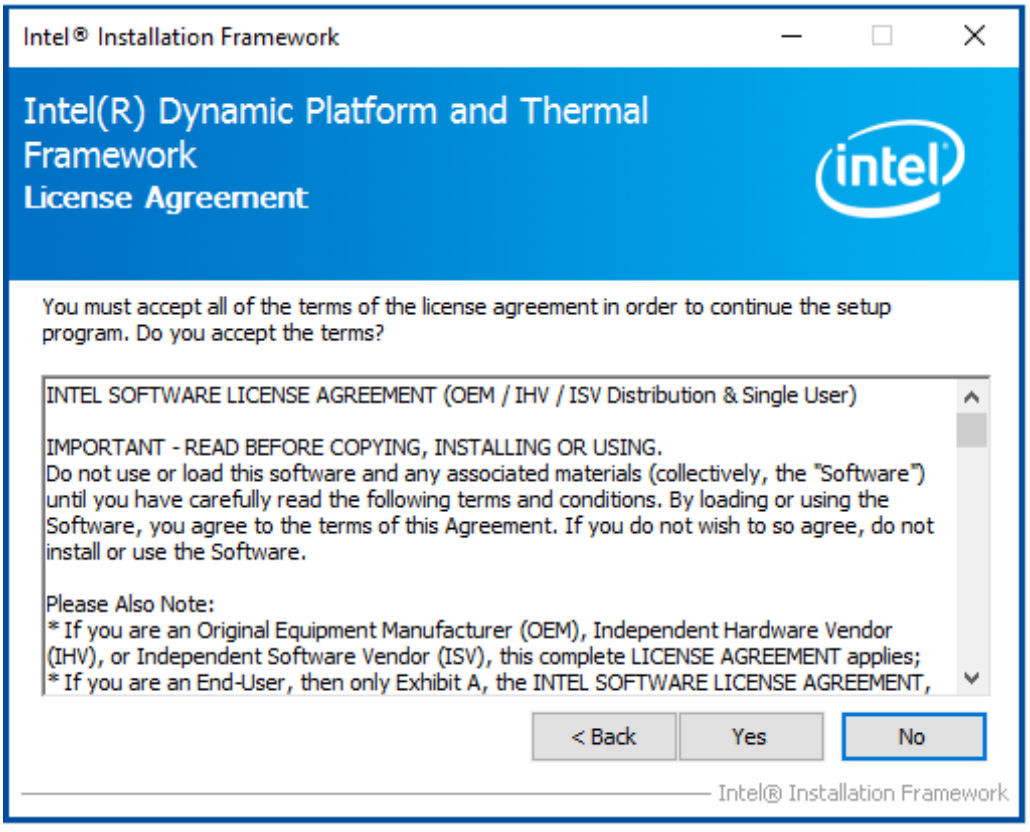
Step 6. Click **Finish** to complete the installation and start install Intel DPTF driver for Windows.



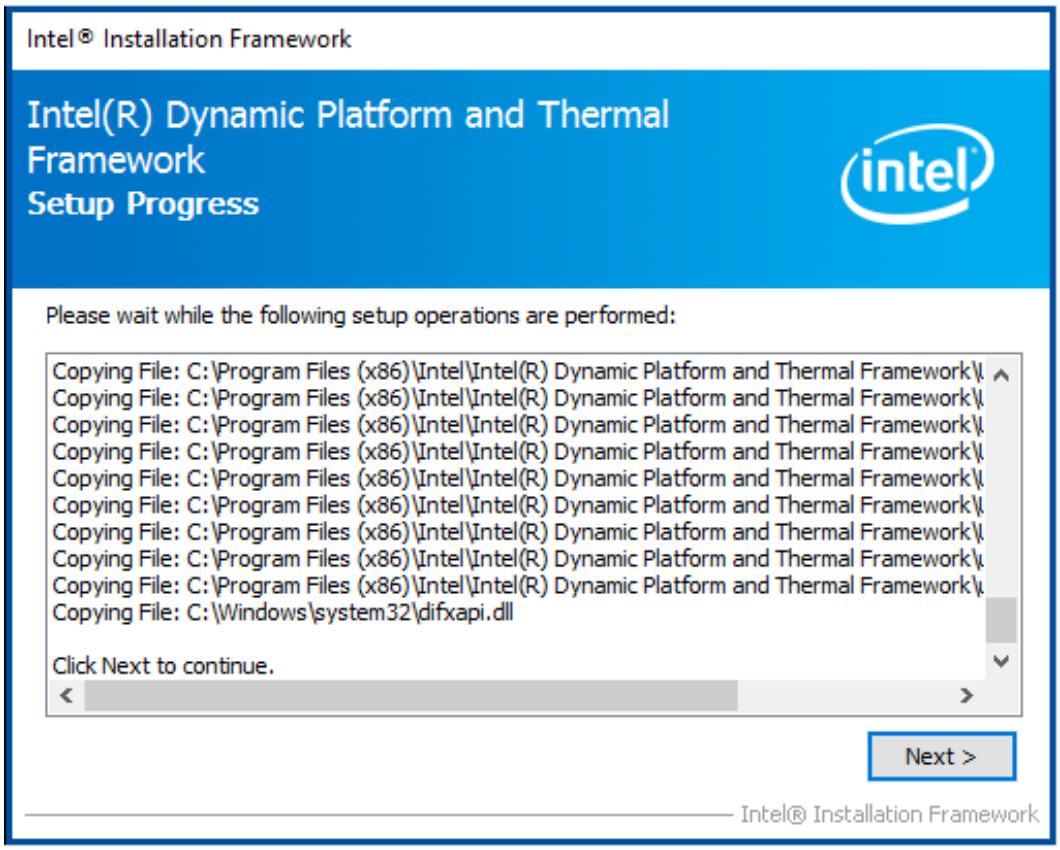
Step 7. Click **Next** to start the installation.



Step 8. Read the license agreement. Click **Yes** to accept all of the terms of the license agreement.



Step 9. Click **Next** to continues.



Step 10. Click **Finish** to complete the installation.