# Approval Sheet

| | |
|---|---|
| **Customer** | |
| **Product Number** | **M0SB-12PB6C03-J** |
| **Module speed** | **PC-133** |
| **Pin** | **144 Pin** |
| **CAS Latency** | **CL-3** |
| **SDRAM Operating Temp.** | **0 °C ~ 70 °C** |
| **Date** | **2nd November 2023** |

Rev 1.2



The Total Solution For Industrial Flash Storage

# 1. Features

Key Parameter

| Industry Nomenclature | Speed Grade | Data Rate MT/s | | | tRCD (ns) | tRP (ns) | tRC (ns) |
|---|---|---|---|---|---|---|---|
| | | CL=2 | CL=2.5 | CL=3 | | | |
| **PC-133** | **B** | 100 | - | 133 | 20 | 20 | 65 |

- Single Pulsed RAS- interface
- Fully Synchronous to positive CLK edge
- 4 banks controlled by BA0 & BA1
- Multiple Burst Read with single write option
- Automatic and controlled precharge command
- Auto refresh (CBR) and Self-Refresh
- Standard 144-pin Memory Module
- Intend for 133 MHz applications
- Inputs and Outputs are LVTTL compatible
- VDD=VDDQ= 3.3 Volt ± 0.3
- Serial Presence Detect with EEPROM
- SDRAM Operation Temperature *(Note 1)*
  - 0°C ≤ $T_A$ ≤ +70°C
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency:2, 3
- RoHS Compliant *(Section 14)*

Note:*1. The refresh rate is required to double when $T_A$ Exceeds70°C.*

## 2. SDRAM Environmental Requirements

SDR SDRAMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

| Symbol | Parameter | Rating | Units | Notes |
|---|---|---|---|---|
| $T_{OPR}$ | Operating Temperature (ambient) | 0 to +70 | °C | 1 |
| $T_{STG}$ | Storage Temperature | -55 to +150 | °C | |

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the SDR DRAM component specification.

## 3. Ordering Information

| SDR SODIMM | | | | | | |
|---|---|---|---|---|---|---|
| Part Number | Density | Speed | DIMM Organization | Number of DRAM | Number of rank | ECC |
| **M0SB-12PB6C03-J** | 512MB | PC-133 | 64Mx64 | 8 | 2 | N |

## 4. Pin Configurations (Front side/Back side)

| Pin | Front | Pin | Back | Pin | Front | Pin | Back | Pin | Front | Pin | Back |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 1 | $V_{SS}$ | 2 | $V_{SS}$ | 51 | DQM14 | 52 | DQM46 | 95 | DQ21 | 96 | DQ53 |
| 3 | DQ0 | 4 | DQ32 | 53 | DQM15 | 54 | DQM47 | 97 | DQ22 | 98 | DQ54 |
| 5 | DQ1 | 6 | DQ33 | 55 | $V_{SS}$ | 56 | $V_{SS}$ | 99 | DQ23 | 100 | DQ55 |
| 7 | DQ2 | 8 | DQ34 | 57 | NC | 58 | NC | 101 | $V_{DD}$ | 102 | $V_{DD}$ |
| 9 | DQ3 | 10 | DQ35 | 59 | NC | 60 | NC | 103 | A6 | 104 | A7 |
| 11 | $V_{DD}$ | 12 | $V_{DD}$ | Voltage Key | | | | 105 | A8 | 106 | BA0 |
| 13 | DQ4 | 14 | DQ36 | | | | | 107 | $V_{SS}$ | 108 | VSS |
| 15 | DQ5 | 16 | DQ37 | | | | | 109 | A9 | 110 | BA1 |
| 17 | DQ6 | 18 | DQ38 | 61 | **CLK0 | 62 | **CKE0 | 111 | A10/AP | 112 | A11 |
| 19 | DQ7 | 20 | DQ39 | 63 | $V_{DD}$ | 64 | $V_{DD}$ | 113 | $V_{DD}$ | 114 | $V_{DD}$ |
| 21 | $V_{SS}$ | 22 | $V_{SS}$ | 65 | $\overline{RAS}$ | 66 | $\overline{CAS}$ | 115 | DQM2 | 116 | DQM6 |
| 23 | DQM0 | 24 | DQM4 | 67 | $\overline{WE}$ | 68 | **CKE1 | 117 | DQM3 | 118 | DQM7 |
| 25 | DQM1 | 26 | DQM5 | 69 | **$\overline{CS0}$ | 70 | A12 | 119 | $V_{SS}$ | 120 | $V_{SS}$ |
| 27 | $V_{DD}$ | 28 | $V_{DD}$ | 71 | **$\overline{CS1}$ | 72 | *A13 | 121 | DQ24 | 122 | DQ56 |
| 29 | A0 | 30 | A3 | 73 | DU | 74 | **CLK1 | 123 | DQ25 | 124 | DQ57 |
| 31 | A1 | 32 | A4 | 75 | $V_{SS}$ | 76 | $V_{SS}$ | 125 | DQ26 | 126 | DQ58 |
| 33 | A2 | 34 | A5 | 77 | NC | 78 | NC | 127 | DQ27 | 128 | DQ59 |
| 35 | $V_{SS}$ | 36 | $V_{SS}$ | 79 | NC | 80 | NC | 129 | $V_{DD}$ | 130 | $V_{DD}$ |
| 37 | DQ8 | 38 | DQ40 | 81 | $V_{DD}$ | 82 | $V_{DD}$ | 131 | DQ28 | 132 | DQ60 |
| 39 | DQ9 | 40 | DQ41 | 83 | DQ16 | 84 | DQ48 | 133 | DQ29 | 134 | DQ61 |
| 41 | DQ10 | 42 | DQ42 | 85 | DQ17 | 86 | DQ49 | 135 | DQ30 | 136 | DQ62 |
| 43 | DQ11 | 44 | DQ43 | 87 | DQ18 | 88 | DQ50 | 137 | DQ31 | 138 | DQ63 |
| 45 | $V_{DD}$ | 46 | $V_{DD}$ | 89 | DQ19 | 90 | DQ51 | 139 | $V_{SS}$ | 140 | $V_{SS}$ |
| 47 | DQ12 | 48 | DQ44 | 91 | $V_{SS}$ | 92 | $V_{SS}$ | 141 | SDA | 142 | SCL |
| 49 | DQ13 | 50 | DQ45 | 93 | DQ20 | 94 | DQ52 | 143 | $V_{DD}$ | 144 | $V_{DD}$ |

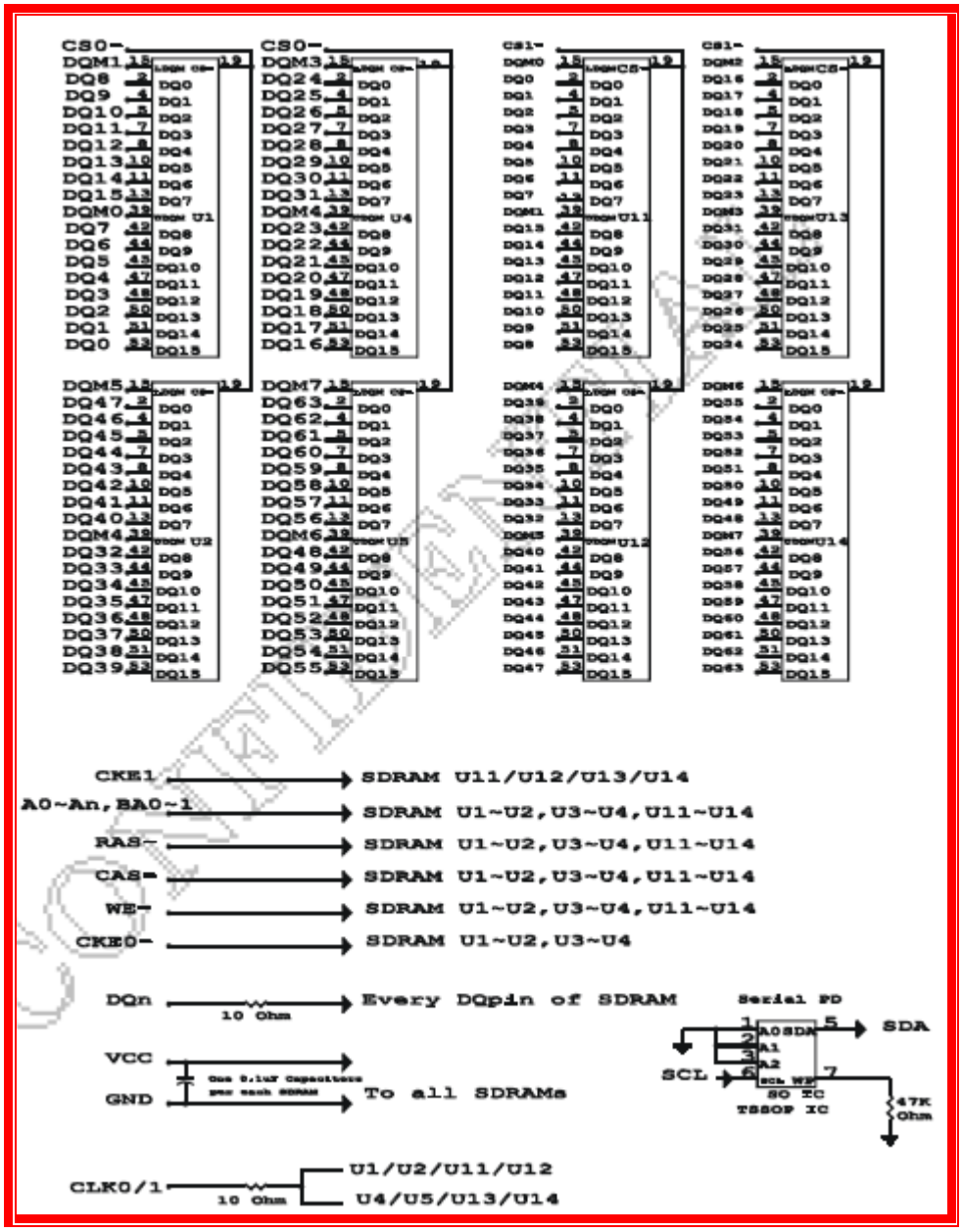
## 5. Architecture

Pin Definition

| Pin Name | Description | Pin Name | Description |
|---|---|---|---|
| A0 - A12 | SDRAM address bus | CKE0 – CKE1 | SDRAM clock enable lines |
| SA0 - SA1 | SDRAM Bank Address Inputs | SCL | Serial Presence Detect Clock Input |
| RAS- | SDRAM row address strobe | SDA | Serial Presence Detect Data input/output |
| CAS- | SDRAM column address strobe | DQM0 – DQM7 | SDRAM data masks |
| WE- | SDRAM write enable | $V_{DD}$ | Power Supply |
| CS0- - CS1- | Chip select input | GND | Ground |
| CLK0 – CLK1 | SDRAM Clock input. | DU | Spare Pin |
| D0 – D63 | DIMM memory data bus | NC | No connection |

## 6. Function Block Diagram:

- (512MB, 2 Ranks, 32Mx16 SDR SDRAMs)



## 7. Absolute Maximum Ratings

| Parameter | Rating | Units |
|---|---|---|
| Storage Temperature | -55 to 150 | °C |
| Input/output voltage | -0.3 to VDD | V |
| Power supply voltage | -0.3 to +4.6 | V |

**Note**: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 8. DC Operating Conditions

- DC Electrical Operating Conditions

| Symbol | Parameter | Min | Typ. | Max | Units | Notes |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V | |
| $V_{DDQ}$ | Supply Voltage | 3.0 | 3.3 | 3.6 | V | |
| $V_{IH}$ (DC) | Input High (Logic1) Voltage | 2.0 | - | $V_{CC}$ + 0.3 | V | 1,2 |
| $V_{IL}$ (DC) | Input Low (Logic0) Voltage | -0.3 | - | 0.8 | V | 1,2 |

**Note:**

1. All voltages referenced to Vss
2. VIH may overshoot to VCC + 2.0 V for pulse width of < 4ns with 3.3V. VIL may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

- DC Electrical Characteristics

| Symbol | Parameter | Min | Max | Units |
|---|---|---|---|---|
| $I_{I(L)}$ | Input Leakage Current, any input<br>($0.0V \le V_{IN} \le V_{DD}$), All Other Pins Not Under Test = 0V | -2 | 2 | µA |
| $I_{O(L)}$ | Output Leakage Current<br>($D_{OUT}$ is disabled, $0.0V \le V_{OUT} \le V_{DDQ}$) | -2 | 2 | µA |
| $V_{OH}$ | Output Level (LVTTL)<br>Output “H” Level Voltage ($I_{OUT}$ = -2.0mA) | 2.4 | - | V |
| $V_{OL}$ | Output Level (LVTTL)<br>Output “L” Level Voltage ($I_{OUT}$ = +2.0mA) | - | 0.4 | V |

## 9. Capacitance

*Note: Capacitance is sampled and not 100% tested.

| Symbol | Parameter | Min. | Max. | Units |
|---|---|---|---|---|
| $C_{CLK}$ | Input Capacitance: CLK | 4.5 | 6 | pF |
| $C_{IN}$ | Input Capacitance: All other input pins and balls | 2.5 | 6 | pF |
| $C_{IO}$ | Input/Output Capacitance: DQ | 4 | 6 | pF |

## 10. Operating, Standby, and Refresh Currents

- 512MB SODIMM (2 Ranks, 32Mx16 SDR SDRAMs)

| Symbol | Parameter/Condition | PC-133 | Unit |
|---|---|---|---|
| $I_{CC1}$ | Operation Current: Burst length = 4, CL = 3, $t_{RC}$> = $t_{RC}$(min), $t_{CK}$> = $t_{CK}$(min), IO = 0 mA, 2 Bank Interleave Operation | 1480 | mA |
| $I_{CC2P}$ | Precharged Standby Current in Power Down Mode: CKE< = $V_{IL}$(max), $t_{CK}$> = $t_{CK}$(min) | 56 | mA |
| $I_{CC2N}$ | Precharged Standby Current in Non-Power Down Mode: CKE> = $V_{IH}$(min), $t_{CK}$> = $t_{CK}$(min), Input changed once in 3 cycles. | 464 | mA |
| $I_{CC3N}$ | Active Standby Current in Non-Power Down Mode: CKE> = $V_{IH}$(min), $t_{CK}$> = $t_{CK}$(min), Input changed one time | 600 | mA |
| $I_{CC3P}$ | Active Standby Current in Power Down Mode: CKE< = $V_{IL}$(max), $t_{CK}$> = $t_{CK}$(min) | 256 | mA |
| $I_{CC4}$ | Burst Operating Current: Burst length = Full Page, $t_{RC}$ = Infinite, CL = 3, $t_{CK}$> = $t_{CK}$(min), IO = 0 mA 2 Banks Activated | 1240 | mA |
| $I_{CC5}$ | Auto Refresh Current: $t_{RC}$>= $t_{RC}$(min) | 2160 | mA |
| $I_{CC6}$ | Self Refresh Current: CKE = <0.2 V | 56 | mA |

1. Currents given are valid for a single device. .
2. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of $t_{CK}$ and $t_{RC}$. Input signals are changed up to three times during $t_{RC}$(min).
3. The specified values are obtained with the output open.
4. Input signals are changed once during $t_{CK}$(min).
5. Input signals are changed once during three clock cycles.
6. Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).
7. Input signals are stable.

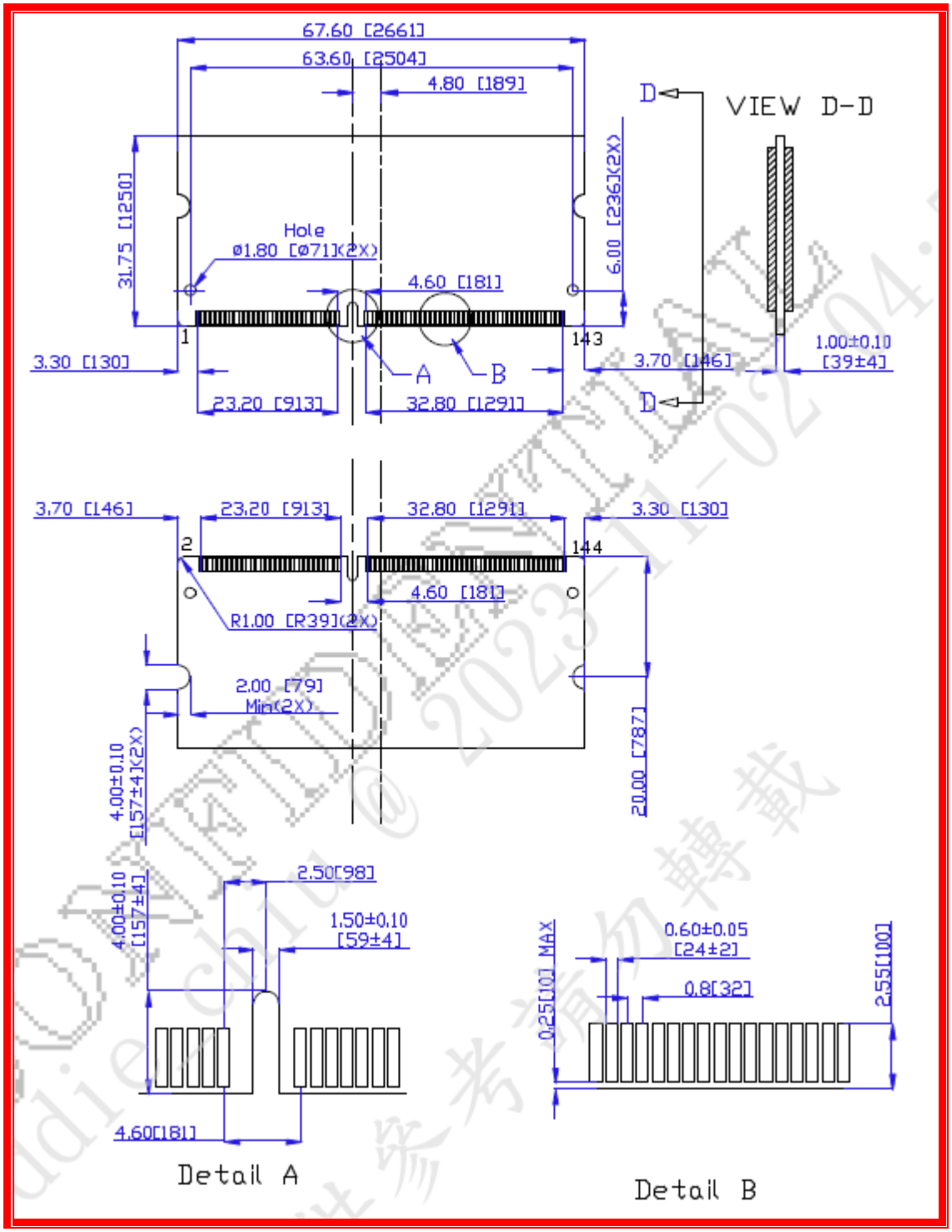
## 11. AC Timing Specifications

| Symbol | Parameter | PC-133 | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **Clock and Clock Enable** | | | | |
| tAC | DQ output access time from CK/CK# | - | 5.4 | ns |
| tCH | CK high-level width | 2.5 | - | ns |
| tCL | CK low-level width | 2.5 | - | ns |
| tCK | Clock frequency | | 133 | MHz |
| tCK | Clock Cycle Time | 7 | | ns |
| tT | Transition time (rise and fall) | 0.3 | 1.5- | ns |
| **Setup and Hold Times** | | | | |
| tIS | input setup time | 1.5 | - | ns |
| tIH | input hold time | 0.8 | - | ns |
| tcks | CKE Setup Time | 1.5 | | ns |
| tckh | CKE Hold Time | 0.8 | | ns |
| tmrd | Mode Register Set Command Cycle Time | 2 | | ns |
| tsb | Power Down Mode Entry Time | 0 | 7 | CLK |
| tds | Data-in Setup Time | 1.5 | | ns |
| tdh | Data-in Hold Time | 0.8 | | ns |
| **Command Parameters** | | | | |
| tRCD | /RAS to /CAS delay | 15 | - | ns |
| tRC | Cycle Time | 65 | - | ns |
| tRAS | Active command Period | 45 | 100K | ns |
| tRP | Precharge Time | 15 | - | ns |
| tRRD | Bank to Bank delay time | 15 | - | ns |
| tCCD | /CAS to /CAS delay time (same bank) | 1 | - | CLK |
| tdpl | Data-in to Precharge Command for Manual precharge | 2 | | CLK |
| **Refresh Cycle** | | | | |

| | | | | |
|---|---|---|---|---|
| $t_{XSR}$ | Self Refresh Exit to Active Time | 1+ $t_{RC}$ | - | ns |
| $t_{REF}$ | Refresh Period (8192 cycles) | - | 64 | ms |
| **Read Cycle** | | | | |
| $t_{OH}$ | Data Out Hold Time | 2.5 | - | ns |
| $t_{LZ}$ | Data Out to Low Impedance Time | 1 | - | Ns |
| $t_{HZ}$ | Data Out to High Impedance Time | 3 | 7 | ns |
| $t_{DQZ}$ | DQM Data Out Disable Latency | - | 2 | CLK |
| **Write Cycle** | | | | |
| $t_{WR}$ | Write Recovery Time for Auto precharge | 2 | - | CLK |
| $t_{DQW}$ | DQM Write Mask Latency | 0 | - | CLK |

## 12. PACKAGE DIMENSION

- (512M, 2 Ranks, 32Mx16 SDR SDRAMs)




Note: All dimensions are in millimeters and should be kept within a tolerance of ±1.27 mm, unless otherwise specified.

## 13. RoHS Declaration

innodisk

宜鼎國際股份有限公司

**Innodisk Corporation**

Page 1/1

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

### RoHS 自我宣告書 (RoHS Declaration of Conformity)

**Manufacturer Product: All Innodisk EM Flash and Dram products**

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

| Name of hazardous substance | Limited of RoHS ppm (mg/kg) |
|---|---|
| 鉛 (Pb) | < 1000 ppm |
| 汞 (Hg) | < 1000 ppm |
| 鎘 (Cd) | < 100 ppm |
| 六價鉻 (Cr 6+) | < 1000 ppm |
| 多溴聯苯 (PBBs) | < 1000 ppm |
| 多溴二苯醚 (PBDEs) | < 1000 ppm |
| 鄰苯二甲酸二(2-乙基己基)酯 (DEHP) | < 1000 ppm |
| 鄰苯二甲酸丁酯苯甲酯 (BBP) | < 1000 ppm |
| 鄰苯二甲酸二丁酯 (DBP) | < 1000 ppm |
| 鄰苯二甲酸二異丁酯 (DIBP) | < 1000 ppm |

**立 保 證 書 人 (Guarantor)**

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2017 / 01 / 18

# Revision Log

| Rev | Date | Modification |
|---|---|---|
| 0.1 | 3rd March 2015 | Preliminary Edition |
| 1.0 | 3rd March 2015 | Official Release. |
| 1.1 | 14th June 2018 | Modified based on PCN change PCB. |
| 1.2 | 2nd November 2023 | Updated 12. PACKAGE DIMENSION |