

Approval Sheet

Customer	
Product Number	M0SB-56PA4CA2-J
Module speed	PC-100
Pin	144 Pin
CAS Latency	CL-2
Operating Temp	0C~70C
Date	2nd November 2023

**The Total Solution For
Industrial Flash Storage**

Rev 1.1

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			CL	tRCD	tRP
		CL=2	CL=2.5	CL=3			
PC-100	A	100	-	100	2	2	2

- Single Pulsed RAS- interface
- Fully Synchronous to positive CLK edge
- 4 banks controlled by BA0 & BA1
- Multiple Burst Read with single write option
- Automatic and controlled precharge command
- Auto refresh (CBR) and Self-Refresh
- Standard 144-pin Memory Module
- Intend for 100 MHz applications
- Inputs and Outputs are LVTTTL compatible
- VDD=VDDQ= 3.3 Volt \pm 0.3
- Serial Presence Detect with EEPROM
- SDRAM Operation Temperature
 - $0^{\circ}\text{C} \leq T_A \leq +70^{\circ}\text{C}$
- Programmable Device Operation:
 - Burst Type: Sequential or Interleave
 - Device CAS# Latency:2, 3
- RoHS Compliant (*Section 14*)

2. Environmental Requirements

SDR SODIMMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
ToPR	Operating Temperature (ambient)	0 to +70	°C	1
Tstg	Storage Temperature	-55 to +150	°C	

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the SDR DRAM component specification.

3. Ordering Information

SDR SODIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M0SB-56PA4CA2-J	256MB	PC-100	32Mx64	8	2	N

4. Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V _{SS}	2	V _{SS}	51	DQM14	52	DQM46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQM15	54	DQM47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	V _{SS}	56	V _{SS}	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	V _{DD}	102	V _{DD}
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	V _{DD}	12	V _{DD}	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	V _{SS}	108	V _{SS}
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38					111	A10/AP	112	A11
19	DQ7	20	DQ39	61	**CLK0	62	**CKE0	113	V _{DD}	114	V _{DD}
21	V _{SS}	22	V _{SS}	63	V _{DD}	64	V _{DD}	115	DQM2	116	DQM6
23	DQM0	24	DQM4	65	RAS	66	CAS	117	DQM3	118	DQM7
25	DQM1	26	DQM5	67	WE	68	**CKE1	119	V _{SS}	120	V _{SS}
27	V _{DD}	28	V _{DD}	69	**CS0	70	A12	121	DQ24	122	DQ56
29	A0	30	A3	71	**CS1	72	*A13	123	DQ25	124	DQ57
31	A1	32	A4	73	DU	74	**CLK1	125	DQ26	126	DQ58
33	A2	34	A5	75	V _{SS}	76	V _{SS}	127	DQ27	128	DQ59
35	V _{SS}	36	V _{SS}	77	NC	78	NC	129	V _{DD}	130	V _{DD}
37	DQ8	38	DQ40	79	NC	80	NC	131	DQ28	132	DQ60
39	DQ9	40	DQ41	81	V _{DD}	82	V _{DD}	133	DQ29	134	DQ61
41	DQ10	42	DQ42	83	DQ16	84	DQ48	135	DQ30	136	DQ62
43	DQ11	44	DQ43	85	DQ17	86	DQ49	137	DQ31	138	DQ63
45	V _{DD}	46	V _{DD}	87	DQ18	88	DQ50	139	V _{SS}	140	V _{SS}
47	DQ12	48	DQ44	89	DQ19	90	DQ51	141	SDA	142	SCL
49	DQ13	50	DQ45	91	V _{SS}	92	V _{SS}	143	V _{DD}	144	V _{DD}
				93	DQ20	94	DQ52				

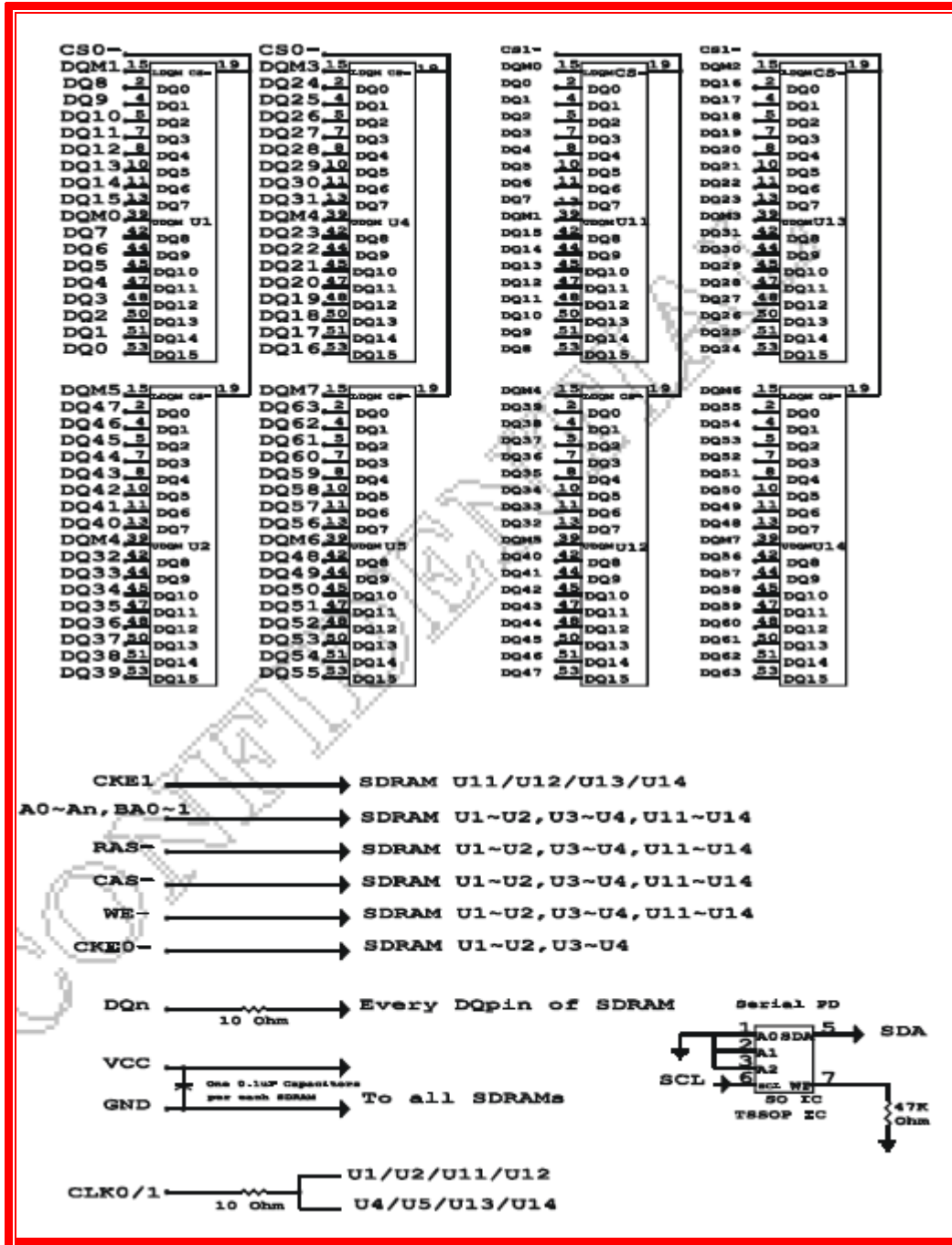
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A12	SDRAM address bus	CKE0 – CKE1	SDRAM clock enable lines
SA0 - SA1	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS-	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS-	SDRAM column address strobe	DQM0 – DQM7	SDRAM data masks
WE-	SDRAM write enable	V _{DD}	Power Supply
CS0- - CS1-	Chip select input	GND	Ground
CLK0 – CLK1	SDRAM Clock input.	DU	Spare Pin
D0 – D63	DIMM memory data bus	NC	No connection

6. Function Block Diagram:

- (256MB, 2 Ranks, 16Mx16 DDR SDRAMs)



7. DC Operating Conditions

- DC Electrical Operating Conditions

Symbol	Parameter	Min	Typ.	Max	Units	Notes
VDD	Supply Voltage	3.0	3.3	3.6	V	1
VDDQ	Supply Voltage	3.0	3.3	3.6	V	1
VIH (DC)	Input High (Logic1) Voltage	2.0	-	VCC + 0.3	V	1,2
VIL (DC)	Input Low (Logic0) Voltage	-0.3	-	0.8	V	1,3

Note:

- All voltages referenced to Vss and VssQ
- VIH (max) = VDD + 1.2V for pulse width ≤ 5ns.
- VIL (min) = VSS + -1.2V for pulse width ≤ 5ns.

- DC Electrical Characteristics

Symbol	Parameter	Min	Max	Units
II(L)	Input Leakage Current, any input (0.0V ≤ VIN ≤ VDD), All Other Pins Not Under Test = 0V	-10	10	μA
IO(L)	Output Leakage Current (DOUT is disabled, 0.0V ≤ VOUT ≤ VDDQ)	-10	10	μA
VOH	Output Level (LVTTTL) Output "H" Level Voltage (IOUT = -2.0mA)	2.4	-	V
VOL	Output Level (LVTTTL) Output "L" Level Voltage (IOUT = +2.0mA)	-	0.4	V

8. Capacitance

*Note: Capacitance is sampled and not 100% tested.

Symbol	Parameter	Max	Units
C _{I1}	Input Capacitance (A0 to A11, /RAS, /CAS, /WE)	5	pF
C _{I2}	Input Capacitance (/CS0, /CSI)	5	pF
C _{IcL}	Input Capacitance (CLK0-CLK1)	4	pF
C _{IO}	Input/Output Capacitance	6.5	pF

9. Operating, Standby, and Refresh Currents

- 256MB SODIMM (2 Ranks, 16Mx16 SDR SDRAMs)

Symbol	Parameter/Condition	PC-100	Unit
I _{CC1}	Operation Current: Burst length = 4, CL = 3, t _{RC} > = t _{RC} (min), t _{CK} > = t _{CK} (min), IO = 0 mA, 2 Bank Interleave Operation	840	mA
I _{CC2P}	Precharged Standby Current in Power Down Mode: CKE< = V _{IL} (max), t _{CK} > = t _{CK} (min)	80	mA
I _{CC2N}	Precharged Standby Current in Non-Power Down Mode: CKE> = V _{IH} (min), t _{CK} > = t _{CK} (min), Input changed once in 3 cycles.	240	mA
I _{CC3N}	Active Standby Current in Non-Power Down Mode: CKE> = V _{IH} (min), t _{CK} > = t _{CK} (min), Input changed one time	400	mA
I _{CC3P}	Active Standby Current in Power Down Mode: CKE< = V _{IL} (max), t _{CK} > = t _{CK} (min)	240	mA
I _{CC4}	Burst Operating Current: Burst length = Full Page, t _{RC} = Infinite, CL = 3, t _{CK} > = t _{CK} (min), IO = 0 mA 2 Banks Activated	720	mA
I _{CC5}	Auto Refresh Current: t _{RC} >= t _{RC} (min)	800	mA
I _{CC6}	Self Refresh Current: CKE = <0.2 V	40	mA

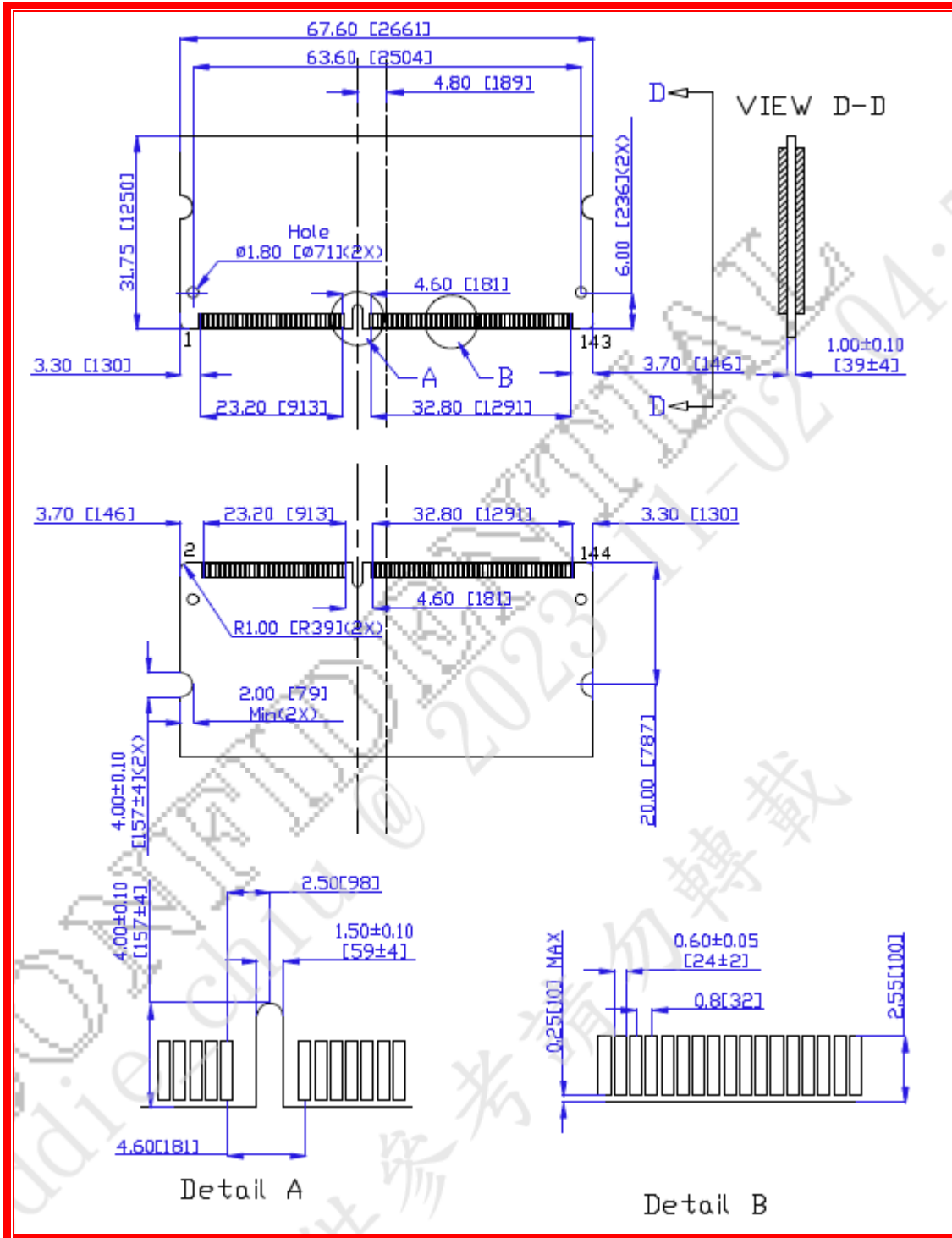
10. AC Timing Specifications

Symbol	Parameter	PC-100		Unit
		Min.	Max.	
Clock and Clock Enable				
tAc	DQ output access time from CK/CK#	-	6	ns
tCH	CK high-level width	2.5	-	ns
tCL	CK low-level width	2.5	-	ns
tCK	Clock frequency		100	MHz
tCK	Clock Cycle Time	10		ns
tT	Transition time (rise and fall)	0.3	1.5	ns
Setup and Hold Times				
tIS	input setup time	1.5	-	ns
tIH	input hold time	0.8	-	ns
tcks	CKE Setup Time	1.5		ns
tckh	CKE Hold Time	0.8		ns
tMRD	Mode Register Set Command Cycle Time	2		ns
tsb	Power Down Mode Entry Time	0	7	CLK
tds	Data-in Setup Time	1.5		ns
tdh	Data-in Hold Time	0.8		ns
Command Parameters				
tRCD	/RAS to /CAS delay	15	-	ns
tRC	Cycle Time	65	-	ns
tRAS	Active command Period	45	100K	ns
tRP	Precharge Time	15	-	ns
tRRD	Bank to Bank delay time	15	-	ns
tCCD	/CAS to /CAS delay time (same bank)	1	-	CLK
tdpl	Data-in to Precharge Command for Manual precharge	2		CLK
Refresh Cycle				

tXSR	Self Refresh Exit to Active Time	1+ tRC	-	ns
tREF	Refresh Period (8192 cycles)	-	64	ms
Read Cycle				
tOH	Data Out Hold Time	2.5	-	ns
tLZ	Data Out to Low Impedance Time	1	-	Ns
tHZ	Data Out to High Impedance Time	3	7	ns
tDQZ	DQM Data Out Disable Latency	-	2	CLK
Write Cycle				
tWR	Write Recovery Time for Auto precharge	2	-	CLK
tDQW	DQM Write Mask Latency	0	-	CLK

11. PACKAGE DIMENSION

- (256M, 2 Ranks, 16Mx16 SDR SODIMM)



Note: All dimensions are in millimeters and should be kept within a tolerance of ± 1.27 mm, unless otherwise specified.

12. RoHS Declaration

innodisk

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RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

- 一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及 (EU) 2015/863 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.
- 二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.
- 三、 本公司聲明我們的產品符合 RoHS 指令的附件中 (7a)、(7c-1) 允許豁免。
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.
- ※ (7a) Lead in high melting temperature type solders (i.e. lead-based alloys containing 85% by weight or more lead).
 - ※ (7C-1) Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯 (DEHP)	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯 (BBP)	< 1000 ppm
鄰苯二甲酸二丁酯 (DBP)	< 1000 ppm
鄰苯二甲酸二異丁酯 (DIBP)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司Company Representative 公司代表人： Randy Chien 簡川勝Company Representative Title 公司代表人職稱： Chairman 董事長Date 日期： 2018 / 07 / 01

Revision Log

Rev	Date	Modification
0.1	5 th June 2020	Preliminary Edition
1.0	5 th June 2020	Official Released.
1.1	2 nd November 2023	Updated 12. PACKAGE DIMENSION