Approval Sheet

Customer	
Product Number	**M0SB-28PA4CA2-J**
Module speed	**PC-100**
Pin	**144 Pin**
CAS Latency	**CL-2**
SDRAM Operating Temp.	**0 °C ~ 70 °C**
Date	**2nd November 2023**

The Total Solution For
Industrial Flash Storage

Rev 1.1

1. Features

Key Parameter

Industry Nomenclature	**Speed Grade**	**Data Rate MT/s**			**tRCD (ns)**	**tRP (ns)**	**tRC (ns)**
		CL=2	**CL=2.5**	**CL=3**			
PC-100	**A**	100	-	100	20	20	70

- Single Pulsed RAS- interface
- Fully Synchronous to positive CLK edge
- 4 banks controlled by BA0 & BA1
- Multiple Burst Read with single write option
- Automatic and controlled precharge command
- Auto refresh (CBR) and Self-Refresh
- Standard 144-pin Memory Module
- Intend for 100 MHz applications
- Inputs and Outputs are LVTTL compatible
- VDD=VDDQ= 3.3 Volt ± 0.3
- Serial Presence Detect with EEPROM
- SDRAM Operation Temperature *(Note 1)*
  - 0°C ≤ T_A ≤ +70°C
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency:2, 3
- RoHS Compliant *(Section 14)*

Note:*1. The refresh rate is required to double when T_A Exceeds70°C.*

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +70	°C	1
TSTG	Storage Temperature	-55 to +150	°C	

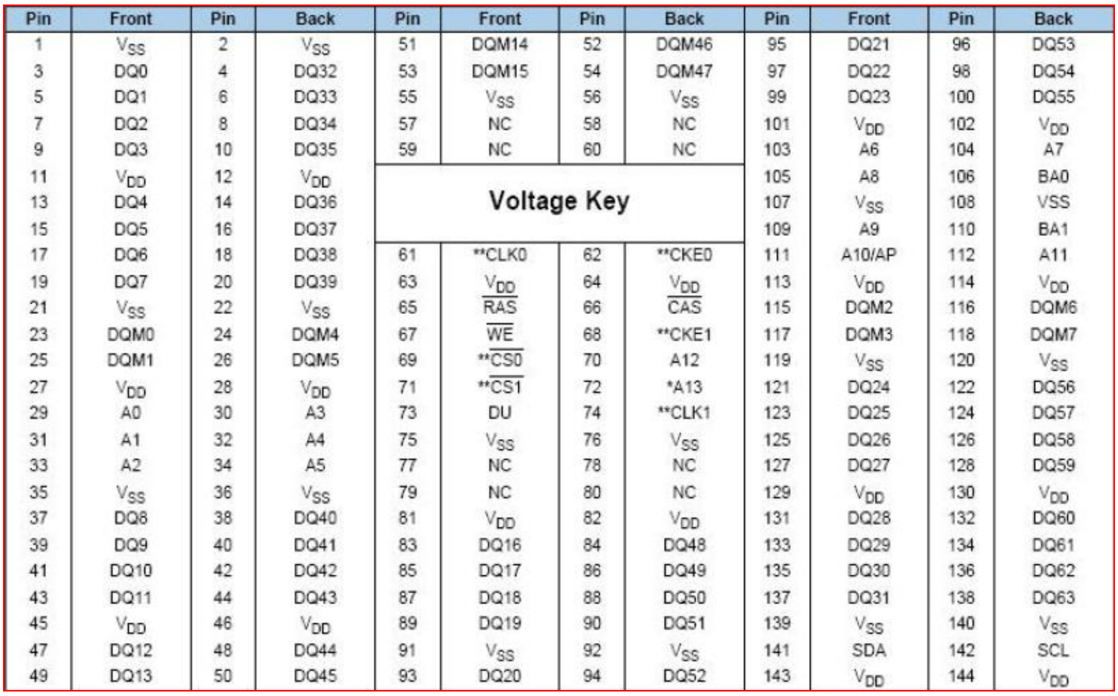
1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.

3. Ordering Information

SDR SODIMM

Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC
M0SB-28PA4CA2-J	128MB	PC-100	16Mx16	4	1	N

4. Pin Configurations (Front side/Back side)



Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{SS}	2	V_{SS}	51	DQM14	52	DQM46	95	DQ21	96	DQ53
3	DQ0	4	DQ32	53	DQM15	54	DQM47	97	DQ22	98	DQ54
5	DQ1	6	DQ33	55	V_{SS}	56	V_{SS}	99	DQ23	100	DQ55
7	DQ2	8	DQ34	57	NC	58	NC	101	V_{DD}	102	V_{DD}
9	DQ3	10	DQ35	59	NC	60	NC	103	A6	104	A7
11	V_{DD}	12	V_{DD}	Voltage Key				105	A8	106	BA0
13	DQ4	14	DQ36					107	V_{SS}	108	VSS
15	DQ5	16	DQ37					109	A9	110	BA1
17	DQ6	18	DQ38	61	**CLK0	62	**CKE0	111	A10/AP	112	A11
19	DQ7	20	DQ39	63	V_{DD}	64	V_{DD}	113	V_{DD}	114	V_{DD}
21	V_{SS}	22	V_{SS}	65	$\overline{RAS}$	66	$\overline{CAS}$	115	DQM2	116	DQM6
23	DQM0	24	DQM4	67	$\overline{WE}$	68	**CKE1	117	DQM3	118	DQM7
25	DQM1	26	DQM5	69	**$\overline{CS0}$	70	A12	119	V_{SS}	120	V_{SS}
27	V_{DD}	28	V_{DD}	71	**$\overline{CS1}$	72	*A13	121	DQ24	122	DQ56
29	A0	30	A3	73	DU	74	**CLK1	123	DQ25	124	DQ57
31	A1	32	A4	75	V_{SS}	76	V_{SS}	125	DQ26	126	DQ58
33	A2	34	A5	77	NC	78	NC	127	DQ27	128	DQ59
35	V_{SS}	36	V_{SS}	79	NC	80	NC	129	V_{DD}	130	V_{DD}
37	DQ8	38	DQ40	81	V_{DD}	82	V_{DD}	131	DQ28	132	DQ60
39	DQ9	40	DQ41	83	DQ16	84	DQ48	133	DQ29	134	DQ61
41	DQ10	42	DQ42	85	DQ17	86	DQ49	135	DQ30	136	DQ62
43	DQ11	44	DQ43	87	DQ18	88	DQ50	137	DQ31	138	DQ63
45	V_{DD}	46	V_{DD}	89	DQ19	90	DQ51	139	V_{SS}	140	V_{SS}
47	DQ12	48	DQ44	91	V_{SS}	92	V_{SS}	141	SDA	142	SCL
49	DQ13	50	DQ45	93	DQ20	94	DQ52	143	V_{DD}	144	V_{DD}

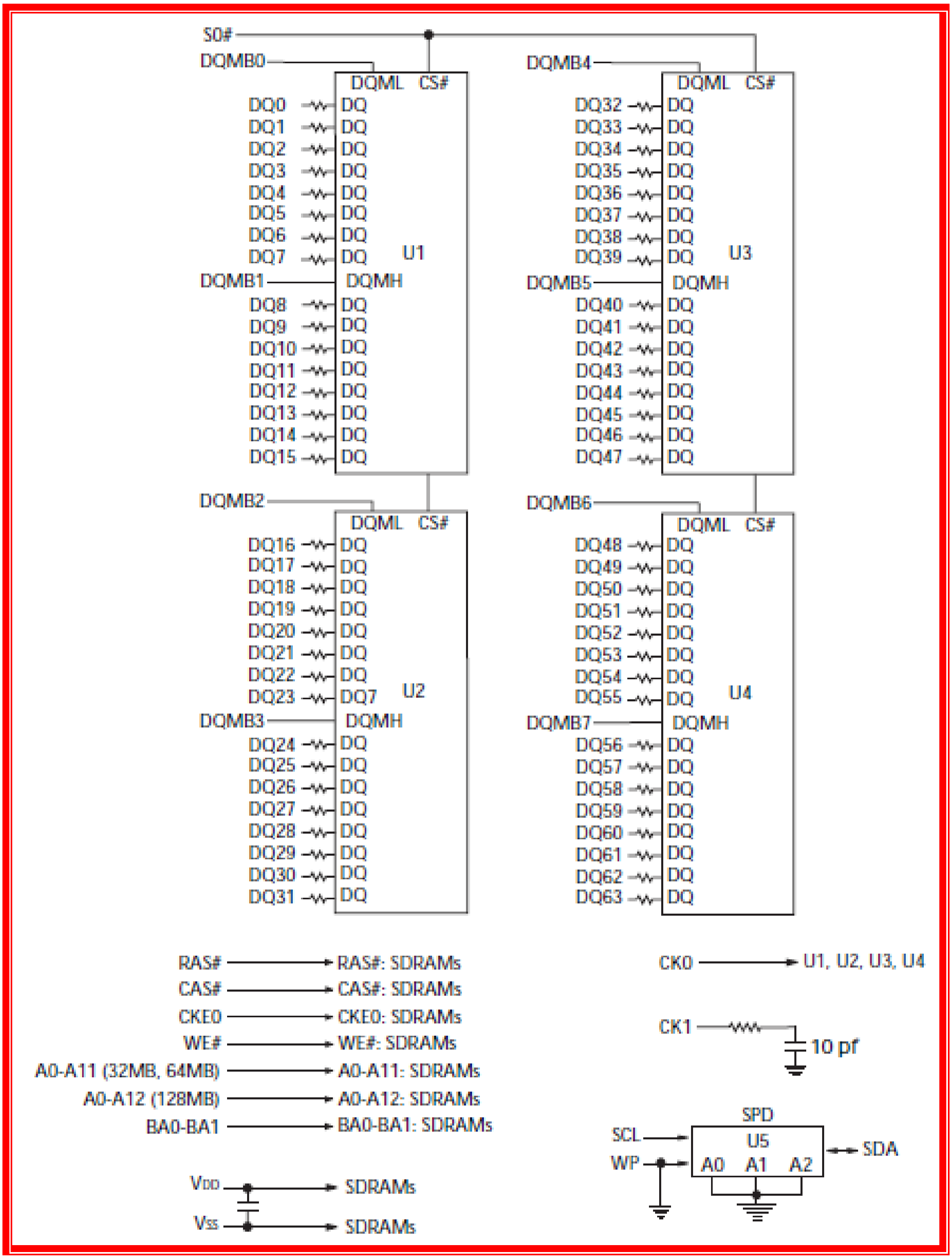
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A12	SDRAM address bus	CKE0 – CKE1	SDRAM clock enable lines
SA0 - SA1	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS-	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS-	SDRAM column address strobe	DQM0 – DQM7	SDRAM data masks
WE-	SDRAM write enable	V_{DD}	Power Supply
CS0- - CS1-	Chip select input	GND	Ground
CLK0 – CLK1	SDRAM Clock input.	DU	Spare Pin
D0 – D63	DIMM memory data bus	NC	No connection

6. Function Block Diagram:

- (128MB, 1 Rank, 16Mx16 SDR SDRAMs)



7. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
T_{STG}	Storage Temperature	-55 to 150	°C
V_{INPUT}	Voltage input pins relative to Vss	-0.3 to +4.6	V
V_{DD}	Voltage on VDD supply relative to Vss	-0.3 to +4.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-0.3 to +4.6	V

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. DC Operating Conditions

- DC Electrical Operating Conditions

(T_A =-0 °C ~ 70 °C; V_{SS} = 0V)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
VDD	Supply Voltage	3.0	3.3	3.6	V	1
VDDQ	Supply Voltage	3.0	3.3	3.6	V	1
VIH (DC)	Input High (Logic1) Voltage	2.0	-	VCC + 0.3	V	1,2
VIL (DC)	Input Low (Logic0) Voltage	-0.5	-	0.8	V	1,3

Note:

1. All voltages referenced to Vss and VssQ
2. **VIH (max) = VDD** + 1.2V for pulse width ≤ 5ns.
3. **VIL (min) = VSS** +-1.2V for pulse width ≤ 5ns.

- DC Electrical Characteristics

(T_A = 0 °C ~ 70 °C; V_{SS} = 0V)

Symbol	Parameter	Min	Max	Units
II(L)	Input Leakage Current, any input (0.0V ≤ VIN ≤ VDD), All Other Pins Not Under Test = 0V	-2	2	µA
IO(L)	Output Leakage Current (DOUT is disabled, 0.0V ≤ VOUT ≤ VDDQ)	-2	2	µA
VOH	Output Level (LVTTL) Output “H” Level Voltage (IOUT = -2.0mA)	2.4	-	V
VOL	Output Level (LVTTL) Output “L” Level Voltage (IOUT = +2.0mA)	-	0.4	V

9. Capacitance

(T_A = 0 °C ~ 70 °C; VDD = 3.3±0.3V)

Symbol	Parameter	Min.	Max.	Units
C_{CLK}	Input Capacitance: CLK	4.5	6	pF
C_{IN}	Input Capacitance: All other input pins and balls	2.5	6	pF
C_{IO}	Input/Output Capacitance: DQ	4	6	pF

10. Operating, Standby, and Refresh Currents

- 128MB SODIMM (1 Rank, 16Mx16 SDR SDRAMs T_A = 0 °C ~ 70 °C; V_{DDQ} = V_{DD} = 3.3±0.3V)

Symbol	Parameter/Condition	PC-100	Unit
I_{CC1}	Operation Current: Burst length = 4, CL = 3, t_{RC}> = t_{RC}(min), t_{CK}> = t_{CK}(min), IO = 0 mA, 2 Bank Interleave Operation	440	mA
I_{CC2P}	Precharged Standby Current in Power Down Mode: CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)	40	mA
I_{CC2N}	Precharged Standby Current in Non-Power Down Mode: CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min), Input changed once in 3 cycles.	120	mA
I_{CC3N}	Active Standby Current in Non-Power Down Mode: CKE> = V_{IH}(min), t_{CK}> = t_{CK}(min), Input changed one time	200	mA
I_{CC3P}	Active Standby Current in Power Down Mode: CKE< = V_{IL}(max), t_{CK}> = t_{CK}(min)	120	mA
I_{CC4}	Burst Operating Current: Burst length = Full Page, t_{RC} = Infinite, CL = 3, t_{CK}> = t_{CK}(min), IO = 0 mA 2 Banks Activated	400	mA
I_{CC5}	Auto Refresh Current: t_{RC}>= t_{RC}(min)	460	mA
I_{CC6}	Self Refresh Current: CKE = <0.2 V	20	mA

1. Currents given are valid for a single device. .
2. These parameters depend on the cycle rate and are measured with the cycle determined by the minimum value of t_{CK} and t_{RC}. Input signals are changed up to three times during t_{RC}(min).
3. The specified values are obtained with the output open.
4. Input signals are changed once during t_{CK}(min).
5. Input signals are changed once during three clock cycles.
6. Active Standby Current will be higher if Clock Suspend is entered during a burst read cycle (add 1mA per DQ).
7. Input signals are stable.

11. AC Timing Specifications

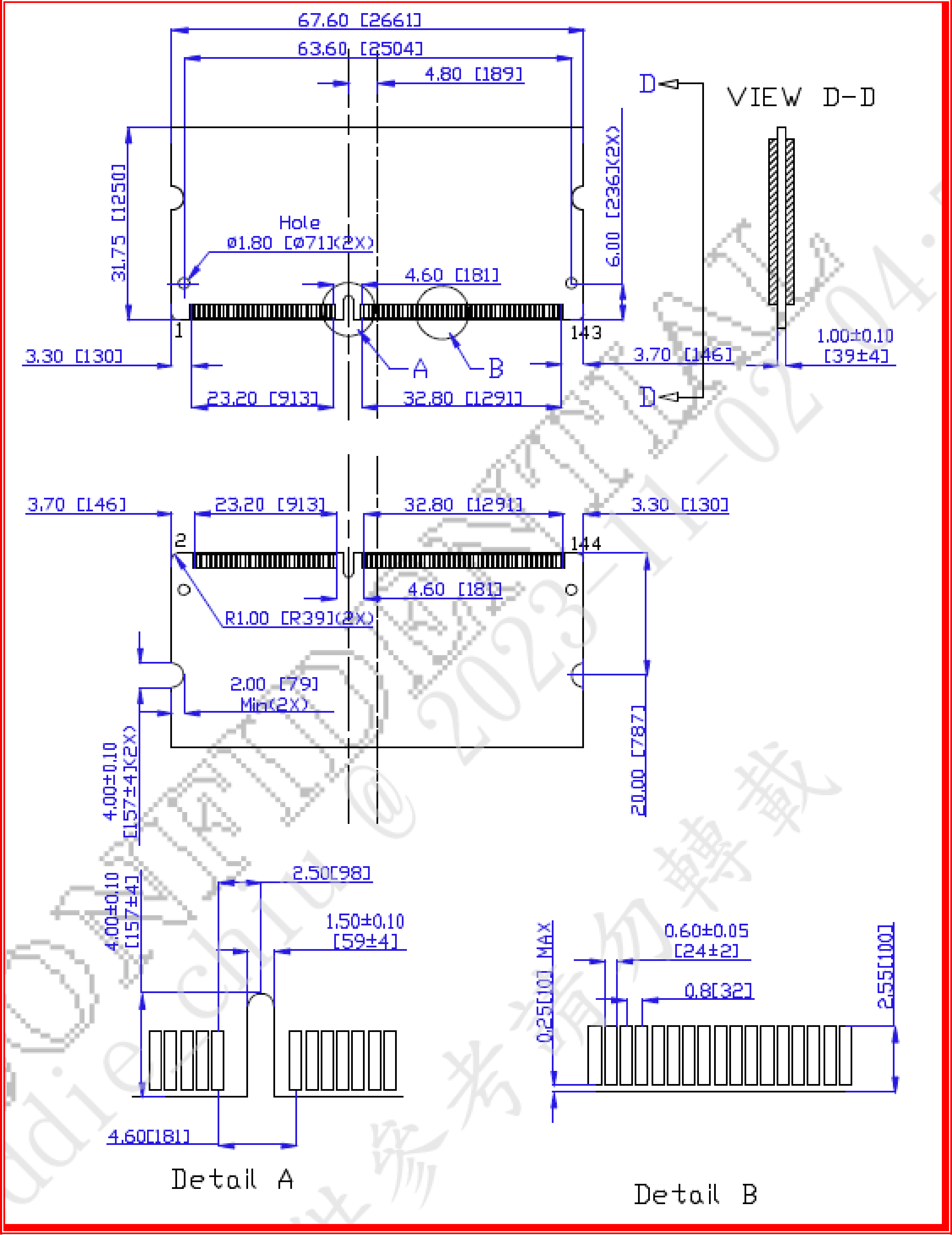
(T_A =0 °C ~ 70 °C; V_{DDQ} = V_{DD} , See AC Characteristics)

Symbol	Parameter	PC-100		Unit
		Min.	Max.	
Clock and Clock Enable				
tAC	DQ output access time from CK/CK#	-	6	ns
tCH	CK high-level width	2.5	-	ns
tCL	CK low-level width	2.5	-	ns
fCK	System frequency	-	100	MHz
tCK	Clock Cycle Time	10		ns
tT	Transition time (rise and fall)	0.3	1.2	ns
Command Parameters				
tRCD	/RAS to /CAS delay	20	-	ns
tRC	Cycle Time	70	-	ns
tRAS	Active command Period	50	100K	ns
tRP	Precharge Time	20	-	ns
tRRD	Bank to Bank delay time	20	-	ns
tCCD	/CAS to /CAS delay time (same bank)	1	-	CLK
Refresh Cycle				
tXSR	Self Refresh Exit to Active Time	1	-	ns
tREF	Refresh Period (8192 cycles)	-	64	ms
Symbol	**Parameter**	**PC-100**		**Unit**
		Min.	Max.	
Read Cycle				
tOH	Data Out Hold Time	2.5	-	ns
tLZ	Data Out to Low Impedance Time	1	-	Ns
tHZ	Data Out to High Impedance Time	-	6	ns
tDQZ	DQM Data Out Disable Latency	-	2	CLK
Write Cycle				

t_{WR}	Write Recovery Time for Auto precharge	2	-	CLK
t_{DQW}	DQM Write Mask Latency	0	-	CLK

12. PACKAGE DIMENSION

- (128MB, 1 Rank, 16Mx16 DDR SDRAMs)



Note: Device position is only for reference.

13. RoHS Declaration

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟2011/65/EU 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) requirement

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI（Cr+6）	< 1000 ppm
Polybromodiphenyl ether（PBDE）	< 1000 ppm
Polybrominated Biphenyls（PBB）	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Richard Lee 李鍾亮

Company Representative Title 公司代表人職稱： CEO 執行長

Date 日期： 2014 / 07 / 29

(Company Stamp/公司大小章)

Revision Log

Rev	Date	Modification
0.1	30th March 2015	Preliminary Edition
1.0	30th March 2015	Official Release.
1.1	2nd November 2023	Updated 12. PACKAGE DIMENSION