

# Approval Sheet

|                       |                                      |
|-----------------------|--------------------------------------|
| <b>Customer</b>       |                                      |
| <b>Product Number</b> | <b>M1UF-12MC2C03-J</b>               |
| <b>Module speed</b>   | <b>PC-3200</b>                       |
| <b>Pin</b>            | <b>184 pin</b>                       |
| <b>CAS Latency</b>    | <b>CL-3</b>                          |
| <b>Operating Temp</b> | <b>0 °C ~ 70 °C</b>                  |
| <b>Date</b>           | <b>12<sup>nd</sup> February 2019</b> |

**The Total Solution For  
Industrial Flash Storage**

Rev 1.0

## 1. Features

### Key Parameter

| Industry<br>Nomenclature | Speed<br>Grade | Data Rate MT/s |        |      | tRCD<br>(ns) | tRP<br>(ns) | tRC<br>(ns) |
|--------------------------|----------------|----------------|--------|------|--------------|-------------|-------------|
|                          |                | CL=2           | CL=2.5 | CL=3 |              |             |             |
| PC-3200                  | F              | 266            | 333    | 400  | 15           | 15          | 55          |

- JEDEC Standard 184-pin Dual In-Line Memory Module
- Intend for 400 MHz applications
- Inputs and Outputs are SSTL-2 compatible
- VDD=VDDQ= 2.6 Volt  $\pm$  0.1 (PC-3200)
- Differential clock input
- DLL aligns DQ and DQS transition with CK transition
- Bi-Directional data strobe with one clock cycle
- Built with 512Mb DDR SDRAMs
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Auto & self refresh 7.8 $\mu$ s ( $T_A \leq +70^\circ\text{C}$ )
- SDRAM Operation Temperature
  - $-0^\circ\text{C} \leq T_A \leq +70^\circ\text{C}$
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 2,2.5,3
  - Burst Length: 2, 4 or 8
- RoHS Compliant (*Section 11*)

## 2. Ordering Information

| DDR UDIMM       |         |         |                   |                |                |     |
|-----------------|---------|---------|-------------------|----------------|----------------|-----|
| Part Number     | Density | Speed   | DIMM Organization | Number of DRAM | Number of rank | ECC |
| M1UF-12MC2C03-J | 512MB   | PC-3200 | 64M x64           | 8              | 1              | N/A |

### 3. Pin Configurations (Front side/Back side)

| Front |        |     |        | Back |           |     |           |
|-------|--------|-----|--------|------|-----------|-----|-----------|
| Pin   | Name   | Pin | Name   | Pin  | Name      | Pin | Name      |
| 1     | VREF   | 48  | A0     | 93   | VSS       | 140 | NC        |
| 2     | DQ0    | 49  | NC     | 94   | DQ4       | 141 | A10       |
| 3     | VSS    | 50  | VSS    | 95   | DQ5       | 142 | NC        |
| 4     | DQ1    | 51  | NC     | 96   | VDDQ      | 143 | VDDQ      |
| 5     | DQS0   | 52  | BA1    | 97   | DM0/DQS9  | 144 | NC        |
| 6     | DQ2    | Key |        | 98   | DQ6       | Key |           |
| 7     | VDD    | 53  | DQ32   | 99   | DQ7       | 145 | VSS       |
| 8     | DQ3    | 54  | VDDQ   | 100  | VSS       | 146 | DQ36      |
| 9     | NC,A15 | 55  | DQ33   | 101  | NC        | 147 | DQ37      |
| 10    | NC     | 56  | DQS4   | 102  | NC,TEST   | 148 | VDDQ      |
| 11    | VSS    | 57  | DQ34   | 103  | A13       | 149 | DM4/DQS13 |
| 12    | DQ8    | 58  | VSS    | 104  | VDDQ      | 150 | DQ38      |
| 13    | DQ9    | 59  | BA0    | 105  | DQ12      | 151 | DQ39      |
| 14    | DQS1   | 60  | DQ35   | 106  | DQ13      | 152 | VSS       |
| 15    | VDDQ   | 61  | DQ40   | 107  | DM1/DQS10 | 153 | DQ44      |
| 16    | CK1    | 62  | VDDQ   | 108  | VDD       | 154 | /RAS      |
| 17    | /CK1   | 63  | /WE    | 109  | DQ14      | 155 | DQ45      |
| 18    | VSS    | 64  | DQ41   | 110  | DQ15      | 156 | VDDQ      |
| 19    | DQ10   | 65  | /CAS   | 111  | CKE1      | 157 | /S0       |
| 20    | DQ11   | 66  | VSS    | 112  | VDDQ      | 158 | /S1       |
| 21    | CKE0   | 67  | DQS5   | 113  | BA2       | 159 | DM5/DQS14 |
| 22    | VDDQ   | 68  | DQ42   | 114  | DQ20      | 160 | VSS       |
| 23    | DQ16   | 69  | DQ43   | 115  | A12       | 161 | DQ46      |
| 24    | DQ17   | 70  | VDD    | 116  | VSS       | 162 | DQ47      |
| 25    | DQS2   | 71  | NC,/S2 | 117  | DQ21      | 163 | NC,/S3    |
| 26    | VSS    | 72  | DQ48   | 118  | A11       | 164 | VDDQ      |
| 27    | A9     | 73  | DQ49   | 119  | DM2/DQS11 | 165 | DQ52      |
| 28    | DQ18   | 74  | VSS    | 120  | VDD       | 166 | DQ53      |
| 29    | A7     | 75  | /CK2   | 121  | DQ22      | 167 | NC,A13    |
| 30    | VDDQ   | 76  | CK2    | 122  | A8        | 168 | VDD       |
| 31    | DQ19   | 77  | VDDQ   | 123  | DQ23      | 169 | DM6/DQS15 |
| 32    | A5     | 78  | DQS6   | 124  | VSS       | 170 | DQ54      |
| 33    | DQ24   | 79  | DQ50   | 125  | A6        | 171 | DQ55      |
| 34    | VSS    | 80  | DQ51   | 126  | DQ28      | 172 | VDDQ      |
| 35    | DQ25   | 81  | VSS    | 127  | DQ29      | 173 | NC,A14    |
| 36    | DQS3   | 82  | VDDID  | 128  | VDDQ      | 174 | DQ60      |
| 37    | A4     | 83  | DQ56   | 129  | DM3/DQS12 | 175 | DQ61      |
| 38    | VDD    | 84  | DQ57   | 130  | A3        | 176 | VSS       |
| 39    | DQ26   | 85  | VDD    | 131  | DQ30      | 177 | DM7/DQS16 |
| 40    | DQ27   | 86  | DQS7   | 132  | VSS       | 178 | DQ62      |
| 41    | A2     | 87  | DQ58   | 133  | DQ31      | 179 | DQ63      |
| 42    | VSS    | 88  | DQ59   | 134  | NC        | 180 | VDDQ      |
| 43    | A1     | 89  | VSS    | 135  | NC        | 181 | SA0       |
| 44    | NC     | 90  | NC     | 136  | VDDQ      | 182 | SA1       |
| 45    | NC     | 91  | SDA    | 137  | CK0       | 183 | SA2       |
| 46    | VDD    | 92  | SCL    | 138  | /CK0      | 184 | VDDSPD    |
| 47    | NC     |     |        | 139  | VSS       |     |           |

## 4. Architecture

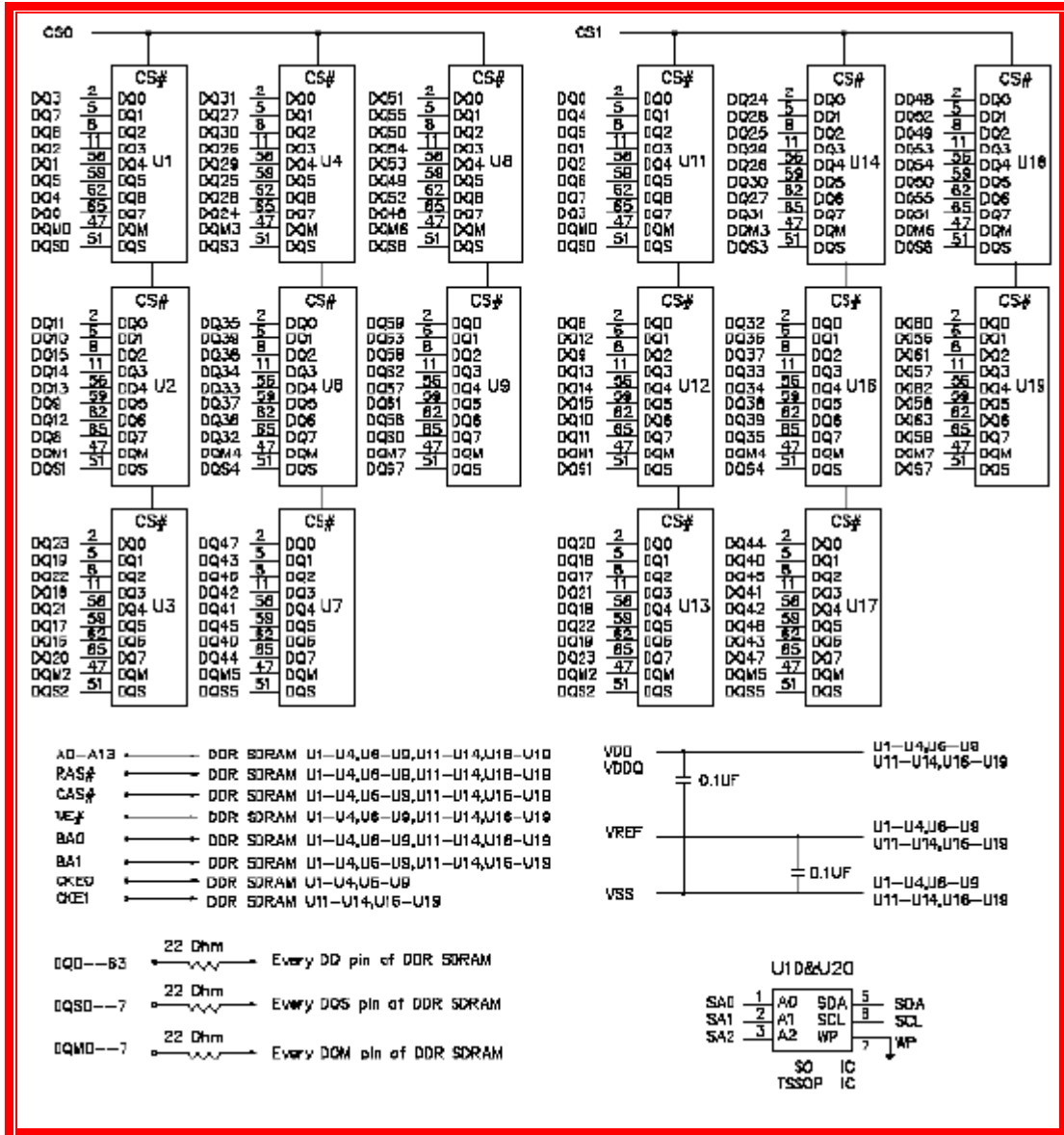
### Pin Definition

| Pin Name          | Description  | Pin Name           | Description  |
|-------------------|--|--------------------|--|
| A0–A15            | SDRAM address bus  | CK0 - CK2          | SDRAM clock (positive lines of 3 differential pairs)   |
| BA0–BA1           | SDRAM bank select  | /CK0 - /CK2        | SDRAM clock (negative lines of these three pairs)  |
| DQ0–DQ63          | DIMM memory data bus                                       | SCL                | I <sup>2</sup> C serial bus clock for EEPROM   |
| CB0–CB7           | DIMM ECC check bits  | SDA                | I <sup>2</sup> C serial bus data line for EEPROM   |
| /RAS              | SDRAM row address strobe                                   | SA0-SA2            | I <sup>2</sup> C slave address select for EEPROM   |
| /CAS              | SDRAM column address strobe                                | V <sub>DD</sub> *  | SDRAM positive power supply  |
| /WE               | SDRAM write enable   | V <sub>DDQ</sub> * | SDRAM I/O Driver positive power supply   |
| /S0 - /S1         | SDRAM chip select lines (Phys. banks 0 and 1)              | V <sub>REF</sub>   | SDRAM I/O reference supply   |
| CKE0–CKE1         | SDRAM clock enable lines                                   | V <sub>SS</sub>    | Power supply return (ground)   |
| DQS0–DQS8         | SDRAM low data strobes                                     | V <sub>DDSPD</sub> | Serial EEPROM positive power supply (2.5 Volts to 3.3 Volts)--V <sub>DDSPD</sub> is not connected to V <sub>DD</sub> or V <sub>DDQ</sub> |
| DM(0-8),DQS(9-17) | SDRAM low data masks/high data strobes (x4, 2 Phys. banks) | NC                 | Spare pins (no connect)  |
| VDDID             | VDD identification flag                                    | TEST               | Used by memory bus analysis tools (unused on memory DIMMs)   |

\*The V<sub>DD</sub> and V<sub>DDQ</sub> pins are tied common to a single power-plane on these designs.

### 5. Function Block Diagram:

- (512MB, 1 Rank 64Mx8 DDR SDRAM base UDIMM)
- U11~U14, U16~U19 empty



## 6. SDRAM Absolute Maximum Ratings

| Symbol      | Parameter                              | Min. | Max.     | Units |
|-------------|--|------|----------|-------|
| $T_{STG}$   | Storage Temperature                    | -55  | 150      | °C    |
| $V_{INPUT}$ | Voltage input pins relative to Vss     | -1.0 | 3.6      | V     |
| $V_{IO}$    | Voltage on I/O pins relative to Vss    | -0.5 | VDDQ+0.5 | V     |
| $V_{DD}$    | Voltage on VDD supply relative to Vss  | -1.0 | 3.6      | V     |
| $V_{DDQ}$   | Voltage on VDDQ supply relative to Vss | -1.0 | 3.6      | V     |
| $I_{OS}$    | Output short Circuit Current           |      | 50       | mA    |

**Note:** Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## 7. AC & DC Operating Conditions

### AC Input Operating Conditions

| Symbol                | Parameter                             | Value                       |                             | Units | Notes |
|-----------------------|---------------------------------------|-----------------------------|-----------------------------|-------|-------|
|                       |                                       | Min                         | Max                         |       |       |
| V <sub>IH</sub> (AC)  | Input High (Logic1) Voltage           | V <sub>REF</sub> + 0.31     | -                           | V     | 1     |
| V <sub>IL</sub> (AC)  | Input Low (Logic0) Voltage            | -                           | V <sub>REF</sub> - 0.31     | V     | 1     |
| V <sub>ID</sub> (AC)  | Input differential Voltage: CK, /CK   | 0.7                         | V <sub>DDQ</sub> + 0.6      | V     | 2     |
| V <sub>IX</sub> (AC)  | Input crossing point Voltage: CK, /CK | 0.5* V <sub>DDQ</sub> - 0.2 | 0.5* V <sub>DDQ</sub> + 0.2 | V     | 3     |
| V <sub>REF</sub> (AC) | I/O reference voltage                 | 0.49*V <sub>DDQ</sub>       | 0.51*V <sub>DDQ</sub>       | V     | 4     |

**Note:**

1. V<sub>IH</sub> overshoot: V<sub>IH,max</sub> = V<sub>DDQ</sub> + 1.5V for a pulse width 3ns, and the pulse width can not be greater than 1/3 of the cycle rate. V<sub>IL</sub> undershoot: V<sub>IL,min</sub> = -1.5V for a pulse width 3ns, and the pulse width can not be greater than 1/3 of the cycle rate.
2. V<sub>ID</sub> is the magnitude of the difference between the input level on CK and the input level on CK#.
3. The value of V<sub>IX</sub> and V<sub>M</sub> is expected to equal V<sub>DDQ</sub>/2 of the transmitting device and must track variations in the DC level of the same.
4. V<sub>REF</sub> is expected to equal V<sub>DDQ</sub>/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on V<sub>REF</sub> may not exceed ±2% of the DC value. Thus, from V<sub>DDQ</sub>/2, V<sub>REF</sub> is allowed ±25mV for DC error and an additional ±25mV for AC noise. This measurement is to be taken at the nearest V<sub>REF</sub> bypass capacitor.



## DC Electrical Characteristics and Operating Conditions

| Symbol  | Parameter                           | Min         | Typ.    | Max         | Units | Notes |
|---------|-------------------------------------|-------------|---------|-------------|-------|-------|
| VDD     | Supply Voltage (DDR266,333)         | 2.3         | 2.5     | 2.7         | V     | 1     |
|         | Supply Voltage (DDR400)             | 2.5         | 2.6     | 2.7         | V     | 1     |
| VDDQ    | Supply Voltage (DDR266,333)         | 2.3         | 2.5     | 2.7         | V     | 1     |
|         | Supply Voltage (DDR400)             | 2.5         | 2.6     | 2.7         | V     | 1     |
| VIH(DC) | Input High (Logic1) Voltage         | VREF + 0.15 | -       | VDD + 0.3   | V     | 2     |
| VIL(DC) | Input Low (Logic0) Voltage          | -0.3        | -       | VREF - 0.15 | V     | 2     |
| VTT     | Termination Voltage                 | VREF-0.04   |         | VREF+0.04   | V     | 3     |
| Ii      | Input leakage current:              | -2          |         | 2           | uA    |       |
| VREF    | I/O Reference Voltage               | 0.49VDDQ    | 0.5VDDQ | 0.51VDDQ    | V     | 4     |
| VIN(DC) | Input Voltage Level: CK, /CK        | -0.3        | -       | VDDQ + 0.3  | V     | 4     |
| VID(DC) | Input Differential Voltage: CK, /CK | 0.36        | -       | VDDQ + 0.6  | V     | 4,5   |

### Note:

- VDD and VDDQ must track each other.
- To maintain a valid level, the transitioning edge of the input must:
  - Sustain a constant slew rate from the current AC level through to the target AC level, VIL(AC) or VIH(AC).
  - Reach at least the target AC level.
  - After the AC target level is reached, continue to maintain at least the target DC level, VIL(DC) or VIH(DC).
- VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, it is expected to be set equal to VREF, and it must track variations in the DC level of VREF.
- VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise (noncommon mode) on VREF may not exceed  $\pm 2\%$  of the DC value. Thus, from VDDQ/2, VREF is allowed  $\pm 25\text{mV}$  for DC error and an additional  $\pm 25\text{mV}$  for AC noise. This measurement is to be taken at the nearest VREF bypass capacitor.
- VID is the magnitude of the difference between the input level on CK and the input level on CK#.

## 8. Operating, Standby, and Refresh Currents

- 512MB UDIMM (1 Rank, 64Mx8 DDR SDRAMs)

| Symbol            | Parameter/Condition  | PC-3200 | Unit |
|-------------------|--|---------|------|
| I <sub>DD0</sub>  | One bank; Active - Precharge; t <sub>RC</sub> =t <sub>RC</sub> (min); t <sub>CK</sub> =t <sub>CK</sub> (min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle                          | 600     | mA   |
| I <sub>DD1</sub>  | One bank; Active - Read - Precharge; Burst Length=2; t <sub>RC</sub> =t <sub>RC</sub> (min); t <sub>CK</sub> =t <sub>CK</sub> (min); address and control inputs changing once per clock cycle  | 680     | mA   |
| I <sub>DD2P</sub> | All banks idle; Power down mode; CKE=Low, t <sub>CK</sub> =t <sub>CK</sub> (min)   | 40      | mA   |
| I <sub>DD2F</sub> | /CS=High, All banks idle; t <sub>CK</sub> =t <sub>CK</sub> (min); CKE= High; address and control inputs changing once per clock cycle.VIN=VREF for DQ, DQS and DM  | 184     | mA   |
| I <sub>DD3P</sub> | One bank active ; Power down mode; CKE=Low, t <sub>CK</sub> =t <sub>CK</sub> (min)   | 144     | mA   |
| I <sub>DD3N</sub> | /CS=HIGH; CKE=HIGH; One bank; Active-Precharge;t <sub>RC</sub> =t <sub>RAS</sub> (max); t <sub>CK</sub> =t <sub>CK</sub> (min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle | 320     | mA   |
| I <sub>DD4R</sub> | Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> =t <sub>CK</sub> (min); IOUT=0mA  | 960     | mA   |
| I <sub>DD4W</sub> | Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; t <sub>CK</sub> =t <sub>CK</sub> (min); DQ, DM and DQS inputs changing twice per clock cycle   | 960     | mA   |
| I <sub>DD5</sub>  | t <sub>RC</sub> =t <sub>RFC</sub> (min) - 8*t <sub>CK</sub> for DDR200 at 100Mhz, 10*t <sub>CK</sub> for DDR266A & DDR266B at 133Mhz; distributed refresh  | 960     | mA   |
| I <sub>DD6</sub>  | CKE=<0.2V; External clock on; t <sub>CK</sub> =t <sub>CK</sub> (min)   | 40      | mA   |
| I <sub>DD7</sub>  | Four bank interleaving with BL=4 Refer to the following page for detailed test condition   | 1840    | mA   |

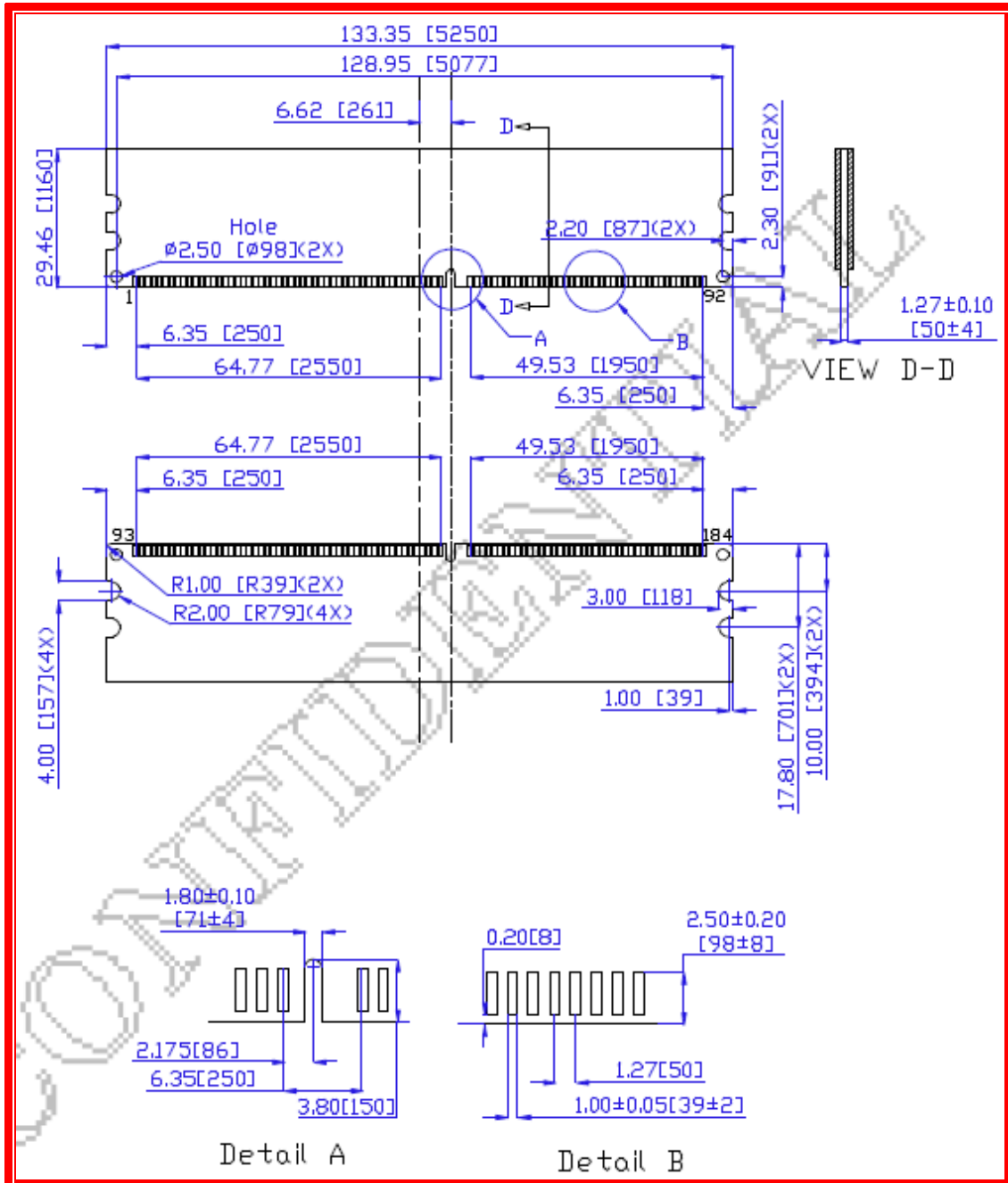
## 9. AC Timing Specifications

| Symbol   | Parameter  | PC2-3200         |      | Unit |
|----------|--|------------------|------|------|
|          |  | Min.             | Max. |      |
| tAC      | DQ output access time from CK/CK#  | -0.7             | 0.7  | ns   |
| tdQSK    | DQS output access time from CK/CK#   | -0.60            | 0.60 | ns   |
| tCH      | CK high-level width  | 0.45             | 0.55 | tCK  |
| tCL      | CK low-level width   | 0.45             | 0.55 | tCK  |
| tHP      | Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time | min<br>(tCL,tCH) | -    | ns   |
| tCK      | Clock Cycle Time   | 5                | 7.5  | ns   |
| tDS      | DQ and DM input setup time(differential data strobe)   | 0.4              | -    | ns   |
| tDH      | DQ and DM input hold time(differential data strobe)  | 0.4              | -    | ns   |
| tIPW     | Input pulse width  | 2.2              | -    | ns   |
| tdIPW    | DQ and DM input pulse width (each input)   | 1.75             | -    | ns   |
| tHZ      | Data-out high-impedance time from CK/CK  | -                | 0.7  | ns   |
| tLZ      | Data-out Low-Z window from CK/CK#  | -0.7             | -    | ns   |
| tdQSQ    | DQS-DQ skew (DQS & associated DQ signals)  | -                | 0.4  | ns   |
| tQHS     | Data hold Skew Factor  | -                | 0.5  | ns   |
| tQH      | Data output hold time from DQS   | tHP -tQHS        | -    | ns   |
| tdQSS    | Write command to 1 <sup>st</sup> DQS latching transition                                     | 0.72             | 1.28 | tCK  |
| tdQSL(H) | DQS input low (high) pulse width (write cycle)   | 0.35             | -    | tCK  |
| tdSS     | DQS falling edge to CK setup time (write cycle)  | 0.2              | -    | tCK  |
| tDSH     | DQS falling edge hold time from CK (write cycle)   | 0.2              | -    | tCK  |
| tMRD     | Mode register set command cycle time   | 10               | -    | ns   |
| tWPST    | Write postamble  | 0.4              | 0.6  | tCK  |
| tWPRE    | Write preamble   | 0.25             | -    | tCK  |
| tIH      | Address and control input hold time  | 0.6              | -    | ns   |
| tIS      | Address and control input setup time   | 0.6              | -    | ns   |
| tRPRE    | Read preamble  | 0.9              | 1.1  | tCK  |

|       |  |     |     |     |
|-------|--|-----|-----|-----|
| tRPST | Read postamble                             | 0.4 | 0.6 | tCK |
| tRRD  | Active bank A to Active bank B command     | 10  | -   | ns  |
| tREFI | Average Periodic Refresh Interval          | -   | 7.8 | μs  |
| tWR   | Write recovery time without Auto-Precharge | 15  |     | ns  |
| tWTR  | Internal write to read command delay       | 2   | -   | tCK |
| tXSNR | Exit self refresh to a Non-read command    | 70  | -   | ns  |
| tXSRD | Exit self refresh to a Read command        | 200 | -   | tCK |

### 10. PACKAGE DIMENSION

- (512MB, 1 Rank 64Mx8 DDR SDRAMs)



Note: All dimensions are in millimeters and should be kept within a tolerance of  $\pm 0.15$ , unless otherwise specified.

## 11. RoHS Declaration

innodisk

宜鼎國際股份有限公司  
Innodisk Corporation

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## RoHS 自我宣告書 (RoHS Declaration of Conformity)

## Manufacturer Product: All Innodisk EM Flash and Dram products

- 一、宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及 (EU) 2015/863 關於 RoHS 之規範要求。  
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.
- 二、本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。  
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.
- 三、本公司聲明我們的產品符合 RoHS 指令的附件中 (7a)、(7c-1) 允許豁免。  
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.
- ※ (7a) Lead in high melting temperature type solders (i.e. lead-based alloys containing 85% by weight or more lead).
- ※ (7C-1) Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.

| Name of hazardous substance | Limited of RoHS ppm (mg/kg) |
|-----------------------------|-----------------------------|
| 鉛 (Pb)                      | < 1000 ppm                  |
| 汞 (Hg)                      | < 1000 ppm                  |
| 鎘 (Cd)                      | < 100 ppm                   |
| 六價鉻 (Cr 6+)                 | < 1000 ppm                  |
| 多溴聯苯 (PBBs)                 | < 1000 ppm                  |
| 多溴二苯醚 (PBDEs)               | < 1000 ppm                  |
| 鄰苯二甲酸二(2-乙基己基)酯 (DEHP)      | < 1000 ppm                  |
| 鄰苯二甲酸丁酯苯甲酯 (BBP)            | < 1000 ppm                  |
| 鄰苯二甲酸二丁酯 (DBP)              | < 1000 ppm                  |
| 鄰苯二甲酸二異丁酯 (DIBP)            | < 1000 ppm                  |

## 立保證書人 (Guarantor)

Company name 公司名稱：Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人：Randy Chien 簡川勝

Company Representative Title 公司代表人職稱：Chairman 董事長

Date 日期：2018 / 07 / 01



## Revision Log

| Rev | Date                           | Modification        |
|-----|--------------------------------|---------------------|
| 0.1 | 12 <sup>nd</sup> February 2019 | Preliminary Edition |
| 1.0 | 12 <sup>nd</sup> February 2019 | Official Released.  |