USER GUIDE

mITX-CFL-S

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MITX-CFL-S - USER GUIDE

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Revision History

Revision	Brief Description of Changes	Date of Issue
1.0	Initial Issue	2019-Feb-20
1.1	Remove C242 SKU	2019-Feb-25
1.2	Update OS support	2019-Mar-26
1.3	Update system diagram and M.2 Key B pin assignment	2019-Apr-12
1.4	Update CR2032 wafer figure	2019-Apr-17
1.5	Remove JP14 default setting	2019-Apr-30
1.6	Adding Coffee Lake Refresh to CPU support	2019-Jun-03
1.7	Update supporting CPU type of C246	2019-Jul-15
1.8	Add RAID support	2019-Nov-21
2.0	Add CE and FCC standards, Max. TDP support for Coffee Lake Refresh	2020-Mar-25
2.1	Add a LPS power supply notice in Sec. 2.1	2020-Apr-10
2.2	Update jumper JP11 pin assignment	2020-Jul-09
2.3	Update CPU max. TDP support	2020-Sep-09
2.4	Add mating connector info	2021-Mar-24
2.5	Audio codec chip replacement	2021-Apr-07
2.6	Modify USB 3.1 to USB 3.2 Gen 2 per new naming	2022-Jul-29
2.7	Add UL certification	2022-Nov-25
2.8	Update battery precautions	2023-Jan-31
3.0	Remove COM port OS patch information	2023-Feb-02

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As a trusted technology innovator and global solutions provider, Kontron extends its embedded market strengths into a services portfolio allowing companies to break the barriers of traditional product lifecycles. Proven product expertise coupled with collaborative and highly-experienced support enables Kontron to provide exceptional peace of mind to build and maintain successful products.

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Customer Comments

If you have any difficulties using this user guide, discover an error, or just want to provide some feedback, contact Kontron support. Detail any errors you find. We will correct the errors or problems as soon as possible and post the revised user guide on our website.

Symbols

The following symbols may be used in this user guide

⚠DANGER	DANGER indicates a hazardous situation which, if not avoided, will result in death or serious injury.
⚠WARNING	WARNING indicates a hazardous situation which, if not avoided, could result in death or serious injury.
NOTICE	NOTICE indicates a property damage message.
⚠CAUTION	CAUTION indicates a hazardous situation which, if not avoided, may result in minor or moderate injury.
	Electric Shock! This symbol and title warn of hazards due to electrical shocks (> 60 V) when touching products or parts of products. Failure to observe the precautions indicated and/or prescribed by the law may endanger your life/health and/or result in damage to your material.
	ESD Sensitive Device! This symbol and title inform that the electronic boards and their components are sensitive to static electricity. Care must therefore be taken during all handling operations and inspections of this product in order to ensure product integrity at all times.
	HOT Surface! Do NOT touch! Allow to cool before servicing.
	Laser! This symbol inform of the risk of exposure to laser beam and light emitting devices (LEDs) from an electrical device. Eye protection per manufacturer notice shall review before servicing.
	This symbol indicates general information about the product and the user guide. This symbol also indicates detail information about the specific product configuration.
	This symbol precedes helpful hints and tips for daily use.

For Your Safety

Your new Kontron product was developed and tested carefully to provide all features necessary to ensure its compliance with electrical safety requirements. It was also designed for a long fault-free life. However, the life expectancy of your product can be drastically reduced by improper treatment during unpacking and installation. Therefore, in the interest of your own safety and of the correct operation of your new Kontron product, you are requested to conform with the following guidelines.

High Voltage Safety Instructions

As a precaution and in case of danger, the power connector must be easily accessible. The power connector is the product's main disconnect device.

⚠CAUTION

Warning

All operations on this product must be carried out by sufficiently skilled personnel only.

⚠CAUTION

Electric Shock!

Before installing a non hot-swappable Kontron product into a system always ensure that your mains power is switched off. This also applies to the installation of piggybacks. Serious electrical shock hazards can exist during all installation, repair, and maintenance operations on this product. Therefore, always unplug the power cable and any other cables which provide external voltages before performing any work on this product.

Earth ground connection to vehicle's chassis or a central grounding point shall remain connected. The earth ground cable shall be the last cable to be disconnected or the first cable to be connected when performing installation or removal procedures on this product.

Special Handling and Unpacking Instruction

NOTICE

ESD Sensitive Device!

Electronic boards and their components are sensitive to static electricity. Therefore, care must be taken during all handling operations and inspections of this product, in order to ensure product integrity at all times.

Do not handle this product out of its protective enclosure while it is not used for operational purposes unless it is otherwise protected.

Whenever possible, unpack or pack this product only at EOS/ESD safe work stations. Where a safe work station is not guaranteed, it is important for the user to be electrically discharged before touching the product with his/her hands or tools. This is most easily done by touching a metal part of your system housing.

It is particularly important to observe standard anti-static precautions when changing piggybacks, ROM devices, jumper settings etc. If the product contains batteries for RTC or memory backup, ensure that the product is not placed on conductive surfaces, including anti-static plastics or sponges. They can cause short circuits and damage the batteries or conductive circuits on the product.

Lithium Battery Precautions

If your product is equipped with a lithium battery, take the following precautions when replacing the battery.

⚠CAUTION

Danger of fire or explosion if the battery is replaced incorrectly.

- Replace only with same or equivalent battery type recommended by the manufacturer.
- Dispose of used batteries according to the manufacturer's instructions.

General Instructions on Usage

In order to maintain Kontron's product warranty, this product must not be altered or modified in any way. Changes or modifications to the product, that are not explicitly approved by Kontron and described in this user guide or received from Kontron Support as a special handling instruction, will void your warranty.

This product should only be installed in or connected to systems that fulfill all necessary technical and specific environmental requirements. This also applies to the operational temperature range of the specific board version that must not be exceeded. If batteries are present, their temperature restrictions must be taken into account.

In performing all necessary installation and application operations, only follow the instructions supplied by the present user guide.

Keep all the original packaging material for future storage or warranty shipments. If it is necessary to store or ship the product then re-pack it in the same manner as it was delivered.

Special care is necessary when handling or unpacking the product. See Special Handling and Unpacking Instruction.

Quality and Environmental Management

Kontron aims to deliver reliable high-end products designed and built for quality, and aims to complying with environmental laws, regulations, and other environmentally oriented requirements. For more information regarding Kontron's quality and environmental responsibilities, visit https://www.kontron.com/about-kontron/corporate-responsibility/quality-management.

Disposal and Recycling

Kontron's products are manufactured to satisfy environmental protection requirements where possible. Many of the components used are capable of being recycled. Final disposal of this product after its service life must be accomplished in accordance with applicable country, state, or local laws or regulations.

WEEE Compliance

The Waste Electrical and Electronic Equipment (WEEE) Directive aims to:

- Reduce waste arising from electrical and electronic equipment (EEE)
- Make producers of EEE responsible for the environmental impact of their products, especially when the product become waste
- Encourage separate collection and subsequent treatment, reuse, recovery, recycling and sound environmental disposal of EEE
- Improve the environmental performance of all those involved during the lifecycle of EEE

Environmental protection is a high priority with Kontron.

Kontron follows the WEEE directive

You are encouraged to return our products for proper disposal.

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1/ Introduction

This user guide describes the mITX-CFL-S board made by Kontron. This board will also be denoted mITX-CFL-S within this user guide.

Use of this user guide implies a basic knowledge of PC-AT hardware and software. This user guide focuses on describing the mITX-CFL-S board's special features and is not intended to be a standard PC-AT textbook.

New users are recommended to study the short installation procedure stated in the following chapter before switching on the power.

All configuration and setup of the CPU board is either carried out automatically or manually by the user via the BIOS setup menus.

Latest revision of this user guide, datasheet, thermal simulations, BIOS, drivers, BSP's (Board Support Packages), mechanical drawings (2D and 3D) can de download from Kontron's Web Page.

2/ Installation Procedures

2.1. Installing the Board

NOTICE

ESD Sensitive Device

Electrostatic discharge (ESD) can damage equipment and impair electrical circuitry.

- Wear ESD-protective clothing and shoes
- Wear an ESD-preventive wrist strap attached to a good earth ground
- Check the resistance value of the wrist strap periodically (1 MΩ to 10 MΩ)
- Transport and store the board in its antistatic bag
- Handle the board at an approved ESD workstation
- Handle the board only by the edges

To get the board running follow these steps. If the board shipped from KONTRON already has components like RAM and CPU cooler mounted, then skip the relevant steps below.

1. **Turn off the PSU (Power Supply Unit)**

NOTICE

Turn off PSU (Power Supply Unit) completely (no mains power connected to the PSU) or leave the Power Connectors unconnected while configuring the board. Otherwise, components (RAM, LAN cards etc.) might get damaged. Make sure to use a standard ATX12V PSU with suitable cable kits and PS-ON# active.

NOTICE

The power supply unit shall comply with the requirements as defined in IEC 62368-1 according Clause 6.2.2 to power source category PS2 "Limited Power Source".

2. **Insert the DDR4 U-DIMM 288-pin module(s)**

   Be careful to push the memory module in the slot(s) before locking the tabs. For a list of approved U-DIMMs contact your Distributor or FAE. See also chapter "System Memory Support". Use U-DIMM with the same memory density in both sockets!

3. **Processor installation**

   Install the processor in the processor socket. Follow the steps in the delivered manual from the processor manufacturer.

4. **Cooler installation**

   You can connect the cooler fan electrically to the CPU FAN connector.

5. **Connecting interfaces**

   Insert all external cables for hard disk, keyboard etc. A monitor must be connected in order to change BIOS settings.

6. **Connect and turn on PSU**

   Connect PSU to the board by the 2x4-pin ATX wafer connector.

7. **BIOS setup**

   Enter the BIOS setup by pressing the <DEL> key during boot up.

   Enter "Exit Menu" and Load Setup Defaults.

   Refer to the "BIOS Configuration / Setup" section of this manual for details on BIOS setup.

To clear all BIOS setting, including Password protection, activate "Clear CMOS Jumper" for 10 sec (without power connected).

8. **Mounting the board in chassis**

NOTICE

When mounting the board to chassis etc. please note that the board contains components on both sides of the PCB that can easily be damaged if board is handled without reasonable care. A damaged component can result in malfunction or no function at all.

When fixing the board on a chassis, it is recommended to use screws with an integrated washer and a diameter of > 7 mm. Do not use washers with teeth, as they can damage the PCB and cause short circuits.

2.2. Chassis Safety Standards

Before installing the mITX-CFL-S in the chassis, users must evaluate the end product to ensure compliance with the requirements of the IEC60950-1 safety standard:

- The board must be installed in a suitable mechanical, electrical and fire enclosure.
- The system, in its enclosure, must be evaluated for temperature and airflow considerations.
- The board must be powered by a CSA or UL approved power supply that limits the maximum input current.
- For interfaces having a power pin such as external power or fan, ensure that the connectors and wires are suitably rated. All connections from and to the product shall be with SELV circuits only.
- Wires have suitable rating to withstand the maximum available power.
- The peripheral device enclosure fulfils the IEC60950-1 fire protecting requirements.

2.3. Lithium Battery Replacement

If replacing the lithium battery follow the replacement precautions stated in the notification below:

⚠CAUTION

Danger of explosion if the lithium battery is incorrectly replaced.

- Replace only with the same or equivalent type recommended by the manufacturer
- Dispose of used batteries according to the manufacturer's instructions

VORSICHT! Explosionsgefahr bei unsachgemäßem Austausch der Batterie.

- Ersatz nur durch denselben oder einen vom Hersteller empfohlenen gleichwertigen Typ
- Entsorgung gebrauchter Batterien nach Angaben des Herstellers

ATTENTION! Risque d'explosion avec l'échange inadéquat de la batterie.

- Remplacement seulement par le même ou un type équivalent recommandé par le producteur
- L'évacuation des batteries usagées conformément à des indications du fabricant

PRECAUCION! Peligro de explosión si la batería se sustituye incorrectamente.

- Sustituya solamente por el mismo o tipo equivalente recomendado por el fabricante
- Disponga las baterías usadas según las instrucciones del fabricante

ADVARSEL! Lithiumbatteri – Eksplosionsfare ved fejlagtig håndtering.

- Udskiftning må kun ske med batteri af samme fabrikat og type

- Levér det brugte batteri tilbage til leverandøren

ADVARSEL! Eksplosjonsfare ved feilaktig skifte av batteri.

- Benytt samme batteritype eller en tilsvarende type anbefalt av apparatfabrikanten
- Brukte batterier kasseres i henhold til fabrikantens instruksjoner

VARNING! Explosionsfara vid felaktigt batteribyte.

- Använd samma batterityp eller en ekvivalent typ som rekommenderas av apparattillverkaren
- Kassera använt batteri enligt fabrikantens instruktion

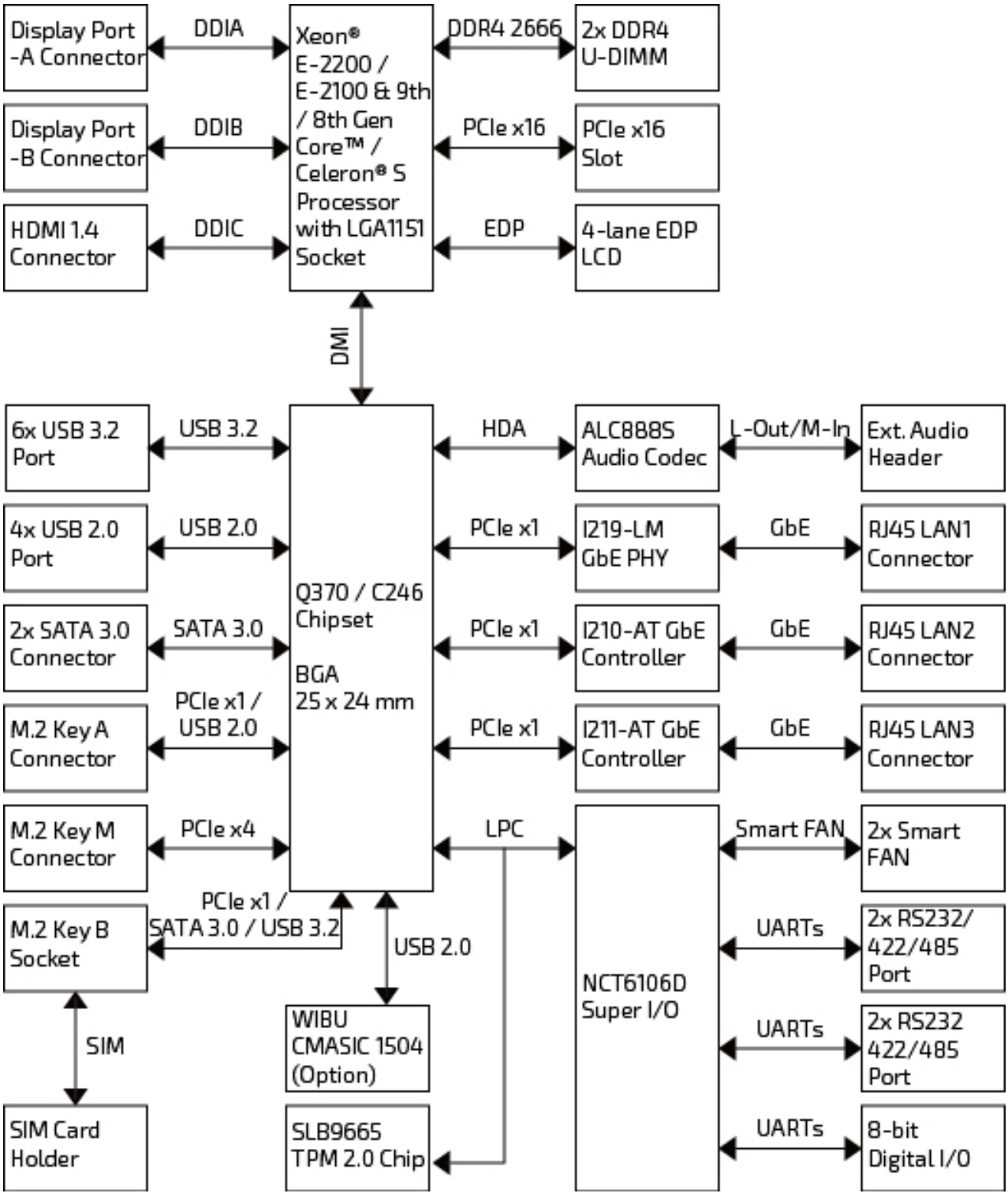
VAROITUS! Paristo voi räjähtää, jos se on virheellisesti asennettu.

- Vaihda paristo ainoastaan lalteval- mistajan suosittelemaan tyyppiln
- Hävitä käytetty paristo valmistajan ohjeiden mukaisesti

3/ System Specifications

3.1. System Block Diagram

Figure 1: System Block Diagram mITX-CFL-S



3.2. Component Main Data

The table below summarizes the features of the mITX-CFL-S motherboard.

Table 1: Component Main Data

System	
Processor	Intel® Xeon® E-2200 Series (LGA1151 socket, max. 35 W TDP support for 8 Core CPU) Intel® Xeon® E-2100 Series (LGA1151 socket) 9th Gen Intel® Core™ S-Series (LGA1151 socket, max. 35 W TDP support for 8 Core CPU) 8th Gen Intel® Core™ S-Series (LGA1151 socket) 8th Gen Intel® Celeron® S-Series (LGA1151 socket)
Chipset	Intel® C246 (Xeon®, Core™ & Celeron® CPU) Intel® Q370 (Core™ & Celeron® CPU)
Memory	2x DDR4 U-DIMM memory socket
Video	
Display Interface	1x eDP 1.4 2x DP (on rear) 1x HDMI 1.4 (on rear)
Multiple Display	Triple
Audio	
Audio Codec	Realtek ALC888S
Audio Interface	1x Line-out (by header) 1x Mic-in (by header) 1x S/PDIF (by header)
Network Connection	
Ethernet	3x GbE LAN (RJ45 on rear, 1x Intel® I219-LM, 1x Intel® I210-AT, 1x Intel® I211-AT)
Peripheral Connection	
USB	2x USB 3.2 Gen 2 (Type A on rear) 4x USB 32. Gen 1 (Type A on rear) 4x USB 2.0 (by header)
Serial Port	4x RS232/422/485 (2x DB9 on rear with 5 V /12 V power output support, 2x by header)
Other I/Os	8x DIO (by wafer)
Storage & Expansion	
Storage & Expansion	2x SATA 3.0 (RAID 0/1 support) 1x M.2 Key A (Type 2230, w/ PCIe x1 / USB 2.0) 1x M.2 Key B (Type 2242, w/ PCIe x1 / SATA 3.0 / USB 3.2 / UIM) 1x M.2 Key M (Type 2280, w/ PCIe x4) 1x PCIe x16 1x SIM Card Cage (Micro Type)
Power	
Connector & Input Voltage	2x4-pin ATX connector (DC 12 V)

Firmware	
BIOS	AMI uEFI BIOS w/ 128 Mb SPI Flash
Watchdog	Programmable WDT to generate system reset event
H/W Monitor	Input & Core Voltages CPU & System Temperatures
Real Time Clock	Chipset integrated RTC
Security	TPM 2.0 (Infineon SLB 9665)
System Control & Monitoring	
FP Header	1x Header for Reset button, HDD LED & External Speaker 1x Header for Power button, Power LED & SM bus 1x Header for M.2 Key A activity LED 1x Header for M.2 Key B activity LED 1x Header for M.2 Key M activity LED
Cooling	
FAN	1x Wafer for CPU Smart Fan 1x Wafer for System Smart Fan
Software	
OS Support	Windows 10 (Core™ i) Windows Server (Xeon® E)
Mechanical	
Dimension (L x W)	Mini-ITX (170 mm x 170 mm / 6.70" x 6.70")

3.3. Environmental Conditions

The mITX-CFL-S is compliant with the following environmental conditions. It is the customer's responsibility to provide sufficient airflow around each of the components to keep them within the allowed temperature range.

Table 2: Environmental Conditions

Operating Temperature	0 °C ~ 60 °C / 32 °F ~ 140 °F (Standard) -20 °C ~ 70 °C / -4 °F ~ 158 °F (Extended)
Storage Temperature	-20 °C ~ 80 °C / -4 °F ~ 176 °F (Standard) -40 °C ~ 85 °C / -40 °F ~ 185 °F (Extended)
Humidity	0 % ~ 95 %

3.4. Standards and Certifications

The mITX-CFL-S meets the following standards and certification tests.

Table 3: Standards and Certifications

CE Class A	EN 55032: 2015 + AC: 2016, CISPR 32: 2015 + COR1: 2016: Class A AS/NZS CISPR 32: 2015: Class A

	▶ EN 61000-3-2: 2014 and IEC 61000-3-2: 2014 ▶ EN 61000-3-3: 2013 and IEC 61000-3-3: 2013 ▶ EN 55024: 2010 + A1: 2015 and CISPR 24: 2010 + A1: 2015 ▶ EN 61000-4-2: 2009 and IEC 61000-4-2: 2008 ▶ EN 61000-4-3: 2006 + A1: 2008 + A2: 2010 and IEC 61000-4-3: 2006 + A1:2007 + A2: 2010 ▶ EN 61000-4-4: 2012 and IEC 61000-4-4: 2012 ▶ EN 61000-4-5: 2014 + A1: 2017 and IEC 61000-4-5: 2014 + A1: 2017 ▶ EN 61000-4-6: 2014 + AC: 2015 and IEC 61000-4-6: 2013 ▶ EN 61000-4-8: 2010 and IEC 61000-4-8: 2009 ▶ EN 61000-4-11: 2004 + A1: 2017 and IEC 61000-4-11: 2004 + A1: 2017
FCC Class A	▶ FCC CFR Title 47 Part 15 Subpart B: Section 15.107 and 15.109 ▶ ANSI C63.4-2014 ▶ Industry Canada Interference-Causing Equipment Standard ICES-003 Issue 6: 2016 ▶ Class A
UL	▶ UL 62368-1, 3rd Ed. 2021-10-22 ▶ CAN/CSA C22.2 No. 62368-1, 3rd Ed. 2021-10-22

3.5. Processor Support

The mITX-CFL-S is designed to support the following processors which are connected to a discrete Intel® C246 or Q370 Chipset Platform Controller Hub on the motherboard.

- 9th Intel® Core™ processors (FCLGA1151 Socket, TDP up to 65 W) for Q370 or C246 chipset
- 8th Intel® Core™ / Celeron® processors (FCLGA1151 Socket, TDP up to 95 W) for Q370 or C246 chipset
- Intel® Xeon® E-2200 Series processors (FCLGA1151 Socket, TDP up to 65 W) for C246 chipset
- Intel® Xeon® E-2100 Series processors (FCLGA1151 Socket, TDP up to 95 W) for C246 chipset

Sufficient cooling must be applied to the CPU in order to remove the effect defined as TDP (Thermal Design Power). The sufficient cooling is also depending on the worst case maximum ambient operating temperature and the actual worst case load of processor.

3.6. System Memory Support

The mITX-CFL-S has two DDR4 U-DIMM sockets. The sockets support the following memory features:

- 2x DDR4 U-DIMM, 1.2 V
- Up to 64 GB / 128 GB (2x 32 GB / 2x 64 GB) depending on processor and memory type
- Dual channel, 288-pin, 2400 / 2666 MT/s
- SPD timing supported
- ECC supported

The installed DDR4 U-DIMM should support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read and configure the memory controller for optimal performance. If non-SPD memory is used, the BIOS will attempt

to configure the memory settings, but performance and reliability may be impacted, or the board may not be able to boot totally.

3.6.1. Memory Operating Frequencies

In all modes, the frequency of system memory is the lowest frequency of all the memory modules placed in the system. Each memory module's frequency can be determined through the SPD registers on the memory modules.

The table below lists the resulting operating memory frequencies based on the combination of U-DIMMs and processor.

Table 4: Memory Operating Frequencies

SO-DIMM Type	Module Name	Memory Data Transfer (MT/s)	Processor System Bus Frequency (MHz)	Resulting Memory Clock Frequency (MHz)	Peak Transfer Rate (MB/s)
DDR4 2400	PC4-19200	2400	1200	300	19200
DDR4 2666	PC4-21333	2667	1333	333	21333

Memory modules have in general a much lower longevity than embedded motherboards, and therefore EOL of modules can be expected several times during lifetime of the motherboard.

As a minimum it is recommend using Kontron memory modules for prototype system(s) in order to prove stability of the system and as for reference.

For volume production you might request to test and qualify other types of RAM. In order to qualify RAM it is recommend configuring 3 systems running RAM Stress Test program in heat chamber at 60° C for a minimum of 24 hours.

3.7. On-board Graphics Subsystem

The mITX-CFL-S supports Intel® UHD Graphics technology for high quality graphics capabilities. All mITX-CFL-S versions support three displays pipes.

Up to three displays can be used simultaneously and be used to implement independent or cloned display configuration.

Table 5: Three-displays Configurations

Display 1	Display 2	Display 3	Max. Resolution (Px) at 60 Hz		
			Display 1	Display 2	Display 3
eDP	DP	DP	4096 x 2304	4096 x 2304	4096 x 2304
eDP	DP	HDMI	4096 x 2304	4096 x 2304	2560 x 1600
DP	DP	HDMI	4096 x 2304	4096 x 2304	2560 x 1600

3.8. Power Supply

In order to ensure safe operation of the board, the input power supply must monitor the supply voltage and shut down if the supply is out of range – refer to the actual power supply specification. Please note, in order to keep the power consumption to a minimal level, boards do not implement a guaranteed minimum load. In some cases, this can lead to compatibility problems with ATX power supplies that require a minimum load to stay in regulation. The mITX-CFL-S board must be powered through the ATX+12V-8p (8-pole) connector using standard ATX12V power supply.

ATX12V supply: ATX+12V-8p connector must be used in according to the ATX12V PSU standard.

NOTICE **Hot Plugging power supply is not supported. Hot plugging might damage the board.**

The requirements to the voltages of ATX power supply are as follows:

Table 6: Supply Voltages

Supply	Min.	Max.	Note
+12 V	11.4 V	12.6 V	Should be ±5% for compliance with the ATX specification

4/ Connector Locations

4.1. Top Side

Figure 2: Top Side

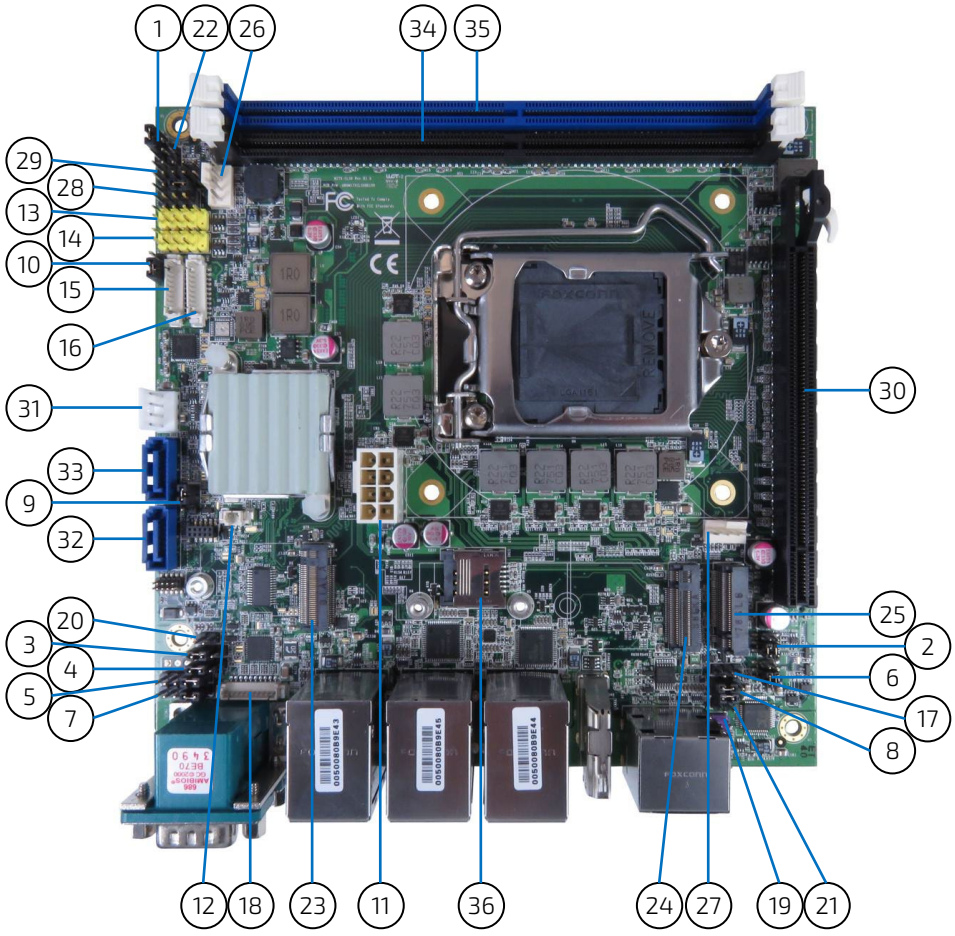


Table 7: Jumper List

Item	Designation	Description	See Chapter
1	JP2	ME F/W Selection	7.18.1
2	JP4	Backlight Power Enable Selection for eDP1	7.18.2
3	JP5	AT / ATX Power Mode Selection	7.18.3
4	JP7	RTC Reset Selection	7.18.4
5	JP8	Pin-9 Selection for COM2	7.18.5
6	JP9	Panel & Backlight Power Selection for eDP1	7.18.6
7	JP10	Pin-9 Selection for COM1	7.18.7
8	JP11	PCIE Configuration Setting for PEG1	7.18.8
9	JP13	USB Power Selection	7.18.9
10	JP14	M.2 Key B Function Selection	7.18.10

Table 8: Top Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter

Item	Designation	Description	See Chapter
11	ATX1	2x4-pin ATX Power Supply Wafer	7.1.1
12	BAT1	CR2032 Battery Power Input Wafer	7.1.2
13	CN1	USB 2.0 Port 13, 14 Pin Header	7.5
14	CN2	USB 2.0 Port 7, 8 Pin Header	7.5
15	CN3	RS-232/422/485 Port 4 Wafer	7.9
16	CN4	RS-232/422/485 Port 3 Wafer	7.9
17	CN6	SPDIF-Out Pin Header	7.7
18	CN7	8-bit Digital Input / Output Pin Header	7.11
19	CN11	Front Panel Audio Pin Header	7.6
20	CN14	M.2 Key A Activity LED Indication Pin Header	7.17
21	CN15	M.2 Key B Activity LED Indication Pin Header	7.17
22	CN16	M.2 Key M Activity LED Indication Pin Header	7.17
23	M2A1	M.2 Key A Slot	7.12
24	M2B1	M.2 Key B Slot	7.13
25	M2M1	M.2 Key M Slot (only support PCIe)	7.14
26	FAN1	System FAN Wafer	7.2
27	FAN2	CPU FAN Wafer	7.2
28	FP1	Front Panel Pin Header 1	7.8
29	FP2	Front Panel Pin Header 2	7.8
30	PEG1	PCIEx16 Slot	7.16
31	CN17	HDD Power Wafer	7.4
32	SATA1	Serial ATA Port-0 Connector	7.3
33	SATA2	Serial ATA Port-1 Connector	7.3
34	DIMM1	DDR4 Memory U-DIMM Socket	3.6
35	DIMM2	DDR4 Memory U-DIMM Socket	3.6
36	SIM1	Micro SIM Interface Slot for M.2 Key B	7.15

4.2. Bottom Side

Figure 3: Bottom Side

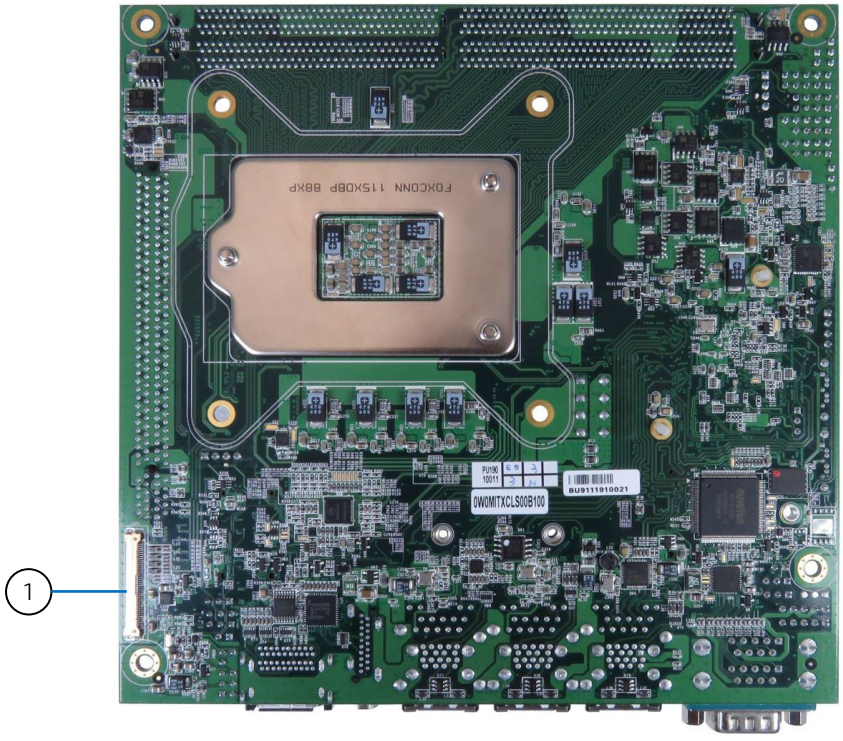


Table 9: Bottom Side Internal Connector Pin Assignment

Item	Designation	Description	See Chapter
1	EDP1	eDP Connector	7.10

4.3. Connector Panel Side

Figure 4: Connector Panel Side

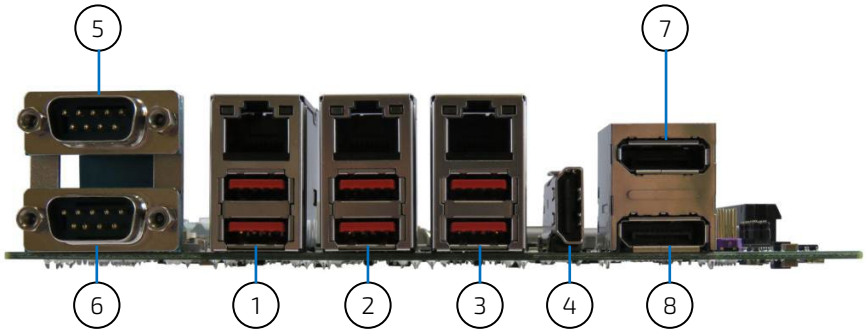


Table 10: Connector Panel Side Connector List

Item	Designation	Description	See Chapter
1	CN8	GbE LAN1 & USB 3.2 Gen 1 Port-1, 2 Connector	6.3 & 6.4
2	CN9	GbE LAN2 & USB 3.2 Gen 1 Port-3, 4 Connector	6.3 & 6.4
3	CN10	GbE LAN3 & USB 3.2 Gen 2 Port-5, 6 Connector	6.3 & 6.4
4	HDMI1	HDMI 1.4 Connector	6.2
5	CN13TOP	RS-232/422/485 COM2 Connector	6.5
6	CN13BOT	RS-232/422/485 COM1 Connector	6.5
7	CN12TOP	Display Port A Connector	6.1
8	CN12BOT	Display Port B Connector	6.1

5/ Connector Definitions

The following defined terms are used within this user guide to give more information concerning the pin assignment and to describe the connector's signals.

Defined Term	Description
Pin	Shows the pin numbers in the connector
Signal	The abbreviated name of the signal at the current pin The notation "XX#" states that the signal "XX" is active low
Note	Special remarks concerning the signal
Designation	Type and number of item described
See Chapter	Number of the chapter within this user guide containing a detailed description

The abbreviation TBD is used for specifications that are not available yet or which are not sufficiently specified by the component vendors.

6/ I/O-Area Connectors

6.1. DP Connector (CN12TOP & CN12BOT)

The DP (DisplayPort) connector is based on standard DP female port.

Figure 5: DP Connector CN12TOP, CN12BOT

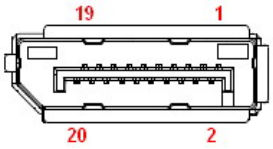


Table 11: Pin Assignment DP Connector CN12TOP, CN12BOT

Pin	Signal	Description	Note
1	TX0+		
2	GND		
3	TX0-		
4	TX1+		
5	GND		
6	TX1-		
7	TX2+		
8	GND		
9	TX2-		
10	TX3+		
11	GND		
12	TX3-		
13	DP_EN		
14	GND		
15	AUX+		
16	GND		
17	AUX-		
18	HPD		
19	GND		
20	PWR		

6.2. HDMI Connector (HDMI1)

The HDMI connector is based on standard HDMI type A and is HDMI 1.4 compatible.

Figure 6: HDMI Connector HDMI1

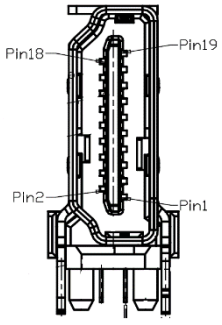


Table 12: Pin Assignment HDMI Connector HDMI1

Pin	Signal	Description	Note
1	TMD_DATA2+		
2	GND		
3	TMD_DATA2–		
4	TMD_DATA1+		
5	GND		
6	TMD_DATA1–		
7	TMD_DATA0+		
8	GND		
9	TMD_DATA0–		
10	TMD_CLK+		
11	GND		
12	TMD_CLK–		
13	CEC		
14	RESERVED		
15	DDC_CLK		
16	DDC_DATA		
17	GND		
18	5 V		
19	HPET		

6.3. Ethernet Connectors (CN8 - LAN1, CN9 - LAN2 & CN10 - LAN3)

The mITX-CFL-S supports three channels of 10/100/1000 Mbit Ethernet, which are based Intel® I219-LM and Intel® I210-AT controllers.

In order to achieve the specified performance of the Ethernet port, Category 5 twisted pair cables must be used with 10/100 MByte and Category 5E, 6 or 6E with 1 Gbit LAN networks.

The signals for the Ethernet ports are as follows:

Figure 7: Ethernet Connectors CN8 - LAN1, CN9 - LAN2, CN10 - LAN3

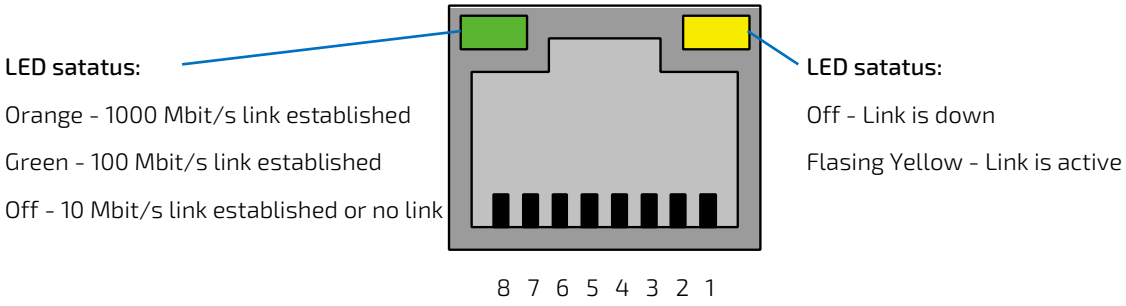


Table 13: Pin Assignment Ethernet Connectors CN8 - LAN1, CN9 - LAN2, CN10 - LAN3

Pin	Signal	Description
1	MDI[0]+	In MDI mode, this is the first pair in 1000Base-T, i.e. the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX.
2	MDI[0]-	
3	MDI[1]+	In MDI mode, this is the second pair in 1000Base-T, i.e. the BI_DB+/- pair, and is the receive pair in 10Base-T and 100Base-TX. In MDI crossover mode, this pair acts as the BI_DA+/- pair, and is the transmit pair in 10Base-T and 100Base-TX.
4	MDI[1]-	
5	MDI[2]+	In MDI mode, this is the third pair in 1000Base-T, i.e. the BI_DC+/- pair. In MDI crossover mode, this pair acts as the BI_DD+/- pair.
6	MDI[2]-	
7	MDI[3]+	In MDI mode, this is the fourth pair in 1000Base-T, i.e. the BI_DD+/- pair. In MDI crossover mode, this pair acts as the BI_DC+/- pair.
8	MDI[3]-	

'MDI' – media dependent Interface

6.4. USB Connectors (I/O Area)

The external I/O connector panel supports one dual USB 3.2 Gen 2 and two dual USB 3.2 Gen 1 connectors.

USB 3.2 Gen 2 ports are backward compatible with USB 3.2 Gen 1 and USB 2.0.
USB 3.2 Gen 1 ports are backward compatible with USB 2.0.

Figure 8: USB 3.2 Gen 1 Connector CN8 - USB Port 1 / 2, CN9 - USB Port 3 / 4 & USB 3.2 Gen 2 Connector CN10 - USB Port 5 / 6

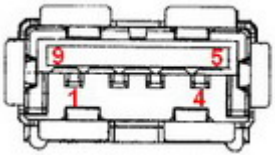
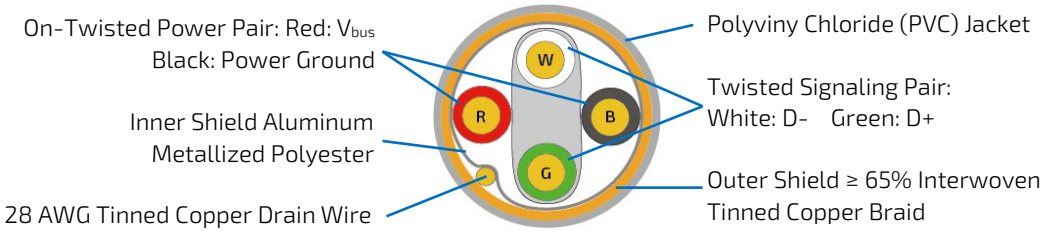


Table 14: Pin Assignment USB 3.2 Gen 1 Connector CN8 - USB Port 1 / 2, CN9 - USB Port 3 / 4 & USB 3.2 Gen 2 Connector CN10 - USB Port 5 / 6

Pin	Signal	Note
1	+USBVCC	+5 V Supply for USB device
2	USB_A-	USB 2.0 Differential Pair (-)
3	USB_A+	USB 2.0 Differential Pair (+)
4	GND	
5	USB3_SSRX-	USB 3.2 Gen 1 / 2 Rx. Differential Pair (-)
6	USB3_SSRX+	USB 3.2 Gen 1 / 2 Rx. Differential Pair (+)
7	GND	
8	USB3_SSTX-	USB 3.2 Gen 1 / 2 Tx. Differential Pair (-)
9	USB3_SSTX+	USB 3.2 Gen 1 / 2 Tx. Differential Pair (+)

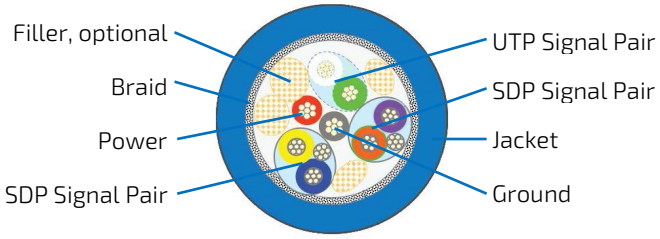
For HiSpeed rates it is required to use a USB cable, which is specified in USB 2.0 standard:

Figure 9: USB 2.0 High Speed Cable



For USB 3.2 Gen 1 / 2 cabling it is required to use only HiSpeed USB cable, specified in USB 3.2 standard:

Figure 10: USB 3.2 High Speed Cable



6.5. Serial COM1 & COM2 Ports (CN13BOT & CN13TOP)

The external I/O connector panel supports one dual DB-9 RS-232/422/485 COM male ports.

Figure 11: Serial COM1 & COM2 Ports CN13BOT, CN13TOP

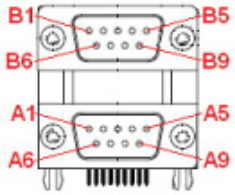


Table 15: Pin Assignment Serial COM1 & COM2 Ports CN13BOT, CN13TOP

Pin	RS232 Signal	RS422 Signal	Half Duplex RS485 Signal	Full Duplex RS485 Signal	Note
Top (COM2)					
B1	DCD	TX-	DATA-	TX-	
B2	RXD	TX+	DATA+	TX+	
B3	TXD	RX+	N/A	RX+	
B4	DTR	RX-	N/A	RX-	
B5	GND	GND	GND	GND	
B6	DSR	N/A	N/A	N/A	
B7	RTS	N/A	N/A	N/A	
B8	CTS	N/A	N/A	N/A	
B9	RI*	N/A	N/A	N/A	
Bottom (COM1)					
A1	DCD	TX-	DATA-	TX-	
A2	RXD	TX+	DATA+	TX+	
A3	TXD	RX+	N/A	RX+	
A4	DTR	RX-	N/A	RX-	
A5	GND	GND	GND	GND	
A6	DSR	N/A	N/A	N/A	
A7	RTS	N/A	N/A	N/A	
A8	CTS	N/A	N/A	N/A	
A9	RI*	N/A	N/A	N/A	

***: Pin configuration can be selected by Jumper JP10 (for COM1) and JP8 (for COM2).**

RS232 / 422 / 485 can be selected in BIOS setup.

Table 16: Signal Description

Signal	Description
TXD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RXD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish communication link.
DSR	Data Set Ready, indicates that the modem etc. is ready to establish a communications link.
RTS	Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.
TX+/-	Transmitted Data differential pair sends data to the communications link.
RX+/-	Received Data differential pair receives data from the communications link.
GND	Power Supply GND signal

7/ Internal Connectors

7.1. Power Connector

The mITX-CFL-S is designed to be supplied from a 2x4-pin +12 VDC power supply.

NOTICE

Hot plugging any of the power connector is not allowed.

Hot plugging might damage the board. In other words, turn off main supply etc. to make sure all the power lines are turned off when connecting to the motherboard.

7.1.1. 2x4-pin ATX Power Supply Wafer (ATX1)

Figure 12: 2x4-pin ATX Power Supply Wafer ATX1

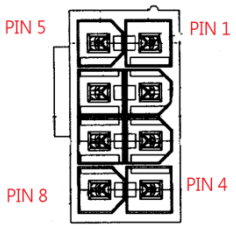


Table 17: Pin Assignment ATX1

Pin	Signal	Description
1	GND	Ground
2	GND	Ground
3	GND	Ground
4	GND	Ground
5	+12V	Power +12 V
6	+12V	Power +12 V
7	+12V	Power +12 V
8	+12V	Power +12 V
Connector Type		
B2W, 2x4-pin, 4.2 mm pitch		
Mating Connector		
Vendor	Joint Tech	
Housing Model No.	C4255HF-2*4P(5557)	
Terminal Model No.	C4255HF-TB	

7.1.2. CR2032 Battery Power Input Wafer (BAT1)

Figure 13: CR2032 Battery Power Input Wafer BAT1

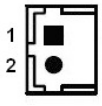


Table 18: Pin Assignment BAT1

Pin	Signal	Description
1	Battery+	
2	Battery-	
Connector Type		
B2W, 1x2-pin, 1.25 mm pitch		
Mating Connector		
Vendor	Pinrex	
Housing Model No.	712-75-02W001	
Terminal Model No.	712-70-T00001	

7.2. Fan Wafers (FAN1 & FAN2)

The CPU FAN Wafer (FAN2) is used for the connection of the FAN for the CPU while the System FAN Wafer (FAN1) for the connection of the FAN for the system.

Figure 14: Fan Wafer FAN1, FAN2

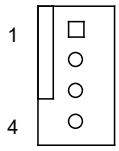


Table 19: Pin Assignment FAN1, FAN2

Pin	Signal	Description
1	GND	Power supply ground signal
2	+12V	+12 V power supply for fan
3	SENSE	Sense input signal from the fan, for rotation speed supervision RPM (Rotations Per Minute). The signal shall be generated by an open collector transistor or similar.
4	PWM	PWM output signal for FAN speed control
Connector Type		
B2W, 1x4-pin, 2.54 mm pitch		

7.3. SATA (Serial ATA) Disk Interfaces (SATA1 & SATA2)

The SATA connectors supply the data connection for the SATA hard disk and are SATA 3.0 compatible.

Figure 15: SATA Connector SATA1, SATA2

Table 20: Pin Assignment SATA1, SATA2

Pin	Signal	Description
1	GND	Ground
2	TX+	Host receiver differential signal pair (+)
3	TX-	Host receiver differential signal pair (-)
4	GND	Ground
5	RX-	Host transmitter differential signal pair (-)
6	RX+	Host transmitter differential signal pair (+)
7	GND	Ground
Connector Type		
B2W, 1x7-pin, 1.27 mm pitch		
Mating Connector		
Vendor	WINWIN	
Model No.	WATC-07DLP02U	

7.4. HDD Power Wafer (CN17)

Figure 16: HDD Power Wafer CN17

Table 21: Pin Assignment CN17

Pin	Signal	Description
1	+12V	12 V power supply
2	GND	Ground
3	GND	Ground
4	+5V	5 V power supply
Connector Type		
B2W, 1x4-pin, 2.5 mm pitch		
Mating Connector		
Vendor **Housing Model No.** **Terminal Model No.**	Joint Tech A2540H-4P A2540-TB	

7.5. USB Connectors (Internal) (CN1 & CN2)

The USB 2.0 Port 7 and 8 are supplied via the internal pin header (CN2).

The USB 2.0 Port 13 and 14 are supplied via the internal pin header (CN1).

Figure 17: USB 2.0 Port Pin Header CN1, CN2

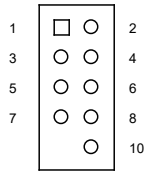


Table 22: Pin Assignment CN1

Pin	Signal	Description
1	+USBVCC	5 V supply for external devices. Protected by active power switch 1 A fuse for each USB port.
2	+USBVCC	5 V supply for external devices. Protected by active power switch 1 A fuse for each USB port.
3	USB_A-	Universal Serial Bus Differentials: Bus Data / Address / Command Bus.
4	USB_B-	Universal Serial Bus Differentials: Bus Data / Address / Command Bus.
5	USB_A+	Universal Serial Bus Differentials: Bus Data / Address / Command Bus.
6	USB_B+	Universal Serial Bus Differentials: Bus Data / Address / Command Bus.
7	GND	Ground
8	GND	Ground
9	KEY	
10	GND	Ground
Connector Type		
B2W, 2x5-pin, 2.54 mm pitch		
Mating Connector		
Vendor	Pinrex	
Housing Model No.	741-75-205B01	
Terminal Model No.	741-70-FT0001	

Table 23: Pin Assignment CN2

Pin	Signal	Description
1	+USBVCC_SB	5 V supply for external devices. SB5V is supplied during power down to allow wakeup on USB device activity. Protected by active power switch 1 A fuse for each USB port.
2	+USBVCC_SB	5 V supply for external devices. SB5V is supplied during power down to allow wakeup on USB device activity. Protected by active power switch 1 A fuse for each USB port.
3	USB_A-	Universal Serial Bus Differentials: Bus Data / Address / Command Bus.
4	USB_B-	Universal Serial Bus Differentials: Bus Data / Address / Command Bus.
5	USB_A+	Universal Serial Bus Differentials: Bus Data / Address / Command Bus.
6	USB_B+	Universal Serial Bus Differentials: Bus Data / Address / Command Bus.
7	GND	Ground

Pin	Signal	Description
8	GND	Ground
9	KEY	
10	GND	Ground
Connector Type		
B2W, 2x5-pin, 2.54 mm pitch		
Mating Connector		
Vendor	Pinrex	
Housing Model No.	741-75-205B01	
Terminal Model No.	741-70-FT0001	

7.6. Front Panel Audio Pin Header (CN11)

The front panel audio pin header provides audio output (Line-Out) and microphone (Mic-In) signals through the pin header CN11.

Figure 18: Front Panel Audio Pin Header CN11

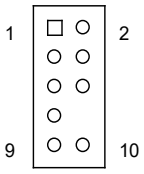


Table 24: Pin Assignment CN11

Pin	Signal	Note
1	MIC2-L	
2	Audio GND	
3	MIC2-R	
4	Audio GND	
5	Line2-R	
6	MIC2_JD	
7	Audio GND	
8	KEY	
9	Line2-L	
10	Line2_JD	
Connector Type		
B2W, 2x5-pin, 2.54 mm pitch		
Mating Connector		
Vendor	Joint Tech	
Housing Model No.	A2546H-2*6P	
Terminal Model No.	WL6008-G-P	

7.7. S/PDIF Out Pin Header (CN6)

The S/PDIF audio output jack is supplied via the internal pin header (CN6).

Figure 19: S/PDIF Out Pin Header CN6

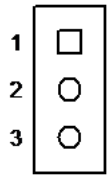


Table 25: Pin Assignment CN6

Pin	Signal	Note
1	SPDIF-out	
2	+VSPDIF	
3	GND	
Connector Type		
B2W, 1x3-pin, 2.54 mm pitch		
Mating Connector		
Vendor	Joint Tech	
Housing Model No.	A2546H-2P	
Terminal Model No.	WL6008-G-P	

7.8. Front Panel Pin Header (FP1 & FP2)

Figure 20: Front Panel Pin Header FP1

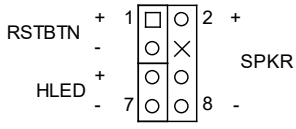


Table 26: Pin Assignment FP1

Pin	Signal	Note
1	Reset Button +	Reset Button. This 2-pin connector is for chassis mounted reset button for system reboot without turning off the system power.
2	Speaker +	System warning speaker. The speaker allows user to hear beeps and warnings.
3	Reset Button -	Reset Button. This 2-pin connector is for chassis mounted reset button for system reboot without turning off the system power.
4	NC	
5	HDD LED +	Hard Disk Drive Activity LED. This 2-pin connector is for HDD Activity LED. Connect the HDD Activity LED cable to this connector. The HDD LED lights up or flashes when data is read from or written to the HDD.
6	Internal Speaker -	System warning speaker. The speaker allows user to hear beeps and warnings.
7	HDD LED -	Hard Disk Drive Activity LED. This 2-pin connector is for HDD Activity LED. Connect the HDD Activity LED cable to this connector. The HDD LED lights up or flashes when data is read from or written to the HDD.
8	Speaker -	System warning speaker. The speaker allows user to hear beeps and warnings.
Connector Type		
B2W, 2x4-pin, 2.54 mm pitch		
Mating Connector		
Vendor	Pinrex	
Housing Model No.	741-75-204B01	
Terminal Model No.	741-70-FT0001	

Internal Buzzer is enabled when Pin6-8 is shorted.

Figure 21: Front Panel Pin Header FP2

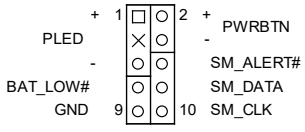


Table 27: Pin Assignment FP2

Pin	Signal	Description
1	Power LED +	System Power LED. The power LED lights up when users turn on the system power, and

Pin	Signal	Description
		blinks when the system is in sleep mode.
2	Power Button +	The 2-pin connector is for the system power button. Pressing the power button turns the system on or puts the system in sleep or soft-off mode depending on the operating system settings. Pressing the power switch for more than four seconds while the system turns from ON to OFF.
3	NC	
4	Power Button -	The 2-pin connector is for the system power button. Pressing the power button turns the system on or puts the system in sleep or soft-off mode depending on the operating system settings. Pressing the power switch for more than four seconds while the system turns from ON to OFF.
5	Power LED -	System Power LED. The power LED lights up when users turn on the system power, and blinks when the system is in sleep mode.
6	SM_ALERT#	System Management Bus Alert
7	BAT_LOW#	Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used to signal some other external power management event.
8	SMBus Data	System Management Bus bidirectional data line
9	GND	Ground
10	SMBus Clock	System Management Bus bidirectional clock line
Connector Type		
B2W, 2x5-pin, 2.54 mm pitch		
Mating Connector		
Vendor	Pinrex	
Housing Model No.	741-75-205B01	
Terminal Model No.	741-70-FT0001	

7.9. Serial COM3 & COM4 Ports (CN4 & CN3)

Figure 22: Serial COM CN4, CN3

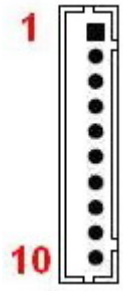


Table 28: Pin Assignment CN4, CN3

Pin	RS232 Signal	RS422 Signal	Half Duplex RS485 Signal	Full Duplex RS485 Signal	Note
1	DCD	TX-	DATA-	TX-	
2	DSR	TX+	DATA+	TX+	
3	RXD	RX+	N/A	RX+	
4	RTS	RX-	N/A	RX-	
5	TXD	N/A	N/A	N/A	
6	CTS	N/A	N/A	N/A	
7	DTR	N/A	N/A	N/A	
8	RI	N/A	N/A	N/A	
9	GND	GND	GND	GND	
10	+5V	N/A	N/A	N/A	
Connector Type					
B2W, 1x10-pin, 1.25 mm pitch					

Table 29: Signal Description

Signal	Description
TXD	Transmitted Data, sends data to the communications link. The signal is set to the marking state (-12 V) on hardware reset when the transmitter is empty or when loop mode operation is initiated.
RXD	Received Data, receives data from the communications link.
DTR	Data Terminal Ready, indicates to the modem etc. that the on-board UART is ready to establish communication link.
DSR	Data Set Ready, indicates that the modem etc. is ready to establish a communications link.
RTS	Request To Send, indicates to the modem etc. that the on-board UART is ready to exchange data.
CTS	Clear To Send, indicates that the modem or data set is ready to exchange data.
DCD	Data Carrier Detect, indicates that the modem or data set has detected the data carrier.
RI	Ring Indicator, indicates that the modem has received a ringing signal from the telephone line.
TX+/-	Transmitted Data differential pair sends data to the communications link.
RX+/-	Received Data differential pair receives data from the communications link.
GND	Power Supply GND signal

7.10. eDP Panel Connector (EDP1)

The eDP connector is based on 40-pin connector type and supports quad-channel eDP cable for LCD panel / display.

Figure 23: eDP Connector EDP1

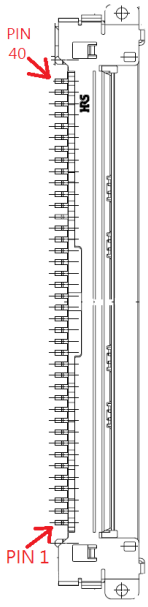


Table 30: Pin Assignment EDP1

Pin	Signal	Description
1	NC	
2	GND	Ground
3	ML3-	eDP Channel 3 differential pair (-)
4	ML3+	eDP Channel 3 differential pair (+)
5	GND	Ground
6	ML2-	eDP Channel 2 differential pair (-)
7	ML2+	eDP Channel 2 differential pair (+)
8	GND	Ground
9	ML1-	eDP Channel 1 differential pair (-)
10	ML1+	eDP Channel 1 differential pair (+)
11	GND	Ground
12	ML0-	eDP Channel 0 differential pair (-)
13	ML0+	eDP Channel 0 differential pair (+)
14	LCD_TEST	
15	AUX+	eDP auxiliary channel differential pair (+)
16	AUX-	eDP auxiliary channel differential pair (-)
17	GND	Ground
18	LCD_VCC(3/5V)*	eDP LCD panel power (3 V / 5 V)
19	LCD_VCC(3/5V)*	eDP LCD panel power (3 V / 5 V)
20	LCD_VCC(3/5V)*	eDP LCD panel power (3 V / 5 V)

Pin	Signal	Description
21	LCD_VCC(3/5V)*	eDP LCD panel power (3 V / 5 V)
22	LCD_TEST	
23	GND	Ground
24	GND	Ground
25	GND	Ground
26	GND	Ground
27	HOT PLUG DETECT	
28	GND	Ground
29	GND	Ground
30	GND	Ground
31	GND	Ground
32	BL_ENABLE**	eDP backlight enable signal
33	BL_PWM	eDP backlight PWM (Pulse Width Modulation) signal
34	NC	
35	NC	
36	BL_PWR(12/5V)*	eDP backlight power (12 V / 5 V)
37	BL_PWR(12/5V)*	eDP backlight power (12 V / 5 V)
38	BL_PWR(12/5V)*	eDP backlight power (12 V / 5 V)
39	BL_PWR(12/5V)*	eDP backlight power (12 V / 5 V)
40	NC	
Connector Type		
B2W, 1x40-pin, 0.5 mm pitch		
Mating Connector		
Vendor	I-PEX	
Housing Model No.	20454-040T	
Terminal Model No.	20453-040T	

* **Panel and backlight power can be selected by JP9.**

** **BL_ENABLE can be selected by JP4.**

7.11. Digital Input / Output Wafer (CN7)

Figure 24: Digital Input / Output Wafer CN7

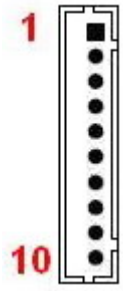


Table 31: Pin Assignment CN7

Pin	Signal	Note
1	+5V	
2	DIO_0	
3	DIO_1	
4	DIO_2	
5	DIO_3	
6	DIO_4	
7	DIO_5	
8	DIO_6	
9	DIO_7	
10	GND	
Connector Type		
B2W, 1x10-pin, 1.25 mm pitch		
Mating Connector		
Vendor **Housing Model No.** **Terminal Model No.**	Pinrex 712-75-10W001 712-70-T00001	

7.12. M.2 Key A Slot (M2A1)

The mITX-CFL-S has an M.2 Key A slot for a Type 2230 module. The M.2 specification supports PCIe x1 and USB 2.0. Intentionally it is reserved for wireless connectivity, such as Wi-Fi, Bluetooth, NFC or a comb of some or all.

Figure 25: M.2 Key A Slot M2A1

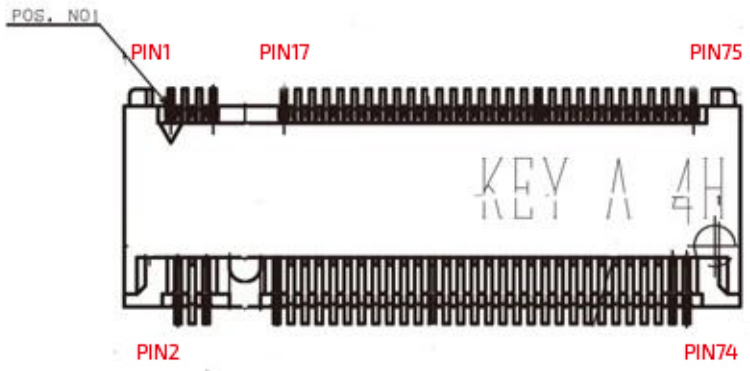


Table 32: Pin Assignment M2A1

Pin	Signal	Description
1	GND	Ground
2	+3.3V	3.3 V power supply
3	USB-D+	USB 2.0 data differential pair (+)
4	+3.3V	3.3 V power supply
5	USB-D-	USB 2.0 data differential pair (-)
6	LED1#	Device active signal
7	GND	Ground
8	KEY A	
9	KEY A	
10	KEY A	
11	KEY A	
12	KEY A	
13	KEY A	
14	KEY A	
15	KEY A	
16	LED2#	Device active signal
17	MLDIR_SENSE	
18	GND	Ground
19	NC	
20	NC	
21	NC	
22	NC	
23	GND	Ground
24	GND	Ground

Pin	Signal	Description
25	NC	
26	NC	
27	NC	
28	NC	
29	GND	Ground
30	GND	Ground
31	NC	
32	NC	
33	GND	Ground
34	NC	
35	PET0+	PCIe Lane 0 module transmitter pair (+)
36	GND	Ground
37	PET0-	PCIe Lane 0 module transmitter pair (-)
38	NC	
39	GND	Ground
40	NC	
41	PER0+	PCIe Lane 0 module receiver pair (+)
42	NC	
43	PER0-	PCIe Lane 0 module receiver pair (-)
44	NC	
45	GND	Ground
46	NC	
47	REFCLK0+	PCIe Lane 0 reference clock pair (+)
48	NC	
49	REFCLK0-	PCIe Lane 0 reference clock pair (-)
50	SUSCLK	32.768 kHz clock module input
51	GND	Ground
52	PERST0#	PCIe Lane 0 fundamental reset
53	CLKREQ0#	Clock request
54	W_DISABLE2	Wireless disable 2
55	PEWAKE0#	PCIe Lane 0 wake
56	W_DISABLE1	Wireless disable 1
57	GND	Ground
58	NC	
59	NC	
60	NC	
61	NC	
62	ALERT	
63	GND	Ground
64	Reserved	
65	NC	
66	PERST1	PCIe Lane 1 fundamental reset

Pin	Signal	Description
67	NC	
68	CLKREQ	Clock request
69	GND	Ground
70	PEWAKE1	PCIe Lane 1 wake
71	NC	
72	+3.3V	3.3 V power supply
73	NC	
74	+3.3V	3.3 V power supply
75	GND	Ground

7.13. M.2 Key B Slot (M2B1)

The mITX-CFL-S has an M.2 Key B slot for a Type 2242 module. The M.2 specification supports PCIe x1 / SATA 3.0, USB 3.2 and UIM. The switch between PCIe x2 and SATA 3.0 can be selected via the jumper (JP14). Intentionally the slot is reserved for M.2 SSD storage or WWAN (3G, 4G ...) connectivity.

Figure 26: M.2 Key B Slot M2B1

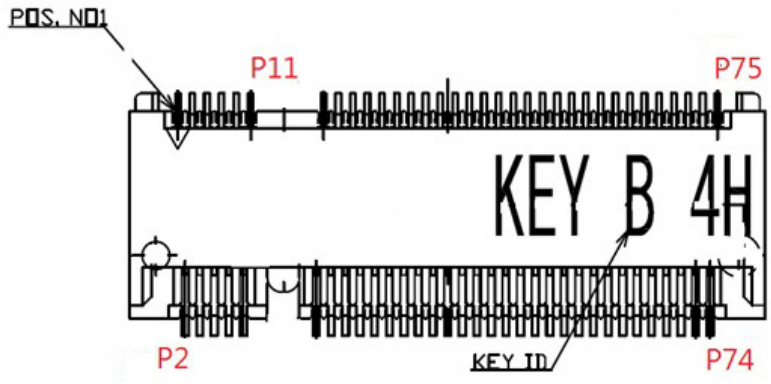


Table 33: Pin Assignment M2B1

Pin	Signal	Description
1	CONFIG3	Define module type
2	+3.3V	3.3 V power supply
3	GND	Ground
4	+3.3V	3.3 V power supply
5	GND	Ground
6	FULL CARD PWR OFF	M.2 module power enable
7	USB-D+	USB 2.0 differential pair (+)
8	W DISABLE#1	Wireless disable 1
9	USB-D-	USB 2.0 differential pair (-)
10	GPIO9	
11	GND	Ground
12	KEY B	
13	KEY B	
14	KEY B	
15	KEY B	
16	KEY B	
17	KEY B	
18	KEY B	
19	KEY B	
20	NC	
21	CONFIG0	Define module type
22	NC	
23	NC	

Pin	Signal	Description
24	NC	
25	NC	
26	NC	
27	GND	Ground
28	NC	
29	USB3.1_RX-	USB 3.2 receiver differential pair (-)
30	UIM RESET	SIM card reset
31	USB3.1_RX+	USB 3.2 receiver differential pair (+)
32	UIM CLK	SIM card clock
33	GND	Ground
34	UIM DATA	SIM card data
35	USB3.1_TX-	USB 3.2 transmitter differential pair (-)
36	UIM PWR	SIM card power
37	USB3.1_TX+	USB 3.2 transmitter differential pair (+)
38	DEVSLP	Device sleep
39	GND	Ground
40	NC	
41	PETn0/SATAB+	PCIe Lane 0 transmitter pair (-) / SATA transmitter differential pair (+)
42	NC	
43	PETp0/SATAB-	PCIe Lane 0 transmitter pair (+) / SATA transmitter differential pair (-)
44	NC	
45	GND	Ground
46	NC	
47	PERn0/SATAA-	PCIe Lane 0 receiver pair (-) / SATA receiver differential pair (-)
48	NC	
49	PERp0/SATAA+	PCIe Lane 0 receiver pair (+) / SATA receiver differential pair (+)
50	PERST	PCIe reset
51	GND	Ground
52	CLKREQ	Reference clock request signal
53	REFCLKN	PCIe reference clock pair (-)
54	PEWAKE	PCIe wake
55	REFCLKP	PCIe reference clock pair (+)
56	NC	
57	GND	Ground
58	NC	
59	NC	
60	NC	
61	NC	
62	NC	
63	NC	
64	NC	
65	NC	

Pin	Signal	Description
66	SIM DETECT	SIM card detect
67	NC	
68	SUSCLK	32.768 kHz clock supply input
69	CONFIG1	Define module type
70	+3.3V	3.3 V power supply
71	GND	Ground
72	+3.3V	3.3 V power supply
73	GND	Ground
74	+3.3V	3.3 V power supply
75	CONFIG2	Define module type

7.14. M.2 Key M Slot (M2M1)

The mITX-CFL-S has an M.2 Key M slot for a Type 2280 module. The M.2 specification supports PCIe x4. Intentionally the slot is reserved for M.2 SSD storage.

Figure 27: M.2 Key M Slot M2M1

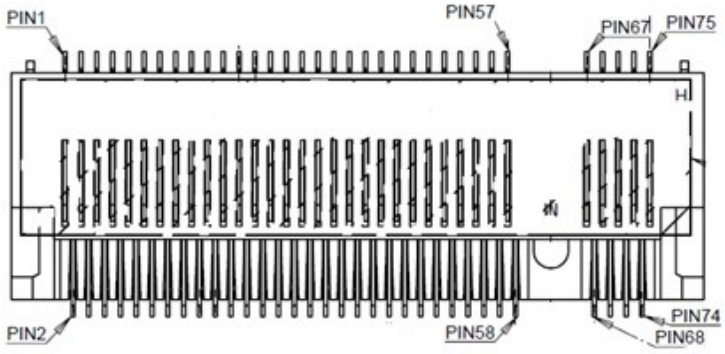


Table 34: Pin Assignment M2M1

Pin	Signal	Description
1	GND	Ground
2	+3.3V	3.3 V power supply
3	GND	Ground
4	+3.3V	3.3 V power supply
5	PERn3	PCIe Lane 3 receiver pair (-)
6	NC	
7	PERp3	PCIe Lane 3 receiver pair (+)
8	NC	
9	GND	Ground
10	LED1#	Device active signal
11	PETn3	PCIe Lane 3 transmitter pair (-)
12	+3.3V	3.3 V power supply
13	PETp3	PCIe Lane 3 transmitter pair (+)
14	+3.3V	3.3 V power supply
15	GND	Ground
16	+3.3V	3.3 V power supply
17	PERn2	PCIe Lane 2 receiver pair (-)
18	+3.3V	3.3 V power supply
19	PERp2	PCIe Lane 2 receiver pair (+)
20	NC	
21	GND	Ground
22	NC	
23	PETn2	PCIe Lane 2 transmitter pair (-)
24	NC	

Pin	Signal	Description
25	PETp2	PCIe Lane 2 transmitter pair (+)
26	NC	
27	GND	Ground
28	NC	
29	PETn1	PCIe Lane 1 transmitter pair (-)
30	NC	
31	PETp1	PCIe Lane 1 transmitter pair (+)
32	NC	
33	GND	Ground
34	NC	
35	PERn1	PCIe Lane 1 receiver pair (-)
36	NC	
37	PERp1	PCIe Lane 1 receiver pair (+)
38	DEVSLP	Device sleep
39	GND	Ground
40	NC	
41	PETn0/SATAB+	PCIe Lane 0 transmitter pair (-) / SATA transmitter differential pair (+)
42	NC	
43	PETp0/SATAB-	PCIe Lane 0 transmitter pair (+) / SATA transmitter differential pair (-)
44	NC	
45	GND	Ground
46	NC	
47	PERn0/SATAA-	PCIe Lane 0 receiver pair (-) / SATA receiver differential pair (-)
48	NC	
49	PERp0/SATAA+	PCIe Lane 0 receiver pair (+) / SATA receiver differential pair (+)
50	PERST	PCIe reset
51	GND	Ground
52	CLKREQ	Reference clock request signal
53	REFCLKN	PCIe reference clock pair (-)
54	PEWAKE	PCIe wake
55	REFCLKP	PCIe reference clock pair (+)
56	NC	
57	GND	Ground
58	NC	
59	KEY M	
60	KEY M	
61	KEY M	
62	KEY M	
63	KEY M	
64	KEY M	
65	KEY M	
66	KEY M	

Pin	Signal	Description
67	NC	
68	SUSCLK	32.768 kHz clock supply input
69	GND	Ground
70	+3.3V	3.3 V power supply
71	GND	Ground
72	+3.3V	3.3 V power supply
73	GND	Ground
74	+3.3V	3.3 V power supply
75	GND	Ground

7.15. Micro SIM Interface Slot for M.2 Key B (SIM1)

Figure 28: Micro SIM Interface Slot SIM1

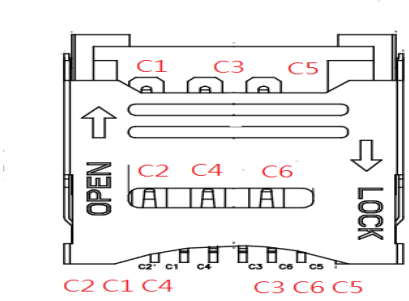


Table 35: Pin Assignment SIM1

Pin	Signal	Description
1	UIM_PWR	Power +3.3V
2	GND	Ground
3	UIM_RST	Reset signal
4	UIM_VPP	Programming voltage input
5	UIM_CLK	Clock signal
6	UIM_DATA	Input or Output for serial data

7.16. PCI Express x16 Slot (PEG1)

The mITX-CFL-S supports PCI Express x16 via slot PEG1 and supports PEG Bifurcation via the jumper (JP11). PEG Bifurcation enables the PCI Expression lanes to be divided into:

- 2x PCIe x8
- 1x PCIe x8 + 2x PCIe x4

For PEG Bifurcation to function a PCIe Riser Card with bifurcation is required.

The 16-lane (x16) PCI Express (PEG1) (PCIe 2.0 and PCIe 3.0) port can be used for external PCI Express cards inclusive graphics card. The maximum theoretical bandwidth using 16 lane is 16 GB/s.

Figure 29: PCI Express x16 Slot PEG1

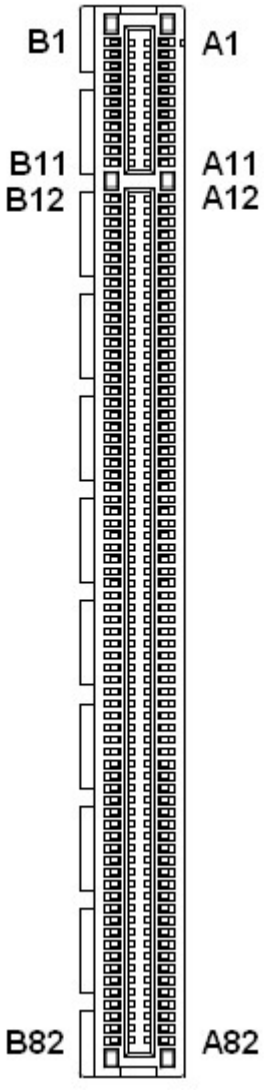


Table 36: Pin Assignment PEG1

Pin	Side B		Side A	
	Signal	Description	Signal	Description
1	+12V	+12 V power	PRSNT1#	Hot plug presence detect
2	+12V	+12 V power	+12V	+12 V power
3	Reserved		+12V	+12 V power
4	Ground		Ground	
5	SMCLK	SMBus clock	Reserved	
6	SMDAT	SMBus data	Reserved	
7	Ground		Reserved	
8	+3.3V	+3.3 V power	Reserved	
9	Reserved		+3.3V	+3.3 V power
10	+3.3VSB	+3.3 V standby power	+3.3V	+3.3 V power
11	WAKE#	Link reactivation	PERST#	PCI Express reset
Mechanical Key				
12	Reserved		Ground	
13	Ground		REFCLK+	Reference clock, differential pair
14	HSOP0	Transmitter Lane 0, Differential pair	REFCLK-	
15	HSON0		Ground	
16	Ground		HSIP0	Receiver Lane 0, Differential pair
17	PRSNT2#	Hot plug presence detect	HSIN0	
18	Ground		Ground	
19	HSOP1	Transmitter Lane 1, Differential pair	Reserved	
20	HSON1		Ground	
21	Ground		HSIP1	Receiver Lane 1, Differential pair
22	Ground		HSIN1	
23	HSOP2	Transmitter Lane 2, Differential pair	Ground	
24	HSON2		Ground	
25	Ground		HSIP2	Receiver Lane 2, Differential pair
26	Ground		HSIN2	
27	HSOP3	Transmitter Lane 3, Differential pair	Ground	
28	HSON3		Ground	
29	Ground		HSIP3	Receiver Lane 3, Differential pair
30	Reserved		HSIN3	
31	PRSNT2#	Hot plug presence detect	Ground	
32	Ground		Reserved	
33	HSOP4	Transmitter Lane 4, Differential pair	Reserved	
34	HSON4		Ground	
35	Ground		HSIP4	Receiver Lane 4, Differential pair
36	Ground		HSIN4	
37	HSOP5	Transmitter Lane 5, Differential pair	Ground	
38	HSON5		Ground	
39	Ground		HSIP5	Receiver Lane 5, Differential pair

Pin	Side B		Side A	
	Signal	Description	Signal	Description
40	Ground		HSIN5	
41	HSOP6	Transmitter Lane 6, Differential pair	Ground	
42	HSON6		Ground	
43	Ground		HSIP6	Receiver Lane 6, Differential pair
44	Ground		HSIN6	
45	HSOP7	Transmitter Lane 7, Differential pair	Ground	
46	HSON7		Ground	
47	Ground		HSIP7	Receiver Lane 7, Differential pair
48	PRSNT2#	Hot plug presence detect	HSIN7	
49	Ground		Ground	
50	HSOP8	Transmitter Lane 8, Differential pair	Reserved	
51	HSON8		Ground	
52	Ground		HSIP8	Receiver Lane 8, Differential pair
53	Ground		HSIP8	
54	HSOP9	Transmitter Lane 9, Differential pair	Ground	
55	HSON9		Ground	
56	Ground		HSIP9	Receiver Lane 9, Differential pair
57	Ground		HSIN9	
58	HSOP10	Transmitter Lane 10, Differential pair	Ground	
59	HSON10		Ground	
60	Ground		HSIP10	Receiver Lane 10, Differential pair
61	Ground		HSIN10	
62	HSOP11	Transmitter Lane 11, Differential pair	Ground	
63	HSON11		Ground	
64	Ground		HSIP11	Receiver Lane 11, Differential pair
65	Ground		HSIN11	
66	HSOP12	Transmitter Lane 12, Differential pair	Ground	
67	HSON12		Ground	
68	Ground		HSIP12	Receiver Lane 12, Differential pair
69	Ground		HSIN12	
70	HSOP13	Transmitter Lane 13, Differential pair	Ground	
71	HSON13		Ground	
72	Ground		HSIP13	Receiver Lane 13, Differential pair
73	Ground		HSIN13	
74	HSOP14	Transmitter Lane 14, Differential pair	Ground	
75	HSON14		Ground	
76	Ground		HSIP14	Receiver Lane 14, Differential pair
77	Ground		HSIN14	
78	HSOP15	Transmitter Lane 15, Differential pair	Ground	
79	HSON15		Ground	
80	Ground		HSIP15	Receiver Lane 15, Differential pair

Pin	Side B		Side A	
	Signal	Description	Signal	Description
81	PRSNT2#	Hot plug presence detect	HSIN15	
82	Reserved		Ground	

7.17. M.2 LED Indicator Pin Header (CN14, CN15 & CN16)

The M.2 Key A LED indicator is supplied via the internal pin header (CN14).

The M.2 Key B LED indicator is supplied via the internal pin header (CN15).

The M.2 Key M LED indicator is supplied via the internal pin header (CN16).

Figure 30: PS/2 Keyboard / Mouse Wafer CN14, CN15, CN16

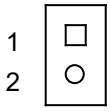


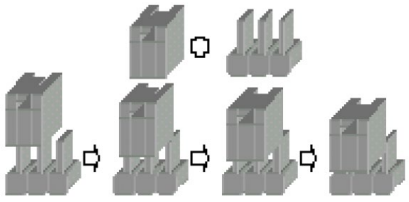
Table 37: Pin Assignment CN14, CN15, CN16

Pin	Signal	Note
1	LED+	
2	LED-	
Connector Type		
B2W, 1x2-pin, 2.54 mm pitch		
Mating Connector		
Vendor **Housing Model No.** **Terminal Model No.**	Joint Tech A2546H-2P WL6008-G-P	

7.18. Switches and Jumpers

The product has several jumpers which must be properly configured to ensure correct operation.

Figure 31: Jumper Connector



For a three-pin jumper (see Figure 35), the jumper setting is designated “1-2” when the jumper connects pins 1 and 2. The jumper setting is designated “2-3” when pins 2 and 3 are connected and so on. You will see that one of the lines surrounding a jumper pin is thick, which indicates pin No.1.

To move a jumper from one position to another, use needle-nose pliers or tweezers to pull the pin cap off the pins and move it to the desired position.

7.18.1. ME F/W Selection (JP2)

Figure 32: ME F/W Selection JP2

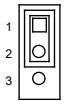


Table 38: Pin Assignment JP2

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Security Measures Defined are Set (Default)
-	X	Security Measures Defined by BIOS are Over-written

“X” = Jumper set (short) and “-” = jumper not set (open)

7.18.2. Backlight Power Enable Selection for eDP1 (JP4)

Figure 33: Backlight Power Enable Selection JP4

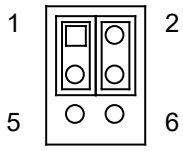


Table 39: Pin Assignment JP4

Jumper 1 Position		Description
Pin 1-3	**Pin 3-5**	
X	-	Backlight Enable Voltage = +3.3V
-	X	Backlight Enable Voltage = +5V
Jumper 2 Position		Description
Pin 2-4	Pin 4-6	
X	-	Active High
-	X	Active Low

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.3. AT / ATX Power Mode Selection (JP5)

Figure 34: AT / ATX Power Mode Selection JP5

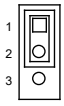


Table 40: Pin Assignment JP5

Jumper 1 Position		Description
Pin 1-2	**Pin 2-3**	
X	-	ATX Mode
-	X	AT Mode

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.4. RTC Reset Selection (JP7)

The "RTC Reset" jumper (JP7) can be used to reset the Real Time Clock (RTC) and drain RTC well.

The jumper has one position: Pin 1-2 mounted (default position) and Pin 2-3 mounted. More information on setting the "RTC Reset" jumper can be founf in the following table.

Figure 35: RTC Reset Selection JP7

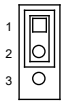


Table 41: Pin Assignment JP7

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	Normal (default position)
-	X	Clear RTC CMOS (board does not boot with the jumper in this position)

"X" = Jumper set (short) and "-" = jumper not set (open)

Do not leave the jumper in position 2-3, otherwise if the power is disconnected, the battery will fully deplete within a few weeks.

7.18.5. Pin-9 Selection for COM2 (JP8)

Figure 36: Pin-9 Selection JP8

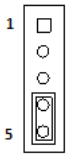


Table 42: Pin Assignment JP8

Jumper Position				Description
Pin 1-2	Pin 2-3	Pin 3-4	Pin 4-5	
X	-	-	-	COM2, Pin-9 = +12V
-	X	-	-	COM2, Pin-9 = +5V
-	-	X	-	COM2, Pin-9 = +5V
-	-	-	X	COM2, Pin-9 = RI

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.6. Panel & Backlight Power Selection for eDP1 (JP9)

Figure 37: Panel & Backlight Power Selection JP9

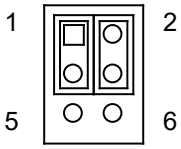


Table 43: Pin Assignment JP9

Jumper 1 Position		Description
Pin 1-3	Pin 3-5	
X	-	Backlight Power = +12V
-	X	Backlight Power = +5V
Jumper 2 Position		Description
Pin 2-4	Pin 4-6	
X	-	Panel Power = +3.3V
-	X	Panel Power = +5V

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.7. Pin-9 Selection for COM1 (JP10)

Figure 38: Pin-9 Selection JP10

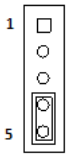


Table 44: Pin Assignment JP10

Jumper Position				Description
Pin 1-2	Pin 2-3	Pin 3-4	Pin 4-5	
X	-	-	-	COM1, Pin-9 = +12V
-	X	-	-	COM1, Pin-9 = +5V
-	-	X	-	COM1, Pin-9 = +5V
-	-	-	X	COM1, Pin-9 = RI

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.8. PCIE Configuration Setting for PEG1 (JP11)

Figure 39: PCIE Configuration Setting JP11

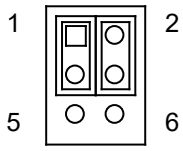


Table 45: Pin Assignment JP11

Jumper 1 Position		Jumper 2 Position		Description
Pin 1-3	Pin 3-5	Pin 2-4	Pin 4-6	
X	-	X	-	x16
X	-	-	X	N/A
-	X	X	-	x8 x8
-	X	-	X	X8 x4 x4

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.9. USB Power Selection (JP13)

Figure 40: Clear ME Register JP13

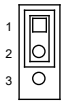


Table 46: Pin Assignment JP13

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	USB Power is always support
-	X	USB Power is only S3 support

"X" = Jumper set (short) and "-" = jumper not set (open)

7.18.10. M.2 Key B Function Selection (JP14)

Figure 41: mPCIE / mSATA Selection JP14

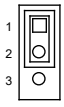


Table 47: Pin Assignment JP14

Jumper 1 Position		Description
Pin 1-2	Pin 2-3	
X	-	SATA
-	X	PCIE

"X" = Jumper set (short) and "-" = jumper not set (open)

8/ BIOS

8.1. Starting the uEFI BIOS

The mITX-CFL-S is provided with a Kontron-customized, pre-installed and configured version of AMI Aptio® V uEFI BIOS. AMI BIOS firmware is based on the Unified Extensible Firmware Interface (UEFI) specification and the Intel® Platform Innovation Framework for EFI. This uEFI BIOS provides a variety of new and enhanced functions specifically tailored to the hardware features of the mITX-CFL-S.

The uEFI BIOS comes with a setup program that provides quick and easy access to the individual function settings for control or modification of the uEFI BIOS configuration. The setup program allows the accessing of various menus that provide functions or access to sub-menus with more specific functions of their own.

To start the uEFI BIOS setup program, follow the steps below:

1. Power on the board.
2. Wait until the first characters appear on the screen (POST messages or splash screen).
3. Press the <DEL> key.
4. If the uEFI BIOS is password-protected, a request for password will appear. Enter either the User Password or the Supervisor Password (see Security menu), press <RETURN>, and proceed with step 5.
5. A setup menu will appear.

The mITX-CFL-S uEFI BIOS setup program uses a hot key-based navigation system. A hot key legend bar is located on the bottom of the setup screens.

The following table provides information concerning the usage of these hot keys.

Table 48: Font Size Table

Hotkeys	Description
<F1>	The <F1> key invokes the General Help window.
<->	The <Minus> key selects the next lower value within a field.
<+>	The <Plus> key selects the next higher value within a field.
<F2>	The <F2> key loads the previous values.
<F3>	The <F3> key loads the standard default values.
<F4>	The <F4> key saves the current settings and exit the uEFI BIOS setup.
<→> or <←>	The <Left/Right> arrows selects major setup menus on the menu bar. For example: Main, Advanced, Security, etc.
< ↑ > or < ↓ >	The <Up/Down> arrows selects fields in the current menu. For example: A setup function or a sub-screen.
<ESC>	The <ESC> key exits a major setup menu and enter the Exit setup menu. Pressing the <ESC> key in a sub-menu displays the next higher menu level.
<RERURN>	The <RETURN> key executes a command or select a submenu.

8.2. Setup Menus

The Setup utility features shows six menus in the selection bar at the top of the screen:

- Main
- Advanced
- Power
- Boot
- Security
- Save & Exit

The Setup menus are selected via the left and right arrow keys. The currently active menu and the currently active uEFI BIOS Setup item are highlighted in white. Each Setup menu provides two main frames. The left frame displays all available functions. Functions that can be configured are displayed in blue. Functions displayed in gray provide information about the status or the operational configuration. The right frame displays an Item Specific Help window providing an explanation of the respective function.

8.2.1. Main Setup Menu

Upon entering the uEFI BIOS Setup program, the Main Setup menu is displayed. This screen lists the Main Setup menu sub-screens and provides basic system information. Additionally functions for setting the system time and date are offered.

Table 49: Main Setup Menu Sub-Screens and Functions

Function	Description
BIOS Information	Read only field. Displays information about the system BIOS
Memory Information	Read only field. Displays information about total memory
ME Information	Read only field. Displays information about Intel Management Engine (ME) version
TXE Information	Read only field. Displays information about TXE information
Firmware Information	Code version and firmware information
System Date	Set System Date
System Time	Set System Time

Figure 42: BIOS Main Menu Screen System Data and Time

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Product Information					
Product Name		mITX-CFL-S-C246			
BIOS Version		R0.07 (x64)			
BIOS Build Date		12/17/2018			
ME Firmware SKU		Corporate SKU			
ME Firmware Version		12.0.10.1127			
CPU Information					
Intel® Core™ i3-8100T CPU @ 3.10GHz					
Microcode Revision		8E			
Processor Cores		4Core(s) / 4Thread(s)			
Memory Information				→ ←: Select Screen ↑ ↓: Select Item	
Total Size		8192 MB (DDR4)		Enter: Select	
Frequency		2400 MHz		+/-: Change Opt.	
				F1: General Help	
System Date		[Mon 02/18/2019]		F2: Previous Values	
System Time		[16:53:58]		F3: Optimized Defaults	
				F4: Save & Exit	
Access Level		Administrator		ESC: Exit	
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Feature	Option	Description
System Date	[dd/mm/yyyy]	Set the Date. Use Tab to switch between Data elements.
System Time	[hh:mm:ss]	Set the Time. Use Tab to switch between Time elements.

8.2.2. Advanced Setup Menu

The Advanced setup menu provides sub-screens and functions for advanced configurations. The following sub-screen functions are included in the menu:

- LAN & Audio Configuration
- Display Configuration
- Super IO Configuration
- CPU Chipset Configuration
- NVMe Configuration
- SATA Configuration
- USB Configuration
- Trusted Computing
- DIO Configuration
- Network Stack
- H/W Monitor

NOTICE

Setting items on this screen to incorrect values may cause the system to malfunction.

Figure 43: BIOS Advanced Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Onboard LAN1 Controller		[Enabled]			
Onboard LAN2 Controller		[Enabled]			
Onboard LAN3 Controller		[Enabled]			
Load I219 UNDI Driver		[Disabled]			
Load I210/I211 UNDI Driver		[Disabled]			
Audio Controller		[Enabled]			
> Display Configuration					
> Super IO Configuration				→←: Select Screen	
> CPU Chipset Configuration				↑ ↓: Select Item	
> NVMe Configuration				Enter: Select	
> SATA Configuration				+/-: Change Opt.	
> USB Configuration				F1: General Help	
> Trusted Computing				F2: Previous Values	
> DIO Configuration				F3: Optimized Defaults	
> Network Stack				F4: Save & Exit	
> H/W Monitor				ESC: Exit	
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Feature	Option	Description
Onboard LAN1 Controller	[Disabled], [Enabled]	Select whether to enable or disable Onboard LAN1 Controller. Intel-i219.
Onboard LAN2 Controller	[Disabled], [Enabled]	Select whether to enable or disable Onboard LAN2 Controller. Intel-i210.
Onboard LAN3 Controller	[Disabled], [Enabled]	Select whether to enable or disable Onboard LAN2 Controller. Intel-i211.
Load I219 UNDI Driver	[Disabled], [Enabled]	Select whether to load LAN UNDI Driver.
Load I210/I211 UNDI Driver	[Disabled], [Enabled]	Select whether to load LAN UNDI Driver.
Audio Controller	[Disabled], [Enabled]	Select whether to enable or disable Audio Controller.

Figure 44: BIOS Advanced Menu - Display Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Display Configuration					
Primary Display		[Auto]		→←: Select Screen	
Aperture Size		[256MB]		↑ ↓: Select Item	
DVMT Pre-Allocated		[32M]		Enter: Select	
DVMT Total Gfx Mem		[256M]		+/-: Change Opt.	
				F1: General Help	
PWM Backlight Control		[By Internal]		F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
Primary Display	[Auto], [IGFX], [PEG], [PCI], [SG]	Select which of IGFX / PEG / PCI Graphics device should be the Primary Display or select SG for Switchable Gfx.
Aperture Size	[128MB], [256MB], [512MB], [1024MB], [2048MB]	Select the Aperture Size. Note: Above 4GB MMIO BIOS assignment is automatically enabled when selecting 2048MB aperture. To use this feature, please disable CSM Support.
DVMT Pre-Allocated	[32M], [64M], [4M], [8M], [12M], [16M], [20M], [24M], [28M], [32M/F7], [36M], [40M], [44M], [48M], [52M], [56M], [60M]	Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
DVMT Total Gfx Mem	[128M], [256M], [MAX]	Select DVMT 5.0 Total Graphic Memory size used by the Internal Graphics Device.
PWM Backlight Control	[By External], [By Internal]	[By External]: Control by external HW circuit. [By Internal]: Control by LBKLT_CTL on the Intel Chipset.

Figure 45: BIOS Advanced Menu - Super IO Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Super IO Configuration					
> Serial Port 1 Configuration				→ ←: Select Screen	
> Serial Port 2 Configuration				↑ ↓: Select Item	
> Serial Port 3 Configuration				Enter: Select	
> Serial Port 4 Configuration				+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Figure 46: BIOS Advanced Menu - Super IO Configuration - Serial Port 1 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Serial Port 1 Configuration					
Serial Port		[Enabled]		→ ←: Select Screen	
Device Settings		IO=3F8h; IRQ=4;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
Serial Port 1 Type		[RS232]		F1: General Help	
RS485 Deplux Mode*		[Half Duplex]		F2: Previous Values	
RS485 Auto Flow Control*		[Disabled]		F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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* These items appear only when selecting RS485 for the Serial Port 1 Type.

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=3F8h; IRQ=4;], [IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	Select an optional setting for Super IO device.

Feature	Option	Description
Serial Port 1 Type	[RS232], [RS422], [RS485]	Select an appropriate type for Serial Port 1.
RS485 Duplex Mode	[Half Duplex], [Full Duplex]	Select an appropriate RS485 Duplex Mode.
RS485 Auto Flow Control	[Disabled], [Enabled]	Select whether to enable or disable RS485 Auto Flow Control.

Figure 47: BIOS Advanced Menu - Super IO Configuration - Serial Port 2 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Serial Port 2 Configuration					
Serial Port		[Enabled]		→ ←: Select Screen	
Device Settings		IO=2F8h; IRQ=3;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
Serial Port 2 Type		[RS232]		F1: General Help	
RS485 Deplux Mode*		[Half Duplex]		F2: Previous Values	
RS485 Auto Flow Control*		[Disabled]		F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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* These items appear only when selecting RS485 for the Serial Port 2 Type.

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=2F8h; IRQ=3;], [IO=3F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	Select an optional setting for Super IO device.
Serial Port 2 Type	[RS232], [RS422], [RS485]	Select an appropriate type for Serial Port 2.
RS485 Duplex Mode	[Half Duplex], [Full Duplex]	Select an appropriate RS485 Duplex Mode.
RS485 Auto Flow Control	[Disabled], [Enabled]	Select whether to enable or disable RS485 Auto Flow Control.

Figure 48: BIOS Advanced Menu - Super IO Configuration - Serial Port 3 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Serial Port 3 Configuration					
Serial Port		[Enabled]		→ ←: Select Screen	
Device Settings		IO=3E8h; IRQ=7;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	
Serial Port 3 Type		[RS232]		F1: General Help	
RS485 Deplux Mode*		[Half Duplex]		F2: Previous Values	
RS485 Auto Flow Control*		[Disabled]		F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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* These items appear only when selecting RS485 for the Serial Port 3 Type.

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=3E8h; IRQ=7;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	Select an optional setting for Super IO device.
Serial Port 3 Type	[RS232], [RS422], [RS485]	Select an appropriate type for Serial Port 3.
RS485 Duplex Mode	[Half Duplex], [Full Duplex]	Select an appropriate RS485 Duplex Mode.
RS485 Auto Flow Control	[Disabled], [Enabled]	Select whether to enable or disable RS485 Auto Flow Control.

Figure 49: BIOS Advanced Menu - Super IO Configuration - Serial Port 4 Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Serial Port 4 Configuration					
Serial Port		[Enabled]		→ ←: Select Screen	
Device Settings		IO=2E8h; IRQ=7;		↑ ↓: Select Item	
				Enter: Select	
Change Setting		[Auto]		+/-: Change Opt.	

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Serial Port 4 Type		[RS232]		F1: General Help	
RS485 Deplux Mode*		[Half Duplex]		F2: Previous Values	
RS485 Auto Flow Control*		[Disabled]		F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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* These items appear only when selecting RS485 for the Serial Port 4 Type.

Feature	Option	Description
Serial Port	[Disabled], [Enabled]	Select whether to enable or disable Serial Port (COM).
Change Settings	[Auto], [IO=2E8h; IRQ=7;], [IO=3E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E8h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2F0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;], [IO=2E0h; IRQ=3, 4, 5, 6, 7, 9, 10, 11, 12;]	Select an optional setting for Super IO device.
Serial Port 4 Type	[RS232], [RS422], [RS485]	Select an appropriate type for Serial Port 4.
RS485 Duplex Mode	[Half Duplex], [Full Duplex]	Select an appropriate RS485 Duplex Mode.
RS485 Auto Flow Control	[Disabled], [Enabled]	Select whether to enable or disable RS485 Auto Flow Control.

Figure 50: BIOS Advanced Menu - CPU Chipset Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
CPU Chipset Configuration					
EIST		[Enabled]		→←: Select Screen	
VT-d		[Enabled]		↑ ↓: Select Item	
Active Processor Cores		[All]		Enter: Select	
Intel (VMX) Virtualization Technology		[Enabled]		+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
EIST	[Disabled], [Enabled]	Select whether to enable or disable Enhanced Intel SpeedStep Technology.
VT-d	[Disabled], [Enabled]	Select whether to enable or disable VT-d capability.
Active Processor Cores	[All], [1], [2], [3]	Select the number of cores to enable in each processor package.
Intel (VMX) Virtualization Technology	[Disabled], [Enabled]	Select whether to enable or disable Intel (VMX) Virtualization Technology. When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

Figure 51: BIOS Advanced Menu - NVMe Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
NVMe Configuration					
No NVME Device Found				→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
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Figure 52: BIOS Advanced Menu - SATA Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
SATA Configuration					
SATA Controller(s)		[Enabled]		→←: Select Screen	
SATA Mode Selection		[AHCI]		↑ ↓: Select Item	
				Enter: Select	
Serial ATA Port 1		Empty		+/-: Change Opt.	
Port 1		[Enabled]		F1: General Help	
Serial ATA Port 2		Empty		F2: Previous Values	
Port 2		[Enabled]		F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
SATA Controller(s)	[Enabled], [Disabled]	Select whether to enable or disable SATA controller.
SATA Mode Selection	[AHCI], [Intel RST Premium With Intel Optane System Acceleration]	Determine how SATA controller(s) operate.
Port 1..2	[Disabled], [Enabled]	Select whether to enable or disable SATA Port 1/2.

Figure 53: BIOS Advanced Menu - USB Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
USB Configuration					
USB Devices:				→ ←: Select Screen	
1 Keyboard, 1 Mouse				↑ ↓: Select Item	
				Enter: Select	
Legacy USB Support		[Enabled]		+/-: Change Opt.	
XHCI Hand-off		[Disabled]		F1: General Help	
USB Mass Storage Driver Support		[Enabled]		F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
Legacy USB Support	[Enabled], [Disabled], [Auto]	Select whether to enable or disable Legacy USB support. AUTO option disables legacy support if no USB devices are connected.
XHCI Hand-off	[Enabled], [Disabled]	Select whether to enable or disable XHCI Hand-off function. This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	[Disabled], [Enabled]	Select whether to enable or disable USB Mass Storage Driver Support.

Figure 54: BIOS Advanced Menu - Trsuted Computing

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Configuration					
Security Device Support		[Disabled]			
NO Security Device Found				→ ←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
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Feature	Option	Description
Security Device Support	[Disabled], [Enabled]	Select whether to enable or disable BIOS support for security device. O.S. will not show Security Device. TCG EFI protocol and INT1A interface will not be available.

Figure 55: BIOS Advanced Menu - DIO Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
DIO Configuration					
User Configuration		[Disabled]			
DIO_0*		[Output High]			
DIO_1*		[Output High]			
DIO_2*		[Output High]			
DIO_3*		[Output High]			
DIO_4*		[Output High]			
DIO_5*		[Output High]			
DIO_6*		[Output High]			
DIO_7*		[Output High]			
DIO_0 Value		1		→←: Select Screen ↑ ↓: Select Item	
DIO_1 Value		1		Enter: Select	
DIO_2 Value		1		+/-: Change Opt.	
DIO_3 Value		1		F1: General Help	
DIO_4 Value		1		F2: Previous Values	
DIO_5 Value		1		F3: Optimized Defaults	
DIO_6 Value		1		F4: Save & Exit	
DIO_7 Value		1		ESC: Exit	
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* These items appear only when enabling "User Configuration".

Feature	Option	Description
User Configuration	[Enabled], [Disabled]	Select whether or not to allow user to set the DIO pin value.
DIO_0..7	[Output Low], [Output High], [Input]	Set up the DIO pin value.

Figure 56: BIOS Advanced Menu - Network Stack

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Network Stack		[Disabled]			
Ipv4 PXE Support*		[Enabled]			
Ipv6 PXE Support*		[Disabled]		→←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
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* These items appear only when enabling "Network Stack".

Feature	Option	Description
Network Stack	[Disabled], [Enabled]	Select whether to enable or disable UEFI Network Stack.
Ipv4 PXE Support	[Disabled], [Enabled]	Select whether to enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.
Ipv6 PXE Support	[Disabled], [Enabled]	Select whether to enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

Figure 57: BIOS Advanced Menu - H/W Monitor

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
PC Health Status					
> Smart FAN Configuration					
System Temperature		: +29 C			
CPU Temperature		: +37 C			
CPU Fan Speed		: 5314 RPM		→ ←: Select Screen	
SYS Fan Speed		: N/A		↑ ↓: Select Item	
				Enter: Select	
+VCORE		: +0.957 V		+/-: Change Opt.	
+12V		: +12.164 V		F1: General Help	
+3.3V		: +3.344 V		F2: Previous Values	
+5V		: +5.066 V		F3: Optimized Defaults	
+VMEN		: +1.213 V		F4: Save & Exit	
+VRTC		: +3.088 V		ESC: Exit	
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Figure 58: BIOS Advanced Menu - H/W Monitor - Smart FAN Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Smart FAN Configuration					
CPU FAN Setting		[Manual]		→ ←: Select Screen	
Manual Duty		255		↑ ↓: Select Item	
				Enter: Select	
System FAN Setting		[Manual]		+/-: Change Opt.	
Manual Duty		255		F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
CPU FAN Setting	[Manual], [Smart]	Switch the CPU FAN control mode.
System FAN Setting	[Manual], [Smart]	Switch the System FAN control mode.

8.2.3. Power Setup Menu

The Power setup menu provides functions and a sub-screen for power configurations. The following sub-screen function is included in the menu:

- WatchDog Timer Configuration

Figure 59: BIOS Power Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Power Configuration					
ACPI Sleep State		[S3 (Suspend to RAM)]			
Restore AC Power Loss		[Power Off]		→←: Select Screen	
Power Saving Mode		[Disabled]		↑ ↓: Select Item	
				Enter: Select	
Resume Event Control				+/-: Change Opt.	
Resume By LAN Device		[Disabled]		F1: General Help	
Resume By PCI-E Device		[Disabled]		F2: Previous Values	
Resume By Ring Device		[Disabled]		F3: Optimized Defaults	
Resume By RTC Alarm		[Disabled]		F4: Save & Exit	
> WatchDog Timer Configuration				ESC: Exit	
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Feature	Option	Description
ACPI Sleep State	[S3 (Suspend to RAM)]	Select whether to enable or disable suspend function and determine an appropriate suspend mode.
Restore AC Power Loss	[Power Off], [Power On], [Last State]	Select AC power state when power is re-applied after a power failure. Select [Power Off] if you want the system to remain off after power restored. Select [Power On] if you use a power strip to turn the system on.
Power Saving Mode	[Disabled], [EUP Enabled]	Configure the Power Saving Mode configuration.
Resume By LAN Device	[Disabled], [Enabled]	Select whether to enable or disable Wake from LAN Device.
Resume By PCI-E Device	[Disabled], [Enabled]	Select whether to enable or disable Wake from PCI-E Device.
Resume By Ring Device	[Disabled], [Enabled]	Select whether to enable or disable Wake from Ring Device.
Resume By RTC Alarm	[Disabled], [Enabled]	Select whether to enable or disable Wake Up on Alarm, to turn on your system on a special day of the month.

Figure 60: BIOS Power Setup Menu - WatchDog Timer Configuration

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
WatchDog Timer Configuration					

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
WDT Function		[Disabled]		→ ←: Select Screen	
WDT Count Mode*		[Second]		↑ ↓: Select Item	
WDT Timer*		30		Enter: Select	
				+/-: Change Opt.	
				F1: General Help	
				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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* These items appear only when enbling "WDT Function".

Feature	Option	Description
WDT Function	[Disabled], [Enabled]	Select whether to enable or disable WatchDog Timer function.
WDT Count Mode	[Second], [Minute]	Select WatchDog count mode: second or minute.

8.2.4. Boot Setup Menu

The boot setup menu lists the for boot device priority order, that is generated dynamically.

Figure 61: BIOS Boot Setup Menu

BIOS SETUP UTILITY					
Main	**Advanced**	**Power**	**Boot**	**Security**	**Save & Exit**
Boot Configuration					
Full Screen LOGO Display		[Disabled]			
Setup Prompt Timeout		1		→ ←: Select Screen	
Bootup NumLock State		[On]		↑ ↓: Select Item	
				Enter: Select	
CSM Support		[Disabled]		+/-: Change Opt.	
Boot Option Filter		[UEFI only]		F1: General Help	
				F2: Previous Values	
Boot Option Priorities				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Option	Description
Full Screen LOGO Display	[Disabled], [Enabled]	Select whether to enable or disable to display logo screen.
Bootup NumLock State	[On], [Off]	Select the state of the NumLock feature of the keyboard after Startup. [On]: The keys on the keypad will act as numeric keys. [Off]: The keys on the keypad will act as cursor keys.
CSM Support	[Enabled], [Disabled]	Select whether to enable or disable CSM support.
Boot Option Filter	[UEFI only]	Control Legacy / UEFI ROMs priority.

8.2.5. Security Setup Menu

The Security setup menu provides information about the passwords and functions for specifying the security settings. The passwords are case-sensitive. The mITX-CFL-S provides no factory-set passwords.

NOTICE

If there is already a password installed, the system asks for this first. To clear a password, simply enter nothing and acknowledge by pressing <RETURN>. To set a password, enter it twice and acknowledge by pressing <RETURN>.

Figure 62: BIOS Boot Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Password Description If ONLY the Administrator's password is set, then this only limits access to Setup and is only asked for when entering Setup If ONLY the User's password is set, then this is a power on password and must be entered to boot or enter Setup. In Setup the User will have Administrator rights The password length must be in the following range: Minimum Length 3 Maximum length 20 Administrator Password User Password > Secure Boot				→ ←: Select Screen ↑ ↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit	
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Feature	Description
Administrator Password	Set administrator password
User Password	Set user password

If only the administrator's password is set, then only access to setup is limited. The password is only entered when entering setup.

If only the user's password is set, then the password is a power on password and must be entered to boot or enter setup. Within the setup menu the user has administrator rights.

Password length requirements are maximum 20 characters and minimum 3 characters.

8.2.5.1. Remember the password

It is highly recommended to keep a record of all passwords in a safe place. Forgotten passwords results in being locked out of the system.

If the system cannot be booted because the User Password or the Supervisor Password are not know, contact Kontron Support for further assistance.

HDD security passwords cannot be cleared using the above method.

8.2.6. Save & Exit Setup Menu

The exit setup menu provides functions for handling changes made to the UEFI BIOS settings and the exiting of the setup program.

Figure 63: BIOS Boot Setup Menu

BIOS SETUP UTILITY					
Main	Advanced	Power	Boot	Security	Save & Exit
Save Changes and Reset					
Discard Changes and Reset					
				→←: Select Screen	
Save Options				↑ ↓: Select Item	
Save Changes				Enter: Select	
Discard Changes				+/-: Change Opt.	
				F1: General Help	
Restore Defaults				F2: Previous Values	
				F3: Optimized Defaults	
				F4: Save & Exit	
				ESC: Exit	
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Feature	Description
Save Changes and Exit	Exit system setup after saving the changes. Once you are finished making your selections, choose this option from the Exit menu to ensure the values you selected are saved to the CMOS RAM. The CMOS RAM is sustained by an onboard backup battery and stays on even when the PC is turned off. When you select this option, a confirmation window appears. Select [Yes] to save changes and exit.
Discard Changes and Exit	Exit system setup without saving any changes. Select this option only if you do not want to save the changes that you made to the Setup program. If you made changes to fields other than system date, system time, and password, the BIOS asks for a confirmation before exiting.
Save Changes	Save changes done so far to any of the setup values. This option allows you to save the selections you made. After selecting this option, a confirmation appears. Select [Yes] to save any changes.
Discard Changes	Discards changes done so far to any of the setup values. This option allows you to discard the selections you made and restore the previously saved values. After selecting this option, a confirmation appears. Select [Yes] to discard any changes and load the previously saved values.
Restore Defaults	Restore Default values for all the setup values. This option allows you to load optimal default values for each of the parameters on the Setup menus, which will provide the best performance settings for your system. The F9 key can be used for this operation.

Appendix A: List of Acronyms

The following table does not contain the complete acronyms used in signal names, signal type definitions or similar. A description of the signals is included in the I/O Connector and Internal connector chapters within this user guide.

Table 50: List of Acronyms

2D	Two-Dimensional
3D	Three-Dimensional
AT	Advanced Technology
ATX	Advanced Technology eXtended
BGA	Ball Grid Array
BIOS	Basic Input / Output System
BSP	Board Support Package
CMOS	Complementary Metal Oxide Semiconductor
CPU	Central Processing Unit
DC	Direct Current
DDC	Display Data Channel
DIO	Digital Input / Output
ECC	Error-Correcting Code
EEE	Electrical and Electronic Equipment
EOS	Electrical OverStress
ESD	ElectroStatic Discharge
GbE	Gigabit Ethernet
HDD	Hard Disk Drive
HDMI	High Definition Multimedia Interface
LAN	Local Area Network
LED	Light Emitting Device
LVDS	Low-Voltage Differential Signaling
ME F/W	Management Engine Firmware
mPCIe	mini Peripheral Component Interconnect express
PC-AT	Personal Computer - Advanced Technology
PCB	Printed Circuit Board
PSU	Power Supply Unit
PVC	PolyViny Chloride
PWM	Pulse Width Modulation
RAM	Random Access Memory
ROM	Read-Only Memory
RTC	Real-Time Clock
SATA	Serial Advanced Technology Attachment
SDP	Serial Download Protocol
SELV	Safety Extra-Low Voltage
SIM	Subscriber Identity Module
SMBus	System Management Bus
SoC	System on Chip
SO-DIMM	Small Outline Dual In-line Memory Module
SPD	Serial Presence Detect
SPI	Serial Peripheral Interface
TDP	Thermal Design Power
TPM	Trusted Platform Module
UEFI	Unified Extensible Firmware Interface
USB	Universal Serial Bus
UTP	Update Transfer Protocol
VGA	Video Graphics Array
WDT	WatchDog Timer
WEEE	Waste Electrical and Electronic Equipment

About Kontron

Kontron is a global leader in IoT / Embedded Computing Technology (ECT) and offers individual solutions in the areas of Internet of Things (IoT) and Industry 4.0 through a combined portfolio of hardware, software and services. With its standard and customized products based on highly reliable state-of-the-art technologies, Kontron provides secure and innovative applications for a wide variety of industries. As a result, customers benefit from accelerated time-to-market, lower total cost of ownership, extended product lifecycles and the best fully integrated applications.

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