Approval Sheet

Customer	
Product Number	**M1UF-12MC2CDB-J**
Module speed	**PC-2600**
Pin	**184 pin**
CAS Latency	**CL-2.5**
SDRAM Operating Temp	**0 ℃ ~ 70 ℃**
Date	**25th October 2014**

Approval by Customer

P/N:

Signature:

Date:

Sales: **Sr. Technical Manager: John Hsieh**

Rev 1.0

The Total Solution For Industrial Flash Storage

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tRCD (ns)	tRP (ns)	tRC (ns)
		CL=2	CL=2.5	CL=3			
PC-2600	D	266	333	333	15	15	55

- JEDEC Standard 184-pin Dual In-Line Memory Module
- Intend for 266MHz and 333MHz applications
- Inputs and Outputs are SSTL-2 compatible
- VDD=VDDQ= 2.5 Volt ± 0.2
- Differential clock input
- DLL aligns DQ and DQS transition with CK transition
- Bi-Directional data strobe with one clock cycle
- Built with 512Mb DDR SDRAMs in 400 mil TSOP IIpackages
- Auto Refresh (CBR) and Self Refresh Modes support.
- Serial Presence Detect with EEPROM
- Auto & self refresh 7.8μs ($T_A \leq +70°C$)
- Operation Temperature
  - Commercial ($0°C \leq T_A \leq +70°C$)
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 2,2.5 and 3
  - Burst Length: 2, 4 or 8
- RoHS Compliant *(Section 13)*

2. Environmental Requirements

iDIMM's SDRAMs are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
T_{OPR}	Operating Temperature (ambient)	0 to +70	°C	1
T_{STG}	Storage Temperature	-50 to +100	°C	1

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.

3. Ordering Information

DDR UDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M1UF-12MC2CDB-J	512MB	PC-2600	64M x64	8	1	N/A

4. Pin Configurations (Front side/Back side)

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	V_{REF}	32	A5	62	V_{DDQ}	93	V_{SS}	124	V_{SS}	154	RAS#
2	DQ0	33	DQ24	63	WE#	94	DQ4	125	A6	155	DQ45
3	V_{SS}	34	V_{SS}	64	DQ41	95	DQ5	126	DQ28	156	V_{DDQ}
4	DQ1	35	DQ25	65	CAS#	96	V_{DDQ}	127	DQ29	157	S0#
5	DQS0	36	DQS3	66	V_{SS}	97	DM,DQS9	128	V_{DDQ}	158	S1#
6	DQ2	37	A4	67	DQS5	98	DQ6	129	DM3,DQS12	159	DM5,DQS14
7	V_{DD}	38	V_{DD}	68	DQ42	99	DQ7	130	A3	160	V_{SS}
8	DQ3	39	DQ26	69	DQ43	100	V_{SS}	131	DQ30	161	DQ46
9	NC	40	DQ27	70	V_{DD}	101	NC	132	V_{SS}	162	DQ47
10	RESET#	41	A2	71	NC	102	NC	133	DQ31	163	NC
11	V_{SS}	42	V_{SS}	72	DQ48	103	NC	134	CB4**/NC	164	V_{DDQ}
12	DQ8	43	A1	73	DQ49	104	V_{DDQ}	135	CB5**/NC	165	DQ52
13	DQ9	44	CB0**/NC	74	V_{SS}	105	DQ12	136	V_{DDQ}	166	DQ53
14	DQS1	45	CB1**/NC	75	NC	106	DQ13	137	CK0	167	A13*/NC
15	V_{DDQ}	46	V_{DD}	76	NC	107	DM1, DQS10	138	Ck0#	168	V_{DD}
16	NC	47	DQS8**	77	V_{DDQ}	108	V_{DD}	139	V_{SS}	169	DM6
17	NC	48	A0	78	DQS6	109	DQ14	140	DM8,DQS17**	170	DQS4
18	V_{SS}	49	CB2**/NC	79	DQS0	110	DQ15	141	A10	171	DQ55
19	DQ10	50	V_{SS}	80	DQ51	111	CKE1	142	CB6**/NC	172	V_{DDQ}
20	DQ11	51	CB3**/NC	81	V_{SS}	112	V_{DDQ}	143	V_{DDQ}	173	NC
21	CKE0	52	BA1	82	V_{DDID}	113	NC	144	CB7**/NC	174	DQ60
22	V_{DDQ}	Key		83	DQ56	114	DQ20	Key		175	DQ61
23	DQ16	53	DQ32	84	DQ57	115	A12	145	V_{SS}	176	V_{SS}
24	DQ17	54	V_{DDQ}	85	V_{DD}	116	V_{SS}	146	DQ36	177	DM7/DQS16
25	DQS2	55	DQ33	86	DQS7	117	DQ21	147	DQ37	178	DQ62
26	V_{SS}	56	DQS4	87	DQ58	118	A11	148	V_{DD}	179	DQ63
27	A9	57	DQ34	88	DQ59	119	DM2/DQS11	149	DM4,DQS13	180	V_{DDQ}
28	DQ18	58	V_{SS}	89	V_{SS}	120	V_{DD}	150	DQ38	181	SA0
29	A7	59	BA0	90	NC	121	DQ22	151	DQ39	182	SA1
30	V_{DDQ}	60	DQ35	91	SDA	122	A8	152	V_{SS}	183	SA2
31	DQ19	61	DQ40	92	SCL	123	DQ23	153	DQ44	184	V_{DDSPD}

NC = No Connect
* A13 is used for 2GB Unbuffered DIMM.
** Pin# 44, 45, 47, 49, 51, 134, 135, 140, 142, 144 are used on x72 module and are not used on x64 module.

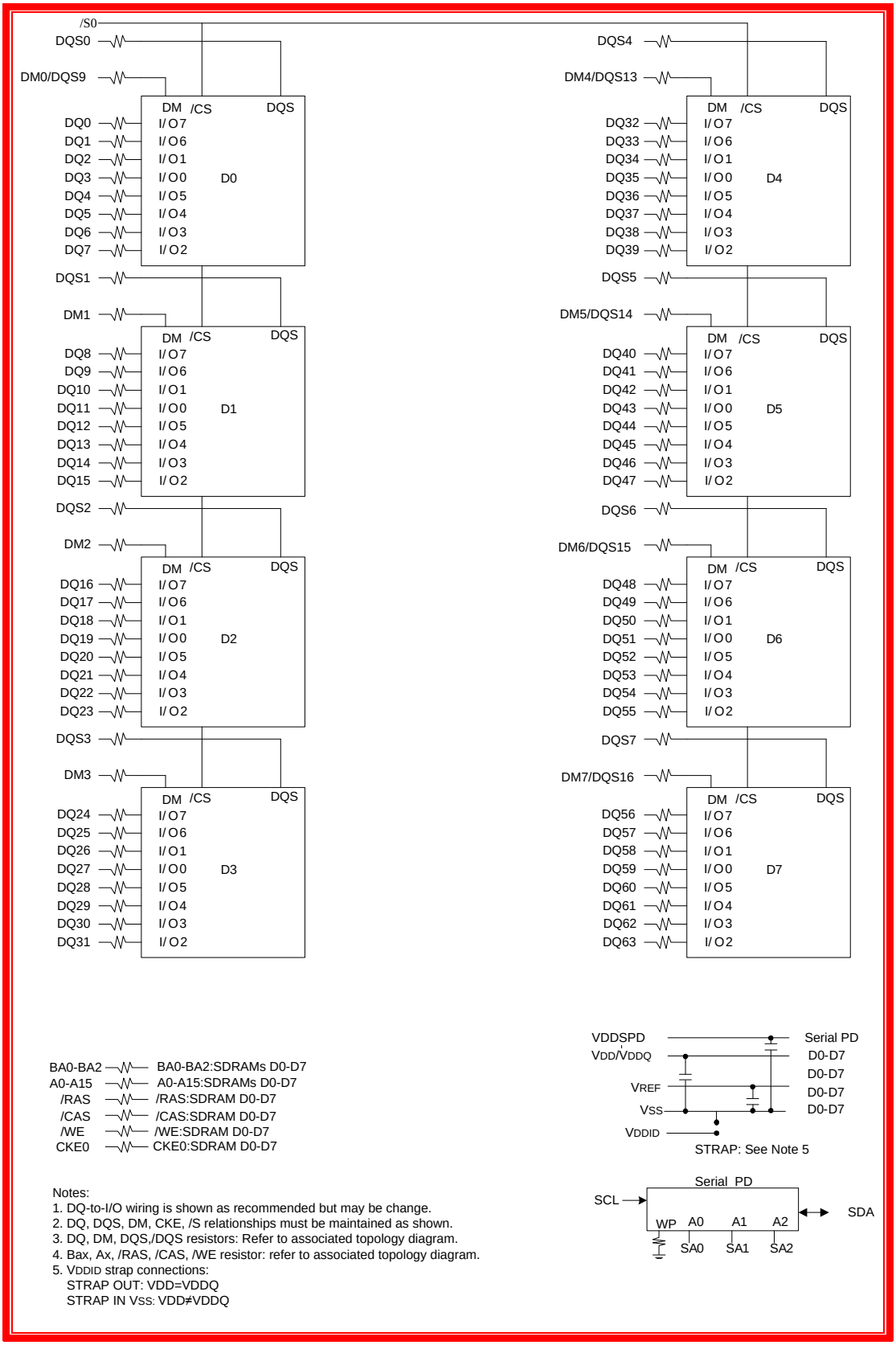
5. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	CK0 – CK1 CK0# - CK1#	Differential SDRAM Clocks
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SCL	Serial Presence Detect Clock Input
RAS#	SDRAM row address strobe	SDA	Serial Presence Detect Data input/output
CAS#	SDRAM column address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
WE#	SDRAM write enable	V_{DD}	Power Supply
S0# - S1#	DIMM Rank Select Lines	V_{DDID}	V_{DD} Identification Flag
CK0 – CKE1	SDRAM clock enable lines	V_{DDQ}	SDRAM I/O Driver power supply
DQ0 – DQ63	DIMM memory data bus	V_{REF}	SDRAM I/O Reference supply
CB0 – CB7	DIMM ECC check bit	V_{SS}	Ground
DQS0 – DQS17	SDRAM data strobes	V_{DDSPD}	Serial EEPROM positive power supply
DM0 – DM7	SDRAM data masks	Reset	Reset enable
NC	Spare Pin		

6. Function Block Diagram:

- (512MB, 1 Rank, 64Mx8 DDR UDIMM)



Rev 1.0

October 2014

7. Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
T_A	Operation Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{INPUT}	Voltage input pins relative to Vss	-1.0 to +3.6	V
V_{IO}	Voltage on I/O pins relative to Vss	-0.5 to +3.6	V
V_{DD}	Voltage on VDD supply relative to Vss	-1.0 to +3.6	V
V_{DDQ}	Voltage on VDDQ supply relative to Vss	-1.0 to +3.6	V
I_{OS}	Output short Circuit Current	50	mA

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

8. AC & DC Operating Conditions

- AC Operating Conditions

(T_{CASE} = 0 °C ~ 70 °C; V_{SS}=0V)

Symbol	Parameter	Value		Units	Notes
		Min	Max		
V_{IH} (AC)	Input High (Logic1) Voltage	V_{REF} + 0.31	-	V	
V_{IL} (AC)	Input Low (Logic0) Voltage	-	V_{REF} + 0.31	V	
V_{ID} (AC)	Input differential Voltage: CK, /CK	0.7	V_{DDQ} + 0.6	V	1
V_{IX} (AC)	Input crossing point Voltage: CK, /CK	0.5* V_{DDQ} + 0.2	0.5* V_{DDQ} - 0.2	V	2

Note:

1. VID is the magnitude of the difference between the input level on CK and the input on /CK.
2. The value of VIX is expected to equal 0.5*V DDQ of the transmitting device and must track variations in the DC level of the same.

- DC Electrical Characteristics and Operating Conditions

(T_{CASE} = 0 °C ~ 70 °C; V_{SS} = 0V)

Symbol	Parameter	Min	Typ.	Max	Units	Notes
V_{DD}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
V_{DDQ}	Supply Voltage (DDR266,333)	2.3	2.5	2.7	V	
	Supply Voltage (DDR400)	2.5	2.6	2.7	V	
$V_{IH\ (DC)}$	Input High (Logic1) Voltage	V_{REF} + 0.15	-	V_{DDQ} + 0.3	V	1
$V_{IL\ (DC)}$	Input Low (Logic0) Voltage	-0.3	-	V_{REF} - 0.15	V	1
V_{TT}	Termination Voltage	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
V_{REF}	I/O Reference Voltage	0.49V_{DDQ}	0.5V_{DDQ}	0.51V_{DDQ}	V	2
$V_{IN(DC)}$	Input Voltage Level: CK, /CK	-0.3	-	V_{DDQ} + 0.3	V	
$V_{ID(DC)}$	Input Differential Voltage: CK, /CK	0.36	-	V_{DDQ} + 0.6	V	
$V_{I(RATIO)}$	V-I Matching	0.71	-	1.4	V	

Note:

1. Inputs are not recognized as valid until V_{REF} stabilizes.
2. V_{REF} is expected to be equal to 0.5 V_{DDQ} of the transmitting device, and to track variations in the DC level of the same. Peak-to-peak noise on V_{REF} may not exceed 2% of the DC value.
3. V_{TT} of transmitting device must track V_{REF} of receiving device.

9. Operating, Standby, and Refresh Currents

- 512MB UDIMM (1 Rank, 64Mx8 DDR SDRAMs T_{CASE} = 0 °C ~ 70 °C)

Symbol	Parameter/Condition	PC-2600	Unit
I_{DD0}	One bank; Active - Precharge; tRC=tRC(min); tCK=tCK(min); DQ,DM and DQS inputs changing twice per clock cycle; address and control inputs changing once per clock cycle	520	mA
I_{DD1}	One bank; Active - Read - Precharge; Burst Length=2; tRC=tRC(min); tCK=tCK(min); address and control inputs changing once per clock cycle	600	mA
I_{DD2P}	All banks idle; Power down mode; CKE=Low, tCK=tCK(min)	40	mA
I_{DD2F}	/CS=High, All banks idle; tCK=tCK(min); CKE= High; address and control inputs changing once per clock cycle.VIN=VREF for DQ, DQS and DM	184	mA
I_{DD3P}	One bank active ; Power down mode; CKE=Low, tCK=tCK(min)	112	mA
I_{DD3N}	/CS=HIGH; CKE=HIGH; One bank; Active-Precharge;tRC=tRAS(max); tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle; Address and other control inputs changing once per clock cycle	304	mA
I_{DD4R}	Burst=2; Reads; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); IOUT=0mA	680	mA
I_{DD4W}	Burst=2; Writes; Continuous burst; One bank active; Address and control inputs changing once per clock cycle; tCK=tCK(min); DQ, DM and DQS inputs changing twice per clock cycle	760	mA
I_{DD5}	tRC=tRFC(min) - 8*tCK for DDR200 at 100Mhz, 10*tCK for DDR266A & DDR266B at 133Mhz; distributed refresh	840	mA
I_{DD6}	CKE=<0.2V; External clock on; tCK=tCK(min)	40	mA
I_{DD7}	Four bank interleaving with BL=4 Refer to the following page for detailed test condition	1680	mA

10. AC Timing Specifications

(T_{CASE} = 0 °C ~ 70 °C; V_{DDQ} = V_{DD} , See AC Characteristics)

Symbol	Parameter	PC-2600		Unit
		Min.	Max.	
tAC	DQ output access time from CK/CK#	-0.7	0.7	ns
tDQSCK	DQS output access time from CK/CK#	-0.60	0.60	ns
tCH	CK high-level width	0.45	0.55	tCK
tCL	CK low-level width	0.45	0.55	tCK
tHP	Minimum half clk period for any given cycle; defined by clk high (tCH) or clk low (tCL) time	Min (tCL,tCH)	-	ns
tCK	Clock Cycle Time	6	12	ns
tDS	DQ and DM input setup time(differential data strobe)	0.45	-	ns
tDH	DQ and DM input hold time(differential data strobe)	0.45	-	ns
tIPW	Input pulse width	2.2	-	ns
tDIPW	DQ and DM input pulse width (each input)	1.75	-	ns
tHZ	Data-out high-impedance time from CK/CK	-	0.7	ns
tLZ(DQS)	DQS low-impedance time from CK/CK	-0.7	0.7	ns
tLZ(DQ)	DQ low-impedance time from CK/CK	-0.7	0.7	ns
tDQSQ	DQS-DQ skew (DQS & associated DQ signals)	-	0.45	ns
tQHS	Data hold Skew Factor	-	0.55	ns
tQH	Data output hold time from DQS	tHP -tQHS	-	ns
tDQSS	Write command to 1st DQS latching transition	0.75	1.25	tCK
tDQSL,(H)	DQS input low (high) pulse width (write cycle)	0.35	-	tCK
tDSS	DQS falling edge to CK setup time (write cycle)	0.35	-	tCK
tDSH	DQS falling edge hold time from CK (write cycle)	0.2	-	tCK
tMRD	Mode register set command cycle time	2	-	tCK
tWPST	Write postamble	0.4	0.6	tCK
tWPRE	Write preamble	0.25	0.25	tCK
tIH	Address and control input hold time	0.75	-	ns

tIS	Address and control input setup time	0.75	-	ns
tRPRE	Read preamble	0.9	1.1	tCK
tRPST	Read postamble	0.4	0.6	tCK
tRRD	Active bank A to Active bank B command	12	-	ns
tREFI	Average Periodic Refresh Interval ($85ºC < T_{CASE} \leq 95ºC$)	-	3.9	µs
	Average Periodic Refresh Interval ($0ºC \leq T_{CASE} \leq 85ºC$)	-	7.8	µs
tWR	Write recovery time without Auto-Precharge	15		ns
tDAL	Auto precharge write recovery + precharge time	-	-	tCK
tWTR	Internal write to read command delay	1	-	ns
tXSNR	Exit self refresh to a Non-read command	75	-	ns
tXSRD	Exit self refresh to a Read command	200	-	tCK
tCKE	CKE minimum pulse width	-	-	tCK

11. SPD

Serial Presence Detect – (512MB)

64Mx64 1 RANK UNBUFFERED DDR SDRAM DIMM based on 64Mx8, 4Banks, 8K Refresh, 2.6V DDR2 SDRAMs with SPD

Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
0	Number of Serial PD Bytes Written during Production	80	
1	Total Number of Bytes in Serial PD device	08	
2	Fundamental Memory Type	07	
3	Number of Row Addresses on Assembly	0D	
4	Number of Column Addresses on Assembly	0B	
5	Number of DIMM Bank, Package, and Height	01	
6	Data Width of this Assembly	40	
7	Reserved	00	
8	Voltage Interface Level of this Assembly	04	
9	DDR2 SDRAM Cycle Time at CL=5 (ns)	60	
10	DDR2 SDRAM Access Time from Clock at CL=5 (ns)	70	

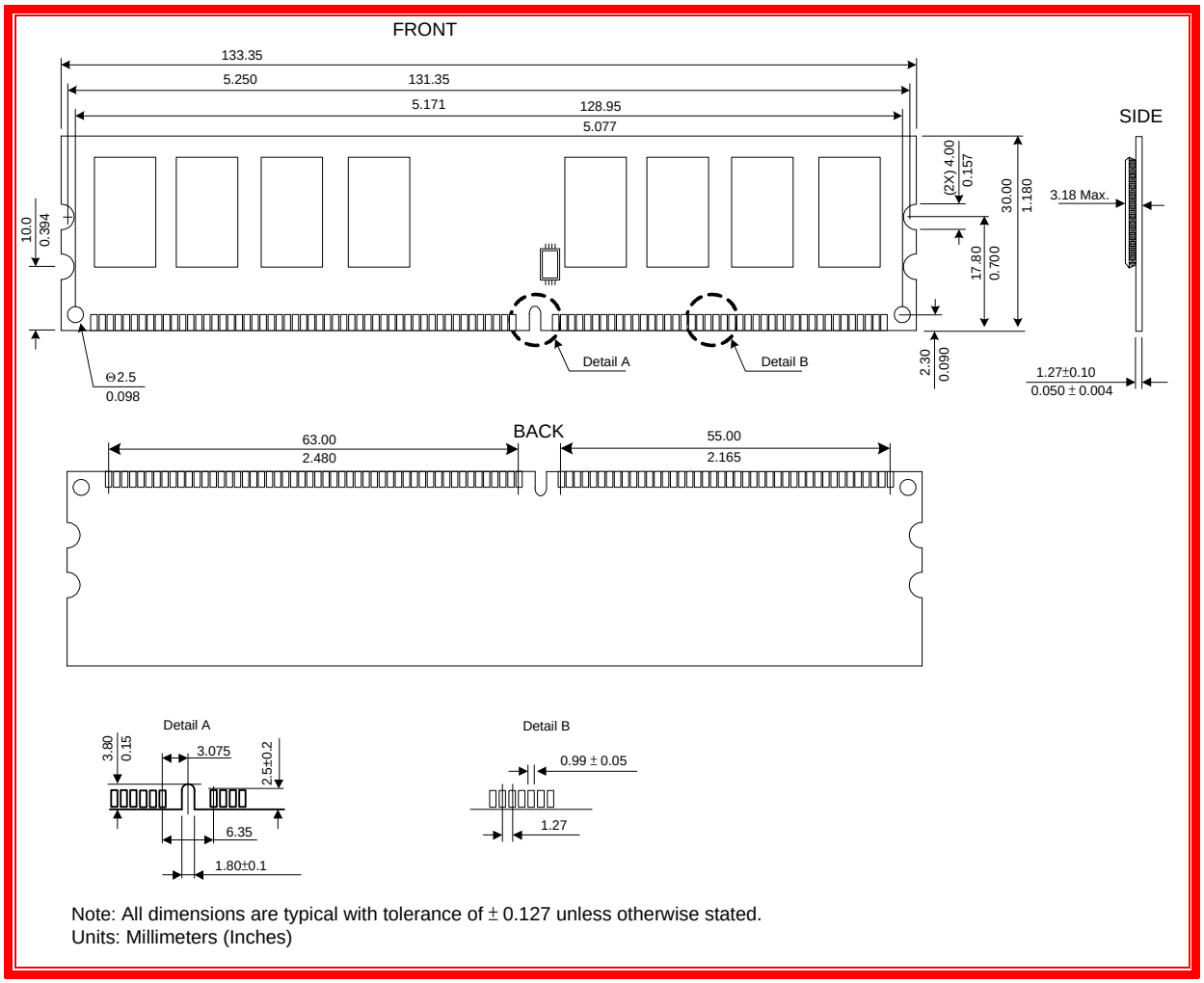
11	DIMM Configuration Type	00	
12	Refresh Rate/Type	82	
13	Primary DDR2 SDRAM Width	08	
14	Error Checking DDR2 SDRAM Device Width	00	
15	Reserved	01	
16	DDR2 SDRAM Device Attributes: Burst Length Supported	0E	
17	DDR2 SDRAM Device Attributes: Number of Device Banks	04	
18	DDR2 SDRAM Device Attributes: ΧΑΣ Latencies Supported	0C	
19	Reserved	01	
20	DDR2 SDRAM DIMM Type Information	02	
21	DDR2 SDRAM Module Attributes:	20	
22	DDR2 SDRAM Device Attributes: General	C0	
23	Minimum Clock Cycle at CL=4	75	
24	Maximum Data Access Time (t_{ac}) from Clock at CL=4 (ns)	70	
25	Minimum Clock Cycle Time at CL=3 (ns)	00	
26	Maximum Data Access Time (t_{ac}) from Clock at CL=3 (ns)	00	
27	Minimum Row Precharge Time (t_{RP}) (ns)	48	
28	Minimum Row Active to Row Active delay (t_{RRD})	30	
29	Minimum RAS to CAS delay (t_{RCD}) (ns)	48	
30	Minimum RAS Pulse Width (t_{RAS})	28	
31	Module Bank Density	80	
32	Address and Command Setup Time Before Clock (t_{IS}) (ns)	75	
33	Address and Command Hold Time After Clock (t_{IH}) (ns)	75	
34	Data Input Setup Time Before Clock (t_{DS})	45	
35	Data Input Hold Time After Clock (t_{DH}) (ns)	45	
36	Write Recovery Time (t_{WR})	00	
37	Internal Write to Read Command delay (t_{WTR})	00	
38	Internal Read to Precharge delay (t_{RTP})	00	
39	Memory Analysis Probe Characteristics	00	
40	Extension of Byte 41 t_{RC} and Byte 42 t_{RFC}	00	

41	Minimum Core Cycle Time (t_{RC}) (ns)	3C	
42	Min. Auto Refresh Command Cycle Time (t_{RFC})	48	
43	Maximum Clock Cycle Time (t_{CK})	30	
44	Max. DQS-DQ Skew Factor (t_{DQS}) (ns)	2D	
45	Read Data Hold Skew Factor (t_{QHS}) (ns)	55	
46	PLL Relock Time	00	
47	Tcasemax DT4R4W Delta	00	
48	Thermal Resistance of DRAM Package from Top (Case) to Ambient (Psi-T-A DRAM)	00	
49	DRAM Case Temperature Rise from Ambient due to Activate-Precharge/Mode Bits (DT0/Mode Bits)	00	
50	DRAM Case Temperature Rise from Ambient due to Precharge/Quiet Standby (DT2N/DT2Q)	00	
51	DRAM Case Temperature Rise from Ambient due to Precharge Power-Down (DT2P)	00	
52	DRAM Case Temperature Rise from Ambient due to Active Standby (DT3N)	00	
53	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Fast PDN Exit (DT3Pfast)	00	
54	DRAM Case Temperature Rise from Ambient due to Active Power-Down with Slow PDN Exit (DT3Pslow)	00	
55	DRAM Case Temperature Rise from Ambient due to Page Open Burst Read/DT4R4W Mode Bit (DT4R/DT4R4W Mode Bit)	00	
56	DRAM Case Temperature Rise from Ambient due to Burst Refresh (ST5B)	00	
57	DRAM Case Temperature Rise from Ambient due to Bank interleave Reads with Auto-Precharge (DT7)	00	
58	Thermal Resistance of PLL Package from Top (Case) to Ambient (Psi T-A PLL)	00	
59	Thermal Resistance of Register Package from Top (Case) to Ambient (Psi T-A Register)	00	

60	PLL Case Temperature Rise from Ambient due to PLL Active (DT PLL Active)	00	
61	Register Case Temperature Rise from Ambient due to Register Active/Mode Bit (DT Register Active/Mode Bit)	00	
62	SPD Reversion	11	
63	Checksum for byte 0-62	52	
64-71	Manufacture's JEDEC ID Code	InnoDisk	
72	Module Manufacturing Location	Manufacturing Code	
73-91	Module Part number	Module Part Number in ASCII	
92-255	Reserved	Undefined	

12. PACKAGE DIMENSION

- (512MB, 1 Rank, 64Mx8 DDR SDRAMs)



Note: Device position is only for reference.

13. RoHS Declaration

Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M1UF-12MC2CDB-(X) complies with the requirement of RoHS directives 2002/95/EC and 2006/122/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

- RoHS Exemptions Applied Of 7(C)-I for Resist.

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
Cd	＜ 100 ppm
Pb	＜ 1000 ppm
Hg	＜ 1000 ppm
Chromium VI（Cr+6）	＜ 1000 ppm
Polybromodiphenyl ether（PBDE）	＜ 1000 ppm
Polybrominated Biphenyls（PBB）	＜ 1000 ppm
Perfluorooctane Sulfonate (PFOS)	Not Contained

Date issued : 2014/05/22

Manufacturer: ：Innodisk Co., Ltd.
Address：221 5F, No. 237, Sec.1 Datong Rd.,Xizhi City, New Taipei City, Taiwan

Authorized Signature：

QA Dept. Director – Ryan Tsai

Revision Log

Rev	Date	Modification
0.1	8th July 2014	Preliminary Edition
1.0	8th July 2014	Official Released.
1.1	27th August 2014	Corrected Cover page on SDRAM temperature range
1.2	25th October 2014	Modified AC parameter and SPD.