

**MODEL:
NANO-ULT3**

**EPIC SBC with 14nm Intel® Core™ i7/i5/i3 or Celeron® On-board SoC,
LVDS, HDMI, iDP, Dual PCIe GbE, USB 3.2 Gen 1,
PCIe Mini, SATA 6Gb/s, mSATA, RS-232/422/485, Audio, and RoHS**

User Manual

Revision

Date	Version	Changes
July 6, 2021	1.03	Updated Section 2.3: Packing List Updated Chapter 6: Software Drivers Changed audio IC to ALC888S
February 7, 2018	1.02	Changed mSATA capability of the NANO-ULT3-C SKU from "not supported" to "supported".
May 11, 2017	1.01	Added new SKU (NANO-ULT3-CE) information
May 26, 2016	1.00	Initial release

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Manual Conventions



WARNING

Warnings appear where overlooked details may cause damage to the equipment or result in personal injury. Warnings should be taken seriously.



CAUTION

Cautionary messages should be heeded to help reduce the chance of losing data or damaging the product.



NOTE

These messages inform the reader of essential but non-critical information. These messages should be read carefully as any directions or instructions contained therein can help avoid making mistakes.

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Chapter

1

Introduction

1.1 Introduction

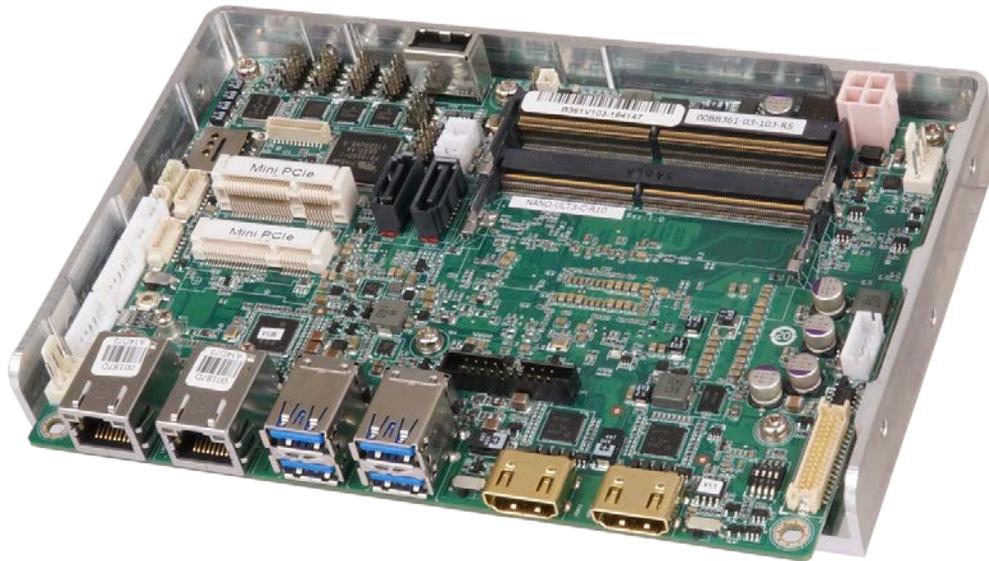


Figure 1-1: NANO-ULT3

The NANO-ULT3 series is an EPIC form factor single board computer. It has an on-board 14nm Intel® Core™ i7/i5/i3 or Celeron® processor, and supports two 260-pin 2133/1866 MHz dual-channel DDR4 non-ECC unbuffered SDRAM SO-DIMM slots with up to 32.0 GB of memory.

The NANO-ULT3 series includes an internal DisplayPort connector, two HDMI connectors and an 18-/24-bit LVDS connector for triple independent display.

Expansion and I/O include one full-size PCIe Mini slot supporting mSATA and 3G modules, one half-size PCIe Mini slot for expansion, four USB 3.2 Gen 1 (5Gb/s) connectors on the rear panel, two USB 2.0 connectors by pin header, one USB 2.0 type A connector on board and two SATA 6Gb/s connectors. Serial device connectivity is provided by two internal RS-232 connectors and one internal RS-232/422/485 connector. Two RJ-45 GbE connectors provide the system with smooth connections to an external LAN. One on-board SIM card socket also supports for 3G/LTE expansion.

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1.2 Model Variations

The model variations of the NANO-ULT3 series are listed below.

Model No.	SoC	mSATA
NANO-ULT3-i7	Intel® Core™ i7-6600U on-board SoC (up to 3.4 GHz, dual-core, 4 MB cache, TDP=15 W)	Supported
NANO-ULT3-i5	Intel® Core™ i5-6300U on-board SoC (up to 3.0 GHz, dual-core, 3 MB cache, TDP=15 W)	Supported
NANO-ULT3-i3	Intel® Core™ i3-6100U on-board SoC (up to 2.3 GHz, dual-core, 3 MB cache, TDP=15 W)	Supported
NANO-ULT3-C	Intel® Celeron® 3955U on-board SoC (up to 2.0 GHz, dual-core, 2 MB cache, TDP=15 W)	Supported
NANO-ULT3-CE (MOQ: 100 pcs/lot)	Intel® Celeron® 3855U on-board SoC (up to 1.6 GHz, dual-core, 2 MB cache, TDP=15 W)	Not supported

Table 1-1: NANO-ULT3 Model Variations

1.3 Features

Some of the NANO-ULT3 motherboard features are listed below:

- Thin EPIC motherboard with 6th generation Intel® ULT processor
- Triple independent display
- Two 2133/1866 MHz DDR4 SO-DIMM slots support up to 32 GB of memory
- Easy assembly heat spreader for thermal management
- Full-size PCIe Mini card slot with SIM card socket for 3G/LTE expansion
- Two SATA 6Gb/s connectors with power output
- Four USB 3.2 Gen 1 (5Gb/s) external connectors
- Two RS-232 connectors and one RS-232/422/485 connector
- Optional 8 GB eMMC 5.0
- Support mSATA modules (except NANO-ULT3-CE SKU)

1.4 Connectors

The connectors on the NANO-ULT3 are shown in the figure below.

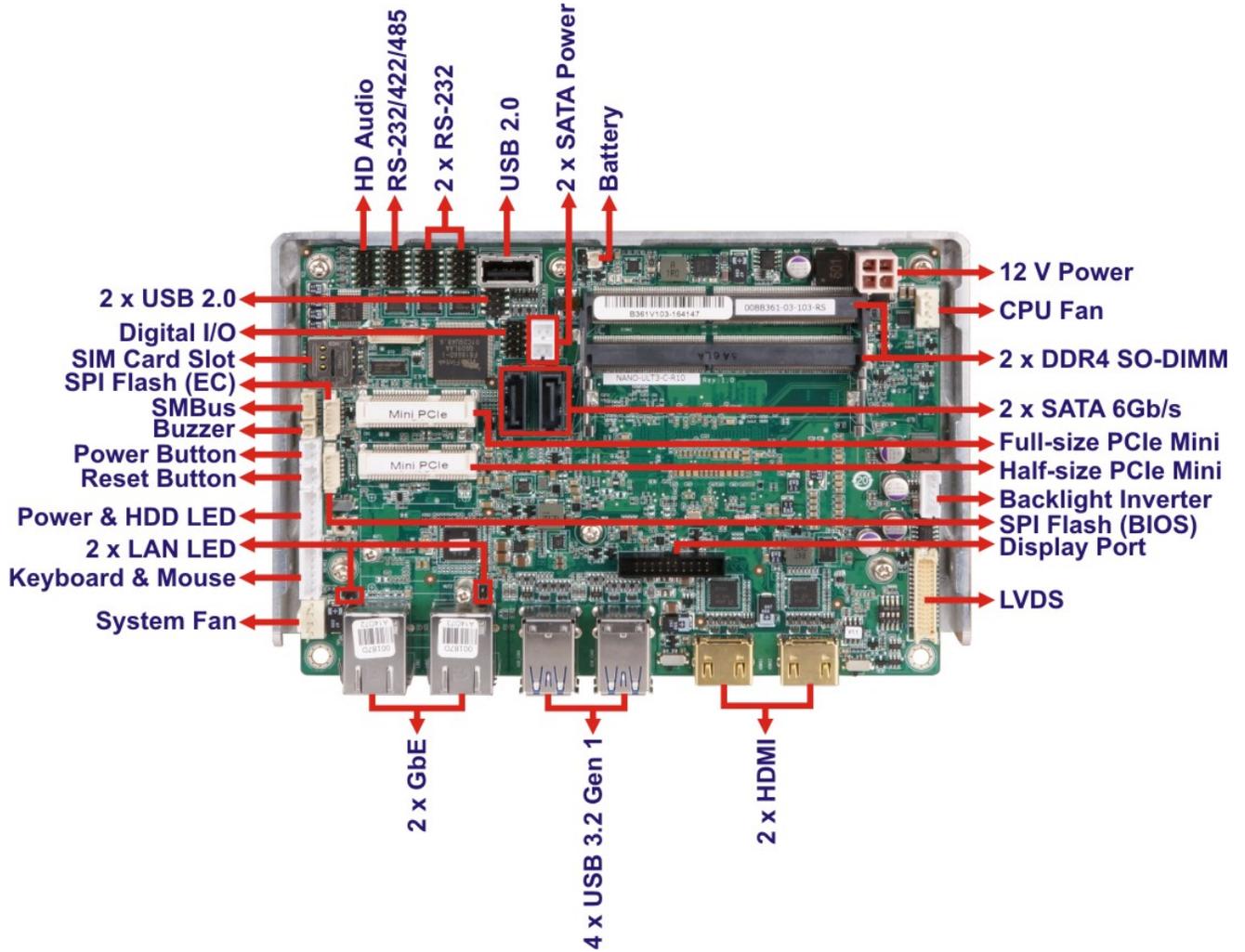


Figure 1-2: Connectors

NANO-ULT3 SBC

1.5 Dimensions

The dimensions of the board are listed below:

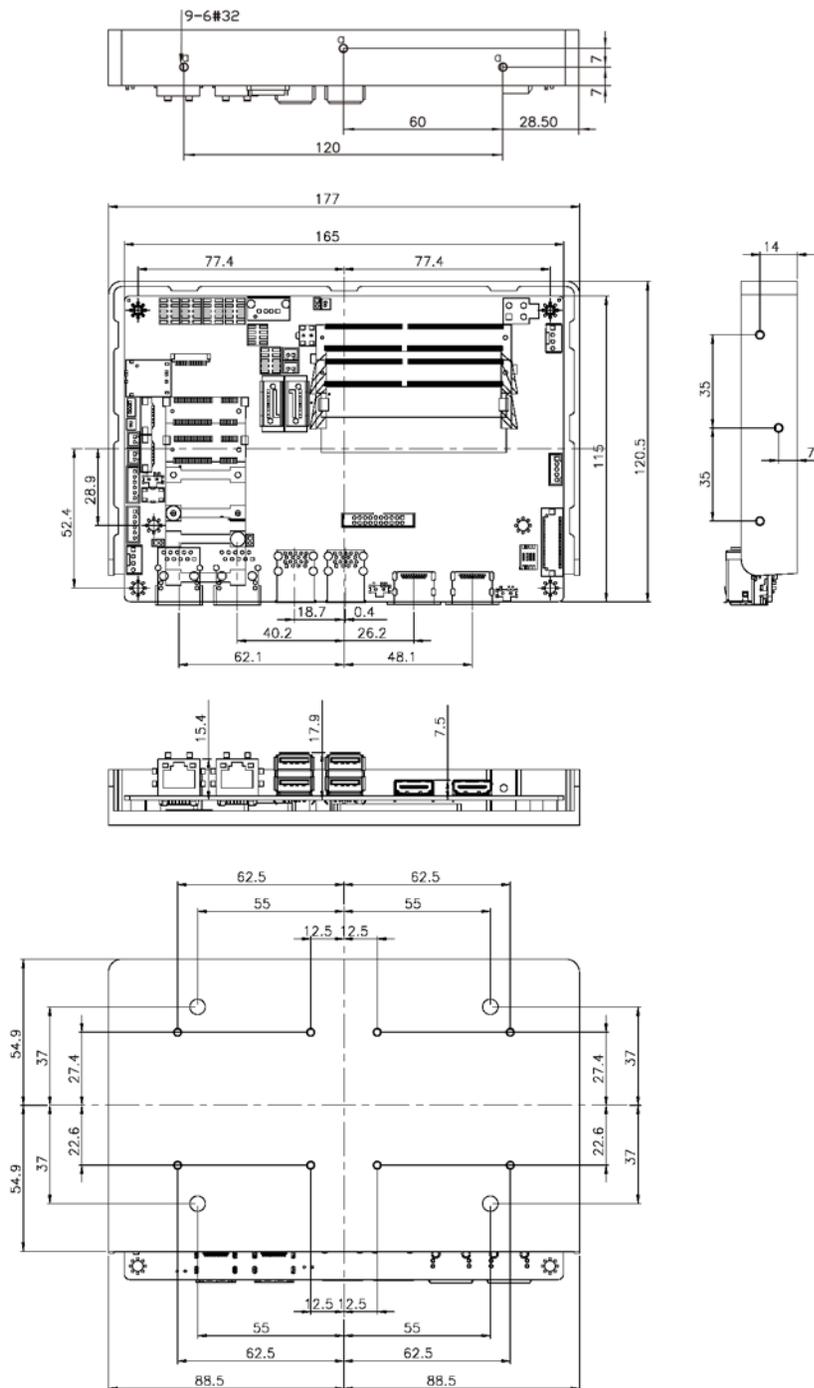


Figure 1-3: Dimensions (mm)

1.6 Data Flow

Figure 1-4 shows the data flow between the system chipset, the CPU and other components installed on the motherboard.

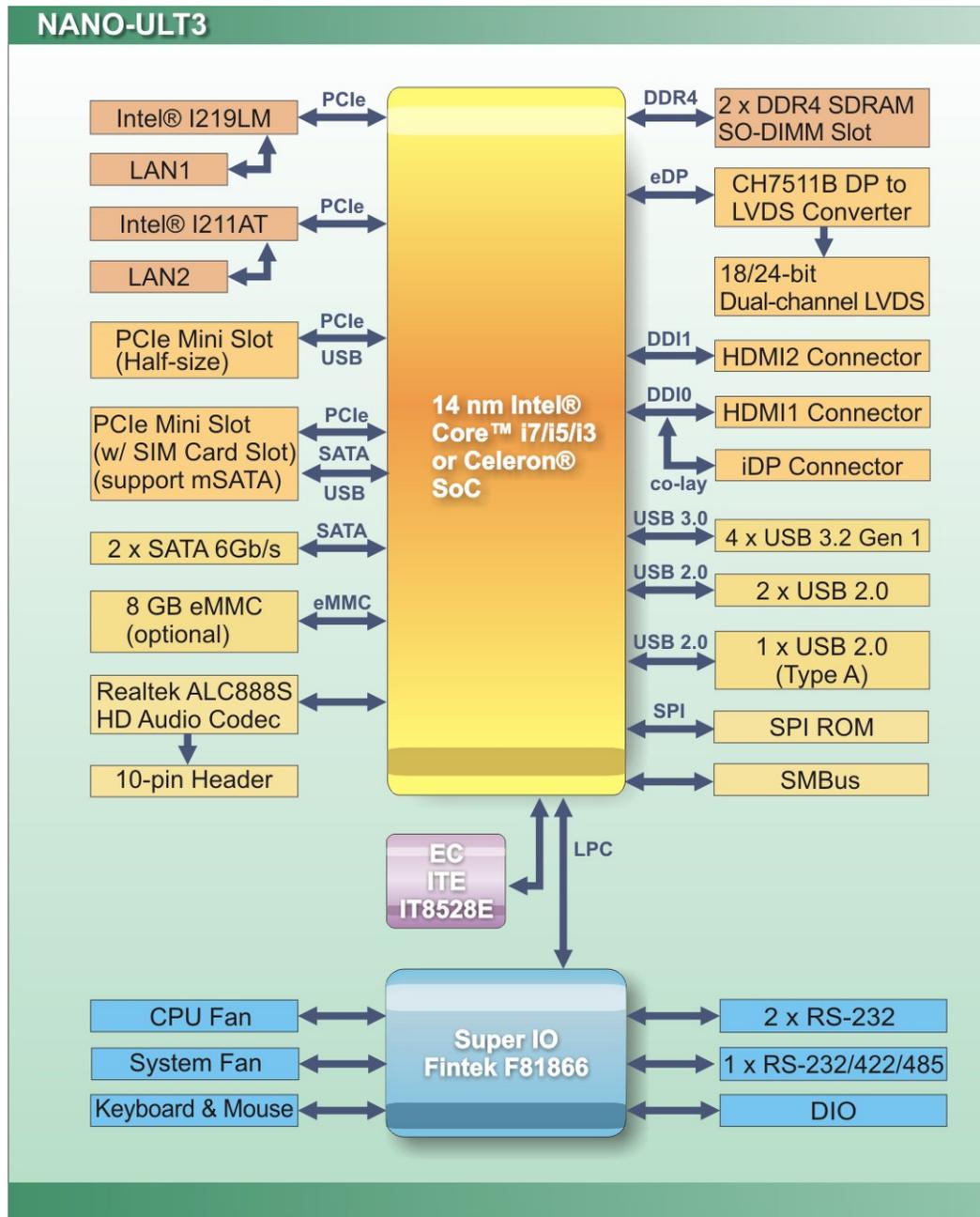


Figure 1-4: Data Flow Diagram

NANO-ULT3 SBC

1.7 Technical Specifications

NANO-ULT3 technical specifications are listed below.

Specification	NANO-ULT3
SoC	<p>6th generation Intel® mobile ULT on-board SoC:</p> <ul style="list-style-type: none"> ▪ Intel® Core™ i7-6600U on-board SoC (up to 3.4 GHz, dual-core, 4 MB cache, TDP=15 W) ▪ Intel® Core™ i5-6300U on-board SoC (up to 3.0 GHz, dual-core, 3 MB cache, TDP=15 W) ▪ Intel® Core™ i3-6100U on-board SoC (up to 2.3 GHz, dual-core, 3 MB cache, TDP=15 W) ▪ Intel® Celeron® 3955U on-board SoC (up to 2.0 GHz, dual-core, 2 MB cache, TDP=15 W) ▪ Intel® Celeron® 3855U on-board SoC (up to 1.6 GHz, dual-core, 2 MB cache, TDP=15 W)
BIOS	AMI UEFI BIOS
Memory	Two 260-pin 2133/1866 MHz dual-channel DDR4 non-ECC unbuffered SO-DIMM slots (system max. 32 GB)
Graphics	9 th generation Intel® HD Graphics with 16 low-power execution units, supporting DX11, DX12, OpenGL 4.3/4.4 and OpenCL2.x, ES 2.0
Display Output	<p>Triple independent display</p> <p>2 x HDMI (HDMI2 connector supports up to 4096x2160 @ 24Hz)</p> <p>1 x 18/24-bit dual-channel LVDS by CH7511B DP to LVDS converter (up to 1920x1200 @ 60Hz)</p> <p>1 x iDP interface for HDMI, LVDS, VGA, DVI, DP (up to 4096x2304 @ 60Hz) (co-lay with HDMI1)</p>
Ethernet	<p>LAN1: Intel® I219-LM PHY with Intel® AMT 11.0 support</p> <p>LAN2: Intel® I211-AT PCIe GbE controller</p>
Digital I/O	8-bit digital I/O by 10-pin (2x5) header

Specification	NANO-ULT3
Super IO	Fintek F81866D-I
Embedded Controller	ITE IT8528E/FX
Audio	Realtek ALC888S HD codec
Watchdog Timer	Software programmable support 1~255 sec. system reset
I/O Interface	
Audio Connector	1 x Analog audio by 10-pin (2x5) header
Ethernet	2 x RJ-45 GbE port
Keyboard/Mouse	1 x KB/MS by 6-pin (1x6) wafer
Serial Ports	1 x RS-232/422/485 by 10-pin (2x5) header 2 x RS-232 by 10-pin (2x5) header
USB Ports	4 x USB 3.2 Gen 1 (5Gb/s) on rear I/O 2 x USB 2.0 by 8-pin (2x4) header 1 x USB 2.0 on board by type A connector (180°)
Front Panel	1 x Power LED and HDD LED connector by 6-pin (1x6) wafer 1 x Power button connector by 2-pin (1x2) wafer 1 x Reset button connector by 2-pin (1x2) wafer
LAN LED	2 x LAN link LED connector by 2-pin header
Fan	1 x CPU fan connector by 4-pin (1x4) wafer 1 x System fan connector by 4-pin (1x4) wafer
SMBus	1 x SMBus connector by 4-pin (1x4) wafer
Storage	2 x SATA 6Gb/s with 5 V SATA power connectors (support RAID 0, 1) 8 GB eMMC (optional)

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Specification	NANO-ULT3
Expansion	<p>1 x Half-size PCIe Mini card* slot</p> <p>1 x Full-size PCIe Mini card* slot (with SIM card socket and mSATA** support)</p> <p>* The PCIe Mini slots on the NANO-ULT3-CE SKU are PCI Express 2.0 slots that do not support PCI Express 3.0, and the half-size PCIe Mini slot does not support USB 2.0 signal.</p> <p>** The NANO-ULT3-CE SKU with Intel® Celeron® 3855U CPU does not support mSATA modules.</p>
Environmental and Power Specifications	
Power Supply	12 V DC input only (AT/ATX support)
Power Connector	1 x Internal power connector by 4-pin (2x2) connector
Power Consumption	+12 V @ 2.48 A (Intel® Core™ i3-6100U with two 8 GB DDR4 memory)
Operating Temperature	-20°C ~ 60°C
Storage Temperature	-30°C ~ 70°C
Humidity	5% ~ 95%, non-condensing
Physical Specifications	
Dimensions	115 mm x 165 mm
Weight GW/NW	850 g / 350 g

Table 1-2: Technical Specifications

Chapter

2

Unpacking

NANO-ULT3 SBC

2.1 Anti-static Precautions



WARNING!

Static electricity can destroy certain electronics. Make sure to follow the ESD precautions to prevent damage to the product, and injury to the user.

Make sure to adhere to the following guidelines:

- **Wear an anti-static wristband:** Wearing an anti-static wristband can prevent electrostatic discharge.
- **Self-grounding:** Touch a grounded conductor every few minutes to discharge any excess static buildup.
- **Use an anti-static pad:** When configuring any circuit board, place it on an anti-static mat.
- **Only handle the edges of the PCB:** Don't touch the surface of the motherboard. Hold the motherboard by the edges when handling.

2.2 Unpacking Precautions

When the NANO-ULT3 is unpacked, please do the following:

- Follow the antistatic guidelines above.
- Make sure the packing box is facing upwards when opening.
- Make sure all the packing list items are present.

2.3 Packing List



NOTE:

If any of the components listed in the checklist below are missing, do not proceed with the installation. Contact the IEI reseller or vendor the NANO-ULT3 was purchased from or contact an IEI sales representative directly by sending an email to sales@ieiworld.com.

The NANO-ULT3 is shipped with the following components:

Quantity	Item and Part Number	Image
1	NANO-ULT3 single board computer	
1	Audio cable	
1	Power cable	
1	RS-232 cable	
1	SATA with power cable kit	
1	Quick Installation Guide	

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2.4 Optional Items

The following are optional components which may be separately purchased:

Item and Part Number	Image
KB/MS PS/2 Y-cable, 155mm/130mm, p=2.0 (P/N: 32006-001100-201-RS)	
Dual USB cable (wo bracket), 210 mm, p=2.0 (P/N: 32001-008600-200-RS)	

Chapter

3

Connectors

NANO-ULT3 SBC

3.1 Peripheral Interface Connectors

This chapter details all the jumpers and connectors.

3.1.1 NANO-ULT3 Layout

The figures below show all the connectors and jumpers.

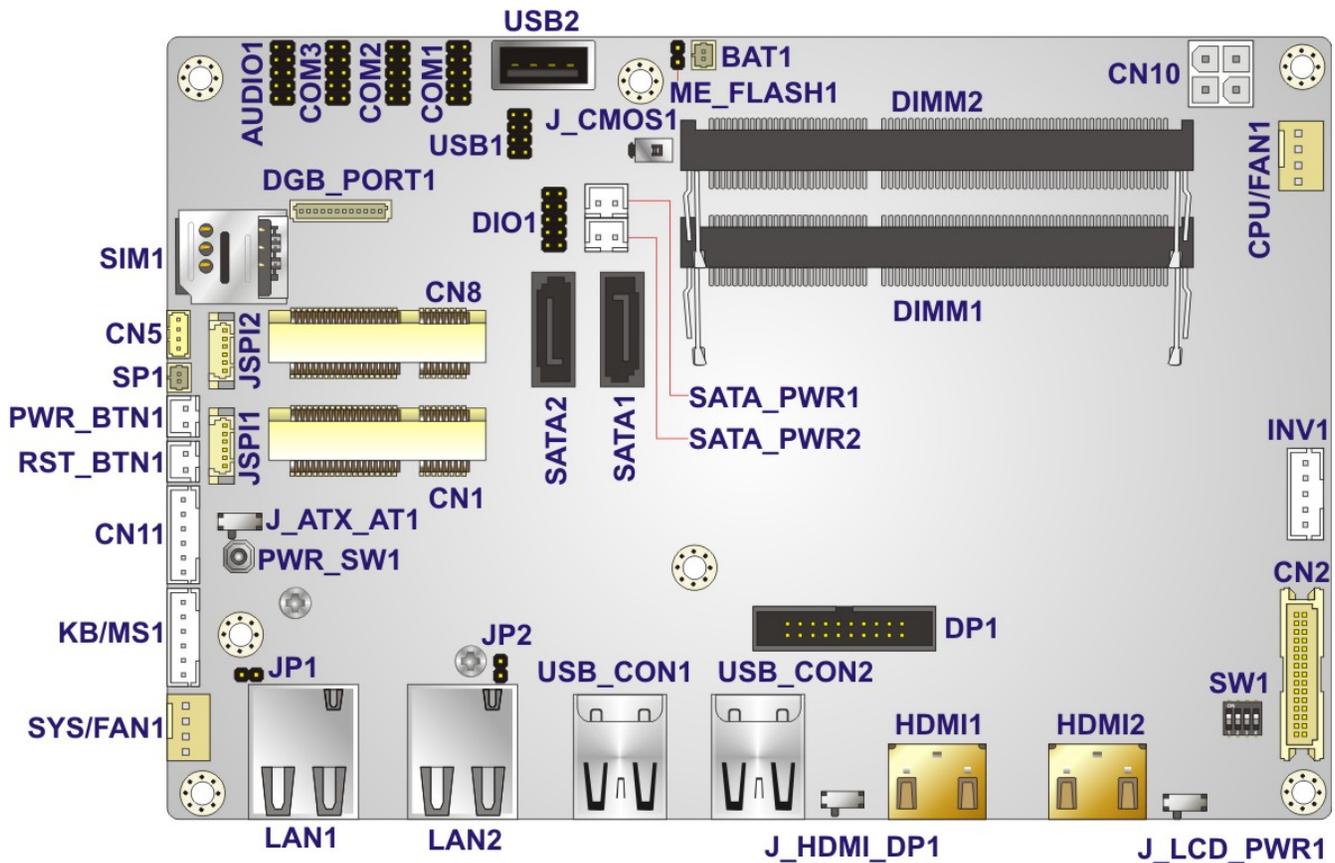


Figure 3-1: Connector and Jumper Locations

3.1.2 Peripheral Interface Connectors

The table below lists all the connectors on the board.

Connector	Type	Label
+12V DC-IN power connector	4-pin Molex	CN10
Audio connector	10-pin header	AUDIO1

Battery connector	2-pin wafer	BAT1
Buzz connector	2-pin wafer	SP1
Digital I/O connector	10-pin header	DIO1
Debug card connector	12-pin wafer	DBG_PORT1
Fan connector, CPU	4-pin wafer	CPU/FAN1
Fan connector, system	4-pin wafer	SYS/FAN1
Front panel connector	6-pin wafer	CN11
Internal DisplayPort connector	20-pin box header	DP1
Keyboard & mouse connector	6-pin wafer	KB/MS1
LCD backlight inverter connector	5-pin wafer	INV1
LVDS LCD connector	30-pin crimp	CN2
LAN LED connectors	2-pin header	JP1, JP2
Memory slot	260-pin DDR4 SO-DIMM	DIMM1, DIMM2
PCIe Mini card slot, half-size	Half-size PCIe Mini slot	CN1
PCIe Mini card slot, full-size	Full-size PCIe Mini slot	CN8
Power button (on board)	Push button	PWR_SW1
Power button connector	2-pin wafer	PWR_BTN1
Reset button connector	2-pin wafer	RST_BTN1
RS-232 serial port connectors	10-pin header	COM1, COM2
RS-232/422/485 serial port connector	10-pin header	COM3
SATA 6Gb/s drive connectors	7-pin SATA connector	SATA1, SATA2
SATA power connectors	2-pin wafer	SATA_PWR1, SATA_PWR2
SMBus connector	4-pin wafer	CN5

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SIM card slot	SIM slot	SIM1
SPI flash connector, BIOS	6-pin wafer	JSPI1
SPI flash connector, EC	6-pin wafer	JSPI2
USB 2.0 connector	8-pin header	USB1
USB 2.0 connector	USB type A	USB2

Table 3-1: Peripheral Interface Connectors**3.1.3 External Interface Panel Connectors**

The table below lists the connectors on the external I/O panel.

Connector	Type	Label
LAN connectors	RJ-45	LAN1, LAN2
HDMI connectors	HDMI	HDMI1, HDMI2
USB 3.2 Gen 1 (5Gb/s) connectors	USB Type-A	USB_CON1, USB_CON2

Table 3-2: Rear Panel Connectors

3.2 Internal Peripheral Connectors

The section describes all of the connectors on the NANO-ULT3.

3.2.1 +12V DC-IN Power Connector

- CN Label:** CN10
- CN Type:** 4-pin Molex, p=4.2 mm
- CN Location:** See **Figure 3-2**
- CN Pinouts:** See **Table 3-3**

The connector supports the +12V power supply.

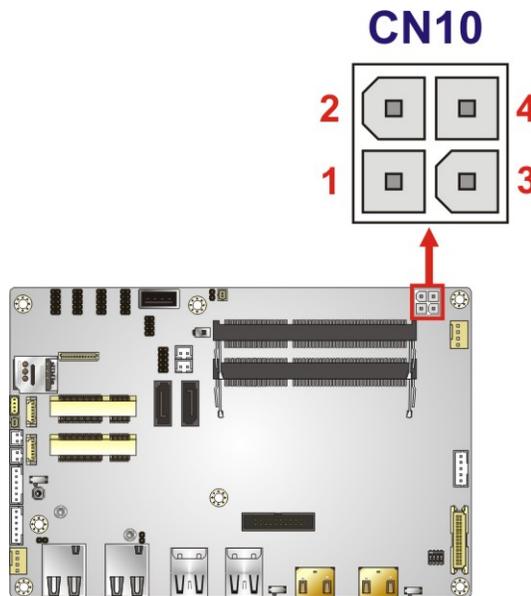


Figure 3-2: +12V DC-IN Power Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	GND
3	+12V	4	+12V

Table 3-3: +12V DC-IN Power Connector Pinouts

NANO-ULT3 SBC

3.2.2 Audio Connector

- CN Label:** AUDIO1
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See **Figure 3-3**
- CN Pinouts:** See **Table 3-4**

The audio connector is connected to external audio devices including speakers and microphones for the input and output of audio signals to and from the system.

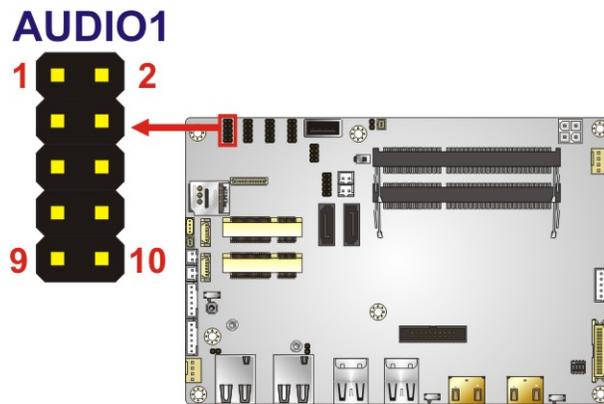


Figure 3-3: Audio Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	LINE_OUTR	2	LINEIN_R
3	ANALOG_GND	4	ANALOG_GND
5	LINE_OUTL	6	LINEIN_L
7	ANALOG_GND	8	ANALOG_GND
9	MICIN1	10	MICIN2

Table 3-4: Audio Connector Pinouts

3.2.3 Battery Connector



CAUTION:

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

CN Label:	BAT1
CN Type:	2-pin wafer, p=1.25 mm
CN Location:	See Figure 3-4
CN Pinouts:	See Table 3-5

The battery connector is connected to the system battery. The battery provides power to the system clock to retain the time when power is turned off. **NOTE:** It is recommended to attach the RTC battery onto the system chassis in which the NANO-ULT3 is installed.

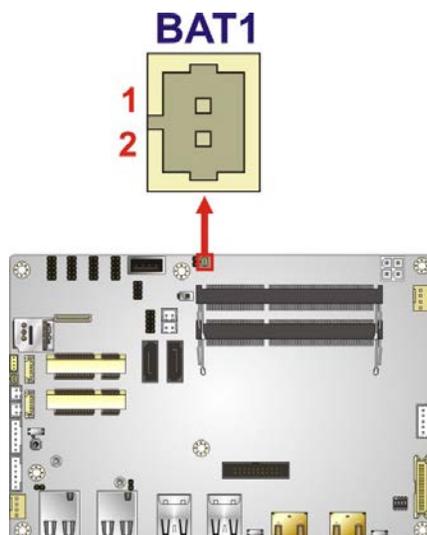


Figure 3-4: Battery Connector Location

NANO-ULT3 SBC

Pin	Description
1	VBAT+
2	GND

Table 3-5: Battery Connector Pinouts

3.2.4 Buzzer Connector

CN Label:	SP1
CN Type:	2-pin wafer, p=1.25 mm
CN Location:	See Figure 3-5
CN Pinouts:	See Table 3-6

The buzzer connector is connected to the buzzer. **NOTE:** If you cannot find a good place to put a buzzer on the NANO-ULT3, it is recommended to attach the buzzer onto the system chassis in which the NANO-ULT3 is installed.

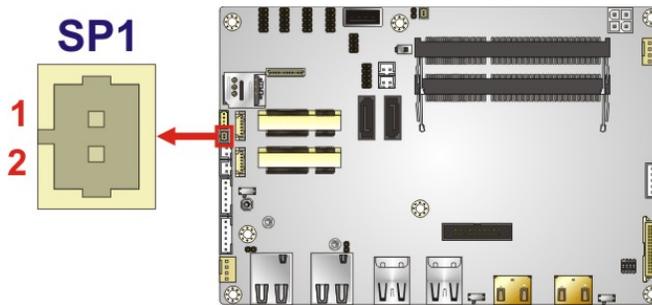


Figure 3-5: Buzzer Connector Location

Pin	Description
1	Buzzer+
2	Buzzer-

Table 3-6: Buzzer Connector Pinouts

3.2.5 Digital I/O Connector

- CN Label:** DIO1
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See **Figure 3-6**
- CN Pinouts:** See **Table 3-7**

The 8-bit digital I/O connector provides programmable input and output for external devices.

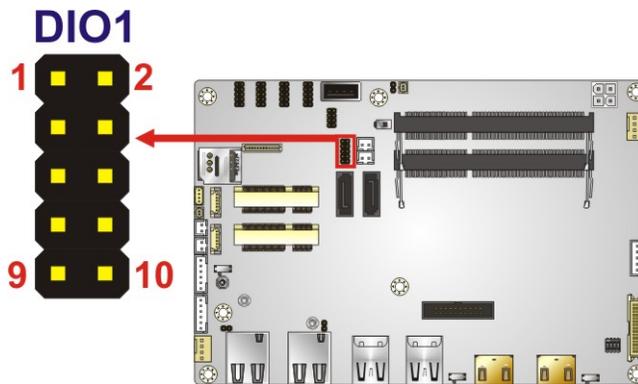


Figure 3-6: Digital I/O Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	GND	2	+5V
3	DOUT3	4	DOUT2
5	DOUT1	6	DOUT0
7	DIN3	8	DIN2
9	DIN1	10	DIN0

Table 3-7: Digital I/O Connector Pinouts

NANO-ULT3 SBC

3.2.6 Fan Connectors

CN Label: CPU/FAN1, SYS/FAN1

CN Type: 4-pin wafer, p=2.54 mm

CN Location: See **Figure 3-7**

CN Pinouts: See **Table 3-8**

The fan connector attaches to a cooling fan.



Figure 3-7: Fan Connector Locations

Pin	Description
1	GND
2	+12V
3	FANIO
4	PWM

Table 3-8: Fan Connector Pinouts

3.2.7 Front Panel Connector

- CN Label:** CN11
- CN Type:** 6-pin wafer, p=2.00 mm
- CN Location:** See **Figure 3-8**
- CN Pinouts:** See **Table 3-9**

The front panel connector connects to the power LED indicator and HDD LED indicator on the system front panel.

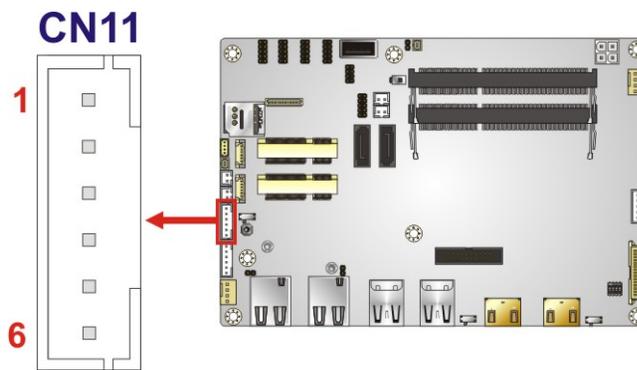


Figure 3-8: Front Panel Connector Location

Pin	Description
1	VCC
2	GND
3	PWR_LED+
4	PWR_LED-
5	HDD_LED+
6	HDD_LED-

Table 3-9: Front Panel Connector Pinouts

NANO-ULT3 SBC

3.2.8 Internal DisplayPort Connector



NOTE:

The iDP connector is disabled by default since the iDP connector is co-lay with the HDMI1 connector. To enable the iDP connector, use the HDMI/DP select switch to configure the settings. Please refer to **Section 4.6.4** for detailed information.

CN Label:	DP1
CN Type:	20-pin box header, p=2.00 mm
CN Location:	See Figure 3-9
CN Pinouts:	See Table 3-10

The internal DisplayPort (iDP) connector supports HDMI, LVDS, VGA, DVI and DisplayPort devices with up to 4096x2304 resolutions.

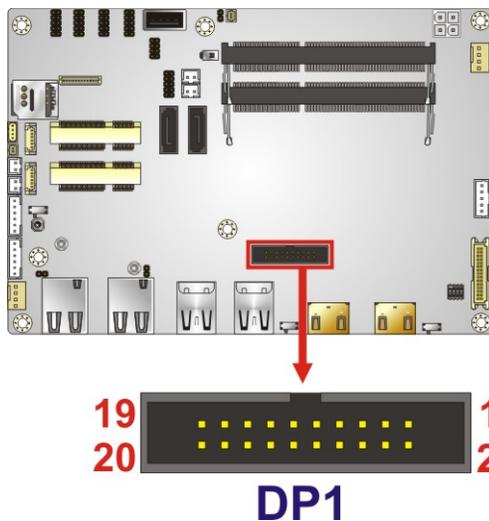


Figure 3-9: Internal DisplayPort Connector Location

Pin	Description	Pin	Description
1	HPD	2	AUX+
3	GND	4	AUX-
5	CAD	6	GND
7	GND	8	Lane2+
9	Lane3+	10	Lane2-
11	Lane3-	12	GND
13	GND	14	Lane0+
15	Lane1+	16	Lane0-
17	Lane1-	18	VCC3
19	VCC5	20	NC

Table 3-10: Internal DisplayPort Connector Pinouts

3.2.9 Keyboard and Mouse Connector

- CN Label:** KB/MS1
- CN Type:** 6-pin wafer, p=2.00 mm
- CN Location:** See **Figure 3-10**
- CN Pinouts:** See **Table 3-11**

The keyboard/mouse connector connects to a PS/2 Y-cable that can be connected to a PS/2 keyboard and mouse.

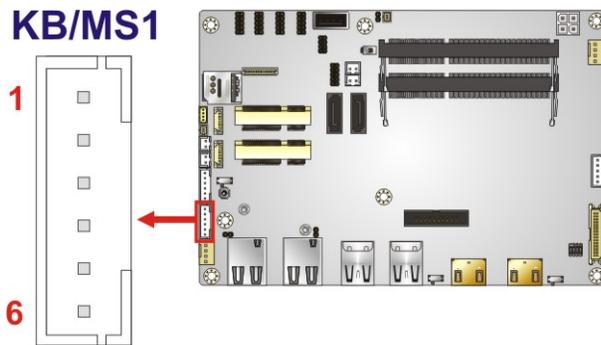


Figure 3-10: Keyboard and Mouse Connector Location

NANO-ULT3 SBC

Pin	Description
1	VCC5V
2	Mouse Data
3	Mouse Clock
4	Keyboard Data
5	Keyboard Clock
6	GND

Table 3-11: Keyboard and Mouse Connector Pinouts

3.2.10 LVDS Backlight Inverter Connector

- CN Label:** INV1
- CN Type:** 5-pin wafer, p=2.00 mm
- CN Location:** See **Figure 3-11**
- CN Pinouts:** See **Table 3-12**

The backlight inverter connector provides power to an LCD panel.

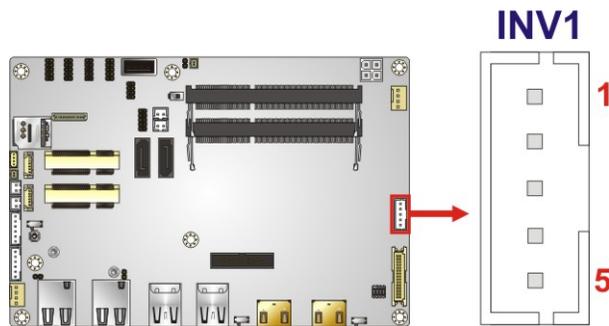


Figure 3-11: Backlight Inverter Connector Location

Pin	Description
1	LCD_BKLTCTL
2	GND
3	+12V
4	GND
5	BACKLIGHT_ENABLE

Table 3-12: Backlight Inverter Connector Pinouts

3.2.11 LVDS LCD Connector

- CN Label:** CN2
- CN Type:** 30-pin crimp, p=1.25 mm
- CN Location:** See **Figure 3-12**
- CN Pinouts:** See **Table 3-13**

The LVDS connector is for an LCD panel to connect to the board.

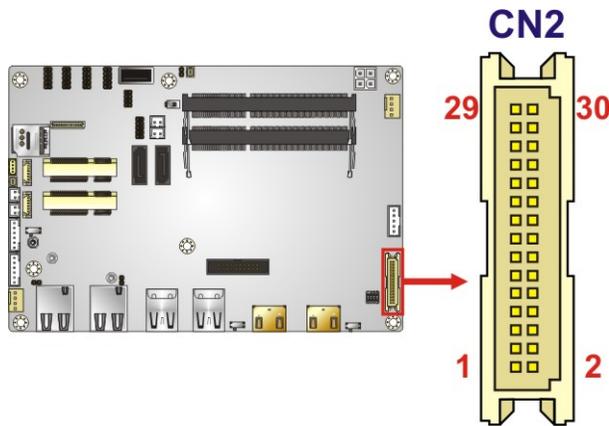


Figure 3-12: LVDS Connector Location

Pin	Description	Pin	Description
1	GROUND	2	GROUND
3	LVDS_A_TX0-P	4	LVDS_A_TX0-N
5	LVDS_A_TX1-P	6	LVDS_A_TX1-N
7	LVDS_A_TX2-P	8	LVDS_A_TX2-N
9	LVDS_A_TXCLK-P	10	LVDS_A_TXCLK-N
11	LVDS_A_TX3-P	12	LVDS_A_TX3-N
13	GROUND	14	GROUND
15	LVDS_B_TX0-P	16	LVDS_B_TX0-N
17	LVDS_B_TX1-P	18	LVDS_B_TX1-N
19	LVDS_B_TX2-P	20	LVDS_B_TX2-N
21	LVDS_B_TXCLK-P	22	LVDS_B_TXCLK-N
23	LVDS_B_TX3-P	24	LVDS_B_TX3-N
25	GROUND	26	GROUND

NANO-ULT3 SBC

Pin	Description	Pin	Description
27	+LCD VCC	28	+LCD VCC
29	+LCD VCC	30	+LCD VCC

Table 3-13: LVDS Connector Pinouts

3.2.12 LAN LED Connectors

- CN Label:** JP1, JP2
- CN Type:** 2-pin header, p=2.00 mm
- CN Location:** See Figure 3-13
- CN Pinouts:** See Table 3-14

The LAN LED connectors connect to the LAN link LEDs on the system.

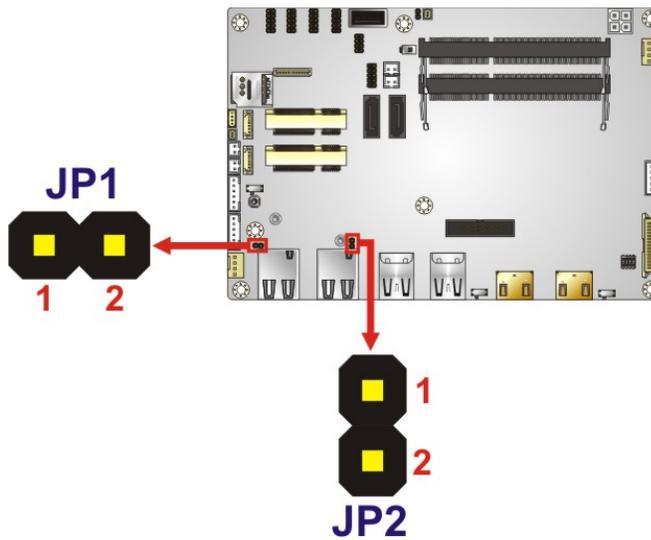


Figure 3-13: LAN LED Connector Locations

Pin	Description
1	+3.3VLAN
2	LAN_LED_LINK#

Table 3-14: LAN LED Connector Pinouts

3.2.13 PCIe Mini Card Slot, Full-size

- CN Label:** CN8
- CN Type:** Full-size PCIe Mini card slot
- CN Location:** See **Figure 3-14**
- CN Pinouts:** See **Table 3-15**

The PCIe Mini card slot supports PCIe Mini cards with USB interface, including mSATA modules and 3G modules.



NOTE:

1. The NANO-ULT3-CE SKU with Intel® Celeron® 3855U CPU does not support mSATA modules.
2. The PCIe Mini slots on the NANO-ULT3-CE SKU are PCI Express 2.0 slots that do not support PCI Express 3.0.
3. If the mSATA module installed on the NANO-ULT3 can not be detected, please set CN8 as an mSATA slot manually in BIOS option (Chipset > PCH-IO Configuration > PCI Express Configuration > Full Size PCIE Mini Card Selection). Please refer to **Section 5.4.2.1**.

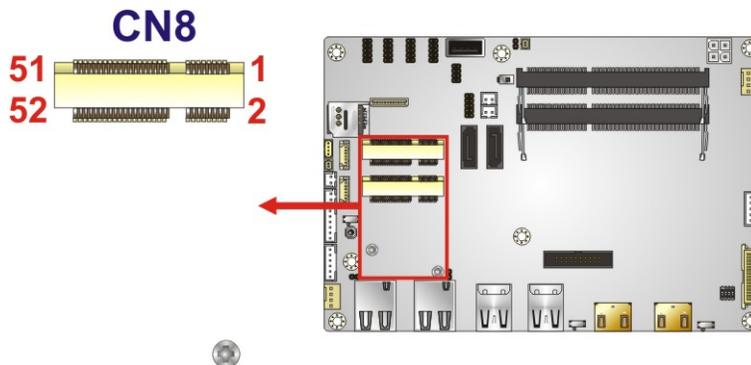


Figure 3-14: Full-size PCIe Mini Card Slot Location

NANO-ULT3 SBC

Pin	Description	Pin	Description
1	PCIE_WAKE#	2	VCC3
3	N/C	4	GND
5	N/C	6	1.5 V
7	VCC3	8	SIM_VCC
9	GND	10	SIM_IO
11	CLK-	12	SIM_CLK
13	CLK+	14	SIM_RST
15	GND	16	SIM_VPP
17	BUF_PLT_RST#	18	GND
19	N/C	20	VCC3
21	GND	22	BUF_PLT_RST#
23	SATA_RXN2_C	24	VCC3
25	SATA_RXP2_C	26	GND
27	GND	28	1.5 V
29	GND	30	SMBCLK
31	SATA_TXN2	32	SMBDATA
33	SATA_TXP2	34	GND
35	GND	36	USB7-
37	GND	38	USB7+
39	VCC3	40	GND
41	VCC3	42	N/C
43	GND	44	RF_LINK#
45	N/C	46	BLUELED#
47	N/C	48	1.5 V
49	N/C	50	GND
51	M-SATADET	52	VCC3

Table 3-15: Full-size PCIe Mini Card Slot Pinouts

3.2.14 PCIe Mini Card Slot, Half-size

- CN Label:** CN1
- CN Type:** Half-size PCIe Mini card slot
- CN Location:** See **Figure 3-15**
- CN Pinouts:** See **Table 3-16**

The PCIe Mini card slot is for installing a half-size PCIe Mini expansion card with USB interface.



NOTE:

This half-size PCIe Mini slot on the NANO-ULT3-CE SKU is a PCI Express 2.0 slot, and it does not support USB 2.0 signal.

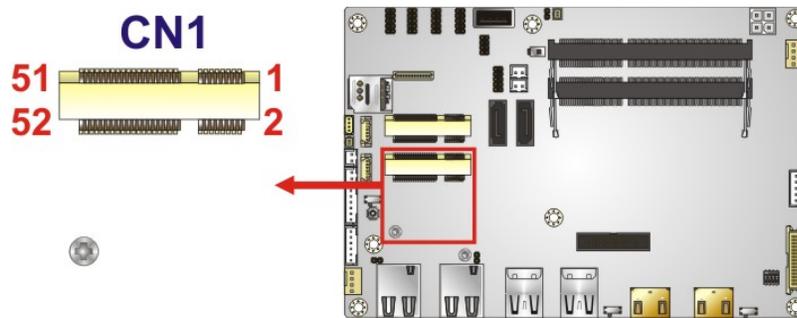


Figure 3-15: Half-size PCIe Mini Slot Location

Pin	Description	Pin	Description
1	PCIE_WAKE#	2	VCC3
3	N/C	4	GND
5	N/C	6	1.5 V
7	VCC3	8	N/C
9	GND	10	N/C
11	CLK_PCIE_MINI2_N	12	N/C
13	CLK_PCIE_MINI2_P	14	N/C
15	GND	16	N/C

NANO-ULT3 SBC

Pin	Description	Pin	Description
17	BUF_PLT_RST#	18	GND
19	N/C	20	VCC3
21	GND	22	BUF_PLT_RST#
23	PCIE_RX4DN	24	VCC3
25	PCIE_RX4DP	26	GND
27	GND	28	1.5V
29	GND	30	SMBCLK
31	PCIE_TX4DN	32	SMBDATA
33	PCIE_TX4DP	34	GND
35	GND	36	USB8-
37	GND	38	USB8+
39	VCC3	40	GND
41	VCC3	42	N/C
43	GND	44	RF_LINK#
45	N/C	46	BLUELED#
47	N/C	48	1.5 V
49	N/C	50	GND
51	N/C	52	VCC3

Table 3-16: Half-size PCIe Mini Slot Pinouts

3.2.15 Power Button

CN Label: PWR_SW1

CN Type: Push button

CN Location: See Figure 3-16

The on-board power button controls system power.

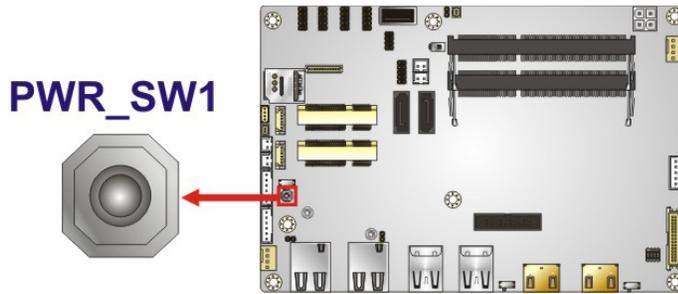


Figure 3-16: Power Button Location

3.2.16 Power Button Connector

- CN Label:** PWR_BTN1
- CN Type:** 2-pin wafer, p=2.00 mm
- CN Location:** See **Figure 3-17**
- CN Pinouts:** See **Table 3-17**

The power button connector is connected to a power switch on the system chassis to enable users to turn the system on and off.

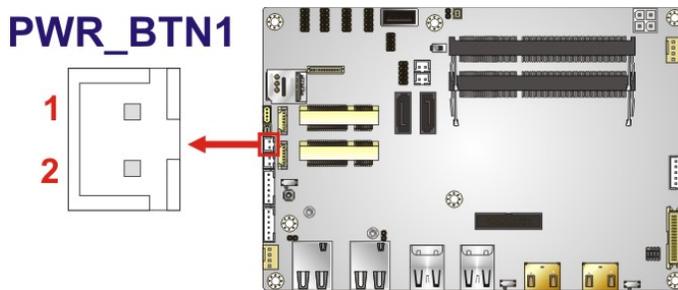


Figure 3-17: Power Button Connector Location

Pin	Description
1	PWR_BTN+
2	PWR_BTN-

Table 3-17: Power Button Connector Pinouts

NANO-ULT3 SBC

3.2.17 Reset Button Connector

- CN Label:** RST_BTN1
- CN Type:** 2-pin wafer, p=2.00 mm
- CN Location:** See **Figure 3-18**
- CN Pinouts:** See **Table 3-18**

The reset button connector is connected to a reset switch on the system chassis to enable users to reboot the system when the system is turned on.

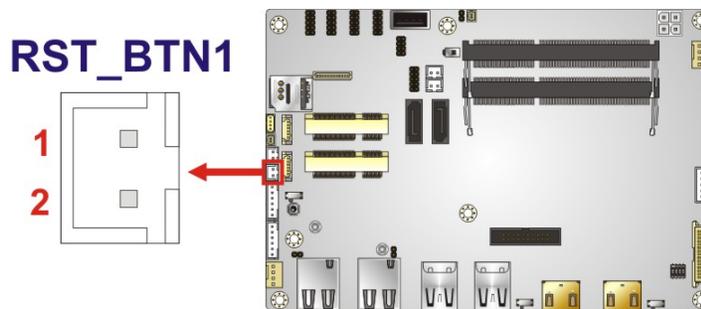


Figure 3-18: Reset Button Connector Location

Pin	Description
1	RESET+
2	RESET-

Table 3-18: Reset Button Connector Pinouts

3.2.18 RS-232 Serial Port Connectors

- CN Label:** COM1, COM2
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See **Figure 3-19**
- CN Pinouts:** See **Table 3-19**

The serial connector provides RS-232 connection.

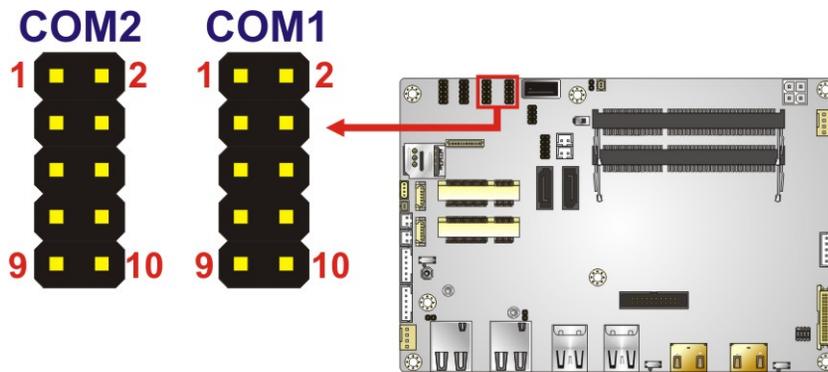


Figure 3-19: RS-232 Serial Port Connector Locations

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	DCD	2	DSR
3	SIN	4	RTS
5	SOUT	6	CTS
7	DTR	8	RI
9	GND	10	GND

Table 3-19: RS-232 Serial Port Connector Pinouts

NANO-ULT3 SBC

3.2.19 RS-232/422/485 Serial Port Connector

- CN Label:** COM3
- CN Type:** 10-pin header, p=2.00 mm
- CN Location:** See **Figure 3-20**
- CN Pinouts:** See **Table 3-20**

This connector provides RS-232, RS-422 or RS-485 communications. The default mode is set to RS-232 in BIOS. To configure the connector as RS-422 or RS-485, please refer to **Section 5.3.3.1.3**.

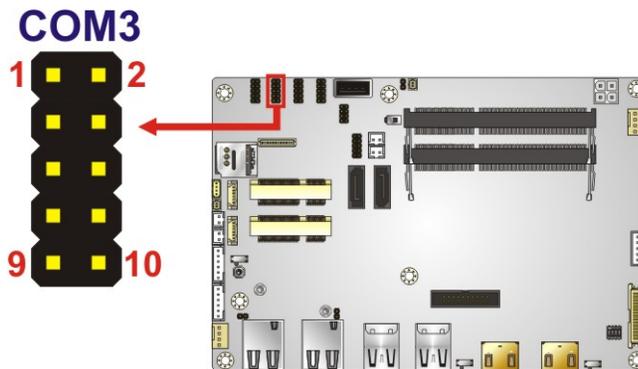


Figure 3-20: RS-232/422/485 Connector Location

Pin	RS-232	RS-422	RS-485
1	DCD	TX-	D-
2	DSR		
3	SIN	TX+	D+
4	RTS		
5	SOUT	RX+	
6	CTS		
7	DTR	RX-	
8	RI		
9	GND		
10	GND		

Table 3-20: RS-232/422/485 Connector Pinouts

Use the optional RS-422/485 cable to connect to a serial device. The pinouts of the DB-9 connector are listed below.

RS-422 Pinouts	RS-485 Pinouts

Table 3-21: DB-9 RS-422/485 Pinouts

3.2.20 SATA 6Gb/s Drive Connectors

- CN Label:** SATA1, SATA2
- CN Type:** 7-pin SATA connector
- CN Location:** See **Figure 3-21**

The SATA 6Gb/s drive connector is connected to a SATA 6Gb/s drive. The SATA 6Gb/s drive transfers data at speeds as high as 6Gb/s.

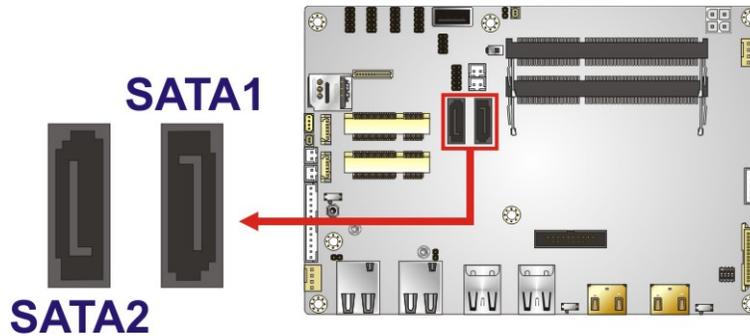


Figure 3-21: SATA 6Gb/s Drive Connectors Locations

NANO-ULT3 SBC

3.2.21 SATA Power Connectors

CN Label: SATA_PWR1, SATA_PWR2

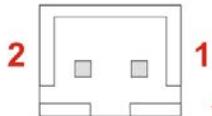
CN Type: 2-pin wafer, p=2.00 mm

CN Location: See Figure 3-22

CN Pinouts: See Table 3-22

The SATA power connector provides +5 V power output to the SATA connector.

SATA_PWR1



SATA_PWR2

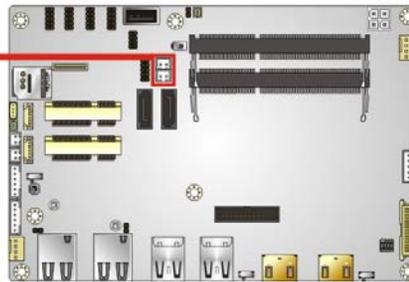
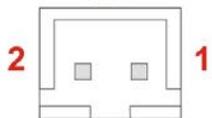


Figure 3-22: SATA Power Connector Locations

Pin	Description
1	+5V
2	GND

Table 3-22: SATA Power Connector Pinouts

3.2.22 SMBus Connector

- CN Label:** CN5
- CN Type:** 4-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-23**
- CN Pinouts:** See **Table 3-23**

The SMBus (System Management Bus) connector provides low-speed system management communications.

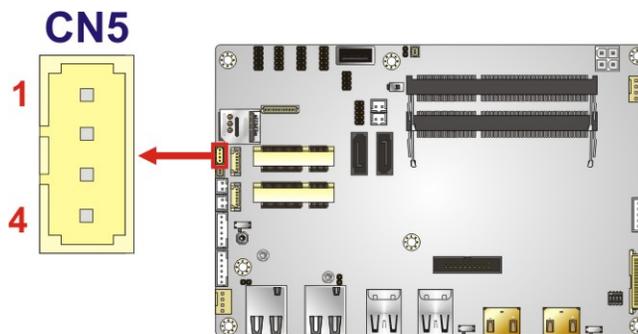


Figure 3-23: SMBus Connector Location

Pin	Description
1	GND
2	SMB_DATA
3	SMB_CLK
4	+5V

Table 3-23: SMBus Connector Pinouts

NANO-ULT3 SBC

3.2.23 SIM Card Slot

CN Label:	SIM1
CN Type:	SIM card slot
CN Location:	See Figure 3-24

The SIM card slot accepts a SIM card for 3G network communication.



NOTE:

A WWAN module must be installed in the full-size PCIe Mini slot (CN8) to provide WWAN communication.

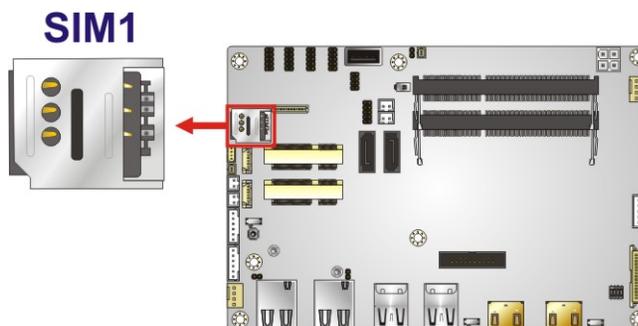


Figure 3-24: SIM Card Slot Location

3.2.24 SPI Flash Connector, BIOS

- CN Label:** JSPI1
- CN Type:** 6-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-25**
- CN Pinouts:** See **Table 3-24**

The 6-pin SPI Flash connector is used to flash the BIOS.

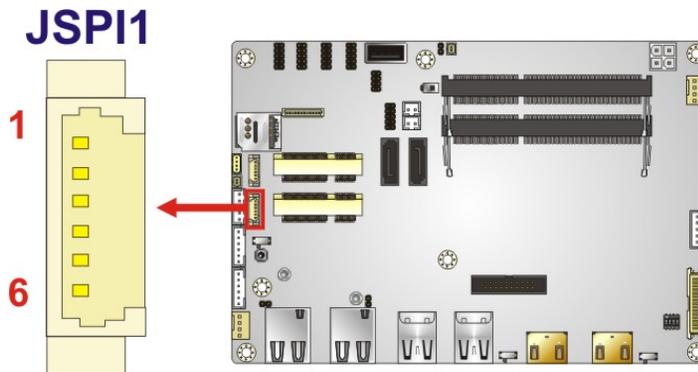


Figure 3-25: SPI Flash Connector Location

Pin	Description
1	+3.3VA
2	SPI_CS
3	SPI_SO_SW
4	SPI_CLK_SW
5	SPI_SI_SW
6	GND

Table 3-24: SPI Flash Connector Pinouts

NANO-ULT3 SBC

3.2.25 SPI Flash Connector, EC

- CN Label:** JSPI2
- CN Type:** 6-pin wafer, p=1.25 mm
- CN Location:** See **Figure 3-26**
- CN Pinouts:** See **Table 3-25**

The 6-pin SPI Flash connector is used to flash the embedded controller.

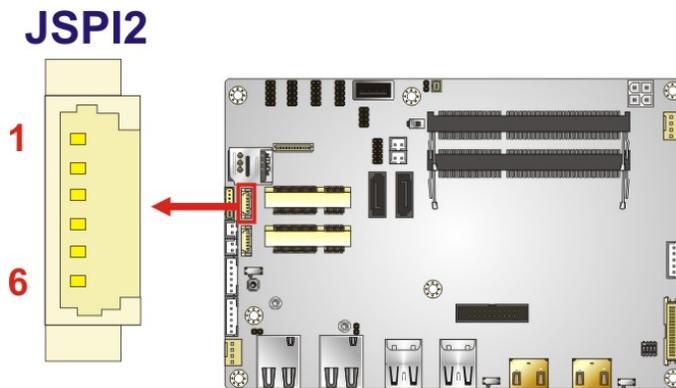


Figure 3-26: SPI Flash Connector Location

Pin	Description
1	+3.3VA
2	SPI_CS#0_CN_EC
3	SPI_SO_SW_EC
4	SPI_CLK_SW_EC
5	SPI_SI_SW_EC
6	GND

Table 3-25: SPI Flash Connector Pinouts

3.2.26 USB Connector

- CN Label:** USB1
- CN Type:** 8-pin header, p=2.00 mm
- CN Location:** See **Figure 3-27**
- CN Pinouts:** See **Table 3-26**

The USB connector provides two USB 2.0 ports by dual-port USB cable.

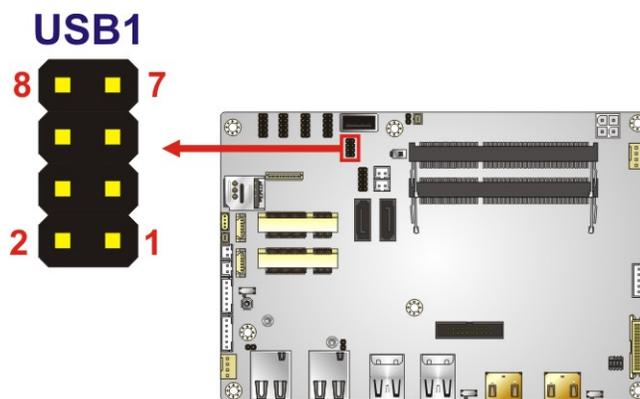


Figure 3-27: USB Connector Location

PIN NO.	DESCRIPTION	PIN NO.	DESCRIPTION
1	VCC	2	GND
3	DATA4-	4	DATA5+
5	DATA4+	6	DATA5-
7	GND	8	VCC

Table 3-26: USB Connector Pinouts

NANO-ULT3 SBC

3.2.27 USB Connector, Type A

- CN Label:** USB2
- CN Type:** USB Type A
- CN Location:** See **Figure 3-27**
- CN Pinouts:** See **Table 3-26**

The USB connector can be connected to USB 2.0 devices.

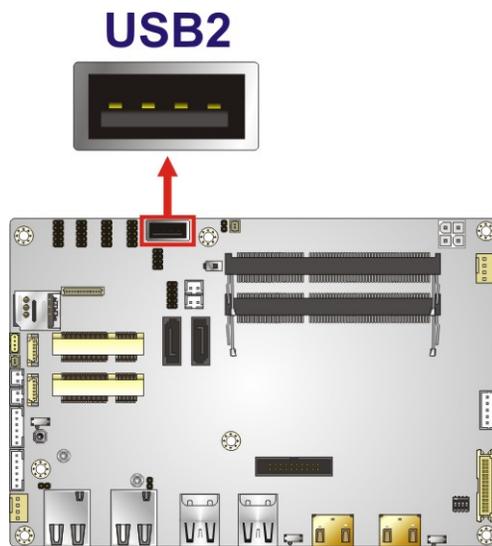


Figure 3-28: USB Connector Location (Type A)

Pin	Description
1	VCC
2	DATA6+
3	DATA6-
4	GND

Table 3-27: USB Connector Pinouts (Type A)

3.3 External Peripheral Interface Connector Panel

Figure 3-29 shows the NANO-ULT3 external peripheral interface connector (EPIC) panel. The EPIC panel consists of the following:

- 2 x GbE connector
- 2 x HDMI connector
- 4 x USB 3.2 Gen 1 (5Gb/s) connector

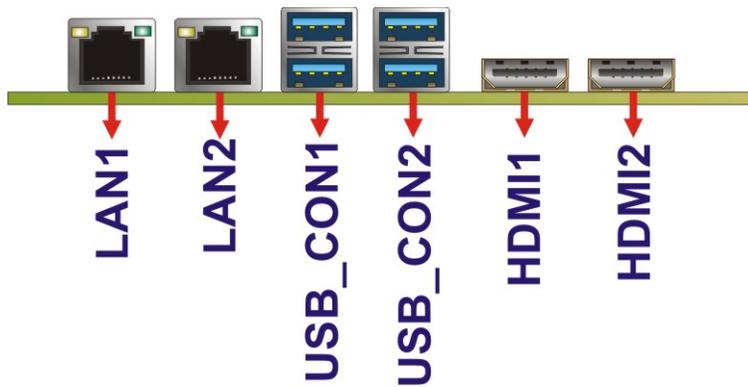


Figure 3-29: External Peripheral Interface Connector

3.3.1 HDMI Connectors

- CN Label:** HDMI1, HDMI2
- CN Type:** HDMI connector
- CN Location:** See Figure 3-29
- CN Pinouts:** See Table 3-28

The HDMI connectors can connect to HDMI devices.

Pin	Description	Pin	Description
1	HDMI_DATA2	2	GND
3	HDMI_DATA2#	4	HDMI_DATA1
5	GND	6	HDMI_DATA1#
7	HDMI_DATA0	8	GND
9	HDMI_DATA0#	10	HDMI_CLK
11	GND	12	HDMI_CLK#

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Pin	Description	Pin	Description
13	N/C	14	N/C
15	HDMI_SCL	16	HDMI_SDA
17	GND	18	+5V
19	HDMI_HPD	20	HDMI_GND
21	HDMI_GND	22	HDMI_GND
23	HDMI_GND		

Table 3-28: HDMI Connector Pinouts

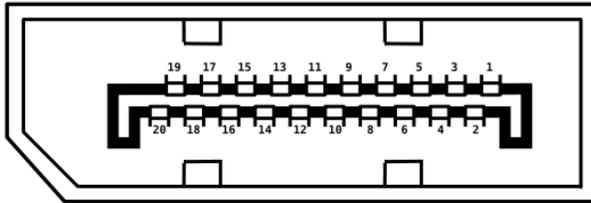


Figure 3-30: HDMI Connector Pinout Locations



NOTE:

The HDMI1 connector is co-lay with the iDP connector. When the iDP connector is enabled, the HDMI1 connector will be disabled. This is controlled by the HDMI/DP select switch. Please refer to **Section 4.6.4** for detailed information.

3.3.2 LAN Connectors

- CN Label:** LAN1, LAN2
- CN Type:** RJ-45
- CN Location:** See **Figure 3-29**
- CN Pinouts:** See **Figure 3-31** and **Table 3-29**

The LAN connector connects to a local network.

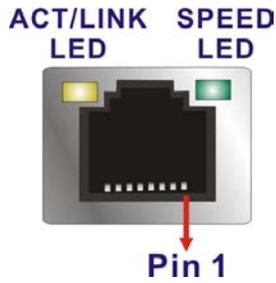


Figure 3-31: LAN Connector

Pin	Description	Pin	Description
1	TRD0+	5	TRD2+
2	TRD0-	6	TRD2-
3	TRD1+	7	TRD3+
4	TRD1-	8	TRD3-

Table 3-29: LAN Pinouts

3.3.3 USB Connectors

CN Label: USB_CON1, USB_CON2

CN Type: USB Type-A port

CN Location: See **Figure 3-29**

CN Pinouts: See **Table 3-30**

The NANO-ULT3 has four external USB 3.2 Gen 1 (5Gb/s) ports. The USB connector can be connected to a USB 2.0 or USB 3.2 Gen 1 device. The pinouts of USB 3.2 Gen 1 connectors are shown below.

Pin	Description	Pin	Description
1	+5V	2	USB2P0-
3	USB2P0+	4	GND
5	USB3P0_RXDN1	6	USB3P0_RXDP1
7	GND	8	USB3P0_TXDN1
9	USB3P0_TXDP1		

Table 3-30: USB 3.2 Gen 1 Port Pinouts

Chapter

4

Installation

4.1 Anti-static Precautions



WARNING:

Failure to take ESD precautions during the installation of the NANO-ULT3 may result in permanent damage to the NANO-ULT3 and severe injury to the user.

Electrostatic discharge (ESD) can cause serious damage to electronic components, including the NANO-ULT3. Dry climates are especially susceptible to ESD. It is therefore critical that whenever the NANO-ULT3 or any other electrical component is handled, the following anti-static precautions are strictly adhered to.

- **Wear an anti-static wristband:** Wearing a simple anti-static wristband can help to prevent ESD from damaging the board.
- **Self-grounding** Before handling the board, touch any grounded conducting material. During the time the board is handled, frequently touch any conducting materials that are connected to the ground.
- **Use an anti-static pad:** When configuring the NANO-ULT3, place it on an anti-static pad. This reduces the possibility of ESD damaging the NANO-ULT3.
- **Only handle the edges of the PCB:** When handling the PCB, hold the PCB by the edges.

4.2 Installation Considerations



NOTE:

The following installation notices and installation considerations should be read and understood before installation. All installation notices must be strictly adhered to. Failing to adhere to these precautions may lead to severe damage and injury to the person performing the installation.

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WARNING:

The installation instructions described in this manual should be carefully followed in order to prevent damage to the NANO-ULT3, NANO-ULT3 components and injury to the user.

Before and during the installation please **DO** the following:

- Read the user manual:
 - The user manual provides a complete description of the NANO-ULT3 installation instructions and configuration options.
- Wear an electrostatic discharge cuff (ESD):
 - Electronic components are easily damaged by ESD. Wearing an ESD cuff removes ESD from the body and helps prevent ESD damage.
- Place the NANO-ULT3 on an antistatic pad:
 - When installing or configuring the motherboard, place it on an antistatic pad. This helps to prevent potential ESD damage.
- Turn all power to the NANO-ULT3 off:
 - When working with the NANO-ULT3, make sure that it is disconnected from all power supplies and that no electricity is being fed into the system.

Before and during the installation of the NANO-ULT3 **DO NOT:**

- Remove any of the stickers on the PCB board. These stickers are required for warranty validation.
- Use the product before verifying all the cables and power connectors are properly connected.
- Allow screws to come in contact with the PCB circuit, connector pins, or its components.

4.3 SO-DIMM Installation

To install an SO-DIMM, please follow the steps below and refer to **Figure 4-1**.



CAUTION:

For dual channel configuration, always install two identical memory modules that feature the same capacity, timings, voltage, number of ranks and the same brand.

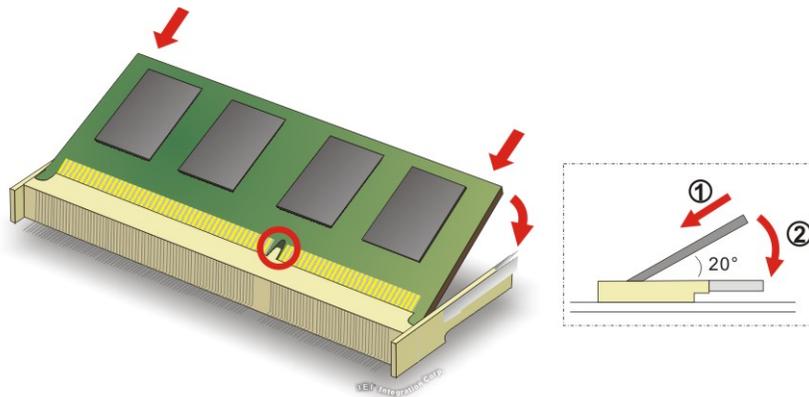


Figure 4-1: SO-DIMM Installation

- Step 1:** Locate the SO-DIMM socket. Place the board on an anti-static mat.
- Step 2:** Align the SO-DIMM with the socket. Align the notch on the memory with the notch on the memory socket.
- Step 3:** Insert the SO-DIMM. Push the memory in at a 20° angle. (See **Figure 4-1**)
- Step 4:** Seat the SO-DIMM. Gently push downwards and the arms clip into place. (See **Figure 4-1**)

**CAUTION:**

For dual channel configuration, always install two identical memory modules that feature the same capacity, timings, voltage, number of ranks and the same brand.

4.4 PCIe Mini Card Installation

4.4.1 Full-size PCIe Mini Card Installation

To install a full-size PCIe Mini card, please follow the steps below.

Step 1: Locate the full-size PCIe Mini card slot. See **Chapter 3**.

Step 2: Remove the retention screw. Remove the retention screw as shown in **Figure 4-2**.

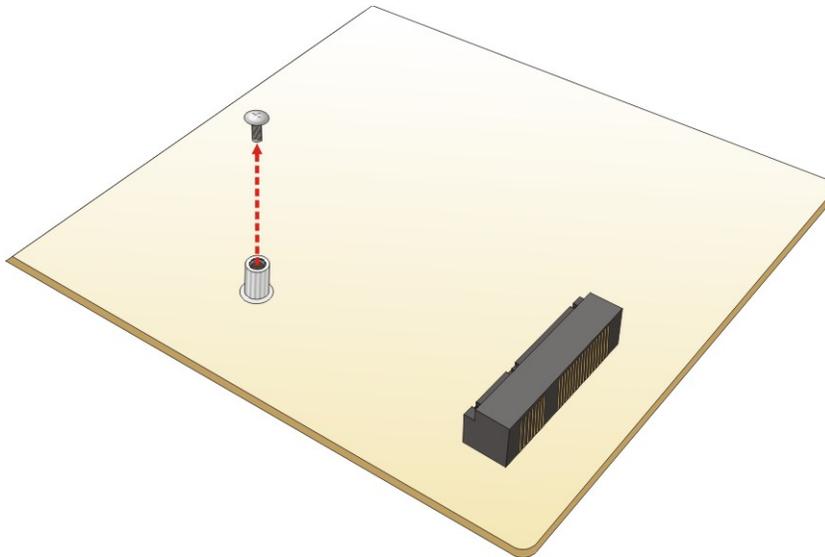


Figure 4-2: Removing the Retention Screw

Step 3: Insert into the socket at an angle. Line up the notch on the card with the notch on the slot. Slide the PCIe Mini card into the socket at an angle of about 20° (Figure 4-3).

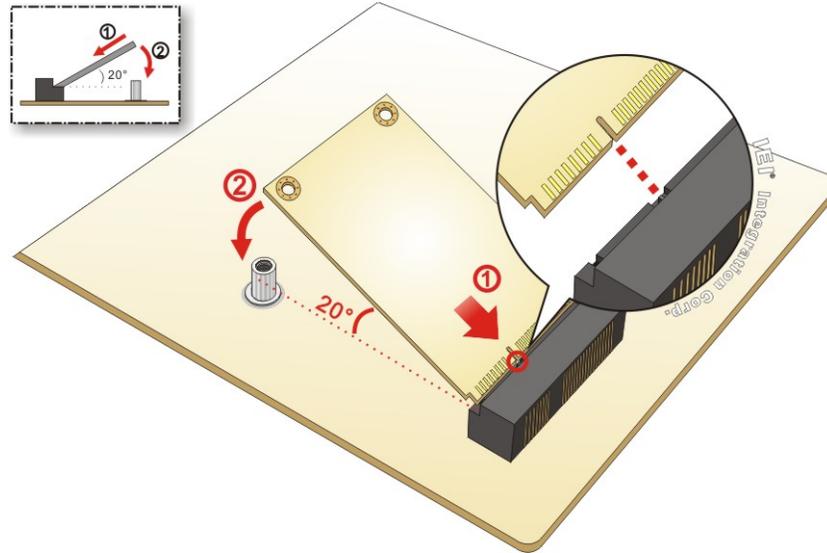


Figure 4-3: Inserting the Full-size PCIe Mini Card into the Slot at an Angle

Step 4: Secure the full-size PCIe Mini card. Secure the full-size PCIe Mini card with the retention screw previously removed (Figure 4-4).

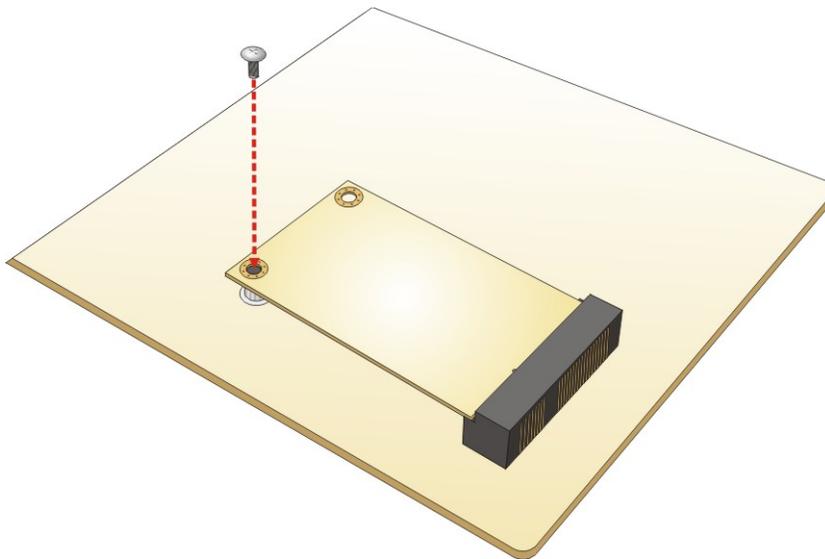


Figure 4-4: Securing the Full-size PCIe Mini Card

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4.4.2 Half-size PCIe Mini Card Installation

To install a half-size PCIe Mini card, please follow the steps below.

Step 1: Locate the half-size PCIe Mini card slot. See Chapter 3.

Step 2: Remove the retention screw. See Figure 4-5.

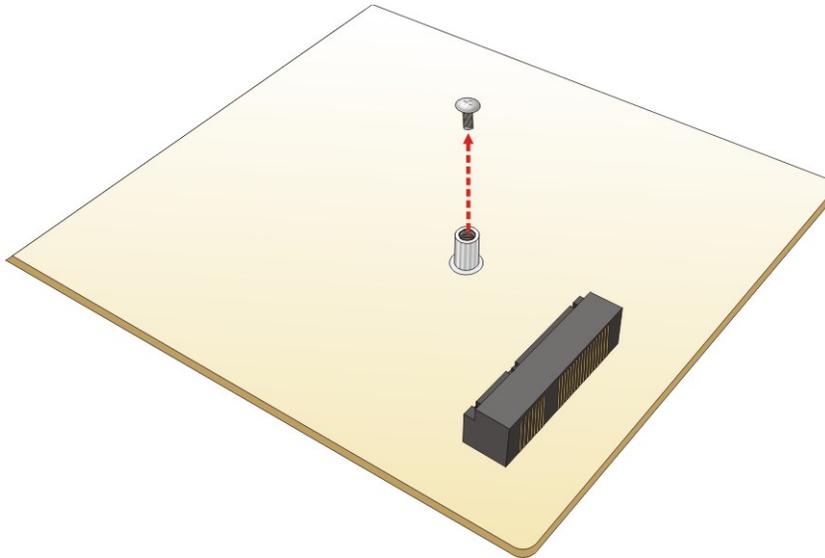


Figure 4-5: Removing Retention Screw

Step 3: Insert into the socket at an angle. Line up the notch on the card with the notch on the slot. Slide the PCIe Mini card into the slot at an angle of about 20° (Figure 4-6).

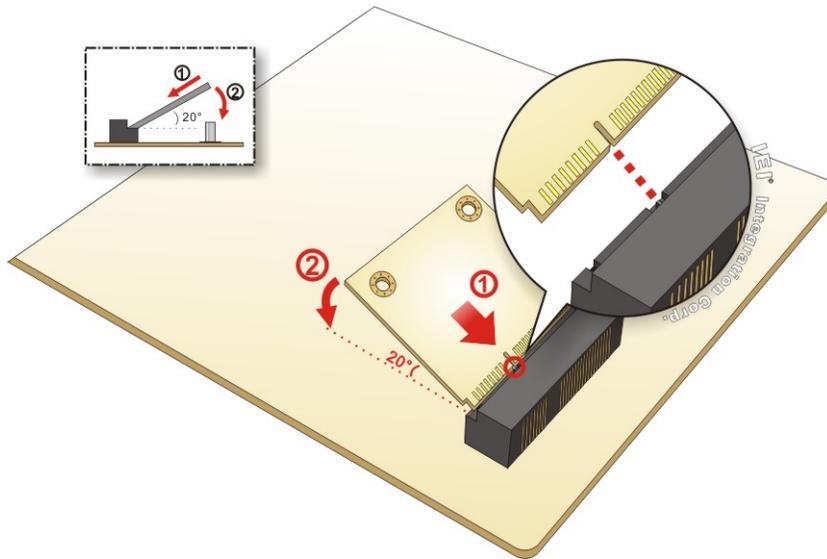


Figure 4-6: Inserting the Half-size PCIe Mini Card into the Slot at an Angle

Step 4: **Secure the half-size PCIe Mini card.** Secure the half-size PCIe Mini card with the retention screw previously removed (**Figure 4-7**).

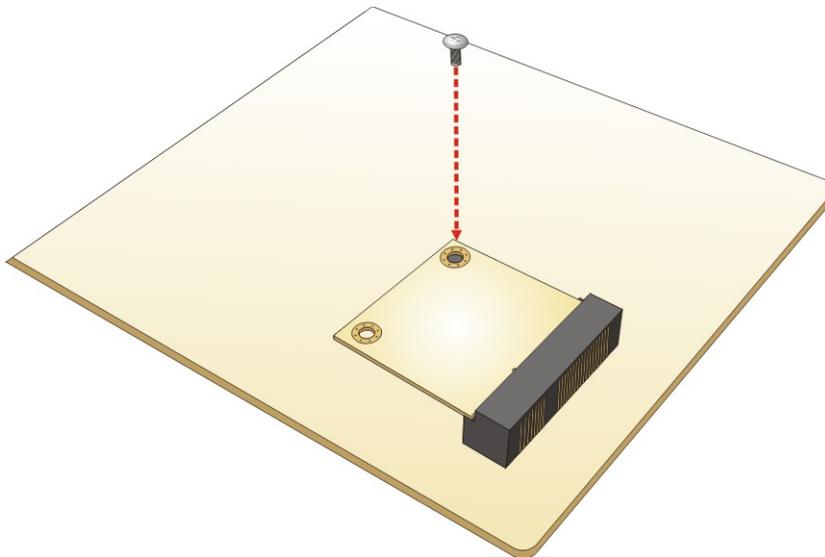


Figure 4-7: Securing the Half-size PCIe Mini Card

4.5 SIM Card Installation

To install a SIM card, please follow the steps below.

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**NOTE:**

A WWAN module must be installed in the full-size PCIe Mini slot (CN8) to provide WWAN communication.

Step 1: Locate the SIM card slot. See **Section 3.2.23**.

Step 2: Unlock the SIM card slot cover by sliding the cover in the direction as shown by the arrow in **Figure 4-8**.



Figure 4-8: Unlock SIM Card Slot Cover

Step 3: Open the slot cover and place a SIM card onto the slot. The cut mark on the corner should be facing away from the slot as shown in **Figure 4-9**.

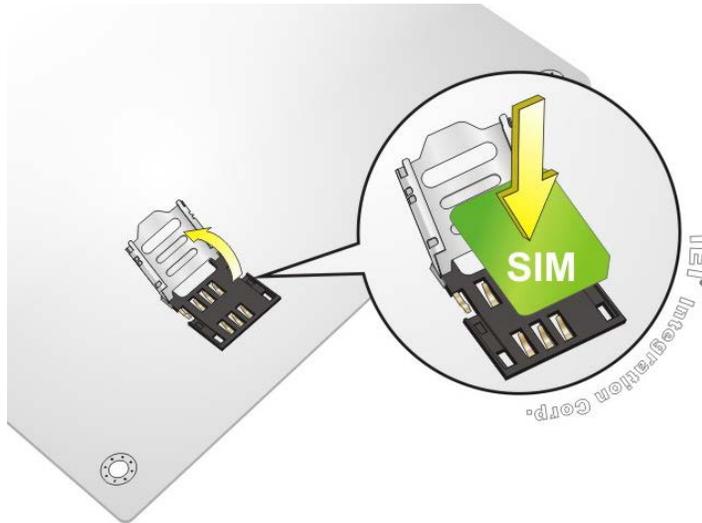


Figure 4-9: SIM Card Installation

Step 4: Close the slot cover and lock it by sliding it in the direction as shown by the arrow in **Figure 4-10**.

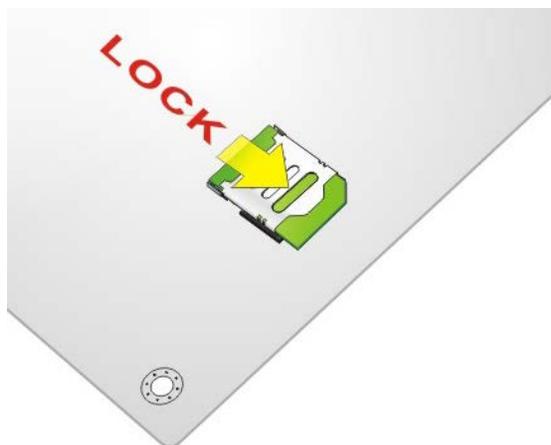


Figure 4-10: Lock SIM Card Slot Cover

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4.6 System Configuration

The system configuration is controlled by buttons, jumpers and switches. The system configuration should be performed before installation.

4.6.1 AT/ATX Mode Select Switch

CN Label:	J_ATX_AT1
CN Type:	Switch
CN Location:	See Figure 4-11
CN Settings:	See Table 4-1

The AT/ATX mode select switch specifies the systems power mode as AT or ATX. AT/ATX mode select switch settings are shown in **Table 4-1**.

Setting	Description
Short A-B	ATX Mode (Default)
Short B-C	AT Mode

Table 4-1: AT/ATX Mode Select Switch Settings

The location of the AT/ATX mode select switch is shown in **Figure 4-11** below.

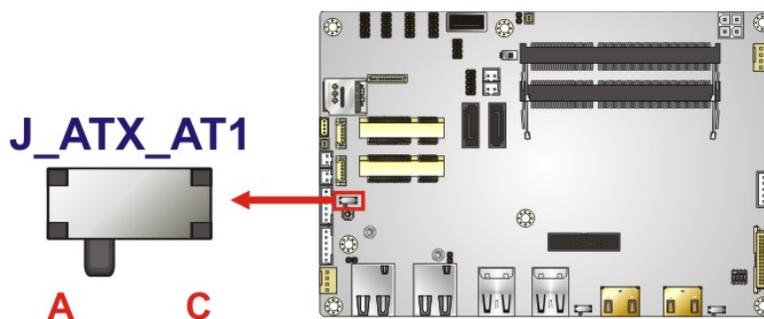


Figure 4-11: AT/ATX Mode Select Switch Location

4.6.2 Clear CMOS Button

CN Label:	J_CMOS1
CN Type:	Button
CN Location:	See Figure 4-12

If the NANO-ULT3 fails to boot due to improper BIOS settings, use the button to clear the CMOS data and reset the system BIOS information.

The location of the clear CMOS button is shown in **Figure 4-12**

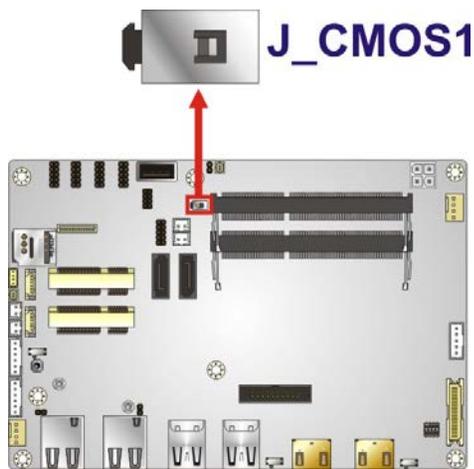


Figure 4-12: Clear CMOS Button Location

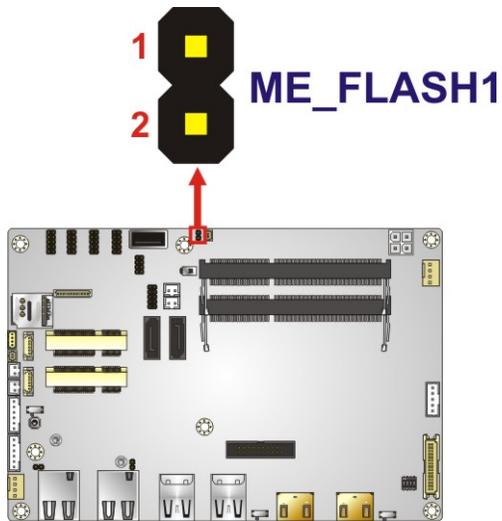
4.6.3 Flash Descriptor Security Override Jumper

CN Label:	ME_FLASH1
CN Type:	2-pin header, p=2.00 mm
CN Location:	See Figure 4-13
CN Settings:	See Table 4-2

The Flash Descriptor Security Override jumper (ME_FLASH1) allows to enable or disable the ME firmware update. Refer to **Figure 4-13** and **Table 4-2** for the jumper location and settings.

NANO-ULT3 SBC

Setting	Description
Open	Disabled (default)
Short	Enabled

Table 4-2: Flash Descriptor Security Override Jumper Settings**Figure 4-13: Flash Descriptor Security Override Jumper Location**

To update the ME firmware, please follow the steps below.

- Step 1:** Before turning on the system power, short the Flash Descriptor Security Override jumper.
- Step 2:** Update the BIOS and ME firmware, and then turn off the system power.
- Step 3:** Remove the metal clip on the Flash Descriptor Security Override jumper to its default setting.
- Step 4:** Restart the system. The system will reboot 2 ~ 3 times to complete the ME firmware update.

4.6.4 HDMI/DP Select Switch

- CN Label:** J_HDMI_DP1
- CN Type:** Switch
- CN Location:** See **Figure 4-14**
- CN Settings:** See **Table 4-3**

Use the HDMI/DP select switch to disable or enable the HDMI1 connector since the iDP connector (DP1) is co-lay with the HDMI1 connector. HDMI/DP select switch settings are shown in **Table 4-3**.

Setting	Description
Short A-B	Enable HDMI1 and disable DisplayPort (DP1) (Default)
Short B-C	Disable HDMI1 and enable DisplayPort (DP1)

Table 4-3: HDMI/DP Select Switch Settings

The location of the HDMI/DP select switch is shown in **Figure 4-11** below.

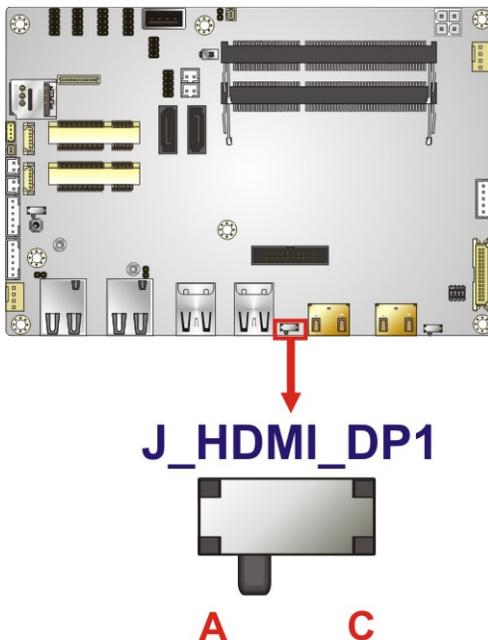


Figure 4-14: HDMI/DP Select Switch Location

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4.6.5 LVDS Panel Resolution Select Switch

Jumper Label:	SW1
Jumper Type:	DIP switch
Jumper Settings:	See Table 4-4
Jumper Location:	See Figure 4-15

Selects the resolution of the LCD panel connected to the LVDS connector.

* ON=0, OFF=1; Single=S, Dual=D

SW1 (4-3-2-1)	Description
0000	800x600 18-bit S (default)
0001	1024x768 18-bit S
0010	1024x768 24-bit S
0011	1280x768 18-bit S
0100	1280x800 18-bit S
0101	1280x960 18-bit S
0110	1280x1024 24-bit D
0111	1366x768 18-bit S
1000	1366x768 24-bit S
1001	1440x960 24-bit D
1010	1400x1050 24-bit D
1011	1600x900 24-bit D
1100	1680x1050 24-bit D
1101	1600x1200 24-bit D
1110	1920x1080 24-bit D
1111	1920x1200 24-bit D

Table 4-4: LVDS Panel Resolution Selection

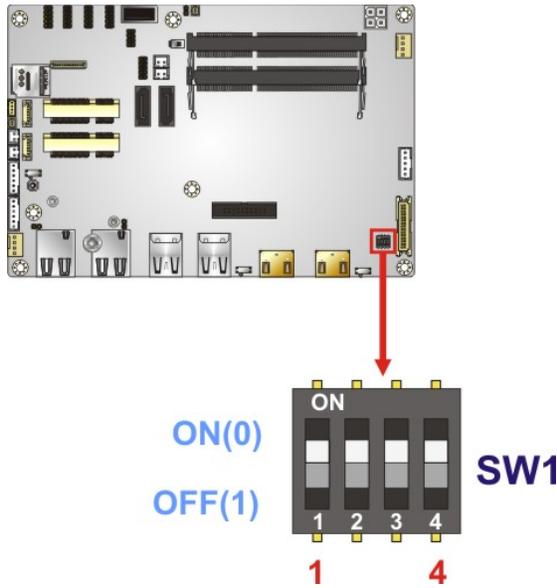


Figure 4-15: LVDS Panel Resolution Select Switch Location

4.6.6 LVDS Voltage Select Jumper



WARNING:

Permanent damage to the screen and NANO-ULT3 may occur if the wrong voltage is selected with this jumper. Please refer to the user guide that came with the monitor to select the correct voltage.

Jumper Label:	J_LCD_PWR1
Jumper Type:	Switch
Jumper Settings:	See Table 4-5
Jumper Location:	See Figure 4-16

The LVDS voltage select switch allows setting the voltage provided to the monitor connected to the LVDS connector. The LVDS voltage select switch settings are shown in **Table 4-1**.

NANO-ULT3 SBC

Setting	Description
Short A-B	+3.3 V (Default)
Short B-C	+5

Table 4-5: LVDS Voltage Select Jumper Settings

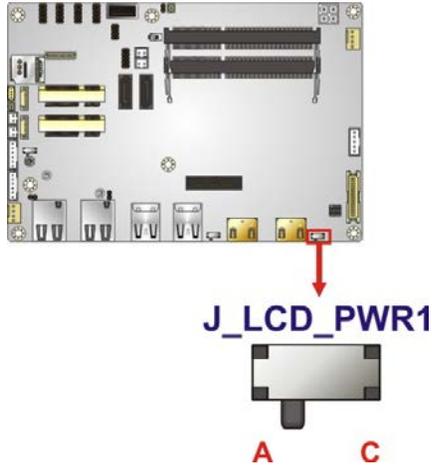


Figure 4-16: LVDS Voltage Select Jumper Location

4.7 Chassis Installation

4.7.1 Heat Sink



WARNING:

Never run the NANO-ULT3 without the heat sink secured to the board. The heat sink ensures the system remains cool and does not need addition heat sinks to cool the system.

**WARNING:**

When running the NANO-ULT3, do not put the NANO-ULT3 directly on a surface that can not dissipate system heat, especially the wooden or plastic surface. It is highly recommended to run the NANO-ULT3

→ on a heat dissipation surface or

→ using copper pillars to hold the board up from the chassis

When the NANO-ULT3 is shipped, a heat sink is secured to the board with six retention screws. If the NANO-ULT3 must be removed from the heat sink, the six retention screws must be removed.

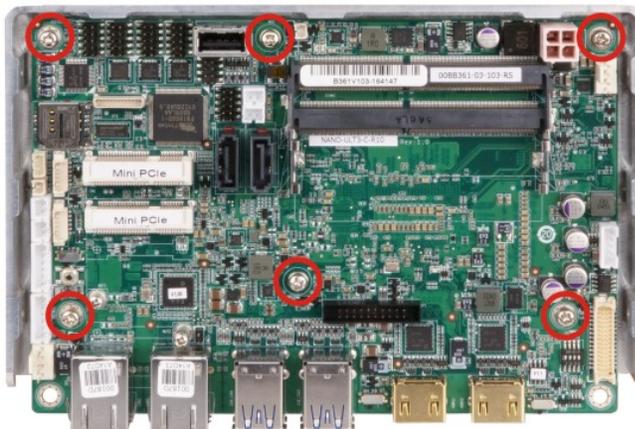


Figure 4-17: Heat Sink Retention Screws

4.7.2 Motherboard Installation

Each side of the heat sink enclosure has several screw holes allowing the NANO-ULT3 to be mounted into a chassis (please refer to **Figure 1-3** for the detailed dimensions). The user can design or select a chassis that has screw holes matching up with the holes on the heat sink enclosure for installing the NANO-ULT3. The following diagram shows an example of motherboard installation.

NANO-ULT3 SBC

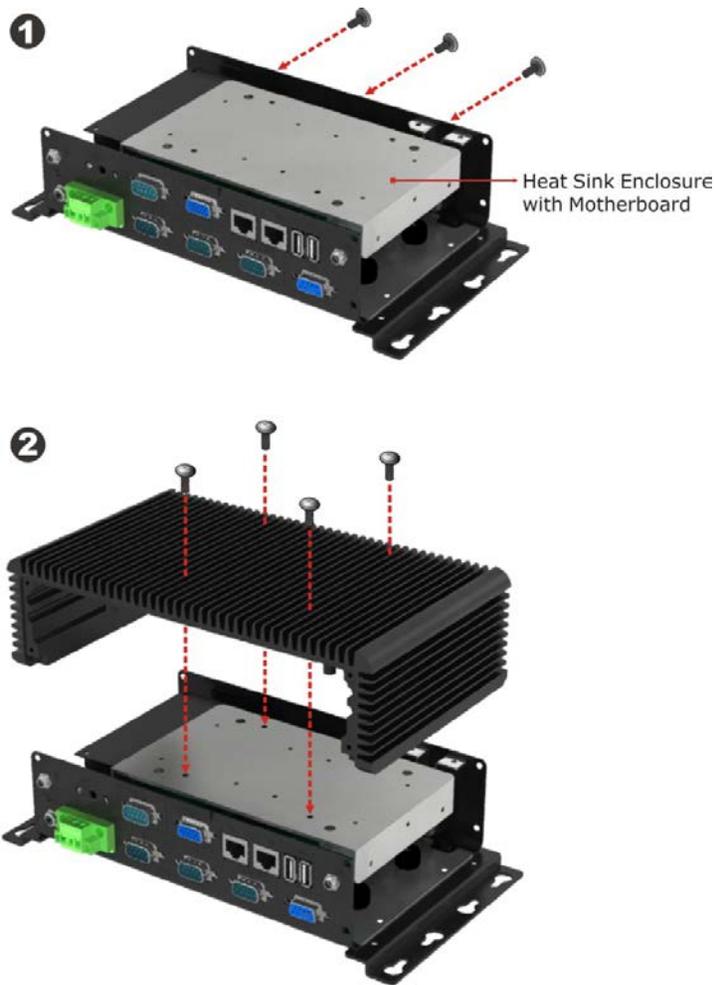


Figure 4-18: Motherboard Installation Example

4.8 Internal Peripheral Device Connections

This section outlines the installation of peripheral devices to the on-board connectors

4.8.1 AT Power Connection

Follow the instructions below to connect the NANO-ULT3 to an AT power supply.



WARNING:

Disconnect the power supply power cord from its AC power source to prevent a sudden power surge to the NANO-ULT3.

Step 1: **Locate the power cable.** The power cable is shown in the packing list in Chapter 2.

Step 2: **Connect the power cable to the motherboard.** Connect the 4-pin (2x2) Molex type power cable connector to the power connector on the motherboard. See Figure 4-19.

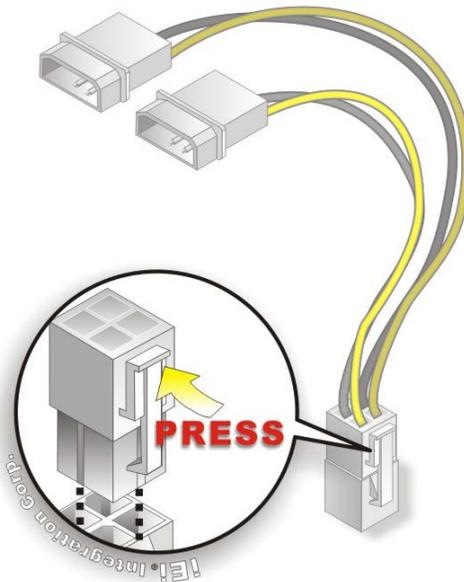


Figure 4-19: Power Cable to Motherboard Connection

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Step 3: Connect power cable to power supply. Connect one of the 4-pin (1x4) Molex type power cable connectors to an AT power supply. See Figure 4-20.

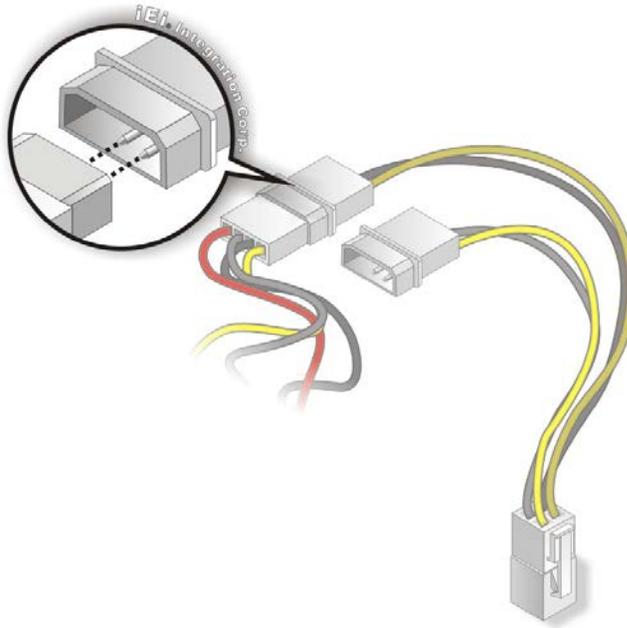


Figure 4-20: Connect Power Cable to Power Supply

4.8.2 Audio Kit Installation

The Audio Kit that came with the NANO-ULT3 connects to the audio connector on the NANO-ULT3. The audio kit consists of three audio jacks. Mic-in connects to a microphone. Line-in provides a stereo line-level input to connect to the output of an audio device. Line-out, a stereo line-level output, connects to two amplified speakers. To install the audio kit, please refer to the steps below:

Step 1: Locate the audio connector. The location of the 10-pin audio connector is shown in Chapter 3.

Step 2: Align pin 1. Align pin 1 on the on-board connector with pin 1 on the audio kit connector. Pin 1 on the audio kit connector is indicated with a white dot. See Figure 4-21.

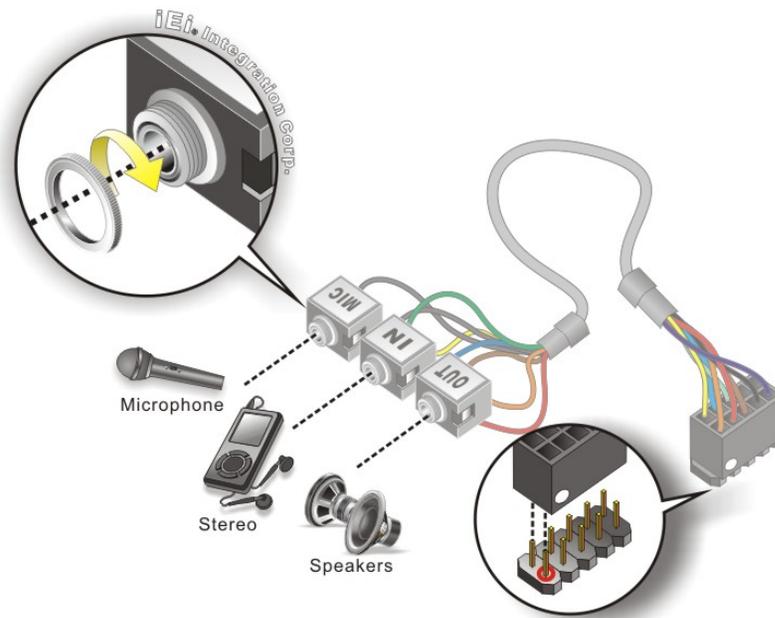


Figure 4-21: Audio Kit Cable Connection

Step 3: **Connect the audio devices.** Connect speakers to the line-out audio jack. Connect the output of an audio device to the line-in audio jack. Connect a microphone to the mic-in audio jack.

4.8.3 RS-232 Cable Connection

The single RS-232 cable consists of one serial port connector attached to a serial communications cable that is then attached to a D-sub 9 male connector. To install the single RS-232 cable, please follow the steps below.

Step 1: **Locate the connector.** The location of the RS-232 connector is shown in Chapter 3.

Step 2: **Insert the cable connector.** Align the cable connector with the onboard connector. Make sure pin 1 on the board and connector line up. Pin 1 on the cable connector is indicated with a white dot. See **Figure 4-22**.

NANO-ULT3 SBC

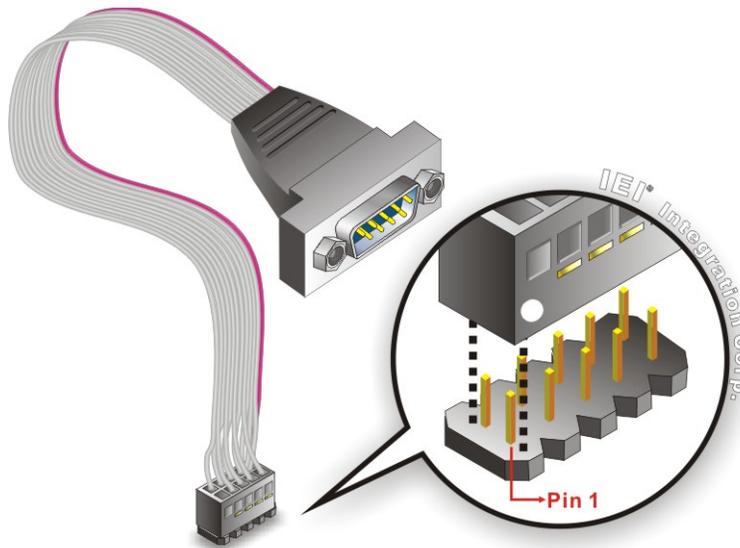


Figure 4-22: Single RS-232 Cable Installation

- Step 3: Secure the bracket.** The single RS-232 connector has two retention screws that must be secured to a chassis or bracket.
- Step 4: Connect the serial device.** Once the single RS-232 connector is connected to a chassis or bracket, a serial communications device can be connected to the system.

4.8.4 SATA Drive Connection

The NANO-ULT3 is shipped with a SATA drive cable. To connect the SATA drive to the connector, please follow the steps below.

- Step 1: Locate the SATA connector and the SATA power connector.** The locations of the connectors are shown in **Chapter 3**.
- Step 2: Insert the cable connector.** Insert the cable connector into the on-board SATA drive connector and the SATA power connector. See **Figure 4-23**.

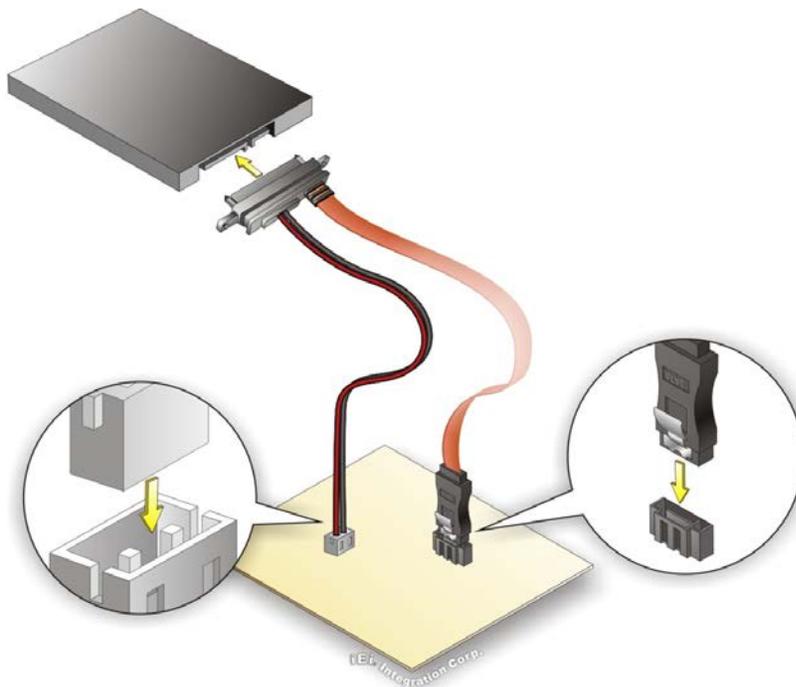


Figure 4-23: SATA Drive Cable Connection

- Step 3:** **Connect the cable to the SATA disk.** Connect the connector on the other end of the cable to the connector at the back of the SATA drive. See **Figure 4-23**.
- Step 4:** To remove the SATA cable from the SATA connector, press the clip on the connector at the end of the cable.

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4.9 Intel® AMT Setup Procedure

The NANO-ULT3 is featured with the Intel® Active Management Technology (AMT). To enable the Intel® AMT function, follow the steps below.

- Step 1:** Make sure at least one of the memory sockets is installed with a DDR4 SO-DIMM.
- Step 2:** Connect an Ethernet cable to the RJ-45 connector labeled **LAN1**.
- Step 3:** The AMI BIOS options regarding the Intel® ME or Intel® AMT must be enabled,
- Step 4:** Properly install the Intel® Management Engine Components drivers from the iAMT Driver & Utility directory obtained from IEI Resource Download Center. See **Chapter 6**.
- Step 5:** Configure the Intel® Management Engine BIOS extension (MEBx). To get into the Intel® MEBx settings, press <Ctrl+P> after a single beep during boot-up process. Enter the Intel® current ME password as it requires (the Intel® default password is **admin**).



NOTE:

To change the password, enter a new password following the strong password rule (containing at least one upper case letter, one lower case letter, one digit and one special character, and be at least eight characters).

Chapter

5

BIOS

NANO-ULT3 SBC

5.1 Introduction

The BIOS is programmed onto the BIOS chip. The BIOS setup program allows changes to certain system settings. This chapter outlines the options that can be changed.



NOTE:

Some of the BIOS options may vary throughout the life cycle of the product and are subject to change without prior notice.

5.1.1 Starting Setup

The UEFI BIOS is activated when the computer is turned on. The setup program can be activated in one of two ways.

1. Press the **DELETE** or **F2** key as soon as the system is turned on or
2. Press the **DELETE** or **F2** key when the “**Press Del to enter SETUP**” message appears on the screen.

If the message disappears before the **DELETE** or **F2** key is pressed, restart the computer and try again.

5.1.2 Using Setup

Use the arrow keys to highlight items, press **ENTER** to select, use the PageUp and PageDown keys to change entries, press **F1** for help and press **ESC** to quit. Navigation keys are shown in.

Key	Function
Up arrow	Move to previous item
Down arrow	Move to next item
Left arrow	Move to the item on the left hand side
Right arrow	Move to the item on the right hand side
+	Increase the numeric value or make changes

Key	Function
-	Decrease the numeric value or make changes
F1 key	General help, only for Status Page Setup Menu and Option Page Setup Menu
F2 key	Load previous values.
F3 key	Load optimized defaults
F4 key	Save changes and Exit BIOS
Esc key	Main Menu – Quit and not save changes into CMOS Status Page Setup Menu and Option Page Setup Menu -- Exit current page and return to Main Menu

5.1.3 Getting Help

When **F1** is pressed a small help window describing the appropriate keys to use and the possible selections for the highlighted item appears. To exit the Help Window press **Esc** or the **F1** key again.

5.1.4 Unable to Reboot after Configuration Changes

If the computer cannot boot after changes to the system configuration is made, CMOS defaults. Use the jumper described in **Section 4.6.2**.

5.1.5 BIOS Menu Bar

The **menu bar** on top of the BIOS screen has the following main items:

- Main – Changes the basic system configuration.
- Advanced – Changes the advanced system settings.
- Chipset – Changes the chipset settings.
- Security – Sets User and Supervisor Passwords.
- Boot – Changes the system boot configuration.
- Save & Exit – Selects exit options and loads default settings

The following sections completely describe the configuration options found in the menu items at the top of the BIOS screen and listed above.

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5.2 Main

The **Main** BIOS menu (**BIOS Menu 1**) appears when the **BIOS Setup** program is entered.

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.					
Main	Advanced	Chipset	Security	Boot	Save & Exit
BIOS Information					
BIOS Vendor		American Megatrends			Set the Date. Use Tab to switch between Data elements.
Core Version		5.11			
Compliancy		UEFI 2.4; PI 1.3			
Project Version		B361AR12.ROM			
Build Date and Time		04/15/2016 15:22:00			
iWDD Vendor			iEi		
iWDD Version		B361ER12.bin			
Access Level		Administrator			
Processor Information					
Name		SkyLake			
Brand String		Intel(R) Celeron(R) CPU 3955U @ 2.00GHz			-----
Frequency		1900 MHz			←→: Select Screen
Processor ID		406E3			↑ ↓: Select Item
Stepping		D0/K0			EnterSelect
Number of Processors		2Core(s) / 2Thread(s)			+/-: Change Opt.
Microcode Revision		7C			F1: General Help
GT Info		GT1			F2: Previous Values
IGFX VBIOS Version		1036			F3: Optimized Defaults
Memory RC Version		1.9.0.0			F4: Save & Exit
Total Memory		4096 MB			ESC: Exit
Memoery Frequency		2133 MHz			
PCH Information					
Name		SKL PCH-LP			
PCH SKU		PCH-LP Mobile (U) Premium SKU			
Stepping		21/C1			
LAN PHY Revision		B2			
ME FW Version		11.0.0.1202			
ME Firmware SKU		Corporate SKU			
SPI Clock Frequency					
D0FR Support		Unsupported			
Read Status Clock Frequency		17 MHz			
Write Status Clock Frequency		17 MHz			
Fast Read Status Clock Frequency		17 MHz			
System Date		[Fri 01/01/2010]			
System Time		[00:18:35]			
Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.					

BIOS Menu 1: Main

The System Overview field also has two user configurable fields:

➔ **System Date [xx/xx/xx]**

Use the **System Date** option to set the system date. Manually enter the day, month and year.

➔ **System Time [xx:xx:xx]**

Use the **System Time** option to set the system time. Manually enter the hours, minutes and seconds.

5.3 Advanced

Use the **Advanced** menu (**BIOS Menu 2**) to configure the CPU and peripheral devices through the following sub-menus:



WARNING!

Setting the wrong values in the sections below may cause the system to malfunction. Make sure that the settings made are compatible with the hardware.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Main  Advanced  Chipset  Security  Boot  Save & Exit
-----
> ACPI Settings
> AMT Configuration
> F81866 Super IO Configuration
> iWDD H/W Monitor
> RTC Wake Settings
> Serial Port Console Redirection
> CPU Configuration
> SATA Configuration
> USB Configuration
> iEi Feature

System ACPI Parameters.
-----
<->: Select Screen
↑ ↓: Select Item
Enter>Select
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save
ESC Exit

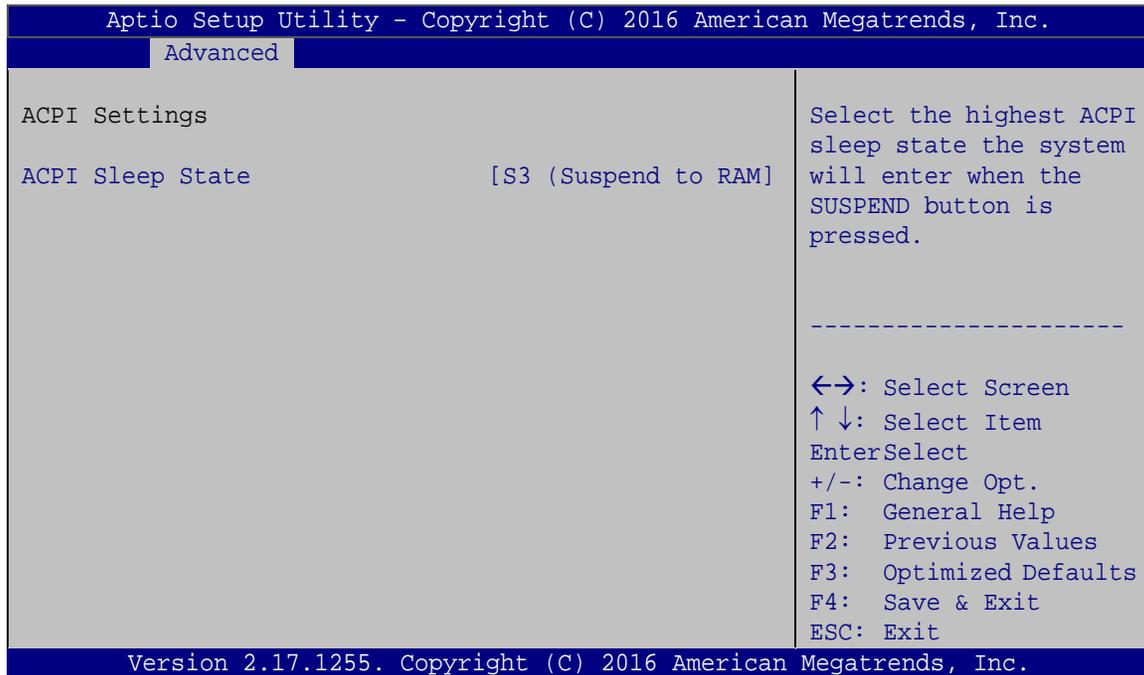
Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
    
```

BIOS Menu 2: Advanced

NANO-ULT3 SBC

5.3.1 ACPI Settings

The **ACPI Settings** menu (**BIOS Menu 3**) configures the Advanced Configuration and Power Interface (ACPI) options.



BIOS Menu 3: ACPI Settings

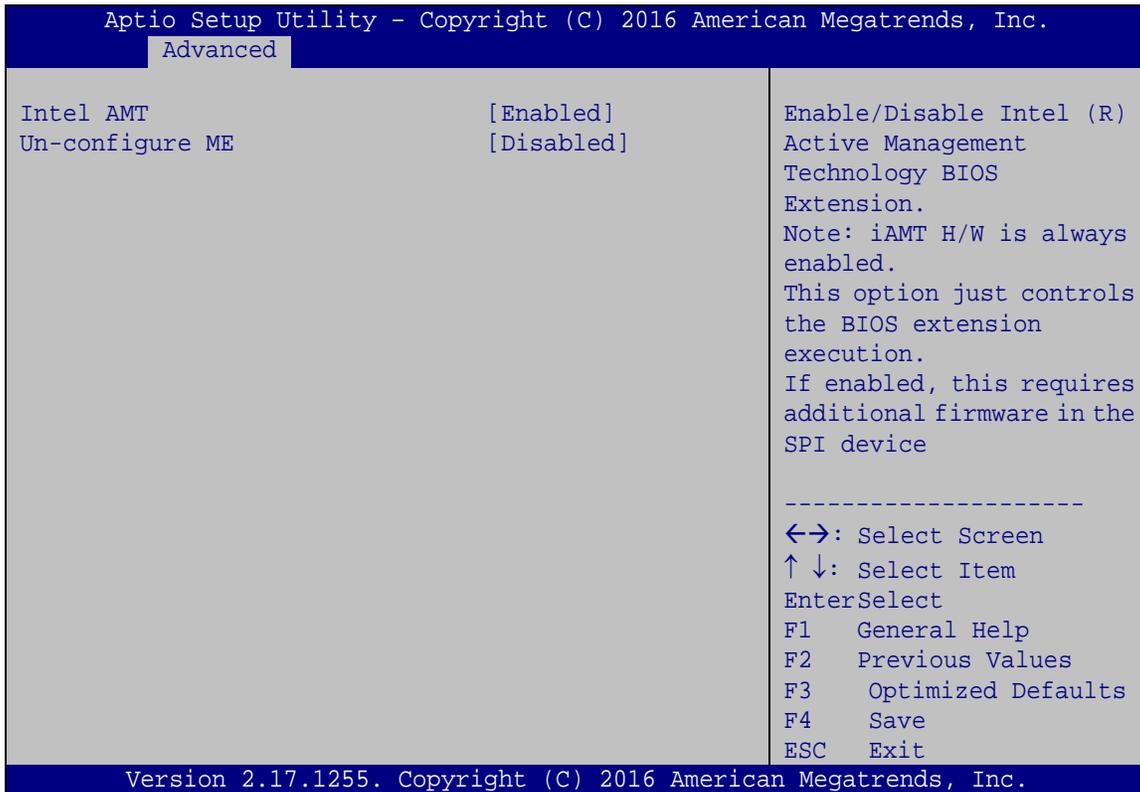
→ **ACPI Sleep State [S3 (Suspend to RAM)]**

Use the **ACPI Sleep State** option to specify the sleep state the system enters when it is not being used.

- **S3 (Suspend to RAM)** **DEFAULT** The caches are flushed and the CPU is powered off. Power to the RAM is maintained. The computer returns slower to a working state, but more power is saved.

5.3.2 AMT Configuration

The **AMT Configuration** menu (**BIOS Menu 4**) allows Intel® Active Management Technology (AMT) options to be configured.



BIOS Menu 4: AMT Configuration

→ Intel AMT [Enabled]

Use **Intel AMT** option to enable or disable the Intel® AMT function.

- **Disabled** Intel® AMT is disabled
- **Enabled** **DEFAULT** Intel® AMT is enabled

→ Un-configure ME [Disabled]

Use the **Un-configure ME** option to perform ME unconfigure without password operation.

- **Disabled** **DEFAULT** Not perform ME unconfigure

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➔ Enabled To perform ME unconfigure

5.3.3 F81866 Super IO Configuration

Use the **F81866 Super IO Configuration** menu (**BIOS Menu 5**) to set or change the configurations for the serial ports.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
  Advanced
F81866 Super IO Configuration
Super IO Chip                      F81866
> Serial Port 1 Configuration
> Serial Port 2 Configuration
> Serial Port 3 Configuration

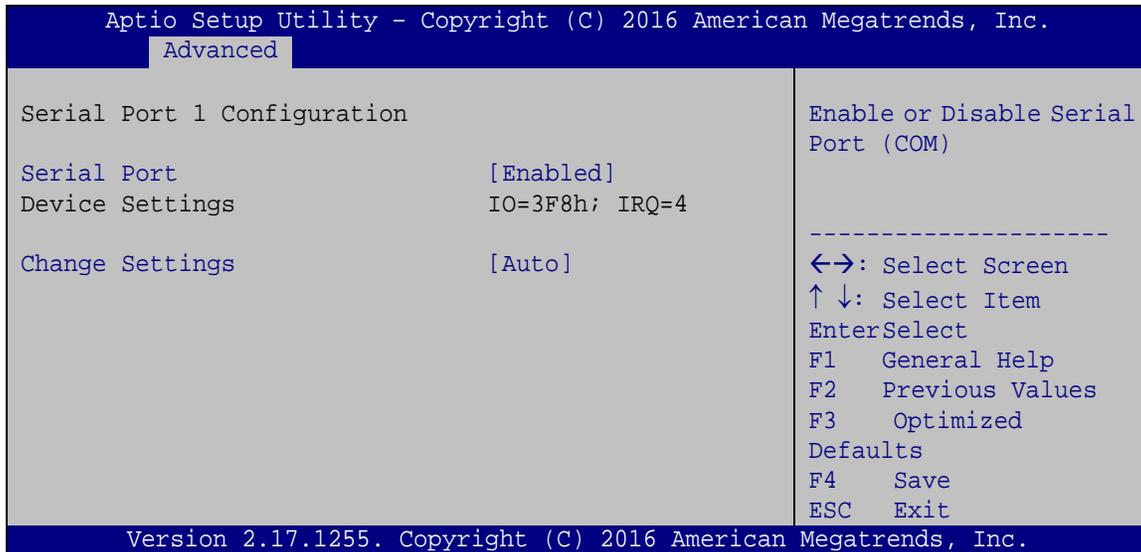
Set Parameters of Serial
Port 1 (COMA)
-----
<->: Select Screen
↑ ↓: Select Item
EnterSelect
F1  General Help
F2  Previous Values
F3  Optimized
Defaults
F4  Save
ESC Exit

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
  
```

BIOS Menu 5: F81866 Super IO Configuration

5.3.3.1 Serial Port n Configuration

Use the **Serial Port n Configuration** menu (**BIOS Menu 6**) to configure the serial port n.



BIOS Menu 6: Serial Port n Configuration

5.3.3.1.1 Serial Port 1 Configuration

→ Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- **Disabled** Disable the serial port
- **Enabled** **DEFAULT** Enable the serial port

→ Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- **Auto** **DEFAULT** The serial port IO port address and interrupt address are automatically detected.
- **IO=3F8h; IRQ=4** Serial Port I/O port address is 3F8h and the interrupt address is IRQ4

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- ➔ **IO=3F8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 3F8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=2F8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 2F8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=3E8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=2E8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12

5.3.3.1.2 Serial Port 2 Configuration

➔ Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** Disable the serial port
- ➔ **Enabled** **DEFAULT** Enable the serial port

➔ Change Settings [Auto]

Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- ➔ **Auto** **DEFAULT** The serial port IO port address and interrupt address are automatically detected.
- ➔ **IO=2F8h; IRQ=3** Serial Port I/O port address is 2F8h and the interrupt address is IRQ3
- ➔ **IO=3F8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 3F8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=2F8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 2F8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=3E8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12

- ➔ **IO=2E8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12

5.3.3.1.3 Serial Port 3 Configuration

➔ Serial Port [Enabled]

Use the **Serial Port** option to enable or disable the serial port.

- ➔ **Disabled** Disable the serial port
- ➔ **Enabled** **DEFAULT** Enable the serial port

➔ Change Settings [Auto]

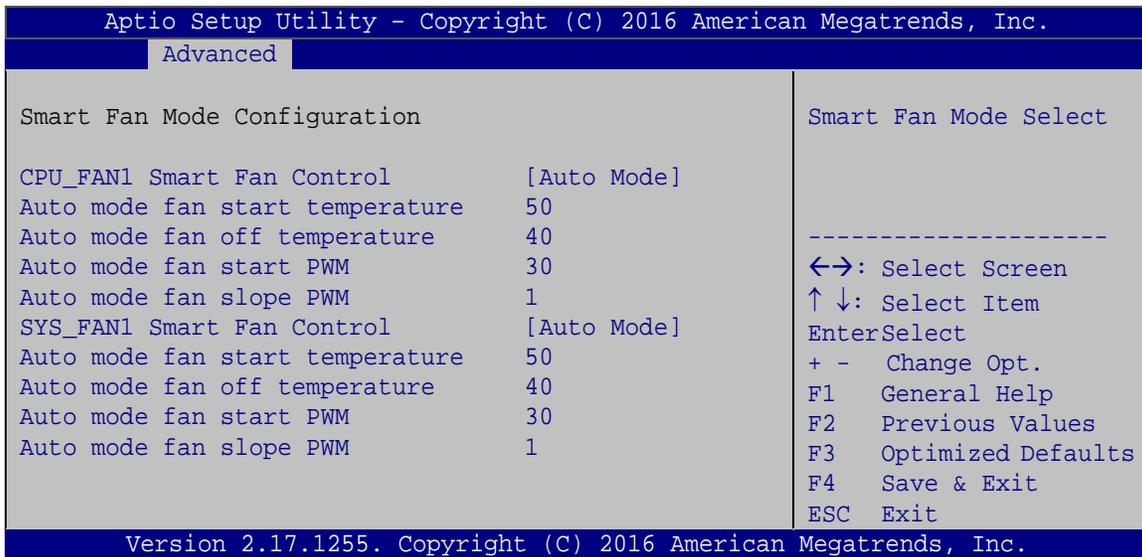
Use the **Change Settings** option to change the serial port IO port address and interrupt address.

- ➔ **Auto** **DEFAULT** The serial port IO port address and interrupt address are automatically detected.
- ➔ **IO=3E8h; IRQ=11** Serial Port I/O port address is 3E8h and the interrupt address is IRQ11
- ➔ **IO=3E8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 3E8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=2E8h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 2E8h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=2F0h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 2F0h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12
- ➔ **IO=2E0h; IRQ=3, 4,5,6,7,9,10,11,12** Serial Port I/O port address is 2E0h and the interrupt address is IRQ3,4,5,6,7,9,10,11,12

- System temperature
- Fan Speed:
 - CPU Fan Speed
 - System Fan Speed
- Voltages
 - CPU_CORE
 - +5V
 - +12V
 - +DDR
 - +5VSB
 - +3.3V
 - +3.3VSB

5.3.4.1 Smart Fan Mode Configuration

Use the **Smart Fan Mode Configuration** submenu (**BIOS Menu 8**) to configure fan temperature and speed settings.



BIOS Menu 8: Smart Fan Mode Configuration

→ CPU_FAN1 Smart Fan Control [Auto Mode]

Use the **CPU_FAN1 Smart Fan Control** BIOS option to configure the CPU Smart Fan.

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- **Manual Mode** **DEFAULT** The fan spins at the speed set in the Manual Mode option
- **Auto Mode** **DEFAULT** The fan adjusts its speed using these settings:
 - Auto mode fan start temperature
 - Auto mode fan off temperature
 - Auto mode fan start PWM
 - Auto mode fan slope PWM

→ **SYS_FAN1 Smart Fan Control [Auto Mode]**

Use the **SYS_FAN1 Smart Fan Control** BIOS option to configure the system smart fan.

- **Manual Mode** The fan spins at the speed set in the Manual Mode option
- **Auto Mode** **DEFAULT** The fan adjusts its speed using these settings:
 - Auto mode fan start temperature
 - Auto mode fan off temperature
 - Auto mode fan start PWM
 - Auto mode fan slope PWM

→ **Auto mode fan start temperature [50]**



WARNING:

Setting this value too high may cause the fan to rotate at full speed only when the CPU is at a very high temperature and therefore cause the system to be damaged.

The **Auto mode fan start temperature** option can only be set if the **SYS_FAN1 Smart Fan Control** option is set to **Auto Mode**. If the system temperature is between **Start Temperature** and **Off Temperature**, the fan speed change to be **Start PWM**. To set a

value, select the **Auto mode fan start temperature** option and enter a decimal number between 1 and 100.

→ **Auto mode fan off temperature [40]**



WARNING:

Setting this value too high may cause the fan to speed up only when the CPU is at a very high temperature and therefore cause the system to be damaged.

The **Auto mode fan off temperature** option can only be set if the **SYS_FAN1 Smart Fan control** option is set to **Auto Mode**. If the system temperature is lower than **Auto mode fan off temperature**, the fan speed change to be lowest. To set a value, select the **Auto mode fan off temperature** option and enter a decimal number between 1 and 100.

→ **Auto mode fan start PWM [30]**

The **Auto mode fan start PWM** option can only be set if the **SYS_FAN1 Smart Fan control** option is set to **Auto Mode**. Use the **Auto mode fan start PWM** option to set the PWM start value. To set a value, select the **Auto mode fan start PWM** option and enter a decimal number between 1 and 100.

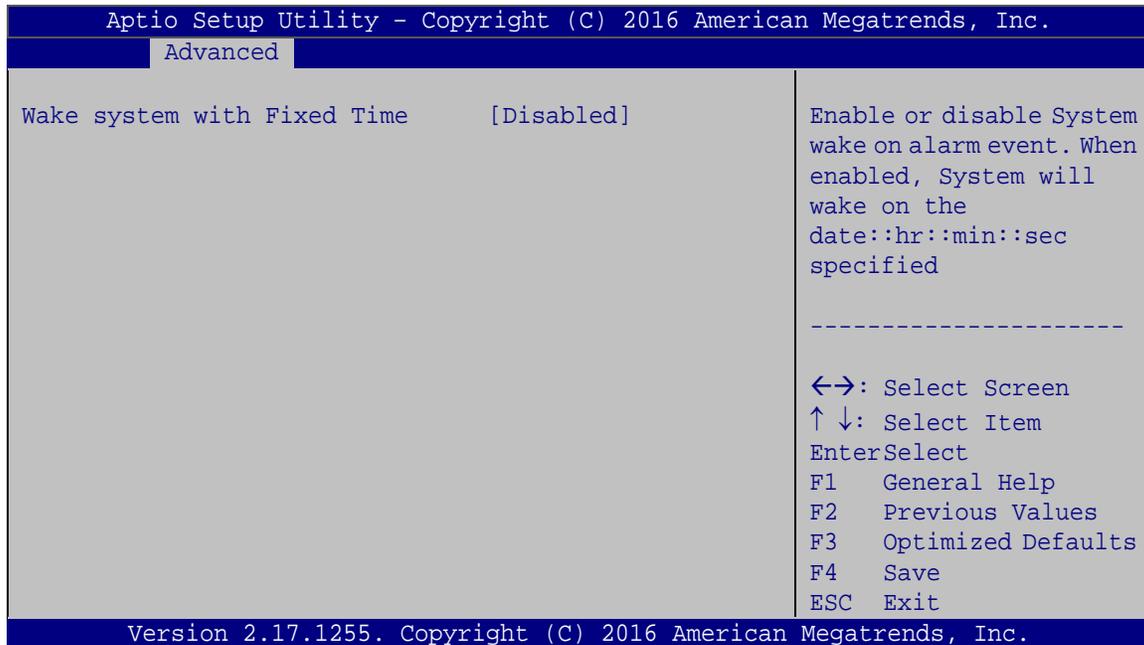
→ **Auto mode fan slope PWM [1]**

The **Auto mode fan slope PWM** option can only be set if the **SYS_FAN1 Smart Fan control** option is set to **Auto Mode**. Use the **Auto mode fan slope PWM** option to select the linear rate at which the PWM mode increases with respect to an increase in temperature. To set a value, select the **Auto mode fan slope PWM** option and enter a decimal number between 1 and 64.

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5.3.5 RTC Wake Settings

The **RTC Wake Settings** menu (**BIOS Menu 9**) configures RTC wake event.



BIOS Menu 9: RTC Wake Settings

→ Wake system with Fixed Time [Disabled]

Use the **Wake system with Fixed Time** option to enable or disable the system wake on alarm event.

- **Disabled** **DEFAULT** The real time clock (RTC) cannot generate a wake event

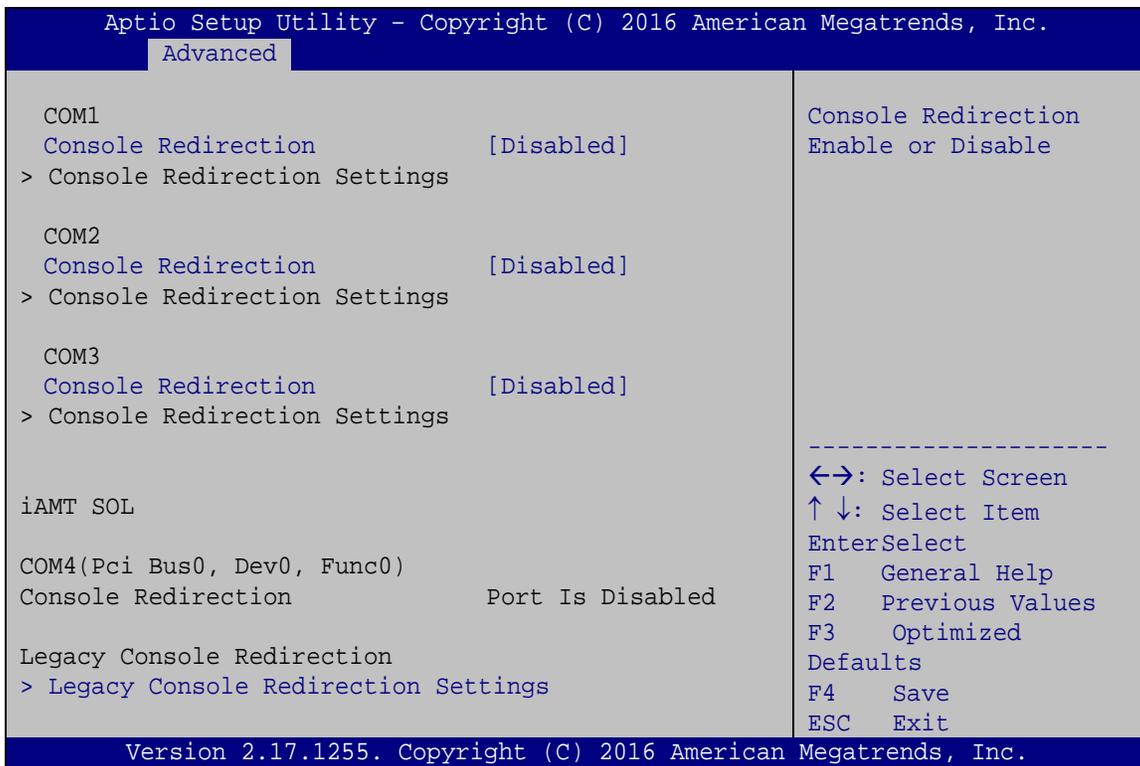
- **Enabled** If selected, the **Wake up every day** option appears allowing you to enable to disable the system to wake every day at the specified time. Besides, the following options appear with values that can be selected:
 - Wake up date
 - Wake up hour
 - Wake up minute

Wake up second

After setting the alarm, the computer turns itself on from a suspend state when the alarm goes off.

5.3.6 Serial Port Console Redirection

The **Serial Port Console Redirection** menu (**BIOS Menu 10**) allows the console redirection options to be configured. Console redirection allows users to maintain a system remotely by re-directing keyboard input and text output through the serial port.



BIOS Menu 10: Serial Port Console Redirection

➔ Console Redirection [Disabled]

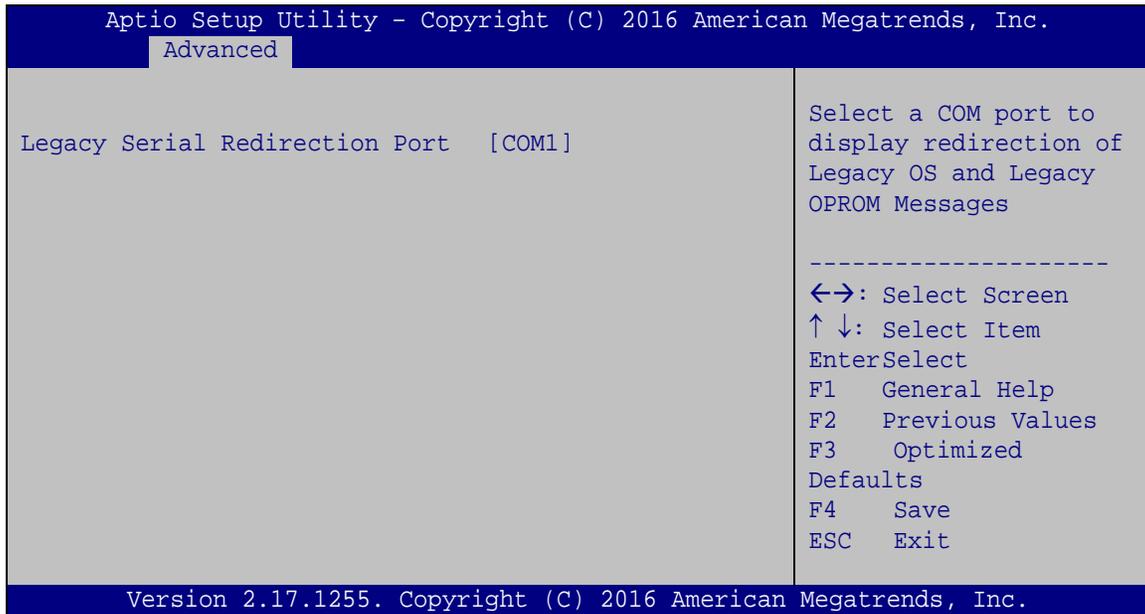
Use **Console Redirection** option to enable or disable the console redirection function.

- ➔ **Disabled** **DEFAULT** Disabled the console redirection function
- ➔ **Enabled** Enabled the console redirection function

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5.3.6.1 Legacy Console Redirection Settings

The **Legacy Console Redirection Settings** menu (**BIOS Menu 11**) allows the legacy console redirection options to be configured.



BIOS Menu 11: Legacy Console Redirection Settings

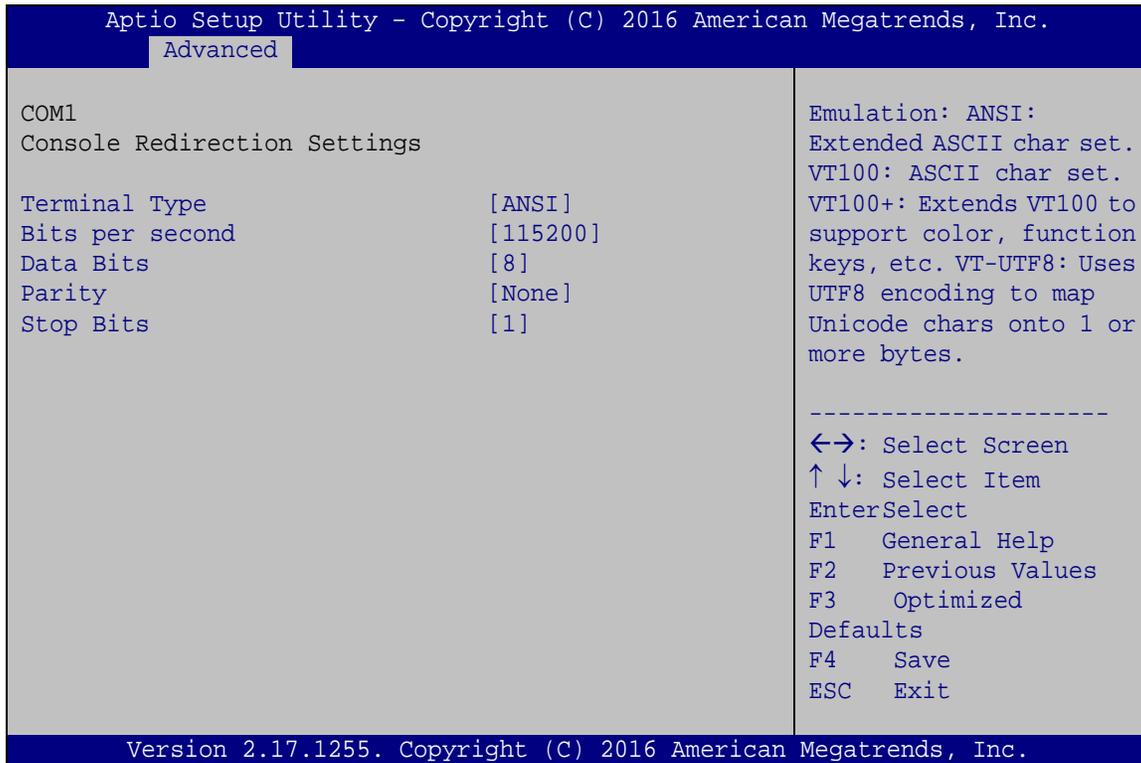
→ Legacy Serial Redirection Port [COM1]

Use the **Legacy Serial Redirection Port** option to specify a COM port to display redirection of legacy OS and legacy OPROM messages. The options include:

- COM1 **DEFAULT**
- COM2
- COM3
- COM4 (Pci Bus0, Dev0, Func0) (Disabled)

5.3.6.2 Console Redirection Settings

The **Console Redirection Settings** menu (**BIOS Menu 12**) allows the console redirection options to be configured. The option is active when Console Redirection option is enabled.



BIOS Menu 12: Console Redirection Settings

→ Terminal Type [ANSI]

Use the **Terminal Type** option to specify the remote terminal type.

- **VT100** The target terminal type is VT100
- **VT100+** The target terminal type is VT100+
- **VT-UTF8** The target terminal type is VT-UTF8
- **ANSI** **DEFAULT** The target terminal type is ANSI

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→ Bits per second [115200]

Use the **Bits per second** option to specify the serial port transmission speed. The speed must match the other side. Long or noisy lines may require lower speeds.

- | | | | |
|---|---------------|----------------|--|
| → | 9600 | | Sets the serial port transmission speed at 9600. |
| → | 19200 | | Sets the serial port transmission speed at 19200. |
| → | 57600 | | Sets the serial port transmission speed at 57600. |
| → | 115200 | DEFAULT | Sets the serial port transmission speed at 115200. |

→ Data Bits [8]

Use the **Data Bits** option to specify the number of data bits.

- | | | | |
|---|----------|----------------|--------------------------|
| → | 7 | | Sets the data bits at 7. |
| → | 8 | DEFAULT | Sets the data bits at 8. |

→ Parity [None]

Use the **Parity** option to specify the parity bit that can be sent with the data bits for detecting the transmission errors.

- | | | | |
|---|--------------|----------------|---|
| → | None | DEFAULT | No parity bit is sent with the data bits. |
| → | Even | | The parity bit is 0 if the number of ones in the data bits is even. |
| → | Odd | | The parity bit is 0 if the number of ones in the data bits is odd. |
| → | Mark | | The parity bit is always 1. This option does not provide error detection. |
| → | Space | | The parity bit is always 0. This option does not provide error detection. |

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→ Active Processor Cores [All]

Use the **Active Processor Cores** BIOS option to enable numbers of cores in the processor package.

- **All** **DEFAULT** Enable all cores in the processor package.
- **1** Enable one core in the processor package.

→ Intel® Virtualization Technology [Enabled]

Use the **Intel® Virtualization Technology** option to enable or disable virtualization on the system. When combined with third party software, Intel® Virtualization technology allows several OSs to run on the same system at the same time.

- **Disabled** Disables Intel® Virtualization Technology.
- **Enabled** **DEFAULT** Enables Intel® Virtualization Technology.

→ Intel® SpeedStep™ [Enabled]

Use the **Intel® SpeedStep™** option to enable or disable the Intel® SpeedStep Technology.

- **Disabled** Disables the Intel® SpeedStep Technology.
- **Enabled** **DEFAULT** Enables the Intel® SpeedStep Technology.

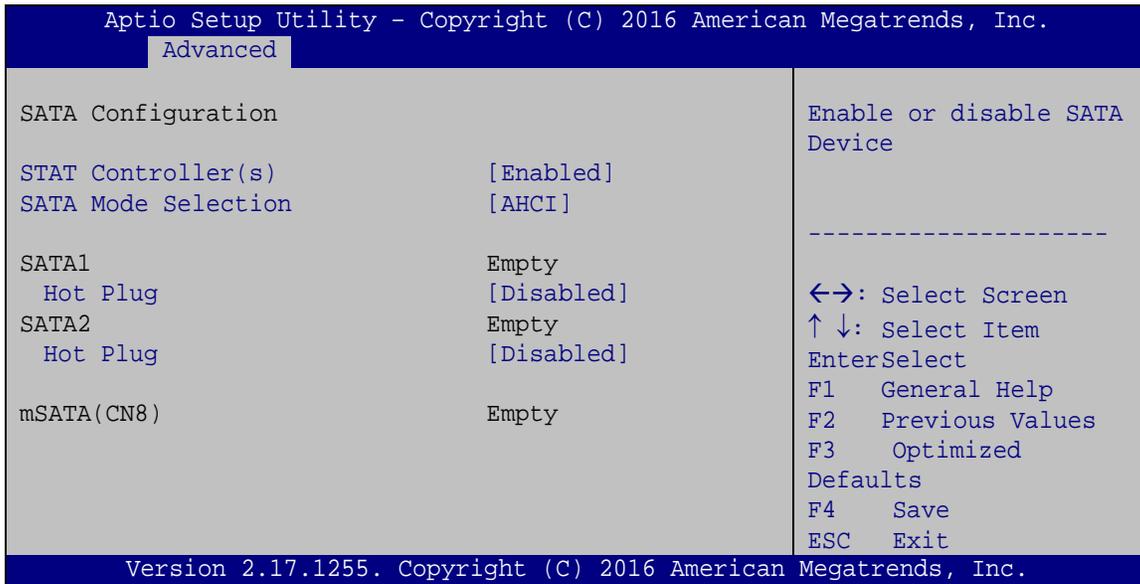
→ CPU C State [Disabled]

Use the **CPU C State** option to enable or disable CPU C state.

- **Disabled** **DEFAULT** Disables CPU C state.
- **Enabled** Enables CPU C state.

5.3.8 SATA Configuration

Use the **SATA Configuration** menu (**BIOS Menu 14**) to change and/or set the configuration of the SATA devices installed in the system.



BIOS Menu 14: SATA Configuration

→ STAT Controller(s) [Enabled]

Use the **STAT Controller(s)** option to enable or disable the SATA device.

- **Enabled** **DEFAULT** Enables the SATA device.
- **Disabled** Disables the SATA device.

→ SATA Mode Selection [AHCI]

Use the **SATA Mode Selection** option to configure SATA devices as AHCI devices.

- **AHCI** **DEFAULT** Configures SATA devices as AHCI device.
- **RAID** Configures SATA devices as RAID device.

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NOTE:

Before accessing the RAID configuration utility, ensure to set the **Option ROM Messages** BIOS option in the **Boot** menu to **Force BIOS**. This is to allow the “Press <CTRL+I> to enter Configuration Utility.....” message to appear during POST. Press Ctrl+I when prompted to enter the RAID configuration utility.

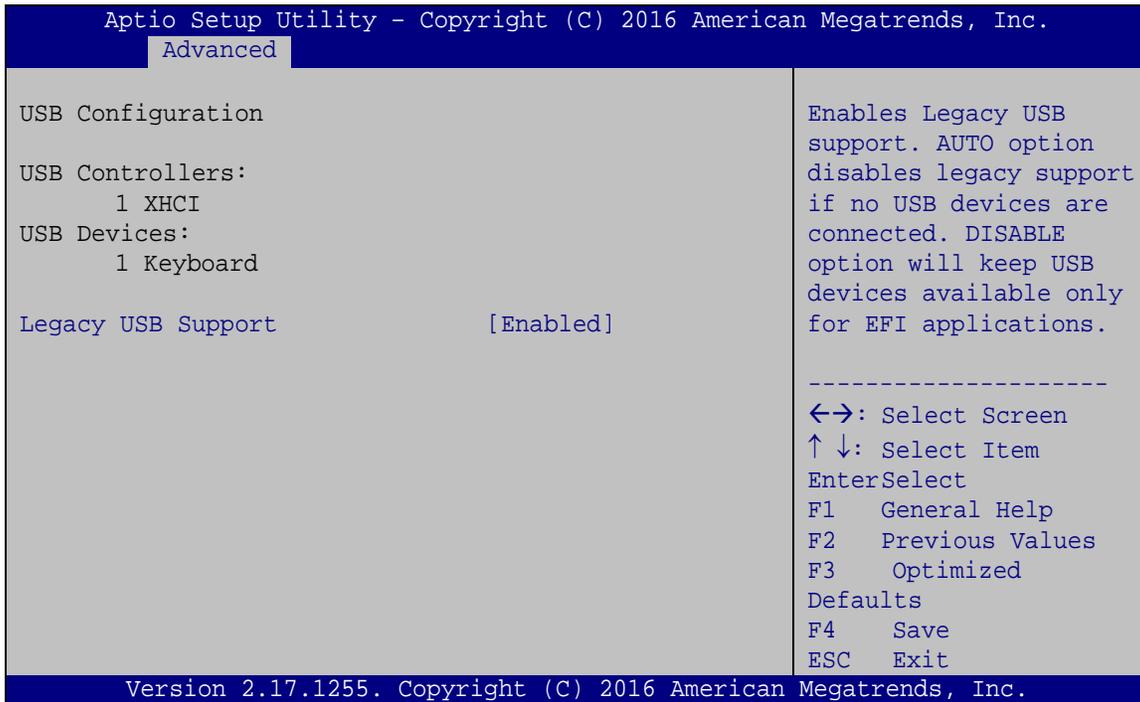
→ Hot Plug [Disabled]

Use the **Hot Plug** option to enable or disable the SATA device hot plug.

- **Disabled** **DEFAULT** Disables the SATA device hot plug.
- **Enabled** Enables the SATA device hot plug

5.3.9 USB Configuration

Use the **USB Configuration** menu (**BIOS Menu 15**) to read USB configuration information and configure the USB settings.



BIOS Menu 15: USB Configuration

➔ USB Devices

The **USB Devices Enabled** field lists the USB devices that are enabled on the system

➔ Legacy USB Support [Enabled]

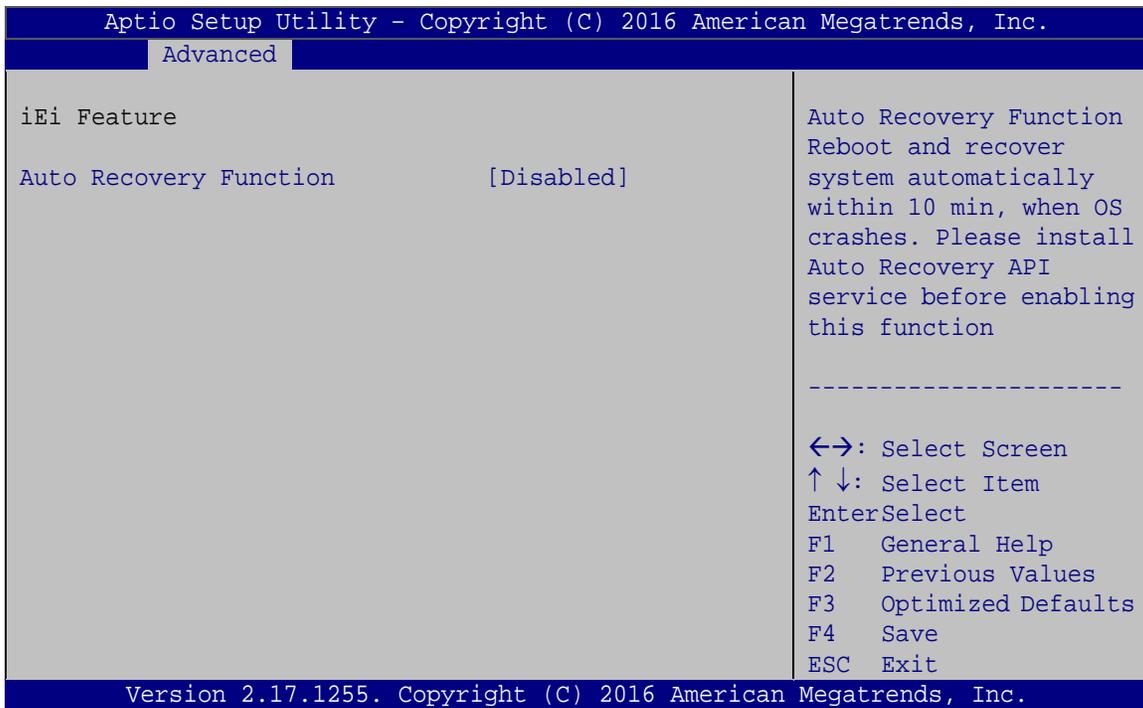
Use the **Legacy USB Support** BIOS option to enable USB mouse and USB keyboard support. Normally if this option is not enabled, any attached USB mouse or USB keyboard does not become available until a USB compatible operating system is fully booted with all USB drivers loaded. When this option is enabled, any attached USB mouse or USB keyboard can control the system even when there is no USB driver loaded onto the system.

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- ➔ **Enabled** **DEFAULT** Legacy USB support enabled
- ➔ **Disabled** Legacy USB support disabled
- ➔ **Auto** Legacy USB support disabled if no USB devices are connected

5.3.10 IEI Feature

Use the **IEI Feature** menu (**BIOS Menu 16**) to configure One Key Recovery function.



BIOS Menu 16: IEI Feature

➔ **Auto Recovery Function [Disabled]**

Use the **Auto Recovery Function** BIOS option to enable or disable the auto recovery function of the IEI One Key Recovery.

- ➔ **Disabled** **DEFAULT** Auto recovery function disabled
- ➔ **Enabled** Auto recovery function enabled

5.4 Chipset

Use the **Chipset** menu (**BIOS Menu 17**) to configure the system chipset.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Main   Advanced  Chipset   Boot   Security  Save & Exit  Server Mgmt
-----
> System Agent (SA) Configuration
> PCH-IO Configuration

System Agent (SA)
Parameters

-----
<=>: Select Screen
↑↓: Select Item
Enter>Select
+ - Change Opt.
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save & Exit
ESC Exit

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
    
```

BIOS Menu 17: Chipset

5.4.1 System Agent (SA) Configuration

Use the **System Agent (SA) Configuration** menu (**BIOS Menu 18**) to configure the System Agent (SA) parameters.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Chipset
-----
VT-d                               [Disabled]          VT-d capability

> Graphics Configuration
> Memory Configuration

-----
<=>: Select Screen
↑↓: Select Item
Enter>Select
+ - Change Opt.
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save & Exit
ESC Exit

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
    
```

BIOS Menu 18: System Agent (SA) Configuration

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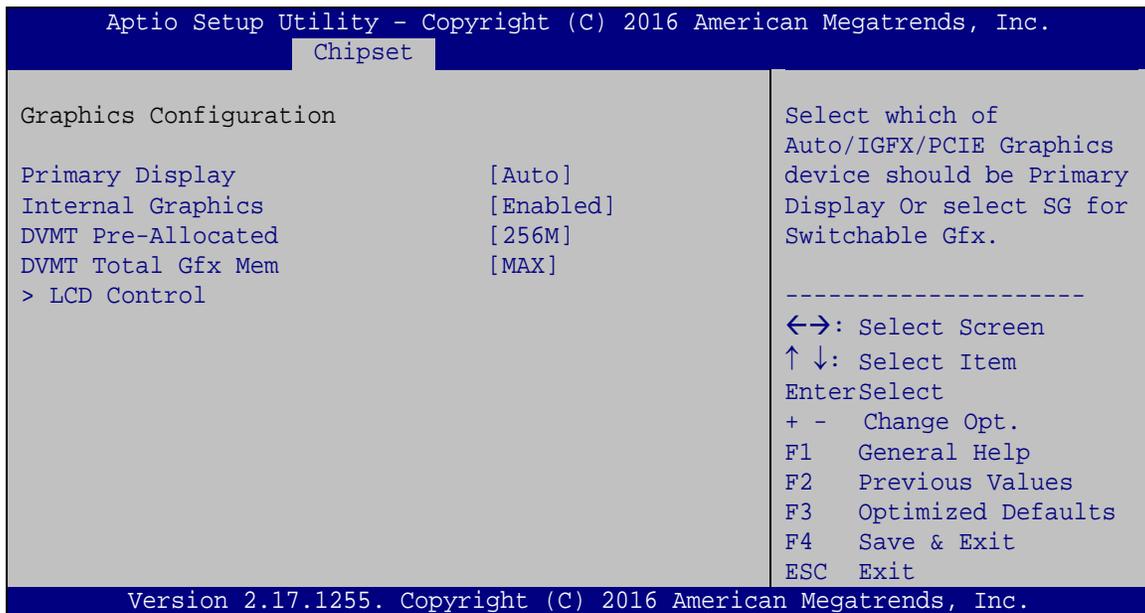
→ VT-d [Disabled]

Use the **VT-d** option to enable or disable VT-d support.

- **Disabled** **DEFAULT** Disable VT-d support.
- **Enabled** Enable VT-d support.

5.4.1.1 Graphics Configuration

Use the **Graphics Configuration** menu (**BIOS Menu 19**) to configure the graphics settings.



BIOS Menu 19: Graphics Configuration

→ Primary Display [Auto]

Use the **Primary Display** option to select the graphics controller used as the primary boot device. Configuration options are listed below:

- Auto **DEFAULT**
- IGFX
- PCIE

→ Internal Graphics [Enabled]

Use the **Internal Graphics** option to enable or disable the internal graphics device.

- Auto** The internal graphics device is automatically detected and enabled.
- Disabled** Disable the internal graphics device.
- Enabled DEFAULT** Enable the internal graphics device. The following options/submenu appear with values that can be selected:

DVMT Pre-Allocated

DVMT Total Gfx Mem

LCD Control

→ DVMT Pre-Allocated [256M]

Use the **DVMT Pre-Allocated** option to set the amount of system memory allocated to the integrated graphics processor when the system boots. The system memory allocated can then only be used as graphics memory, and is no longer available to applications or the operating system. Configuration options are listed below:

- 32M
- 64M
- 128M
- 256M **DEFAULT**
- 512M

→ DVMT Total Gfx Mem [MAX]

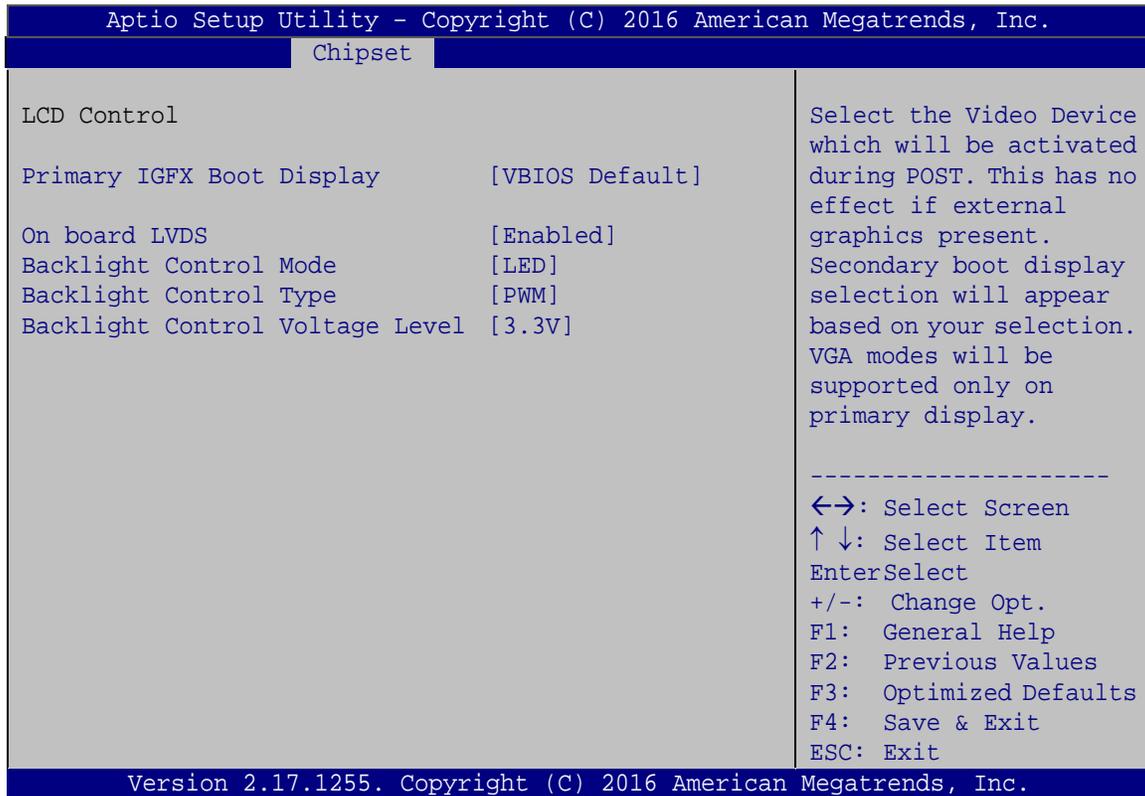
Use the **DVMT Total Gfx Mem** option to select DVMT 5.0 total graphic memory size used by the internal graphics device. The following options are available:

- 128M
- 256M
- MAX **DEFAULT**

NANO-ULT3 SBC

5.4.1.1.1 LCD Control

Use the **LCD Control** submenu (**BIOS Menu 20**) to select a display device which will be activated during POST.



BIOS Menu 20: LCD Control

→ Primary IGFX Boot Display [VBIOS Default]

Use the **Primary IGFX Boot Display** option to select the display device used by the system when it boots.

- VBIOS Default **DEFAULT**
- HDMI2
- LVDS
- DP/HDMI1

→ On board LVDS [Enabled]

Use the **On board LVDS** option enables or disables the on-board LVDS connector.

- Disabled** The on-board LVDS connector is disabled.
- Enabled DEFAULT** The on-board LVDS connector is disabled.

→ Backlight Control Mode [LED]

Use the **Backlight Control Mode** option to specify the backlight control mode. Configuration options are listed below.

- LED **DEFAULT**
- CCFL

→ Backlight Control Type [PWM]

Use the **Backlight Control Type** option to specify the backlight control type. Configuration options are listed below.

- PWM **DEFAULT**
- DC

→ Backlight Control Voltage Level [3.3V]

Use the **Backlight Control Voltage Level** option to specify the backlight control voltage. Configuration options are listed below.

- 3.3V **DEFAULT**
- 5.0V

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5.4.1.2 Memory Configuration

Use the **Memory Configuration** submenu (**BIOS Menu 21**) to display the memory information.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Chipset
Memory Information
Total Memory          4096 MB
DIMM1                 4096 MB
DIMM2                 Not Present
-----
<->: Select Screen
↑ ↓: Select Item
EnterSelect
+ - Change Opt.
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save & Exit
ESC Exit
Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
  
```

BIOS Menu 21: Memory Configuration

5.4.2 PCH-IO Configuration

Use the **PCH-IO Configuration** menu (**BIOS Menu 22**) to configure the PCH-IO chipset.

```

Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Chipset
Auto Power Button Status [Disable (ATX)]
Restore AC Power Loss    [Last State]
> PCI Express Configuration
> HD Audio Configuration
-----
<->: Select Screen
↑ ↓: Select Item
EnterSelect
+ - Change Opt.
F1  General Help
F2  Previous Values
F3  Optimized Defaults
F4  Save & Exit
ESC Exit
Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
  
```

BIOS Menu 22: PCH-IO Configuration

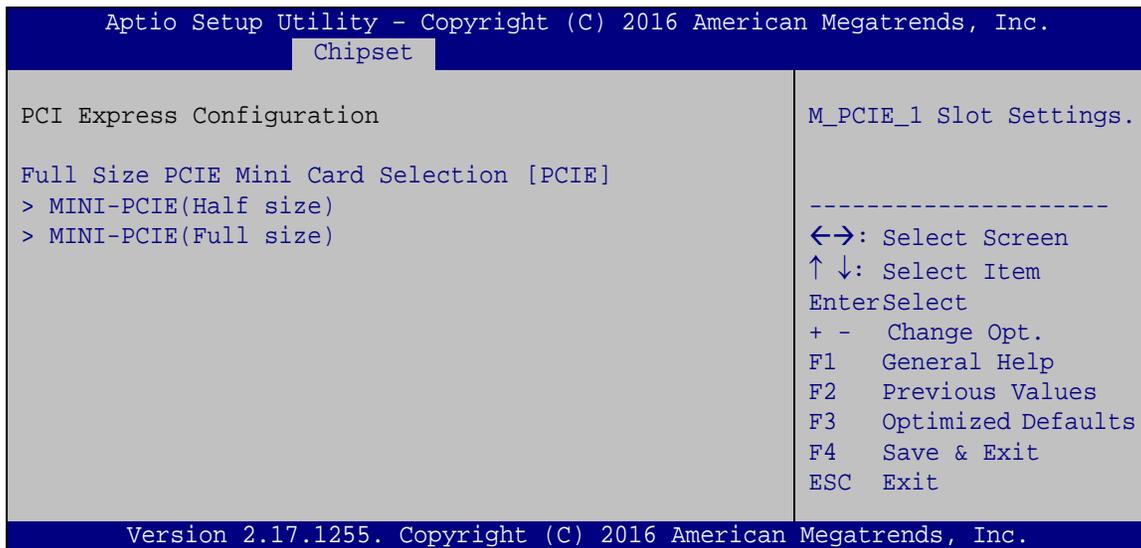
➔ **Restore AC Power Loss [Last State]**

Use the **Restore AC Power** BIOS option to specify what state the system returns to if there is a sudden loss of power to the system.

- ➔ **Power Off** The system remains turned off
- ➔ **Power On** The system turns on
- ➔ **Last State DEFAULT** The system returns to its previous state. If it was on, it turns itself on. If it was off, it remains off.

5.4.2.1 PCI Express Configuration

Use the **PCI Express Configuration** submenu (**BIOS Menu 23**) to configure the PCI Express slots.



BIOS Menu 23: PCI Express Configuration

➔ **Full Size PCIE Mini Card Selection [PCIE]**

Use the **Full Size PCIE Mini Card Selection** BIOS option to configure the full-size PCIe Mini slot (CN8) as PCIe Mini slot or mSATA slot.

- ➔ **PCIE DEFAULT** Configure the full-size PCIe Mini slot as PCIe Mini slot
- ➔ **mSATA** Configure the full-size PCIe Mini slot as mSATA slot

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The **MINI-PCIE (Half size)** and **MINI-PCIE (Full size)** submenus both contain the following options:

→ PCIe Speed [Auto]

Use the **PCIe Speed** option to configure the PCIe interface speed.

- Auto **DEFAULT**
- Gen 1
- Gen 2
- Gen 3

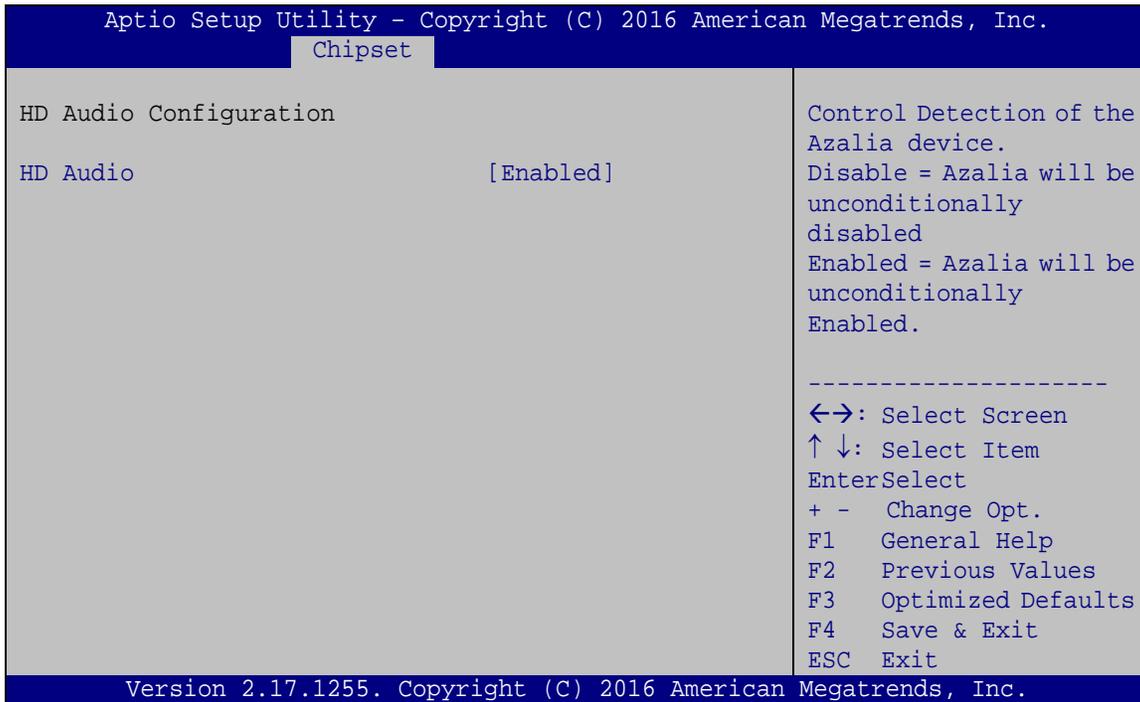
→ Detect Non-Compliance Device [Disabled]

Use the **Detect Non-Compliance Device** option to enable or disable detecting if a non-compliance PCI Express device is connected to the PCI Express slot.

- **Disabled** **DEFAULT** Disables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.
- **Enabled** Enables to detect if a non-compliance PCI Express device is connected to the PCI Express slot.

5.4.2.2 HD Audio Configuration

Use the **HD Audio Configuration** submenu (**BIOS Menu 24**) to configure the High Definition Audio codec.



BIOS Menu 24: HD Audio Configuration

→ HD Audio [Enabled]

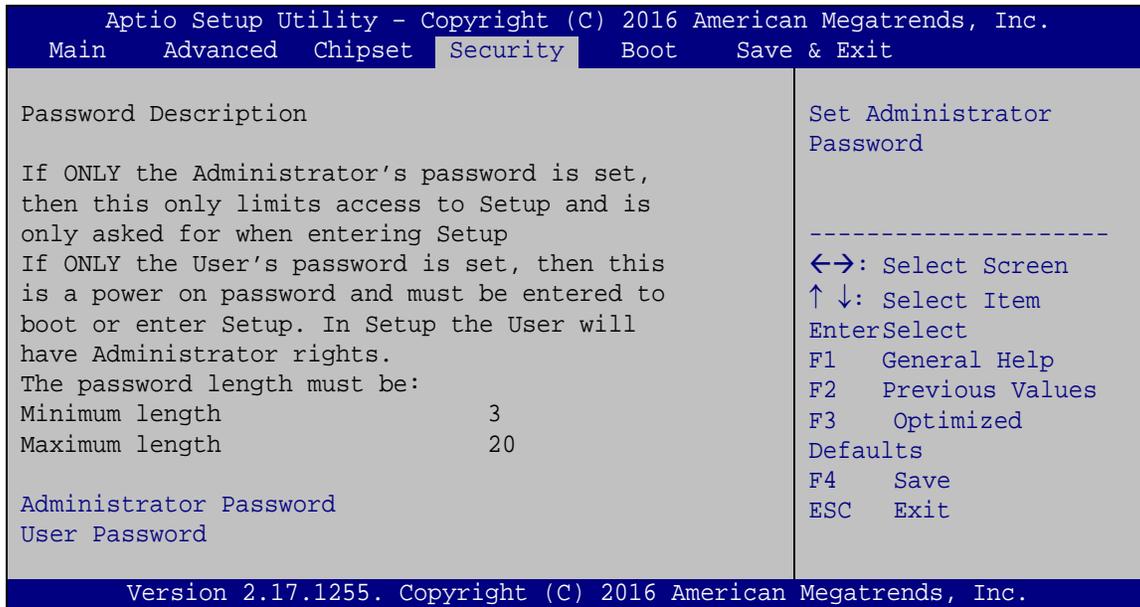
Use the **HD Audio** BIOS option to enable or disable the High Definition Audio controller.

- **Disabled** The High Definition Audio controller is disabled.
- **Enabled** **DEFAULT** The High Definition Audio controller is enabled.

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5.5 Security

Use the **Security** menu (**BIOS Menu 25**) to set system and user passwords.



BIOS Menu 25: Security

➔ Administrator Password

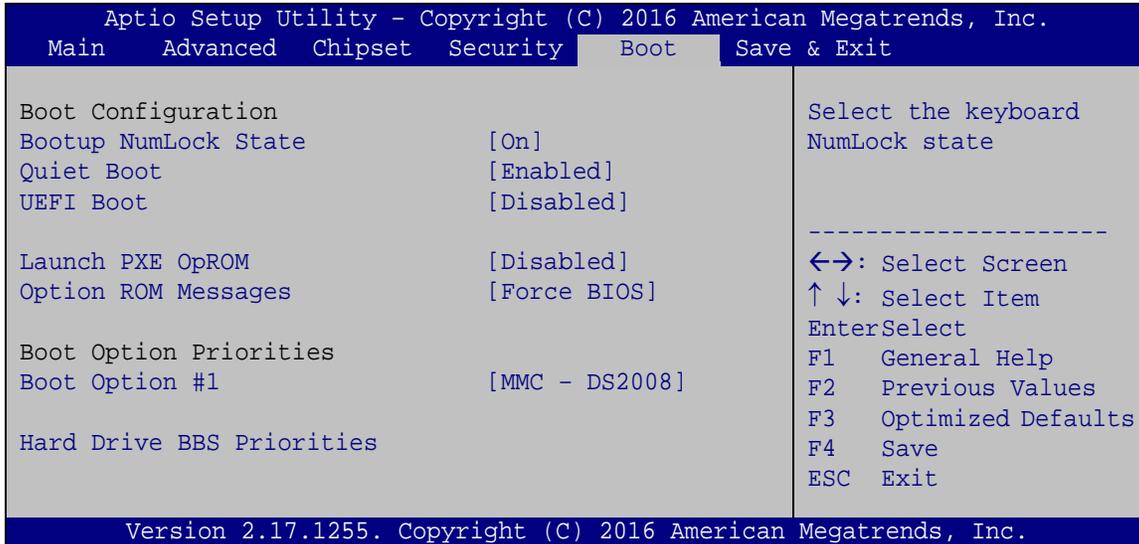
Use the **Administrator Password** to set or change a administrator password.

➔ User Password

Use the **User Password** to set or change a user password.

5.6 Boot

Use the **Boot** menu (**BIOS Menu 26**) to configure system boot options.



BIOS Menu 26: Boot

→ Bootup NumLock State [On]

Use the **Bootup NumLock State** BIOS option to specify if the number lock setting must be modified during boot up.

- **On** **DEFAULT** Allows the Number Lock on the keyboard to be enabled automatically when the computer system boots up. This allows the immediate use of the 10-key numeric keypad located on the right side of the keyboard. To confirm this, the Number Lock LED light on the keyboard is lit.

- **Off** Does not enable the keyboard Number Lock automatically. To use the 10-keys on the keyboard, press the Number Lock key located on the upper left-hand corner of the 10-key pad. The Number Lock LED on the keyboard lights up when the Number Lock is engaged.

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→ Quiet Boot [Enabled]

Use the **Quiet Boot** BIOS option to select the screen display when the system boots.

- **Disabled** Normal POST messages displayed
- **Enabled** **DEFAULT** OEM Logo displayed instead of POST messages

→ UEFI Boot [Disabled]

Use the **UEFI Boot** option to enable or disable to boot from the UEFI devices.

- **Enabled** Boot from UEFI devices is enabled.
- **Disabled** **DEFAULT** Boot from UEFI devices is disabled.

→ Launch PXE OpROM [Disabled]

Use the **Launch PXE OpROM** option to enable or disable boot option for legacy network devices.

- **Disabled** **DEFAULT** Ignore all PXE Option ROMs
- **Enabled** Load PXE Option ROMs.

→ Option ROM Messages [Force BIOS]

Use the **Option ROM Messages** option to set the Option ROM display mode.

- **Force BIOS** **DEFAULT** Sets display mode to force BIOS.
- **Keep Current** Sets display mode to current.

→ Boot Option Priority

Use the **Boot Option Priority** function to set the system boot sequence from the available devices. The drive sequence also depends on the boot sequence in the individual device section.

5.7 Exit

Use the **Exit** menu (**BIOS Menu 27**) to load default BIOS values, optimal failsafe values and to save configuration changes.

```
Aptio Setup Utility - Copyright (C) 2016 American Megatrends, Inc.
Main  Advanced  Chipset  Security  Boot  Save & Exit
-----
Save Changes and Reset
Discard Changes and Reset

Restore Defaults
Save as User Defaults
Restore User Defaults

Reset the system after
saving the changes.

-----
<->: Select Screen
^ v: Select Item
Enter>Select
F1  General Help
F2  Previous Values
F3  Optimized
Defaults
F4  Save
ESC Exit

Version 2.17.1255. Copyright (C) 2016 American Megatrends, Inc.
```

BIOS Menu 27: Exit

→ Save Changes and Reset

Use the **Save Changes and Reset** option to save the changes made to the BIOS options and to exit the BIOS configuration setup program.

→ Discard Changes and Reset

Use the **Discard Changes and Reset** option to exit the system without saving the changes made to the BIOS configuration setup program.

→ Restore Defaults

Use the **Restore Defaults** option to load the optimal default values for each of the parameters on the Setup menus. **F3 key can be used for this operation.**

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→ Save as User Defaults

Use the **Save as User Defaults** option to save the changes done so far as user defaults.

→ Restore User Defaults

Use the **Restore User Defaults** option to restore the user defaults to all the setup options.

Chapter

6

Software Drivers

NANO-ULT3 SBC

6.1 Available Drivers

All the drivers for the NANO-ULT3 are available on IEI Resource Download Center (<https://download.ieiworld.com>). Type NANO-ULT3 and press Enter to find all the relevant software, utilities, and documentation.

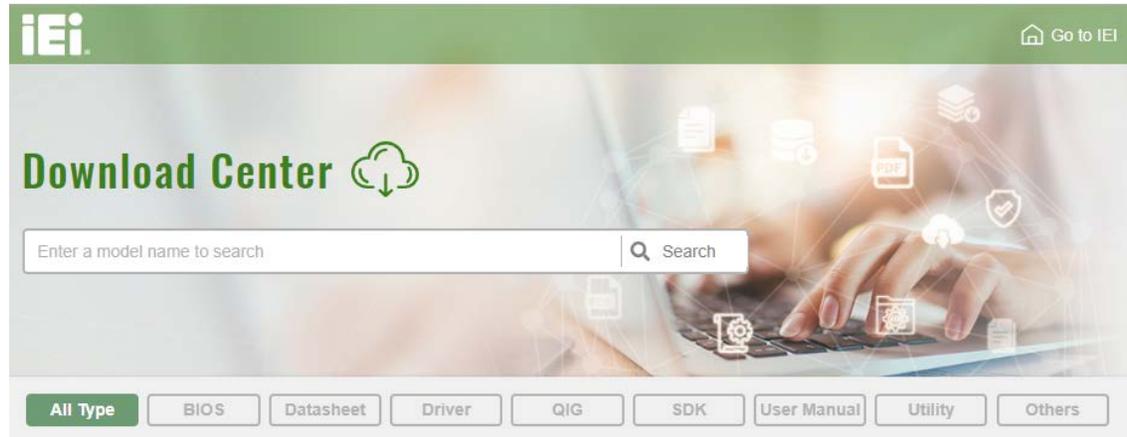
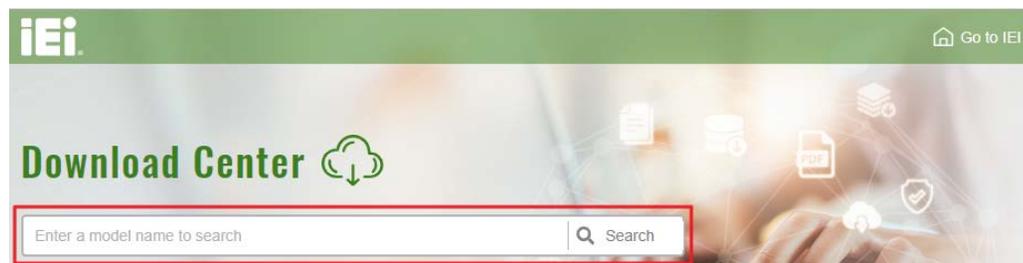


Figure 6-1: IEI Resource Download Center

6.2 Driver Download

To download drivers from IEI Resource Download Center, follow the steps below.

Step 1: Go to <https://download.ieiworld.com>. Type NANO-ULT3 and press Enter.



Step 2: All product-related software, utilities, and documentation will be listed. You can choose **Driver** to filter the result.

i Keyword: "NANO-ULT3", Searching Result : 16 Records.

NANO-ULT3 Product Info ▶

[Embedded Computer](#) ▶ [Single Board Computer](#) ▶ [Embedded Board](#)

EPIC SBC supports Intel® 14nm 6th Generation Mobile Core™ i7/i5/i3 and Celeron® on-board Processor (ULT)

Driver

File Name	Published	Version	File Checksum
7B000-001167-RS_V1.8.iso (1.13 GB)	2017/10/16	1.80	114B70CE3AE5F6E58D3E61586F2D255A

Step 3: Click the driver file name on the page and you will be prompted with the following window. You can download the entire ISO file (❶), or double click an individual item to find its driver file and click the file name to download (❷).

7B000-001167-RS_V1.8.iso X

❶ Click here to download entire ISO file. (1.13 GB)

* Download individual file *

Docs

- 1.Chipset
- ❷ WIN10&8.1&7.zip (2.68 MB)
- 2.VGA
- 3.LAN
- 3.LAN(IMB-H110)
- 4.Audio
- 5.USB3.0
- 6.KMDF
- 7.ME
- 8.RST
- 9.Serial IO
- A.Manual



NOTE:

To install software from the downloaded ISO image file in Windows 8, 8.1 or 10, double-click the ISO file to mount it as a virtual drive to view its content. On Windows 7 system, an additional tool (such as Virtual CD-ROM Control Panel from Microsoft) is needed to mount the file.

Appendix

A

Regulatory Compliance

DECLARATION OF CONFORMITY

This equipment has been tested and found to comply with specifications for CE marking. If the user modifies and/or installs other devices in the equipment, the CE conformity declaration may no longer apply.

FCC WARNING

This equipment complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

- This device may not cause harmful interference, and
- This device must accept any interference received, including interference that may cause undesired operation.

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

Appendix

B

Product Disposal

**CAUTION:**

Risk of explosion if battery is replaced by an incorrect type. Only certified engineers should replace the on-board battery.

Dispose of used batteries according to instructions and local regulations.

- Outside the European Union – If you wish to dispose of used electrical and electronic products outside the European Union, please contact your local authority so as to comply with the correct disposal method.
- Within the European Union – The device that produces less waste and is easier to recycle is classified as electronic device in terms of the European Directive 2012/19/EU (WEEE), and must not be disposed of as domestic garbage.



EU-wide legislation, as implemented in each Member State, requires that waste electrical and electronic products carrying the mark (left) must be disposed of separately from normal household waste. This includes monitors and electrical accessories, such as signal cables or power cords. When you need to dispose of your device, please follow the guidance of your local authority, or ask the shop where you purchased the product. The mark on electrical and electronic products only applies to the current European Union Member States.

Please follow the national guidelines for electrical and electronic product disposal.

Appendix

C

BIOS Menu Options

<input type="checkbox"/>	System Date [xx/xx/xx]	78
<input type="checkbox"/>	System Time [xx:xx:xx]	78
<input type="checkbox"/>	ACPI Sleep State [S3 (Suspend to RAM)]	79
<input type="checkbox"/>	Intel AMT [Enabled]	80
<input type="checkbox"/>	Un-configure ME [Disabled]	80
<input type="checkbox"/>	Serial Port [Enabled]	82
<input type="checkbox"/>	Change Settings [Auto]	82
<input type="checkbox"/>	Serial Port [Enabled]	83
<input type="checkbox"/>	Change Settings [Auto]	83
<input type="checkbox"/>	Serial Port [Enabled]	84
<input type="checkbox"/>	Change Settings [Auto]	84
<input type="checkbox"/>	Device Mode [RS232]	85
<input type="checkbox"/>	PC Health Status	85
<input type="checkbox"/>	CPU_FAN1 Smart Fan Control [Auto Mode]	86
<input type="checkbox"/>	SYS_FAN1 Smart Fan Control [Auto Mode]	87
<input type="checkbox"/>	Auto mode fan start temperature [50]	87
<input type="checkbox"/>	Auto mode fan off temperature [40]	88
<input type="checkbox"/>	Auto mode fan start PWM [30]	88
<input type="checkbox"/>	Auto mode fan slope PWM [1]	88
<input type="checkbox"/>	Wake system with Fixed Time [Disabled]	89
<input type="checkbox"/>	Console Redirection [Disabled]	90
<input type="checkbox"/>	Legacy Serial Redirection Port [COM1]	91
<input type="checkbox"/>	Terminal Type [ANSI]	92
<input type="checkbox"/>	Bits per second [115200]	93
<input type="checkbox"/>	Data Bits [8]	93
<input type="checkbox"/>	Parity [None]	93
<input type="checkbox"/>	Stop Bits [1]	94
<input type="checkbox"/>	Active Processor Cores [All]	95
<input type="checkbox"/>	Intel® Virtualization Technology [Enabled]	95
<input type="checkbox"/>	Intel® SpeedStep™ [Enabled]	95
<input type="checkbox"/>	CPU C State [Disabled]	95
<input type="checkbox"/>	STAT Controller(s) [Enabled]	96
<input type="checkbox"/>	SATA Mode Selection [AHCI]	96
<input type="checkbox"/>	Hot Plug [Disabled]	97

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<input type="checkbox"/>	USB Devices	98
<input type="checkbox"/>	Legacy USB Support [Enabled].....	98
<input type="checkbox"/>	Auto Recovery Function [Disabled].....	99
<input type="checkbox"/>	VT-d [Disabled].....	101
<input type="checkbox"/>	Primary Display [Auto]	101
<input type="checkbox"/>	Internal Graphics [Enabled].....	102
<input type="checkbox"/>	DVMT Pre-Allocated [256M]	102
<input type="checkbox"/>	DVMT Total Gfx Mem [MAX].....	102
<input type="checkbox"/>	Primary IGFX Boot Display [VBIOS Default]	103
<input type="checkbox"/>	On board LVDS [Enabled].....	104
<input type="checkbox"/>	Backlight Control Mode [LED].....	104
<input type="checkbox"/>	Backlight Control Type [PWM]	104
<input type="checkbox"/>	Backlight Control Voltage Level [3.3V].....	104
<input type="checkbox"/>	Restore AC Power Loss [Last State]	106
<input type="checkbox"/>	Full Size PCIE Mini Card Selection [PCIE].....	106
<input type="checkbox"/>	PCle Speed [Auto].....	107
<input type="checkbox"/>	Detect Non-Compliance Device [Disabled]	107
<input type="checkbox"/>	HD Audio [Enabled]	108
<input type="checkbox"/>	Administrator Password	109
<input type="checkbox"/>	User Password	109
<input type="checkbox"/>	Bootup NumLock State [On].....	110
<input type="checkbox"/>	Quiet Boot [Enabled]	111
<input type="checkbox"/>	UEFI Boot [Disabled]	111
<input type="checkbox"/>	Launch PXE OpROM [Disabled].....	111
<input type="checkbox"/>	Option ROM Messages [Force BIOS].....	111
<input type="checkbox"/>	Boot Option Priority.....	111
<input type="checkbox"/>	Save Changes and Reset	112
<input type="checkbox"/>	Discard Changes and Reset	112
<input type="checkbox"/>	Restore Defaults	112
<input type="checkbox"/>	Save as User Defaults	113
<input type="checkbox"/>	Restore User Defaults	113

Appendix

D

Digital I/O Interface

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The DIO connector on the NANO-ULT3 is interfaced to GPIO ports on the Super I/O chipset. The digital inputs and digital outputs are generally control signals that control the on/off circuit of external devices or TTL devices. Data can be read or written to the selected address to enable the DIO functions.

**NOTE:**

For further information, please refer to the datasheet for the Super I/O chipset.

The BIOS interrupt call **INT 15H** controls the digital I/O.

INT 15H:

AH – 6FH	
<u>Sub-function:</u>	
AL – 8	: Set the digital port as INPUT
AL	: Digital I/O input value

Assembly Language Sample 1

```
MOV    AX, 6F08H    ; setting the digital port as input
INT    15H          ;
```

AL low byte = value

AH – 6FH	
<u>Sub-function:</u>	
AL – 9	: Set the digital port as OUTPUT
BL	: Digital I/O output value

Assembly Language Sample 2

```

MOV     AX, 6F09H      ; setting the digital port as output
MOV     BL, 09H        ; digital value is 09H
INT     15H           ;
    
```

Digital Output is 1001b

Appendix

E

Watchdog Timer



NOTE:

The following discussion applies to DOS. Contact IEI support or visit the IEI website for drivers for other operating systems.

The Watchdog Timer is a hardware-based timer that attempts to restart the system when it stops working. The system may stop working because of external EMI or software bugs. The Watchdog Timer ensures that standalone systems like ATMs will automatically attempt to restart in the case of system problems.

A BIOS function call (INT 15H) is used to control the Watchdog Timer.

INT 15H:

AH – 6FH Sub-function:	
AL – 2:	Sets the Watchdog Timer's period.
BL:	Time-out value (Its unit-second is dependent on the item "Watchdog Timer unit select" in CMOS setup).

Table E-1: AH-6FH Sub-function

Call sub-function 2 to set the time-out period of Watchdog Timer first. If the time-out value is not zero, the Watchdog Timer starts counting down. When the timer value reaches zero, the system resets. To ensure that this reset condition does not occur, calling sub-function 2 must periodically refresh the Watchdog Timer. However, the watchdog timer is disabled if the time-out value is set to zero.

A tolerance of at least 10% must be maintained to avoid unknown routines within the operating system (DOS), such as disk I/O that can be very time-consuming.

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**NOTE:**

The Watchdog Timer is activated through software. The software application that activates the Watchdog Timer must also deactivate it when closed. If the Watchdog Timer is not deactivated, the system will automatically restart after the Timer has finished its countdown.

EXAMPLE PROGRAM:

; INITIAL TIMER PERIOD COUNTER

;

W_LOOP:

;

```

MOV      AX, 6F02H      ;setting the time-out value
MOV      BL, 30         ;time-out value is 48 seconds
INT      15H

```

;

; ADD THE APPLICATION PROGRAM HERE

;

```

CMP      EXIT_AP, 1     ;is the application over?
JNE      W_LOOP        ;No, restart the application

```

```

MOV      AX, 6F02H      ;disable Watchdog Timer
MOV      BL, 0          ;
INT      15H

```

;

; EXIT ;

Appendix

F

Error Beep Code

NANO-ULT3 SBC

F.1 PEI Beep Codes

Number of Beeps	Description
1	Memory not Installed
1	Memory was installed twice (InstallPeiMemory routine in PEI Core called twice)
2	Recovery started
3	DXEIPL was not found
3	DXE Core Firmware Volume was not found
4	Recovery failed
4	S3 Resume failed
7	Reset PPI is not available

F.2 DXE Beep Codes

Number of Beeps	Description
1	Invalid password
4	Some of the Architectural Protocols are not available
5	No Console Output Devices are found
5	No Console Input Devices are found
6	Flash update is failed
7	Reset protocol is not available
8	Platform PCI resource requirements cannot be met

**NOTE:**

If you have any question, please contact IEI for further assistance.

Appendix

G

Hazardous Materials Disclosure

NANO-ULT3 SBC

G.1 RoHS II Directive (2015/863/EU)

The details provided in this appendix are to ensure that the product is compliant with the RoHS II Directive (2015/863/EU). The table below acknowledges the presences of small quantities of certain substances in the product, and is applicable to RoHS II Directive (2015/863/EU).

Please refer to the following table.

Part Name	Toxic or Hazardous Substances and Elements									
	Lead (Pb)	Mercury (Hg)	Cadmium (Cd)	Hexavalent Chromium (CR(VI))	Polybrominated Biphenyls (PBB)	Polybrominated Diphenyl Ethers (PBDE)	Bis(2-ethylhexyl) phthalate (DEHP)	Butyl benzyl phthalate (BBP)	Dibutyl phthalate (DBP)	Diisobutyl phthalate (DIBP)
Housing	O	O	O	O	O	O	O	O	O	O
Display	O	O	O	O	O	O	O	O	O	O
Printed Circuit Board	O	O	O	O	O	O	O	O	O	O
Metal Fasteners	O	O	O	O	O	O	O	O	O	O
Cable Assembly	O	O	O	O	O	O	O	O	O	O
Fan Assembly	O	O	O	O	O	O	O	O	O	O
Power Supply Assemblies	O	O	O	O	O	O	O	O	O	O
Battery	O	O	O	O	O	O	O	O	O	O

O: This toxic or hazardous substance is contained in all of the homogeneous materials for the part is below the limit requirement in Directive (EU) 2015/863.

X: This toxic or hazardous substance is contained in at least one of the homogeneous materials for this part is above the limit requirement in Directive (EU) 2015/863.

G.2 China RoHS

此附件旨在确保本产品符合中国 RoHS 标准。以下表格标示此产品中某有毒物质的含量符合中国 RoHS 标准规定的限量要求。

本产品上会附有“环境友好使用期限”的标签，此期限是估算这些物质“不会有泄漏或突变”的年限。本产品可能包含有较短的环境友好使用期限的可替换元件，像是电池或灯管，这些元件将会单独标示出来。

部件名称	有毒有害物质或元素					
	铅 (Pb)	汞 (Hg)	镉 (Cd)	六价铬 (CR(VI))	多溴联苯 (PBB)	多溴二苯醚 (PBDE)
壳体	○	○	○	○	○	○
显示	○	○	○	○	○	○
印刷电路板	○	○	○	○	○	○
金属螺帽	○	○	○	○	○	○
电缆组装	○	○	○	○	○	○
风扇组装	○	○	○	○	○	○
电力供应组装	○	○	○	○	○	○
电池	○	○	○	○	○	○

○: 表示该有毒有害物质在该部件所有物质材料中的含量均在 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求以下。

X: 表示该有毒有害物质至少在该部件的某一均质材料中的含量超出 SJ/T11364-2014 與 GB/T26572-2011 标准规定的限量要求。