# innodisk

# Approval Sheet

| Customer | |
|---|---|
| **Product Number** | **M3D0-8GSS65N9** |
| **Module speed** | **PC3-10600** |
| **Pin** | **204pin** |
| **Cl-tRCD-tRP** | **9-9-9** |
| **Operating Temp** | **-40℃~85℃** |
| **Date** | **20th May 2019** |

The Total Solution For
Industrial Flash Storage

Rev 1.0

## 1. Features

Key Parameter

| Industry Nomenclature | Speed Grade | Data Rate MT/s | | | CL | tRCD | tRP |
|---|---|---|---|---|---|---|---|
| | | CL=7 | CL=9 | CL=11 | | | |
| PC3-10600 | N | 1066 | 1333 | - | 9 | 9 | 9 |

• JEDEC Standard 204-pin Small Outline Dual In-Line Memory Module

• Intend for PC3-10600 applications

• Inputs and Outputs are SSTL-15 compatible

•VDD=VDDQ=1.5 Volt (-0.075/+0.075V)

• Bi-directional Differential Data Strobe

• DLL aligns DQ and DQS transition with CK transition

• SDRAMs have 8 internal banks for concurrent operation

• Normal and Dynamic On-Die Termination support.

• SDRAMs are 78-ball BGA Package

• Gold Plating Thickness 30μ"

• Temperature Sensor with SPD EEPROM

• 8 bit pre-fetch

• Two different termination values (Rtt_Nom & Rtt_WR)

• Auto & self refresh 7.8μs (Tc $\leq$ +85°C)

•16/10/2 Addressing (row/column/rank)-8GB

• SDRAM operating temperature range -40°C $\leq$ Tc $\leq$ +85°C

• Programmable Device Operation:

- Burst Type: Sequential or Interleave

- Device CAS# Latency: 6,7,8,9

- Burst Length: switch on-the-fly: BL=8 or BC 4

• RoHS Compliant *(Section 11)*

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## 2. Ordering Information

| DDR3 W/T ECC SODIMM | | | | | | |
|---|---|---|---|---|---|---|
| Part Number | Density | Speed | DIMM Organization | Number of DRAM | Number of rank | ECC |
| M3D0-8GSS65N9 | 8GB | PC3-10600 | 1Gx72 | 18 | 2 | Y |

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## 3. Pin Configurations (Front side/Back side)

X72 SODIMM

| Front | | | | | | Back | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name | Pin | Name |
| 1 | VREFDQ | 69 | CB0 | 137 | VSS | 2 | VSS | 70 | VSS | 138 | VSS |
| 3 | VSS | 71 | CB1 | 139 | /DQS4 | 4 | DQ4 | 72 | CB4 | 140 | DM4 |
| 5 | DQ0 | 73 | VSS | 141 | DQS4 | 6 | DQ5 | 74 | CB5 | 142 | DQ38 |
| 7 | DQ1 | 75 | /DQS8 | 143 | VSS | 8 | VSS | 76 | DM8 | 144 | DQ39 |
| 9 | VSS | 77 | DQS8 | 145 | DQ34 | 10 | /DQS0 | 78 | VSS | 146 | VSS |
| 11 | DM0 | 79 | VSS | 147 | DQ35 | 12 | DQS0 | 80 | CB6 | 148 | DQ44 |
| 13 | DQ2 | 81 | CB2 | 149 | VSS | 14 | VSS | 82 | CB7 | 150 | DQ45 |
| 15 | DQ3 | 83 | CB3 | 151 | DQ40 | 16 | DQ6 | 84 | VREFCA | 152 | VSS |
| 17 | VSS | 85 | VDD | 153 | DQ41 | 18 | DQ7 | 86 | VDD | 154 | /DQS5 |
| 19 | DQ8 | 87 | CKE0 | 155 | VSS | 20 | VSS | 88 | A15 | 156 | DQS5 |
| 21 | DQ9 | 89 | CKE1 | 157 | DM5 | 22 | DQ12 | 90 | A14 | 158 | VSS |
| 23 | VSS | 91 | BA2 | 159 | DQ42 | 24 | DQ13 | 92 | A9 | 160 | DQ46 |
| 25 | /DQS1 | 93 | VDD | 161 | DQ43 | 26 | VSS | 94 | VDD | 162 | DQ47 |
| 27 | DQS1 | 95 | A12, /BC | 163 | VSS | 28 | DM1 | 96 | A11 | 164 | VSS |
| 29 | VSS | 97 | A8 | 165 | DQ48 | 30 | /RESET | 98 | A7 | 166 | DQ52 |
| 31 | DQ10 | 99 | A5 | 167 | DQ49 | 32 | VSS | 100 | A6 | 168 | DQ53 |
| 33 | DQ11 | 101 | VDD | 169 | VSS | 34 | DQ14 | 102 | VDD | 170 | VSS |
| 35 | VSS | 103 | A3 | 171 | /DQS6 | 36 | DQ15 | 104 | A4 | 172 | DM6 |
| 37 | DQ16 | 105 | A1 | 173 | DQS6 | 38 | VSS | 106 | A2 | 174 | DQ54 |
| 39 | DQ17 | 107 | A0 | 175 | VSS | 40 | DQ20 | 108 | BA1 | 176 | DQ55 |
| 41 | VSS | 109 | VDD | 177 | DQ50 | 42 | DQ21 | 110 | VDD | 178 | VSS |
| 43 | /DQS2 | 111 | CK0 | 179 | DQ51 | 44 | DM2 | 112 | Par_In, NC, CK1 | 180 | DQ60 |
| 45 | DQS2 | 113 | /CK0 | 181 | VSS | 46 | VSS | 114 | Err_out, NC, /CK1 | 182 | DQ61 |
| 47 | VSS | 115 | VDD | 183 | DQ56 | 48 | DQ22 | 116 | VDD | 184 | VSS |
| 49 | DQ18 | 117 | A10, AP | 185 | DQ57 | 50 | DQ23 | 118 | /S3 | 186 | /DQS7 |
| 51 | DQ19 | 119 | BA0 | 187 | VSS | 52 | VSS | 120 | /S2 | 188 | DQS7 |
| 53 | VSS | 121 | /WE | 189 | DM7 | 54 | DQ28 | 122 | /RAS | 190 | VSS |
| 55 | DQ24 | 123 | VDD | 191 | DQ58 | 56 | DQ29 | 124 | VDD | 192 | DQ62 |
| 57 | DQ25 | 125 | /CAS | 193 | DQ59 | 58 | VSS | 126 | ODT0 | 194 | DQ63 |
| 59 | DM3 | 127 | /S0 | 195 | VSS | 60 | /DQS3 | 128 | ODT1 | 196 | VSS |
| 61 | VSS | 129 | /S1 | 197 | SA0 | 62 | DQS3 | 130 | A13 | 198 | /EVENT |
| 63 | DQ26 | 131 | VDD | 199 | VDDSPD | 64 | VSS | 132 | VDD | 200 | SDA |
| 65 | DQ27 | 133 | DQ32 | 201 | SA1 | 66 | DQ30 | 134 | DQ36 | 202 | SCL |
| 67 | VSS | 135 | DQ33 | 203 | VTT | 68 | DQ31 | 136 | DQ37 | 204 | VTT |

* This address might be connected to NC balls of the DRAMs (depending on density); either way they will be connected to the termination resistor.

## 4. Architecture

Pin Definition

| Pin Name | Description | Number | Pin Name | Description | Number |
|---|---|---|---|---|---|
| CK0 | Clock Inputs, positive line | 1 | ODT[1:0] | On-die termination control | 2 |
| /CK0 | Clock inputs, negative line | 1 | DQ[63:0] | Data Input/Output | 64 |
| CK1 | Clock Inputs, positive line | 1 | CB[7:0] | Data check bits Input/Output | 8 |
| /CK1 | Clock inputs, negative line | 1 | DQS[8:0] | Data strobes | 9 |
| CKE[1:0] | Clock Enables | 2 | /DQS[8:0] | Data strobes, negative line | 9 |
| /RAS | Row Address Strobe | 1 | DM[8:0] | Data Masks / Data strobes, Termination data strobes | 9 |
| /CAS | Column Address Strobe | 1 | | | |
| /WE | Write Enable | 1 | | | |
| /S[3:0] | Chip Selects | 4 | /EVENT | Reserved for optional hardware temperature sensing | 1 |
| A[9:0],A11, A[15:13] | Address Inputs | 14 | | | |
| A10,AP | Address Input/Autoprecharge | 1 | /RESET | Register and SDRAM control pin | 1 |
| A12,/BC | Address Input/Burst chop | 1 | $V_{DD}$ | Power Supply | xx |
| BA[2:0] | SDRAM Bank Address | 3 | $V_{SS}$ | Ground | xx |
| SCL | Serial Presence Detect (SPD) Clock Input | 1 | $V_{REFDQ}$ | Reference Voltage for DQ | 1 |
| SDA | SPD Data Input/Output | 1 | $V_{REFCA}$ | Reference Voltage for CA | 1 |
| SA[1:0] | SPD Address Inputs | 2 | $V_{TT}$ | Termination voltage | 2 |
| Par_In | Parity bit for the Address and Control bus | 1 | $V_{DDSPD}$ | SPD Power | 1 |
| /Err_Out | Parity error found on the Address and Control bus | 1 | Total: | | 204 |

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## 5. Function Block Diagram:

- (8GB, 2 Ranks, 512Mx8 DDR3 SDRAMs)
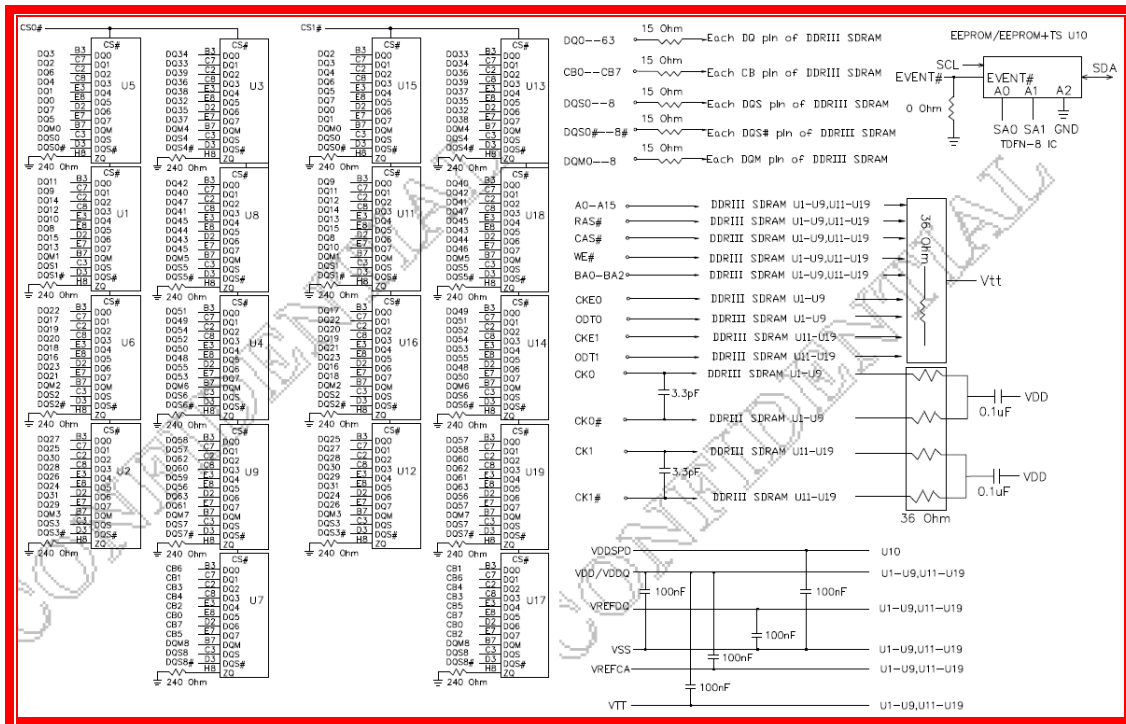
## 6. SDRAM Absolute Maximum Ratings

| Symbol | Parameter | | Rating | Units | Note |
|---|---|---|---|---|---|
| T$_{OPER}$ | Operation Temperature | Operating Temp. | -40 to 85 | °C | 1,2 |
| | | Extended Temp. | 85 to 95 | °C | 1,3 |
| T$_{STG}$ | Storage Temperature | | -55 to 100 | °C | 4,5 |
| V$_{IN}$, V$_{OUT}$ | Voltage on any pins relative to Vss | | -0.4 to +1.8 | V | 4 |
| V$_{DD}$ | Voltage on VDD supply relative to Vss | | -0.4 to +1.8 | V | 4,6 |
| V$_{DDQ}$ | Voltage on VDDQ supply relative to Vss | | -0.4 to +1.8 | V | 4,6 |

**Note**:

1. Operating Temperature TOPER is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Industrial Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between -40 to 85 °C under all operating conditions.

3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:

a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.

b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.

4. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

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## 7. DRAM AC & DC Operating

| Symbol | Parameter | Min | Typ. | Max | Units | Notes |
|---|---|---|---|---|---|---|
| **Recommended DC Operating Conditions** | | | | | | |
| **Recommended DC Operating Conditions - DDR3 (1.5V) operation** | | | | | | |
| V$_{DD}$ | Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1,2 |
| VDDSPD | Supply Voltage | 3 | 3.3 | 3.6 | V | |
| V$_{DDQ}$ | Supply Voltage | 1.425 | 1.5 | 1.575 | V | 1,2 |
| **Single Ended AC/DC Input Levels** | | | | | | |
| V$_{IH (DC) }$ DDR3 | DC Input High (Logic1) Voltage | VREF + 100 | | V$_{DD}$ | V | 3 |
| V$_{IL (DC) }$ DDR3 | DC Input Low (Logic 0) Voltage | VSS | | VREF - 100 | V | 3 |
| V$_{IH (AC) }$ DDR3 | AC Input High (Logic1) Voltage | VREF+ 150 | | | V | 3 |
| V$_{IL (AC) }$ DDR3 | AC Input Low (Logic 0) Voltage | | | VREF - 150 | V | 3 |
| V$_{REFDQ (DC)}$ | Reference Voltage for DQ, DM inputs | 0.49VDDQ | 0.5VDDQ | 0.51VDDQ | V | 4,5 |
| V$_{REFCA (DC)}$ | Reference Voltage for ADD,CMD inputs | 0.49VDDQ | 0.5VDDQ | 0.51VDDQ | V | 4,5 |
| **Single Ended AC/DC Output Levels** | | | | | | |
| V$_{OH (DC)}$ | DC output high measurement level (for IV curve linearity) | - | 0.8 x VDDQ | - | V | |
| V$_{OM (DC)}$ | DC output mid measurement level (for IV curve linearity) | - | 0.5 x VDDQ | - | V | |
| V$_{OL (DC)}$ | DC output low measurement level (for IV curve linearity) | - | 0.2 x VDDQ | - | V | |
| V$_{OH (AC)}$ | AC output high measurement level (for output SR) | - | VTT + 0.1 x VDDQ | - | V | 6 |
| V$_{OL (AC)}$ | AC output low measurement level (for output SR) | | VTT - 0.1 x VDDQ | - | V | 6 |

| Symbol | Parameter | Min | Typ. | Max | Units | Notes |
|---|---|---|---|---|---|---|
| **Differential AC/DC Input Levels** | | | | | | |
| V$_{IHdiff}$ DDR3 | Differential Input high | +0.2 | | Note 9 | V | 7 |
| V$_{ILdiff}$ DDR3 | Differential Input logic Low | Note 9 | - | -0.2 | V | 7 |

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| VIHdiff(ac) DDR3 | Differential Input high ac | 2* (VIH (AC)- VREF) | - | Note 9 | V | 8 |
|---|---|---|---|---|---|---|
| VILdiff(ac) DDR3 | Differential Input logic Low ac | Note 9 | - | 2* (VREF- VIL (AC)) | V | 8 |
| **Differential AC and DC Output Levels** | | | | | | |
| VOHdiff(AC) | AC differential output high measurement level (for output SR) | - | + 0.2 x VDDQ | - | V | 10 |
| VOLdiff(AC) | AC differential output low measurement level (for output SR) | - | - 0.2 x VDDQ | - | V | 10 |

**Note:**

1. Under all conditions VDDQ must be less than or equal to VDD.

2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.

3. For DQ and DM, Vref = VrefDQ. For input ony pins except RESET#, Vref = VrefCA.

4. Recommended DC Operating Conditions - DDR3 (1.5V) operation : The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV); Recommended DC Operating Conditions - DDR3L (1.35V) operation: The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 13.5 mV)

5. For reference: approx. VDD/2.

6. The swing of ± 0.1 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 $\Omega$ and an effective test load of 25 $\Omega$ to VTT = VDDQ/2

7. Used to define a differential signal slew-rate.

8. For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU , DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.

9. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.

10. The swing of ± 0.2 × VDDQ is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 $\Omega$ and an effective test load of 25 $\Omega$ to VTT = VDDQ/2 at each of the differential outputs.

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## 8. Operating, Standby, and Refresh Currents

- 8GB ECC SODIMM (2 Rank, 512Mx8 DDR3 SDRAMs)

| Symbol | Parameter/Condition | | PC3-10600 | Unit |
|--------|---------------------|---|-----------|------|
| I DD0 | One bank; Active - Precharge | | 522 | mA |
| I DD1 | One bank; Active - Read - Precharge | | 720 | mA |
| I DD2N | Precharge Standby Current | | 234 | mA |
| IDD2NT | Precharge Standby ODT Current | | 270 | mA |
| I DD2P | Precharge Power Down Current | Fast Mode | 198 | mA |
| | Precharge Power Down Current | Slow Mode | 198 | mA |
| I DD2Q | Pecharge Quiet Standby Current | | 216 | mA |
| I DD3N | Active Standby Current | | 414 | mA |
| I DD3P | Active Power-Down Current | | 198 | mA |
| I DD4R | Operating Current Burst Read | | 1278 | mA |
| I DD4W | Operating Current Burst Write | | 1278 | mA |
| I DD5B | Burst Refresh Current | | 3600 | mA |
| I DD6 | Self-Refresh Current: Normal Temperature Range | | 270 | mA |
| I DD7 | Operating Bank Interleave Read Current | | 2340 | mA |
| I DD8 | RESET Low Current | | 270 | mA |

Reference only, the actual will be lower than it.

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## 9. Timing Parameters

| Symbol | Parameter | PC3-10600 | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| **Clock Timing** | | | | |
| tCK (DLL-Off) | Minimum Clock Cycle Time | 8 | - | ns |
| tCK (avg) | Average Clock Period | 1.5 | <1.875 | ns |
| tCH (avg) | Average high pulse width | 0.47 | 0.53 | tCK (avg) |
| tCL (avg) | Average low pulse width | 0.47 | 0.53 | tCK (avg) |
| tCK (abs) | Absolute Clock Period | tCK(avg) min + tJIT(per) min | tCK(avg) max + tJIT(per) max - | Ps |
| tCH (abs) | Absolute high pulse width | 0.43 | - | tCK (avg) |
| tCL (abs) | Absolute low pulse width | 0.43 | - | tCK (avg) |
| JIT (per) | Clock Period Jitter | -80 | 80 | Ps |
| TJIT (per, lck) | Clock Period Jitter during DLL locking period. | -70 | 70 | Ps |
| JIT (CC) | Cycle to Cycle Period Jitter | 160 | | Ps |
| TJIT (CC, lck) | Cycle to Cycle Period Jitter during DLL locking period. | 140 | | Ps |
| TERR (2per) | Cumulative error across 2 cycle | -118 | 118 | Ps |
| TERR (3per) | Cumulative error across 3 cycle | -140 | 140 | Ps |
| TERR (4per) | Cumulative error across 4 cycle | -155 | 155 | Ps |
| TERR (5per) | Cumulative error across 5 cycle | -168 | 168 | Ps |
| TERR (6per) | Cumulative error across 6 cycle | -177 | 177 | Ps |
| TERR (7per) | Cumulative error across 7 cycle | -186 | 186 | Ps |
| TERR (8per) | Cumulative error across 3 cycle | -193 | 193 | Ps |
| TERR (9per) | Cumulative error across 4 cycle | -200 | 200 | Ps |
| TERR (10per) | Cumulative error across 5 cycle | -205 | 205 | Ps |
| TERR (11per) | Cumulative error across 6 cycle | -210 | 210 | Ps |
| TERR (12per) | Cumulative error across 7 cycle | -215 | 215 | Ps |

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| | | tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max | | |
|---|---|---|---|---|
| TERR (nper) | Cumulative error across 13~50 cycle | | | Ps |

**Data Timing**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tDQSQ | DQS, DQS# to DQ skew, per group, per access | - | 125 | Ps |
| tQH | DQ output hold time from DQS, DQS# | 0.38 | - | tCK(avg) |
| tLZ (DQ) | DQ low-impedance time from CK, CK# | -500 | 250 | Ps |
| tHZ(DQ) | DQ high impedance time from CK, CK# | - | 250 | Ps |

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| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tDS(base) AC160 | | - | - | Ps |
| tDS(base) AC135 | Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | 45 | - | Ps |
| tDS(base) AC125 | | - | - | Ps |
| tDH(base) DC90 | Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels | 75 | - | Ps |

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| tDS(base) AC175 | | - | - | Ps |
| tDS(base) AC150 | Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels | 30 | - | Ps |
| tDS(base) AC135 | | - | - | Ps |
| tDH(base) DC100 | Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels | 65 | - | Ps |

**Data Strobe Timing**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tRPRE | DQS,DQS# differential READ Preamble | 0.9 | | tCK(avg) |
| tRPST | DQS, DQS# differential READ Postamble | 0.3 | | tCK(avg) |

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| tQSH | DQS, DQS# differential output high time | 0.4 | | tCK(avg) |
|---|---|---|---|---|
| tQSL | DQS, DQS# differential output low time | 0.4 | | tCK(avg) |
| tWPRE | DQS, DQS# differential WRITE Preamble | 0.9 | | tCK(avg) |
| tWPST | DQS, DQS# differential WRITE Postamble | 0.3 | | tCK(avg) |
| tDQSCK | DQS, DQS# rising edge output access time from rising CK, CK# | -225 | 225 | Ps |
| tLZ(DQS) | DQS and DQS# low-impedance time (Referenced from RL - 1) | -500 | 250 | Ps |
| tHZ(DQS) | DQS and DQS# high-impedance time (Referenced from RL + BL/2) | - | 250 | Ps |
| tDQSL | DQS, DQS# differential input low pulse width | 0.45 | 0.55 | tCK(avg) |
| tDQSH | DQS, DQS# differential input high pulse width | 0.45 | 0.55 | tCK(avg) |
| tDQSS | DQS, DQS# rising edge to CK, CK# rising edge | -0.25 | 0.25 | tCK(avg) |
| tDSS | DQS, DQS# falling edge setup time to CK, CK# rising edge | 0.2 | - | tCK(avg) |
| tDSH | DQS, DQS# falling edge hold time from CK, CK# rising edge | 0.2 | - | tCK(avg) |

**Command and Address Timing**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| tDLLK | DLL locking time | 512 | - | nCK |
| tRTP | Internal READ Command to PRECHARGE Command delay | max(4nCK, 7.5ns) | - | |
| tWTR | Delay from start of internal write transaction to Internal read command | max(4nCK, 7.5ns) | - | |
| tWR | WRITE recovery time | 15 | - | ns |
| tMRD | Mode Register Set command cycle time | 4 | - | nCK |
| tMOD | Mode Register Set command update delay | max(12nCK, 15ns) | - | |
| tRCD | Refer to Section 1 Feature | | | |
| tRP | Refer to Section 1 Feature | | | |
| tRC | Refer to Section 1 Feature | | | |

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| | | | | |
|---|---|---|---|---|
| tCCD | | 4 | - | nCK |
| tDAL (min) | Auto precharge write recovery + precharge time | WR + roundup(tRP / tCK(avg)) | | nCK |
| tMPRR | Multi-Purpose Register Recovery Time | 1 | - | nCK |
| tRAS | ACTIVE to PRECHARGE command period | 36 | 9 tREFI | ns |
| tRRD | ACTIVE to ACTIVE command period for 1KB page size | max(4nCK, 6ns) | - | |
| tRRD | ACTIVE to ACTIVE command period for 2KB page size | max(4nCK, 7.5ns) | - | |
| tFAW | Four activate window for 1KB page size | 30 | - | ns |
| tFAW | Four activate window for 2KB page size | 45 | - | ns |
| **1.35V** | | | | |
| tIS(base) AC160 | | 80 | - | Ps |
| tIS(base) AC135 | Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels | 205 | - | Ps |
| tIS(base) AC125 | | - | - | Ps |
| tIH(base) DC90 | Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels | 150 | - | Ps |
| **1.5V** | | | | |
| tIS(base) AC175 | | 65 | - | Ps |
| tIS(base) AC150 | Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels | 190 | - | Ps |
| tIS(base) AC135 | | - | - | Ps |
| tIS(base) AC125 | | - | - | Ps |
| tIH(base) DC100 | Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels | 140 | - | Ps |
| **Calibration Timing** | | | | |

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| Symbol | Parameter | Min. | Max. | Unit |
|--------|-----------|------|------|------|
| tZQinit | Power-up and RESET calibration time | 512 | - | nCK |
| tZQoper | Normal operation Full calibration time | 256 | - | nCK |
| tZQCS | Normal operation Short calibration time | 64 | - | nCK |

**Reset Timing**

| Symbol | Parameter | Min. | Max. | Unit |
|--------|-----------|------|------|------|
| tXPR | Exit Reset from CKE HIGH to a valid command | max(5nCK,tRFC +10ns) | - | |

**Self Refresh Timings**

| Symbol | Parameter | Min. | Max. | Unit |
|--------|-----------|------|------|------|
| tXS | Exit Self Refresh to commands not requiring a locked DLL | Max(5nCK), tRFC+10ns) | | |
| tXSDLL | Exit Self Refresh to commands requiring a locked DLL. | tDLL(min) | - | nCK |
| tCKESR | Minimum CKE low width for Self Refresh entry to exit timing. | tCKE9min)+ 1tCK | - | |
| tCKSRE | Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE) | Max(5nCK, 10ns) | - | |
| tCKSRX | Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit | Max(5nCK, 10ns) | - | |

**Power Down Timings**

| Symbol | Parameter | Min. | Max. | Unit |
|--------|-----------|------|------|------|
| tXP | Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL | max(3nCK, 6ns) | - | |
| tXPDLL | Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL | max(10nCK, 24ns) | - | |

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| | | | | |
|---|---|---|---|---|
| tCKE | CKE minimum pulse width | max(3nCK,5.625ns) | - | |
| tCPDED | Command pass disable delay | 1 | - | nCK |
| tPD | Power Down Entry to Exit Timing | tCKE(min) | 9*tREFI | |
| tACTPDEN | Timing of ACT command to Power Down entry | 1 | - | nCK |
| tPRPDEN | Timing of PRE or PREA command to Power Down entry | 1 | - | nCK |
| tRDPDEN | Timing of RD/RDA command to Power Down entry | RL+4+1 | - | nCK |
| tWRPDEN | Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | WL + 4 + (tWR / tCK(avg) ) | - | nCK |
| tWRAPDEN | Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF) | WL + 4 + WR + 1 | - | nCK |
| tWRPDEN | Timing of WR command to Power Down entry (BC4MRS) | WL + 2 + (tWR / tCK(avg) ) | - | nCK |
| tWRAPDEN | Timing of WRA command to Power Down entry (BC4MRS) | WL + 2 + WR + 1 | - | nCK |
| tREFPDEN | Timing of REF command to Power Down entry | 1 | - | nCK |
| tMRSPDEN | Timing of MRS command to Power Down entry | tMOD(min) | - | nCK |
| **ODT Timings** | | | | |
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Unit** |
| ODTH4 | ODT high time without write command or with write command and BC4 | 4 | - | nCK |
| ODTH8 | ODT high time with Write command and BL8 | 6 | - | nCK |
| tAONPD | Asynchronous RTT turn-on delay (Powe-Down with DLL frozen) | 2 | 8.5 | ns |
| tAOFPD | Asynchronous RTT turn-off delay (Power-Down with DLL frozen) | 2 | 8.5 | ns |

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| | | | | |
|---|---|---|---|---|
| tAON | RTT-turn-on | -250 | 250 | ps |
| tAOF | RTT_Nom and RTT_WR turn-off time from ODTLoff reference | 0.3 | 0.7 | tCK(avg) |
| tADC | RTT dynamic change skew | 0.3 | 0.7 | tCK(avg) |
| **Write Leveling Timing** | | | | |
| **Symbol** | **Parameter** | **Min.** | **Max.** | **Unit** |
| tWLMRD | First DQS/DQS# rising edge after write leveling mode is programmed | 40 | - | nCK |
| tWLDQSEN | DQS/DQS# delay after write leveling mode is programmed | 25 | - | nCK |
| tWLS | Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing | 195 | - | ps |
| tWLH | Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing | 195 | - | ps |
| tWLO | Write leveling output delay | 0 | 9 | ns |
| tWLOE | Write leveling output error | 0 | 2 | ns |

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## 10. PACKAGE DIMENSION

- (8GB, 2 Ranks, 512Mx8 DDR3 base ECC SODIMM)
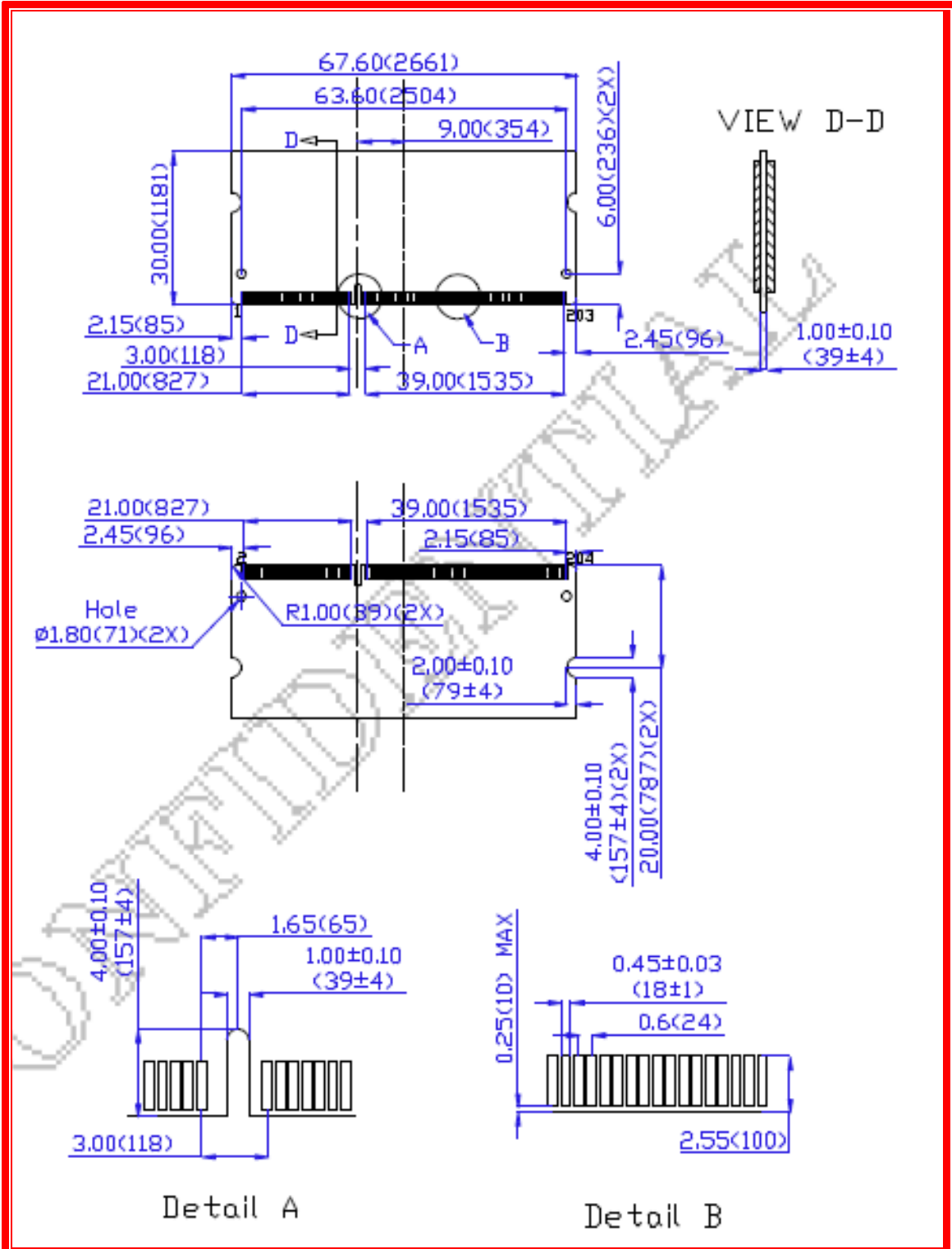


Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless

otherwise specified.

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**May 2019**

## 11. RoHS Declaration

**innodisk**

# 宜鼎國際股份有限公司
# Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

## RoHS 自我宣告書 (RoHS Declaration of Conformity)

### Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及 (EU) 2015/863 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

三、 本公司聲明我們的產品符合 RoHS 指令的附件中(7a)、(7c-I)允許豁免。
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.
 ※ (7a) Lead in high melting temperature type solders(i.e. lead-based alloys containing 85% by weight or more lead).
 ※ (7C-I) Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.

| Name of hazardous substance | Limited of RoHS    ppm（mg/kg） |
|---|---|
| 鉛（Pb） | ＜ 1000 ppm |
| 汞（Hg） | ＜ 1000 ppm |
| 鎘（Cd） | ＜ 100 ppm |
| 六價鉻（Cr 6+） | ＜ 1000 ppm |
| 多溴聯苯（PBBs） | ＜ 1000 ppm |
| 多溴二苯醚（PBDEs） | ＜ 1000 ppm |
| 鄰苯二甲酸二(2-乙基己基)酯（DEHP） | ＜ 1000 ppm |
| 鄰苯二甲酸丁酯苯甲酯（BBP） | ＜ 1000 ppm |
| 鄰苯二甲酸二丁酯（DBP） | ＜ 1000 ppm |
| 鄰苯二甲酸二異丁酯（DIBP） | ＜ 1000 ppm |

### 立 保 證 書 人　(Guarantor)

Company name 公司名稱： Innodisk Corporation　宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien　簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2018 / 07 / 01

Rev 1.0

## Revision Log

| Rev | Date | Modification |
|-----|------|--------------|
| 0.1 | 20th May 2019 | Preliminary Edition |
| 1.0 | 20th May 2019 | Official released. |