ACS-2330/2332

Intel 6th/7th Generation Core i Fanless Box PC

User Manual

Release Date	Revision
May.2018	V1.5

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Revision History

Reversion	Date	Description
1.0	2017/02/18	Official Version
1.1	2017/05/03	● Modify product image ● Remove 1xmSATA ● Modify COM port position ● Modify SSD spec. up to 32GB ● Add LAN LED light description for LAN1~4
1.2	2017/09/20	● Add IP Rating ● Modify serial port, memory, software
1.3	2017/10/11	● Serial port / OS information
1.4	2018/03/09	● Modify Operating Temperature
1.5	2018/05/04	● Add core I 7 CPU/Modify motherboard content ● Modify PCIe description

Warning!_____

This equipment generates, uses and can radiate radio frequency energy and if not installed and used in accordance with the instructions manual, it may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

Electric Shock Hazard – Do not operate the machine with its back cover removed. There are dangerous high voltages inside.

Disclaimer

This information in this document is subject to change without notice. In no event shall Aplex Technology Inc. be liable for damages of any kind, whether incidental or consequential, arising from either the use or misuse of information in this document or in any related materials.

Caution

Risk of explosion if the battery is replaced with an incorrect type.

Batteries should be recycled where possible. Disposal of used batteries must be in accordance with local environmental regulations.

Packing List

Accessories (as ticked) included in this package are:
☐ Adaptor ☐ Driver & manual CD disc ☐ Other._____(please specify)

Safety Precautions

Follow the messages below to prevent your systems from damage:

- Avoid your system from static electricity on all occasions.

- Prevent electric shock. Don‘t touch any components of this card when the card is power-on. Always disconnect power when the system is not in use.

- Disconnect power when you change any hardware devices. For instance, when you connect a jumper or install any cards, a surge of power may damage the electronic components or the whole system.

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Chapter 1 Getting Started

1.1 Features

- Intel 6th/7th Generation Skylake/Kaby Lake Intel Core i7/i5/i3 Processors
- 2 x SO-DIMM, up to 32GB
- Easy accessible storage design
- Fanless Design
- Multi-expansion slot
- Three independent display ports and support 4K UHD display
- Wide range DC 9~36V power input

1.2 Specifications

	ACS-2330	ACS-2332
System		
CPU	Socket H4,6th/ 7th Generation Intel Core-i Processor	
Chipset	Intel 100 series Chipset(H170)	
Memory	2 x 260-pin SO-DIMM up to 32GB DDR4 1866/2133 MHz	
Outside IO Port		
USB:	Front: 4 x USB 3.0 type A, Rear: 2 x USB 2.0 type A	
Serial/Parallel:	Front: 2 x RS-232, COM3/COM4 Rear: 2 x RS-232/422/485 , COM1/COM2, default RS-232	
Audio:	1 x Line-in, 1 x Line-out, 1 x Mic	
Display Interface:	1 x Display port, 1 x DVI-I, 1 x HDMI	
GPIO:	1 x 4-in/4-out digital I/O, 1-5V, 1-GND	
POWER:	1 x 3-pin DC power input terminal, 1 x power button with light	
Storage Space		
Storage	2 x 2.5” SATA3 HDD bay (Easy accessible)	
Expansion		
Expansion Slot	3 x Mini PCIe slots full size (one shared with mSATA) (Only for ACS-2332) 2 x PCIe slot via TB-554 Series: 1 x PCIe x4 or 2 x PCIe x1 slot for option	
Wireless LAN		
Wireless LAN	802.11 b/g/n via Mini-PCIe module card half size for option	

	Rear side design Antenna hole	
Power		
Power Input	DC 9~36V power input	
Power Consumption	MAX: 56.3W	MAX: 60.4W
Mechanical		
Construction	Plating Titanium Gray Aluminum Hearsink and Black Steel Chassis	
Mounting	Wall Mount	
Dimensions	277.8 x 230 x 86.7 mm	280 x 230 x 134.6 mm
Net Weight	4.5 Kg	5.5 kg
IP Rating	IP 20	
Environmental		
Operating Temperature	0~50°C / -20~60°C (option)	
Storage Temperature	-40~85°C	
Storage Humidity	10 to 90% @ 40°C, non-condensing	
Certification	CE / FCC Class A	
Operating System Support	Windows Embedded 8.1 Industry Pro, Windows Embedded 8 Standard, Windows 10 IOT 2016	

1.3 Dimensions

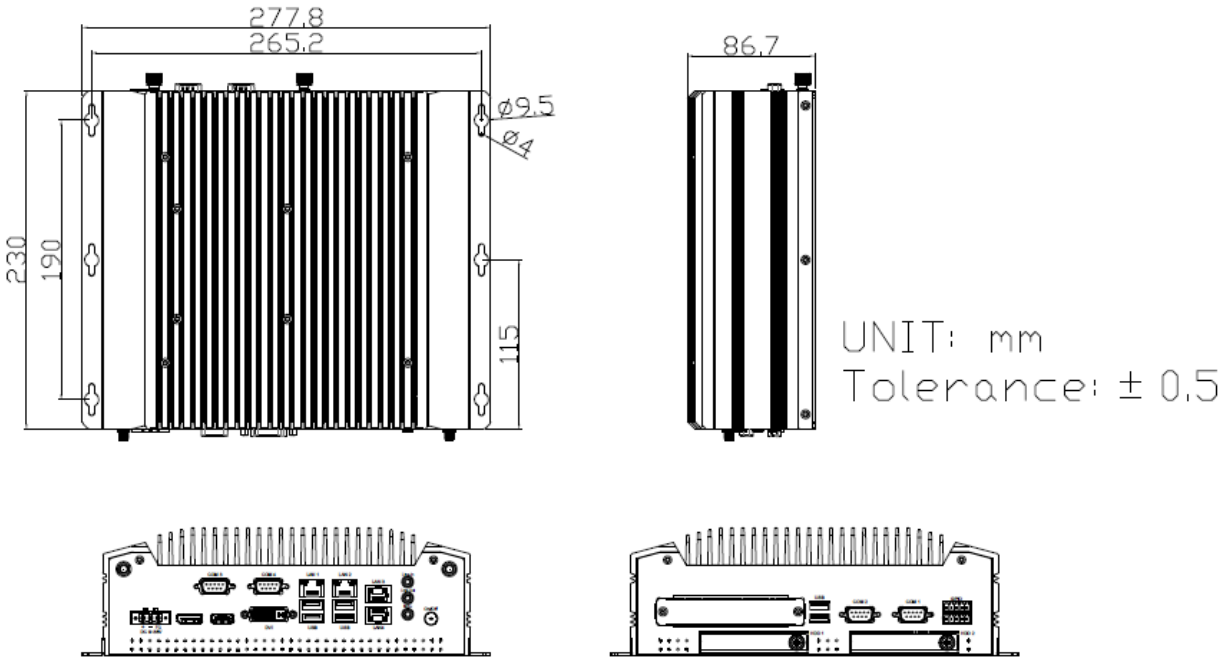


Figure 1.1: Dimensions of ACS-2330

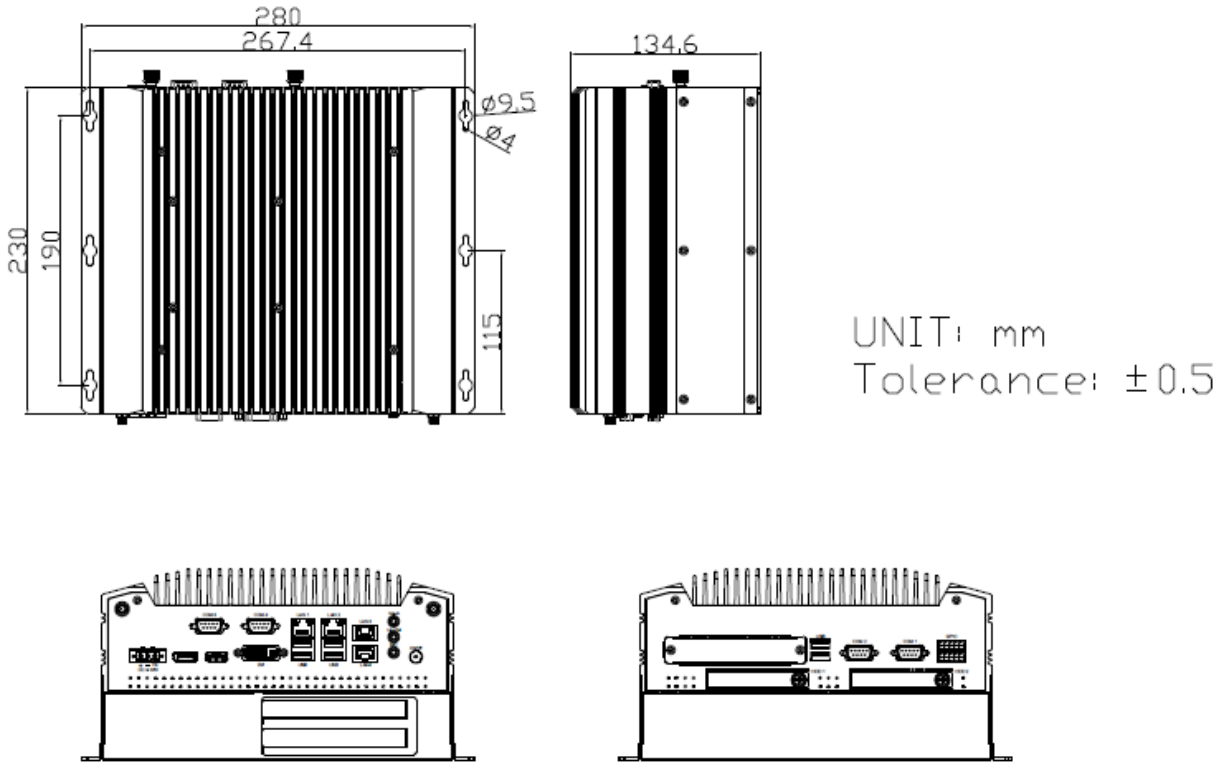


Figure 1.2: Dimensions of ACS-2332

1.4 Brief Description of ACS-2330/2332

The ACS-2330/2332 is a fanless design high-efficiency BOX PC, powered by Intel 6^{th}/7^{th} Generation Skylake/Kaby lake Core i3/i5/i7 CPU and supports 2 x SO-DIMM DDR4 slots 1866/2133 memory. It comes with 4 x USB 3.0 type A, 2 x USB 2.0 type A, 1 x Line-in, 1 x Line-out, 1 x Mic and so on. It supports 2 x 2.5" SATA3 HDD space which is easy accessible designed and wide range DC 9~36V power input. The model has 3 x Mini PCIe full size (one shared with mSATA) slots for expansion. The model is plating titanium gray aluminum heatsink and black steel chassis design, and can be wall mounted. The ACS-2330/2332 works very well along with any of our display series and it absolutely can provide an easy way to perform control and field maintenance.

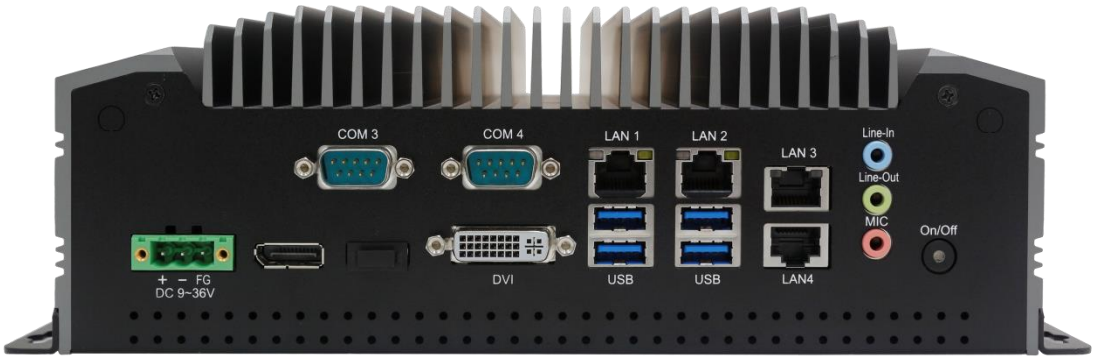


Figure 1.3: Front view of ACS-2330

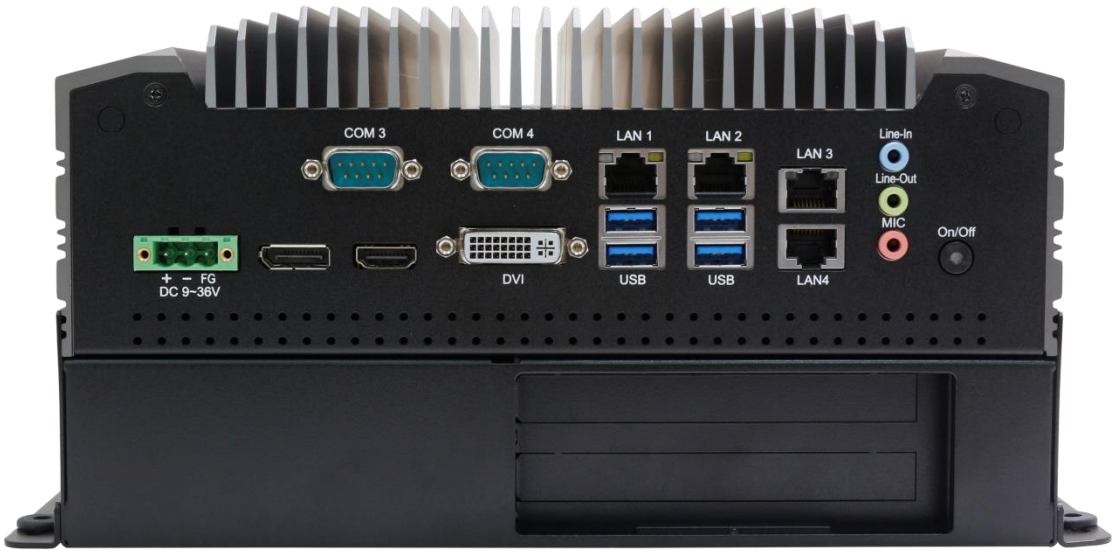


Figure 1.4: Front view of ACS-2332

Figure 1.5: I/O rear view of ACS-2330

Figure 1.6: I/O rear view of ACS-2332

Chapter 2 Hardware

2.1 Motherboard Introduction

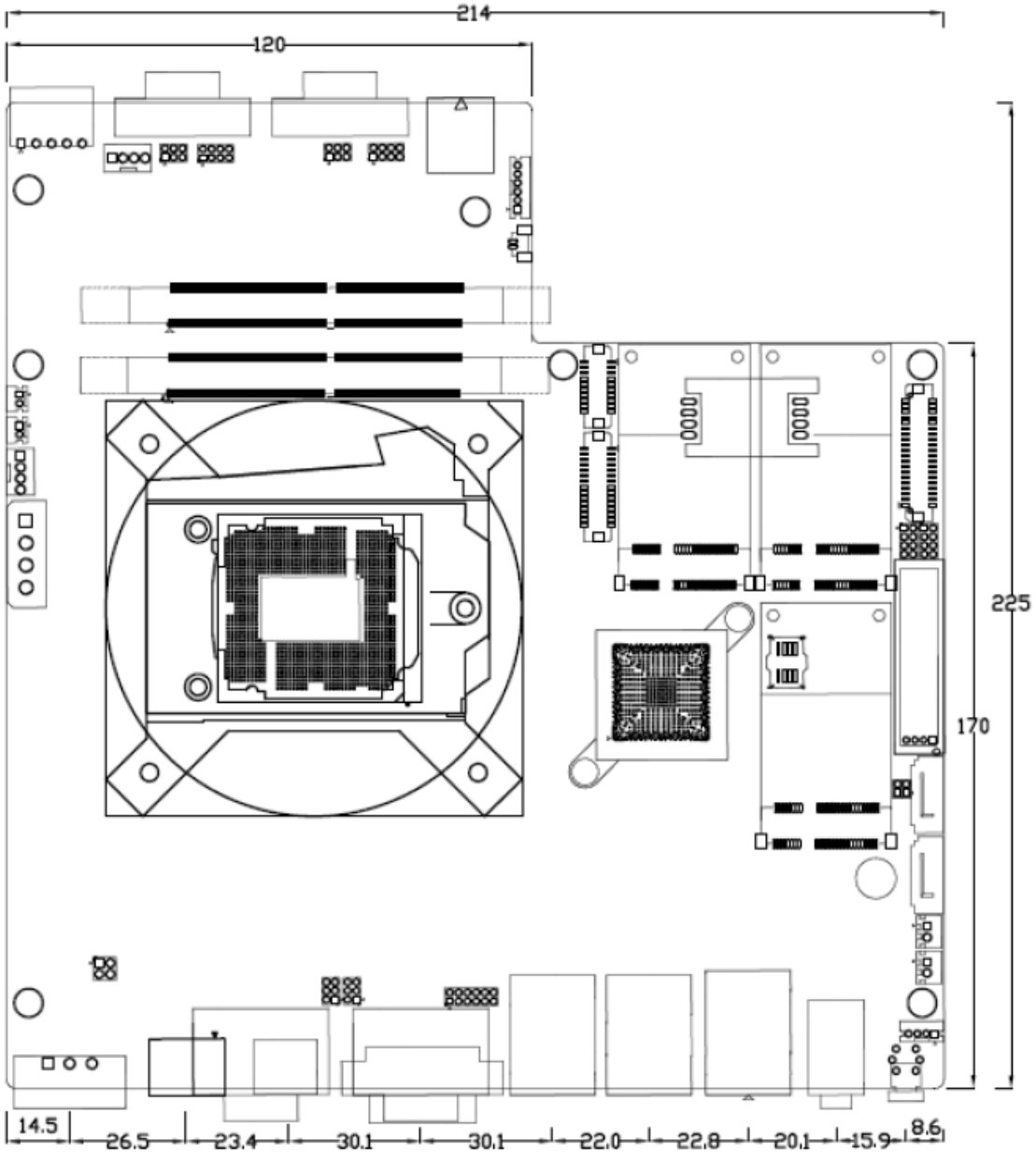
SBC-7113 is a Non-standard industrial motherboard developed on the basis of Intel H170, which provides abundant peripheral interfaces to meet the needs of different customers. Also,it features four GbE ports, 6-COM ports and two Mini PCIE configuration. To satisfy the special needs of high-end customers, ADOtec designed 80Pin PCIe x4 expansion interface. The product is widely used in various sectors of industrial control.

2.2 Specifications

Specifications	
Board Size	214mm x 225mm
CPU Support	installing the 6th Generation intel Core i3/i5/i7 6xxxTE Processors (up to 35W). - Intel Core I3-6100TE 2.70GHz 35W - Intel Core I5-6500TE 2.30 GHz (up to 3.30 GHz) 35W - Intel Core I7-6700TE 2.40 GHz (up to 3.40 GHz) 35W - Intel Pentium Processor G4400TE 2.30GHz 35W - Intel Celeron Processor G3900TE 2.30GHz 35W - Intel Core I3-7101TE 3.40GHz 35W - Intel Core I5-7500T 2.70 GHz (up to 3.30 GHz) 35W - Intel Core I7-7700T 2.90 GHz (up to 3.80 GHz) 35W - Intel Celeron Processor G3930TE 2.70GHz 35W
Chipset	Intel H170
Memory Support	2x SO-DIMM (260pins), up to 32GB DDR4 1866/2133MHz FSB
Graphics	Intel HD Graphics 530（I3-6100TE/I5-6500TE/I7-6700TE） Intel HD Graphics 510（G4400TE/G3900TE） Intel HD Graphics 630（I3-7101TE/I5-7500T/I7-7700T） Intel HD Graphics 610（G3930TE）
Display Mode	1x DVI-I interface 1x HDMI interface

	1x DP interface 1x VGA interface
Support Resolution	Up to 4096 x 2304 for HDMI Up to 4096 x 2304 for Display Port Up to 2560 x 1600 for DVI-I Up to 1920 x 1200 for VGA
Three Display	HDMI + DVI-I + DP HDMI + DVI-I +VGA（option) DVI-I + DP + VGA（option)
Super I/O	Nuvoton NCT6106D
BIOS	AMI/UEFI BIOS
Storage	2x SATA3.0 Connector (SATA1/SATA2) 1x MSATA Connector (M_SATA1)
Ethernet	4x PCIe GbE LAN by Intel 82574L
USB	4x USB 3.0/2.0 stack ports for external (USB3.0：USB3-1/USB3-2/USB3-3/USB3-4) (USB2.0：USB2-1/USB2-2/USB2-3/USB2-4) 2x USB 2.0 stack ports for external (USB_78) 3x USB 2.0 Pin header for MIO1 (USB11/USB12/USB13) 2x USB 3..0/2.0 Pin header for MIO2 (USB3.0:USB3-5/USB3-6, USB2.0:USB2-5/USB2-6) 1x USB 2.0 internal for M-PCIe1 (USB2-10) 1x USB 2.0 internal for M-PCIe2 (USB2-09) 1x USB 2.0 internal for M-SATA1 (USB2-14)
Serial	2x RS232/422/485 port, DB9 connector for external (COM1/COM2) Pin9 w/5V/12V/Ring select 2x RS232 port, DB9 connector for external (COM3/COM4) Pin9 w/5V/12V/Ring select 2x RS232/422/485 select header for internal MIO1 (COM5/COM6)
Digital I/O	8-bit digital I/O by Pin header 4-bit digital Input 4-bit digital Output
Battery	Support CR2477 Li battery by 2-pin header (1000mAh)
Audio	Support Audio via Realtek ALC269-VB HD audio codec

	Support Line-out, Line-in,MIC-in by JACK (AUDIO1) Support a stereo Class-D Speaker Amplifier with 2 watt per channel output power, by 1x4-pin header (SPK1)
Keyboard /Mouse	PS2 K/B and Mouse by 1x6Pin Wafer connector 1x PS/2 keyboard 1x PS/2 mouse
Expansion	1x PCI-express x4 extend by 4x20 pin socket (PCIE_4X) 2x mini-PCI-express slot (M-PCIE1/MPCIE2) 1x CRT 2x5 Pin Header (VGA1)
Power Management	1x 3-pin power input connector (Wide range DC+9V~36V) DC5V/12V output by 1x4 pin Connectors
Switches and LED Indicators	Power on/off switch by MIO1 and MIO2 Power LED status by MIO1 and MIO2 HDD LED status by MIO2 Reset switch by MIO1
External I/O port	4x COM Ports (COM1/COM2/COM3/COM4) 4x USB 3.0 Ports (stack) 2x USB 2.0 Ports (stack) 4x RJ45 GbE LAN Ports 1x DVI-I interface 1x HDMI interface 1x Display Port 1x Audio Ports (Mic in,Line in,Line out)
SIM	1x SIM Socket
LPT	1x LPT Port by DF13-20P (LPT1)
Temperature	Operating: -20℃ to 70℃ Storage: -40℃ to 85℃
Humidity	10% - 90%, non-condensing, operating
Power Consumption	12V/5.2A(Intel i5-6500TE 2.30 GHz Processor with 16GB DDR4/HDD)
EMI/EMS	Meet CE/FCC class A



(units :mm)

Figure 2.1: Motherboard Dimensions

2.3 Jumpers and Connectors Location

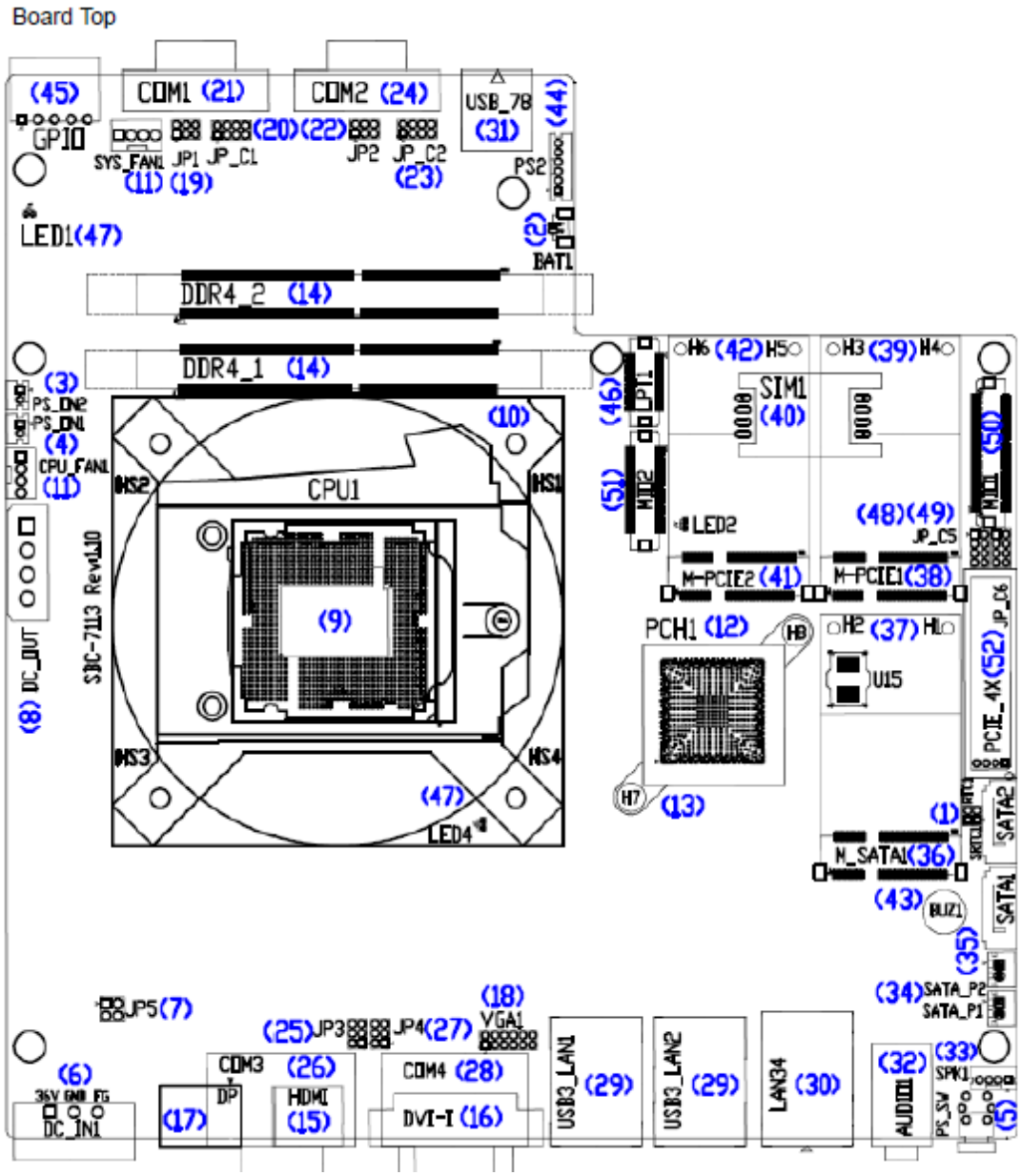


Figure 2.2: Jumpers and Connectors Location- Board Top

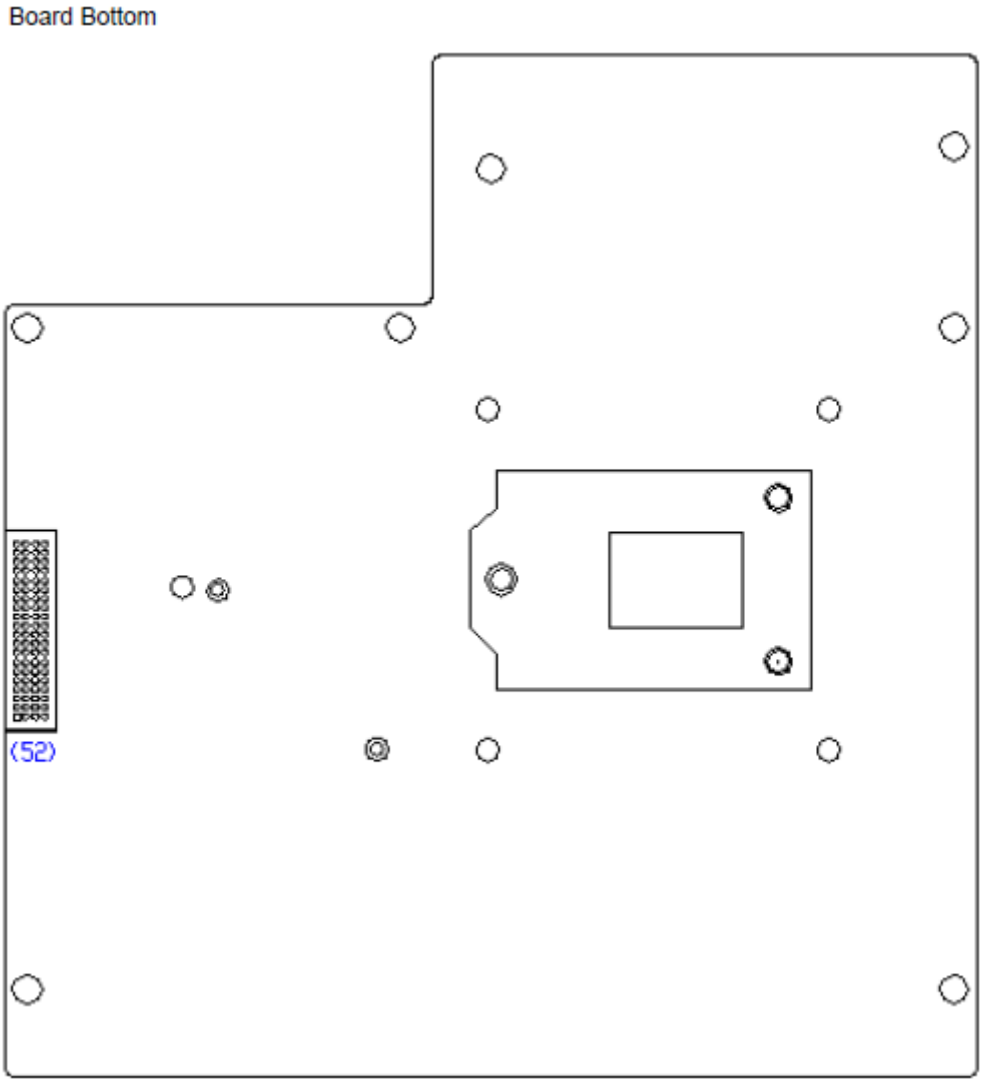
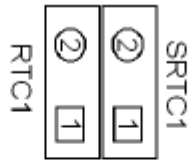


Figure 2.3: Jumpers and Connectors Location- Board Bottom

2.4 Jumpers Setting and Connectors

1. RTC1/SRTC1:

(2.0mm Pitch 1x2 Pin Header)CMOS clear jumper, CMOS clear operation will permanently reset old BIOS settings to factory defaults.



RTC1/SRTC1	CMOS
RTC1 Pin1-SRTC1 Pin1 close （or all open）	NORMAL (Default)
Close 1-2	Clear CMOS

Procedures of CMOS clear:

a) Turn off the system and unplug the power cord from the power outlet.

b) To clear the CMOS settings, use the jumper cap to close pins1 and 2 for about 3 seconds then reinstall the jumper clip back to pins open.

c) Power on the system again.

d) When entering the POST screen, press the <DEL> key to enter CMOS Setup Utility to load optimal defaults.

e) After the above operations, save changes and exit BIOS Setup.

2. BAT1 :

(1.25mm Pitch 1x2 wafer Pin Header) 3.0V Li battery is embedded to provide power for CMOS.

Pin#	Signal Name
Pin1	Ground
Pin2	VCC_RTC

3. PS_ON2:

(2.0mm Pitch 1x2 Wafer Pin Header),ATX Power and Auto Power on jumper setting.

PS_ON2	Mode
Open	**ATX Power(Default)**
Close 1-2	Auto Power on (option)

4. PS_ON1:

(2.0mm Pitch 1x2 Wafer Pin Header) ,**Power on/off**, They are used to connect power switch

button. The two pins are disconnected under normal condition. You may short them temporarily to realize system startup & shutdown or awaken the system from sleep state.

5. PS_SW:

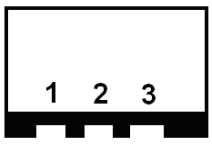
Power on/off button, They are used to connect power switch button.

Power LED Status. Green LED for Motherboard Power status.

Model	PS_ON1	PS_SW	Power LED
SBC-7113HB	●	●	●
SBC-7113HT	●	●	●

6. DC_IN1:

(5.08mm Pitch 1x3 Pin Connector),DC9V ~ DC36V System power input connector。



Pin#	Power Input（DC_IN1）
Pin1	DC+9V~36V
Pin2	Ground
Pin3	FG

DC_IN1(Power Input)	JP5
DC+9V~36V	**NC (Default)**
DC12V only（*）	Option (BOM cost down)

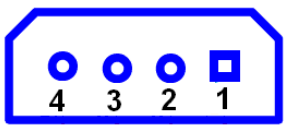
7. JP5 (option):

(2.0mm Pitch 2x2 Pin Pin Header), DC12V System only power **input** jumper setting.

【*please contact technical support】

8. DC_OUT:

(2x2 Pin Connector),DC+12V and DC+5V System power **output** connector.



Pin#	Power output
Pin1	DC+12V（DC12V_S0）
Pin2	Ground
Pin3	Ground
Pin4	DC+5V(DC5V_S0)

Note:

DC+5V Output current of the connector must not be above 0.5A.

DC+12V Output current of the connector must not be above 1A.

9. CPU1:

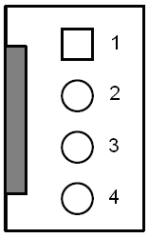
(LGA1151 Socket), installing the 6th Generation intel Core i3/i5/i7CPU Socket.

10. HS1/HS2/HS3/HS4(CPU SCREW HOLES):

CPU FAN SCREW HOLES, Four screw holes for fixed CPU Cooler assemble.

11. CPU_FAN1/SYS_FAN1:

(2.54mm Pitch 1x4 Pin Header),Fan connector, cooling fans can be connected directly for use. You may set the rotation condition of cooling fan in menu of BIOS CMOS Setup.



Pin#	Signal Name	CPU_FAN1	SYS_FAN1
1	Ground	●	●
2	VCC	●	●
3	CPU_FANTACH	●	●
4	CPU_FANPWM	o	●

Note:

Output power of cooling fan must be limited under 5W.

12. PCH1:

(BGA,Package Size:23x24mm),Intel H170 Chipset.

Model	PCH1（Chipset）
SBC-7113HB	Intel H170
SBC-7113HT	Intel H170

13. H7/H8 (option):

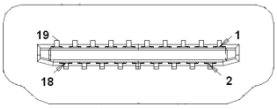
PCH1 HeatSink Screw holes.

14. DDR4_1/DDR4_2:

(SO-DIMM 260Pin socket), DDR4 memory socket, the socket is located at the top of the board and supports 260Pin 1.2V DDR4 1866/2133MHz FSB SO-DIMM memory module up to 32GB.

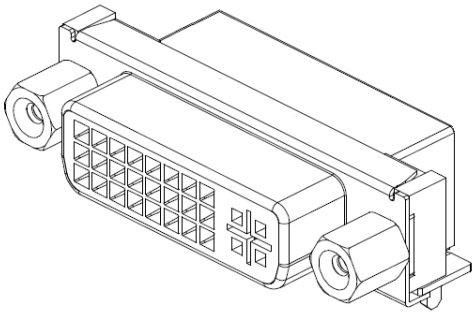
15. HDMI1:

(HDMI 19P Connector), High Definition Multimedia Interface connector.



16. DVI-I:

(DVI-I Connector), Digital Visual Interface-Integrated connector.



17. DP:

(DP Connector), Display Port Interface connector.

18. VGA1:

(CRT 2.0mm Pitch 2X6 Pin Header), Video Graphic Array Port, Provide 2x6Pin cable to VGA Port.The IT6515FN is a high-performance single-chip DisplayPort to VGA converter.

Signal Name	Pin#	Pin#	Signal Name
CRT_RED	1	2	Ground
CRT_GREEN	3	4	Ground
CRT_BLUE	5	6	CRT_SENSE
CRT_H_SYNC	7	8	CRT_DDCDATA

CRT_V_SYNC	9	10	CRT_DDCCLK
Ground	11	12	Ground

19. JP1:

(2.0mm Pitch 2x3 Pin Header),COM1 jumper setting, pin 1~6 are used to select signal out of pin 9 of COM1 port.

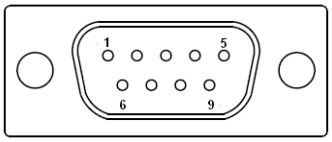
JP1 Pin#	Function
Close 1-2	**COM1 Pin9 RI (Ring Indicator) (default)**
Close 3-4	COM1 Pin9 = +5V (option)
Close 5-6	COM1 Pin9 = +12V (option)

20. JP_C1(option):

(2.0mm Pitch 2x4 Pin Header), Reserve.

21. COM1:

(Type DB9),Rear serial port, standard DB9 Male serial port is provided to make a direct connection to serial devices.



RS232 (Default):	
Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	**JP1 select Setting (RI/5V/12V)**

RS422 (option):	
Pin#	Signal Name

1	422TX-
2	422TX+
3	422RX+
4	422RX-
5	Ground
6	NC
7	NC
8	NC
9	NC

RS485 (option):	
Pin#	Signal Name
1	485-
2	485+
3	NC
4	NC
5	Ground
6	NC
7	NC
8	NC
9	NC

BIOS/Serial Port 1 Configuration/F75111 COM1 Config:
[RS-232 Mode]
[RS-485 Mode]
[RS-422 Mode]

22. JP2:

(2.0mm Pitch 2x3 Pin Header),COM2 jumper setting, pin 1~6 are used to select signal out of pin 9 of COM2 port.

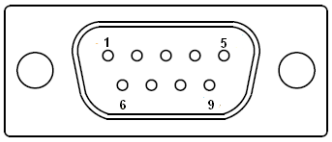
JP2 Pin#	Function	
Close 1-2	**COM2 Pin9 RI (Ring Indicator)**	**(default)**
Close 3-4	COM2 Pin9=+5V	(option)
Close 5-6	COM2 Pin9=+12V	(option)

23. JP_C2(option):

(2.0mm Pitch 2x4 Pin Header), Reserve.

24. COM2:

(Type DB9),Rear serial port, standard DB9 Male serial port is provided to make a direct connection to serial devices.



RS232 (Default):	
Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	**JP2 select Setting (RI/5V/12V)**

RS422 (option):	
Pin#	Signal Name
1	422TX-
2	422TX+
3	422RX+
4	422RX-
5	Ground
6	NC
7	NC
8	NC
9	NC

RS485 (option):	
Pin#	Signal Name
1	485-

2	485+
3	NC
4	NC
5	Ground
6	NC
7	NC
8	NC
9	NC

BIOS/Serial Port 2 Configuration/F75111 COM2 Config: **[RS-232 Mode]** [RS-485 Mode] [RS-422 Mode]

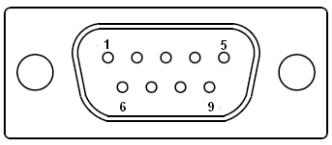
25. JP3:

(2.0mm Pitch 2x3 Pin Header),COM3 jumper setting, pin 1~6 are used to select signal out of pin 9 of COM3 port.

JP3 Pin#	Function
Close 1-2	**COM3 Pin9 RI (Ring Indicator) (default)**
Close 3-4	COM3 Pin9=+5V (option)
Close 5-6	COM32 Pin9=+12V (option)

26. COM3:

(Type DB9),Rear serial port, standard DB9 Male serial port is provided to make a direct connection to serial devices.



RS232 (Default):	
Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)

5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	**JP3 select Setting (RI/5V/12V)**

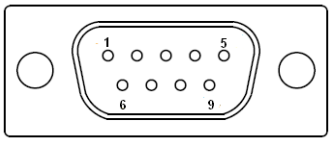
27. JP4:

(2.0mm Pitch 2x3 Pin Header),COM4 jumper setting, pin 1~6 are used to select signal out of pin 9 of COM4 port.

JP4 Pin#	Function
Close 1-2	**COM4 Pin9 RI (Ring Indicator) (default)**
Close 3-4	COM4 Pin9=+5V (option)
Close 5-6	COM4 Pin9=+12V (option)

28. COM4:

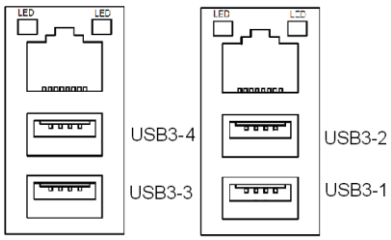
(Type DB9),Rear serial port, standard DB9 Male serial port is provided to make a direct connection to serial devices.



RS232 (Default):	
Pin#	Signal Name
1	DCD# (Data Carrier Detect)
2	RXD (Received Data)
3	TXD (Transmit Data)
4	DTR (Data Terminal Ready)
5	Ground
6	DSR (Data Set Ready)
7	RTS (Request To Send)
8	CTS (Clear To Send)
9	**JP4 select Setting (RI/5V/12V)**

29. USB3_LAN1/USB3_LAN2:

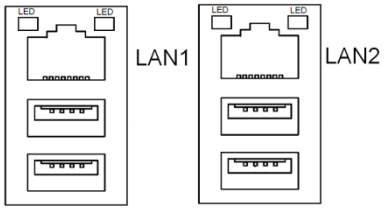
USB3-3/USB3-4/USB3-1/USB3-2：(Double stack USB typeA),Rear USB connector, it provides up to 4 USB3.0 ports,USB 3.0 allows data transfers up to 5.0Gb/s ,support USB2.0 and full-speed and low-speed signaling.



Each USB Type A Receptacle (2 Ports) Current limited value is 2.0A.

If the external USB device current exceeds 2.0A, please separate connectors into different Receptacle.

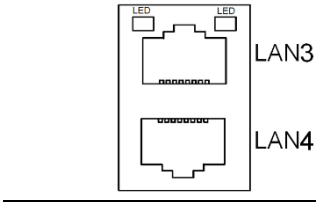
LAN1/LAN2: (RJ45 Connector), Rear LAN port, Two standard 10/100/1000M RJ-45 Ethernet ports are provided. Used Intel 82574L chipset.



LAN LED: There's no light will on while using 10/100M LAN. The green light will on while using Gbe LAN

30. LAN34:

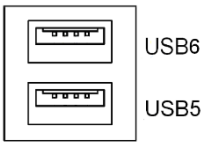
LAN3/LAN4: (RJ45 Connector), Rear LAN port, Two standard 10/100/1000M RJ-45 Ethernet ports are provided. Used Intel 82574L chipset.



LAN LED: There's no light will on while using 10/100M LAN. The green light will on while using Gbe LAN

31. USB78:

USB5/USB6：(Double stack USB type A), Rear USB connector, it provides up to 2 USB2.0 ports, High-speed USB 2.0 allows data transfers up to 480 Mb/s ,support USB full-speed and low-speed signaling.

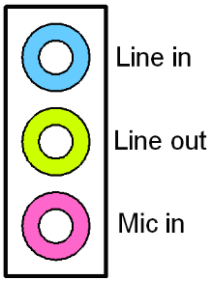


Each USB Type A Receptacle (2 Ports) Current limited value is 1.5A.

If the external USB device current exceeds 1.5A, please separate connectors into different Receptacle.

32. AUDIO1:

(Diameter 3.5mm Three stack Jack), High Definition Audio port, An onboard Realtek ALC269-VB codec is used to provide high quality audio I/O ports.



33. SPK1:

(2.0mm Pitch 1x4 Wafer Pin Header),support a stereo Class-D Speaker Amplifier with 2 watt per channel output power

Pin#	Signal Name
1	SPK_OUTL_P
2	SPK_OUTL_N
3	SPK_OUTR_N
4	SPK_OUTR_P

34. SATA_P1/SATA_P2:

(2.5mm Pitch 1x2 Wafer Pin Header), Two onboard 5V output connectors are reserved to provide power for SATA devices.

Pin#	Signal Name
1	+DC5V_S0
2	Ground

Note:

Output current of the connector must not be above 1A.

35. SATA1/SATA2:

(SATA 7P), SATA Connectors, Two SATA connectors are provided,SATA1 and SATA2 transfer speed up to 6.0Gb/s.

RAID controller supporting RAID0 or RAID1.

36. M_SATA1:

(50.95mmx30mm Socket 52Pin), mSATA socket, it is located at the top, it supports mini PCIe devices with USB2.0 and SMBUS and mSATA signal.**B2 mSATA bus** for flash disk signal.

37. H1/H2:

M_SATA1 SCREW HOLES.

H1 and H2 for mini MSATA card (50.95mmx30mm Socket 52 Pin) assemble.

38. M-PCIE1:

(Socket 52Pin),mini PCIe socket, it is located at the top, it supports mini PCIe devices with USB2.0 and SIM and SMBUS and PCIe signal. MPCIe card size is 30 x 50.95mm.

39. H3/H4:

M-PCIE1 SCREW HOLES, H3 and H4 for mini PCIE card (30mmx50.95mm) assemble.

40. SIM1:

(SIM Socket 6Pin), Support SIM Card devices.

41. M-PCIE2:

(Socket 52Pin),mini PCIe socket, it is located at the top, it supports mini PCIe devices with USB2.0 and LPC and SMBUS and PCIe signal. MPCIe card size is 30 x 50.95mm.

42. H5/H6:

M-PCIE2 SCREW HOLES, H5 and H6 for mini PCIE card (30mmx50.95mm) assemble.

43. BUZZER1:

Onboard buzzer.

44. PS2:

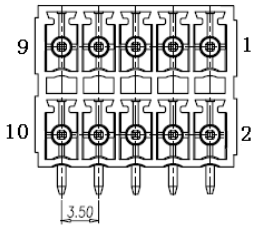
(2.0mm Pitch 1x6 Wafer Pin Header), PS/2 keyboard and mouse port, the port can be connected to PS/2 keyboard and mouse, via a dedicated cable for direct used.

Pin#	Signal Name

1	KBDATA
2	MSDATA
3	Ground
4	+5V
5	KBCLK
6	MSCLK

45. GPIO:

(3.5mm Pitch 2x5 Pin Connector),General-purpose input/output port, it provides a group of self-programming interfaces to customers for flexible use.



Signal Name	Function	Pin#		Function	Signal Name
+5V_S5	5V Power	1	2	Ground	Ground
FT_GPIO_27	GPIO_IN1	3	4	GPIO_IN2	FT_GPIO_26
FT_GPIO_25	GPIO_IN3	5	6	GPIO_IN4	FT_GPIO_24
FT_GPIO_23	GPIO_OUT1	7	8	GPIO_OUT2	FT_GPIO_22
FT_GPIO_21	GPIO_OUT3	9	10	GPIO_OUT4	FT_GPIO_20

46. LPT :

(DF13-20P Connector),For expand output connector,a standard 20 pin parallel port is provided to connect parallel peripherals as required.

Signal Name	Pin#		Signal Name
Ground	2	1	Ground
LPT_AFD-	4	3	LPT_STB-
LPT_ERR-	6	5	LPT_D0
LPT_INIT-	8	7	LPT_D1
LPT_SLIN-	10	9	LPT_D2
LPT_D4	12	11	LPT_D3
LPT_D6	14	13	LPT_D5
LPT_ACK-	16	15	LPT_D7

LPT_PE	18	17	LPT_BUSY
+5V_S0	20	19	LPT_SLCT

47. LED1/LED2/LED4:

LED1 STATUS. Green LED for Motherboard Power status.

LED2 STATUS. Green LED for Motherboard Standby Power Good status.

LED4 STATUS. Green LED for CPU Power status.

48. JP_C5(option):

(2.0mm Pitch 2x4 Pin Header), Reserve.

49. JP_C6(option):

(2.0mm Pitch 2x4 Pin Header), Reserve.

50. MIO1:

(DF13-40P Connector),For expand output connector, It provides two RS232 or RS422 or RS485 ports, three USB ports, one power led, one power button, via a dedicated cable connected to board**.**

Function	Signal Name	Pin#		Signal Name	Function
	Ground	2	1	Ground	
COM5：RS232 or 422 or 485	RXD5 422TX+ 485+	4	3	DCD5- 422TX- 485-	COM5：RS232 or 422 or 485
COM5：RS232 or 422	DTR5- 422RX-	6	5	TXD5 422RX+	COM5：RS232 or 422
COM5：RS232	DSR5-	8	7	RTS5-	COM5：RS232
COM5：RS232	CTS5-	10	9	RI5-	COM5：RS232
	Ground	12	11	Ground	
COM6：RS232 or 422 or 485	RXD6 422TX+ 485+	14	13	DCD6- 422TX- 485-	COM6：RS232 or 422 or 485
COM6：RS232 or 422	DTR6- 422RX-	16	15	TXD6 422RX+	COM6：RS232 or 422
COM6：RS232	DSR6-	18	17	RTS6-	COM6：RS232
COM6：RS232	CTS6-	20	19	RI6-	COM6：RS232
USB_5V	5V_USB1112	22	21	5V_USB1112	USB_5V

USB_5V	5V_USB1112	24	23	5V_USB1112	USB_5V
USB2.0 (USB11)	USB11_N	26	25	USB12_N	USB2.0 (USB12)
	USB11_P	28	27	USB12_P	
	Ground	30	29	Ground	
Power LED	PWRLED+	32	31	USB13_N	USB2.0 (USB13)
	PWRLED-	34	33	USB13_P	
Power Auto on	AUTO_PSON-	36	35	Ground	
Power Button	MIO_PSON-	38	37	Ground	
	Ground	40	39	FP_RESET-	Reset

BIOS/Serial Port 5 Configuration/F75111 COM5 Config:

[RS-232 Mode]

[RS-485 Mode]

[RS-422 Mode]

BIOS/Serial Port 6 Configuration/F75111 COM6 Config:

[RS-232 Mode]

[RS-485 Mode]

[RS-422 Mode]

51. MIO2:

(DF13-30P Connector),Front panel connector.

Function	Signal Name	Pin#		Signal Name	Function
USB3.0/USB2.0	5V_USB0506	2	1	5V_USB0506	USB3.0/USB2.0
	5V_USB0506	4	3	5V_USB0506	
	5V_USB0506	6	5	5V_USB0506	
	USB8_N	8	7	USB7_N	
	USB8_P	10	9	USB7_P	
	Ground	12	11	Ground	
	USB3_RX5_N	14	13	USB3_RX6_N	
	USB3_RX5_P	16	15	USB3_RX6_P	
	Ground	18	17	Ground	
	USB3_TX5_N	20	19	USB3_TX6_N	
	USB3_TX5_P	22	21	USB3_TX6_P	
HDD LED	Ground	24	23	Ground	Power LED
	HDD_LED	26	25	ALL_PWR_LED-	
Power Button	MIO_PSON-	28	27	BUZZER+	BUZZER

	Ground	30	29	BUZZER-	

Pin24-Pin26: **HDD LED**, They are used to connect hard disk activity LED. The LED blinks when the hard disk is reading or writing data.

Pin23- Pin25: **POWER LED**, They are used to connect power LED. When the system is powered on or under S0/S1 state, the LED is normally on, when the system is under S4/S5 state, the LED is off.

Pin28- Pin30: **POWER on/off Button**, They are used to connect power switch button. The two pins are disconnected under normal condition. You may short them temporarily to realize system startup & shutdown or awaken the system from sleep state.

Pin27- Pin29: **BUZZER**, They are used to connect an external buzzer.

Pin01~Pin22: **USB3-5/USB3-6/USB2-7/USB2-8**,Front USB connector,it provides two USB3.0/USB2.0 ports via a dedicated USB cable.

Each USB Type A Receptacle (2 Ports) Current limited value is 2.0A.
If the external USB device current exceeds 2.0A, please separate connectors into different Receptacle.

Note:

When connecting LEDs and buzzer and USB, pay special attention to the signal polarity. Make sure that the connector pins have a one-to-one correspondence with chassis wiring, or it may cause boot up failure.

52. PCIE_4X (option):

(4x20 Pin connector), Riser Card expansion connector. Can expand support one PCIeX4 or four PCIeX1 Signal.

SBC-7113HT：PCIE_4X connector in the top.

SBC-7113HB：PCIE_4X connector in the Bottom.

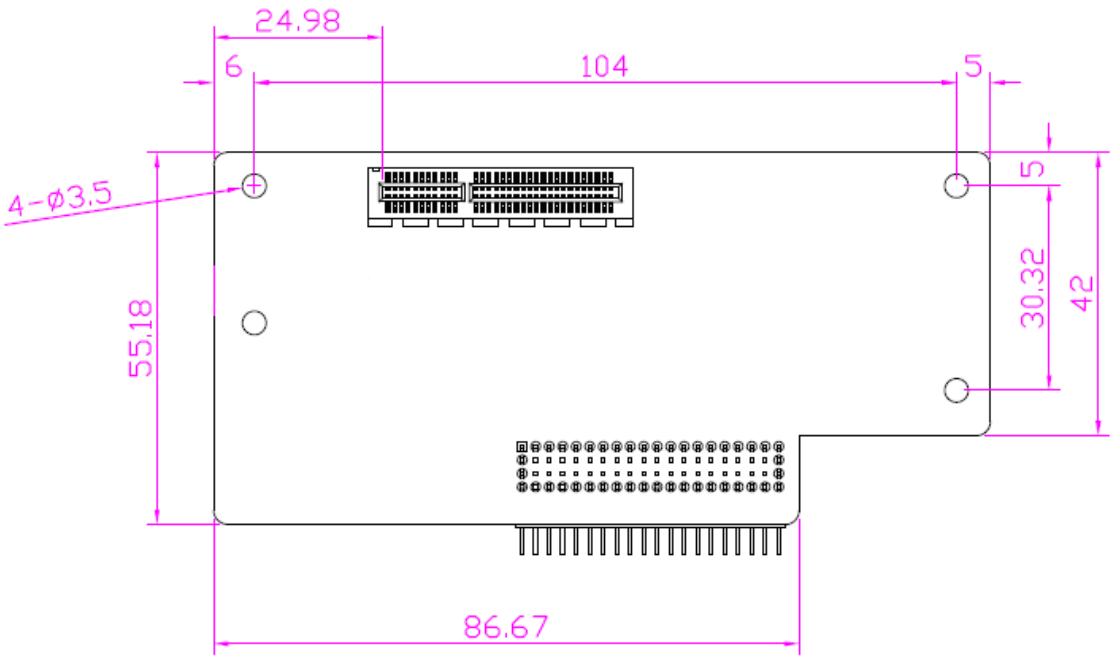
MODEL	PC1E_4X
SBC-7113HT	Top
SBC-7113HB	Bottom

Riser Card	Function	SBC-7113HB	SBC-7113HT

TB-554E41	Pcie 4x slot x1	●	X
TB-554E12	Pcie 1x slot x2	●	X
TB-526E11	Pcie 1x slot x1	●	X
TB-526E12	Pcie 1x slot x2	●	X
TB-526P1	PCI slot x1	●	X
TB-526P2	PCI slot x2	●	X
TB-525E11	Pcie 1x slot x1	X	●
TB-525E12	Pcie 1x slot x2	X	●
TB-525P1	PCI slot x1	X	●
Note: Please correctly assemble the riser card, otherwise it will burn out the motherboard! If you do not know how to assemble, please contact technical support!			

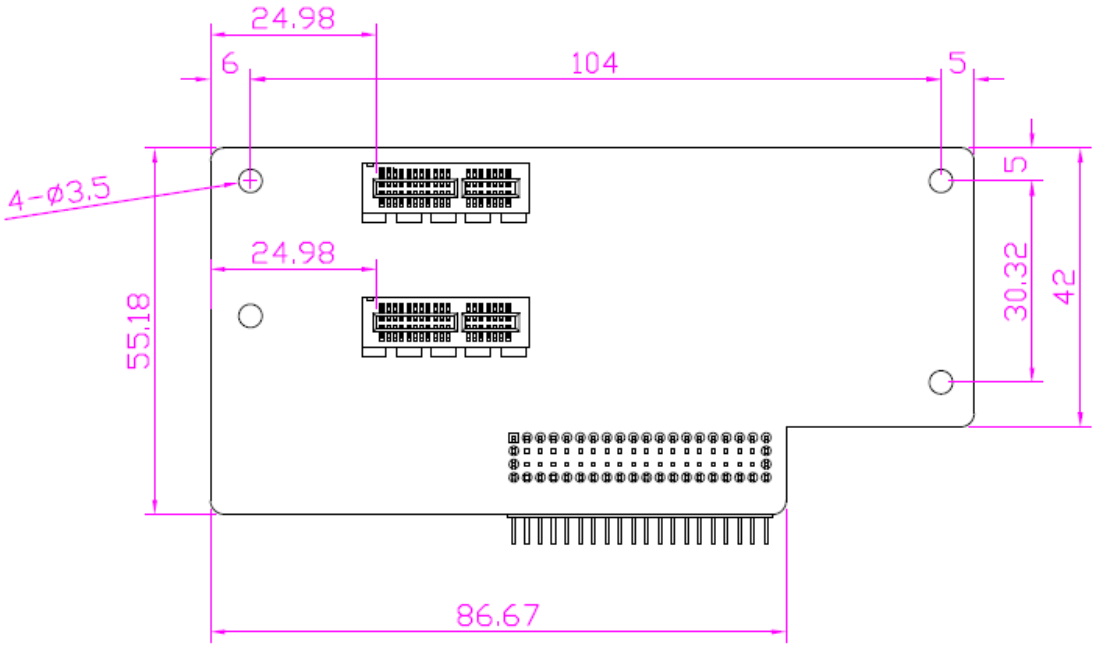
53. TB-554E41:

TB-554E41 connect to SBC-7113HB PCIE_4X connector, PCIE_4X is located at the Bottom, It provides one PCIE X4 slot.



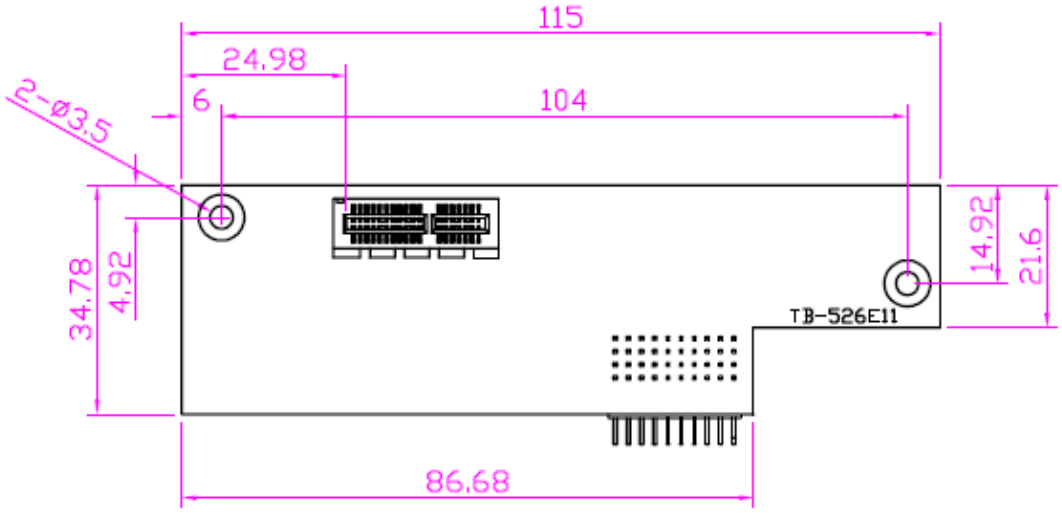
54. TB-554E12:

TB-554E12 connect to SBC-7113HB PCIE_4X connector, PCIE_4X is located at the Bottom, It provides two PCIE X1 slot.



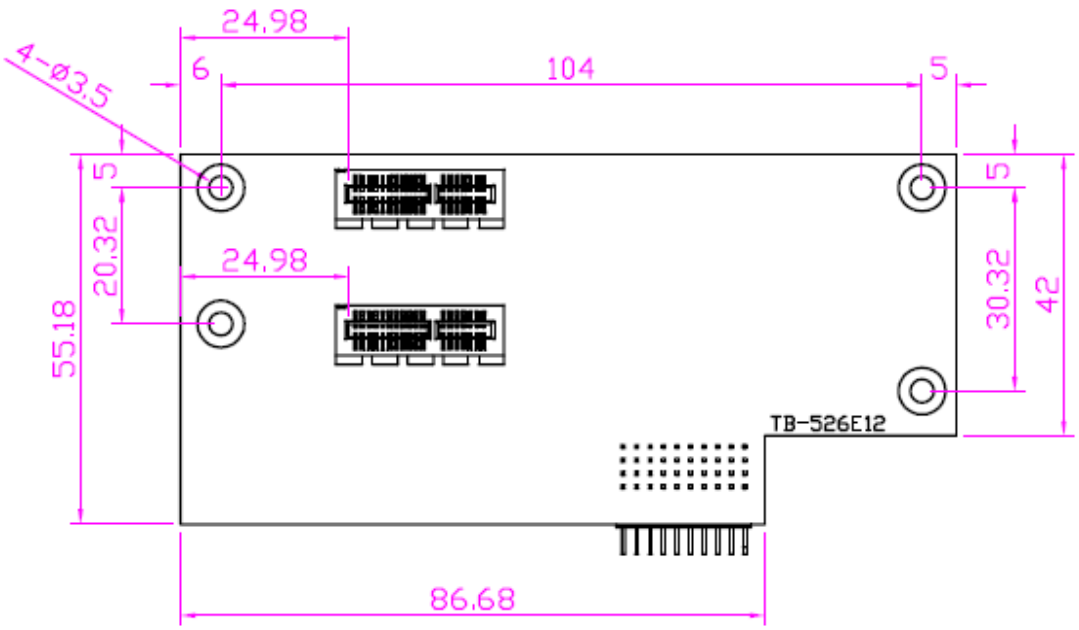
55. TB-526E11:

TB-526E11 connect to SBC-7113HB PCIE_4X connector, PCIE_4X is located at the Bottom, It provides one PCIE X1 slot.



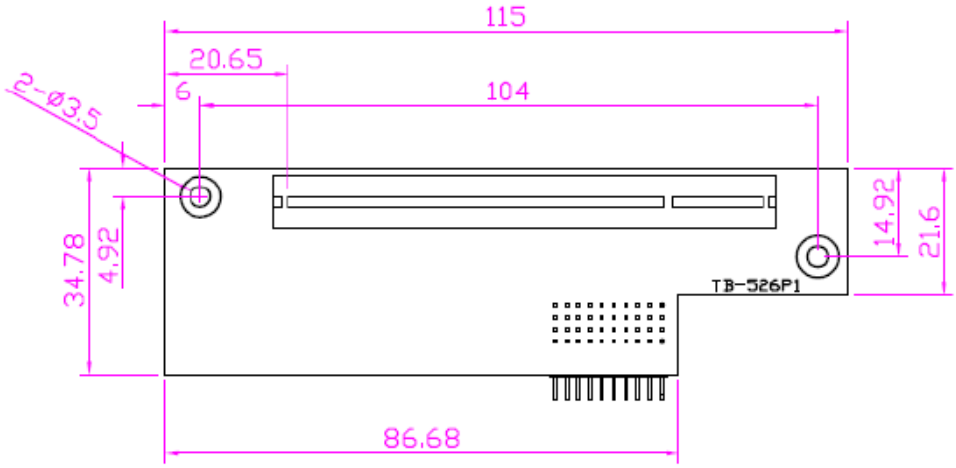
56. TB-526E12:

TB-526E12 connect to SBC-7113HB PCIE_4X connector, PCIE_4X is located at the Bottom, It provides two PCIE X1 slot.



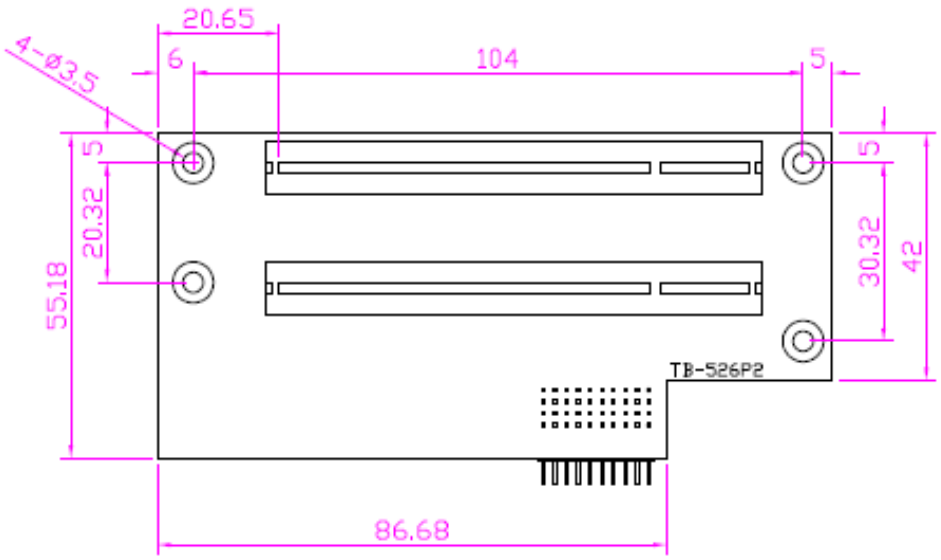
57. TB-526P1:

TB-526P1 connect to SBC-7113HB PCIE_4X connector, PCIE_4X is located at the Bottom, It provides one PCI slot.



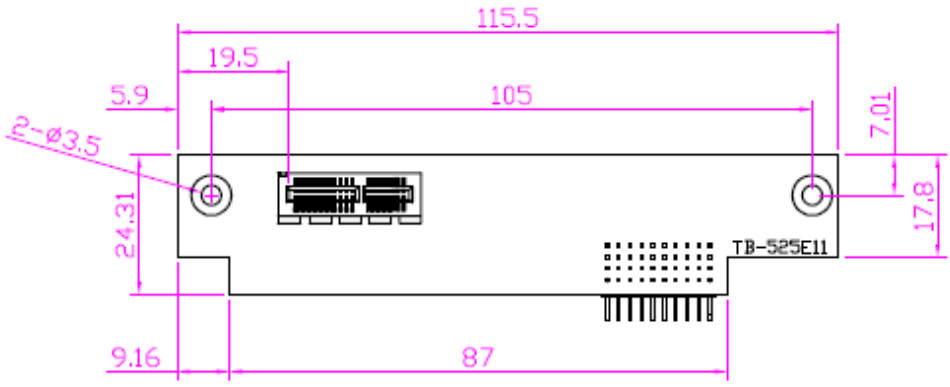
58. TB-526P2:

TB-526P2 connect to SBC-7113HB PCIE_4X connector, PCIE_4X is located at the Bottom, It provides two PCI slot.



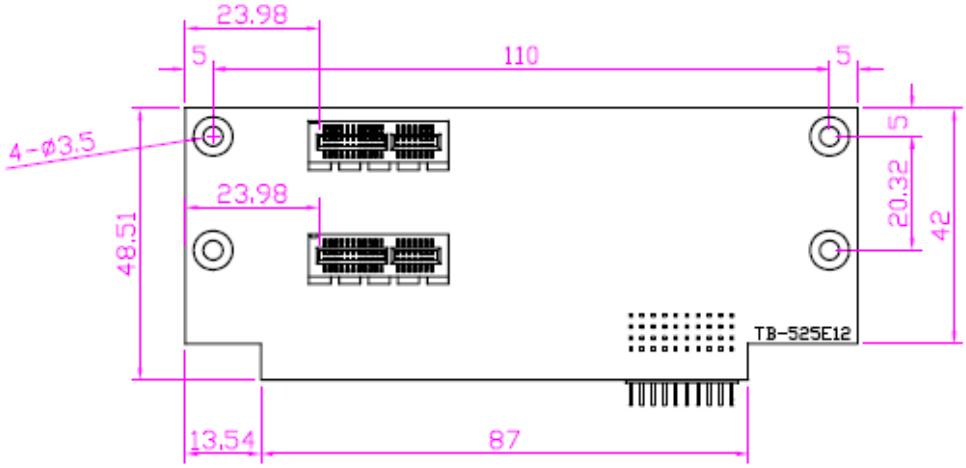
59. TB-525E11:

TB-525E11 connect to SBC-7113HT PCIE_4X connector**,** PCIE_4X is located at the top, It provides one PCIE X1 slot.



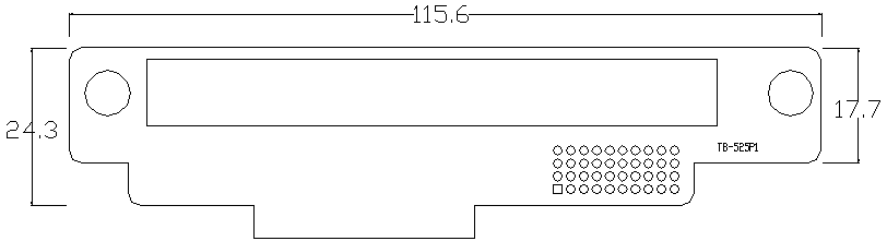
60. TB-525E12:

TB-525E12 connect to SBC-7113HT PCIE_4X connector**,** PCIE_4X is located at the top, It provides two PCIE X1 slot.



61. TB-525P1:

TB-525P1 connect to SBC-7113HT PCIE_4X connector, PCIE_4X is located at the top, It provides one PCI slot.



Chapter 3 BIOS Setup

3.1 Operations after POST Screen

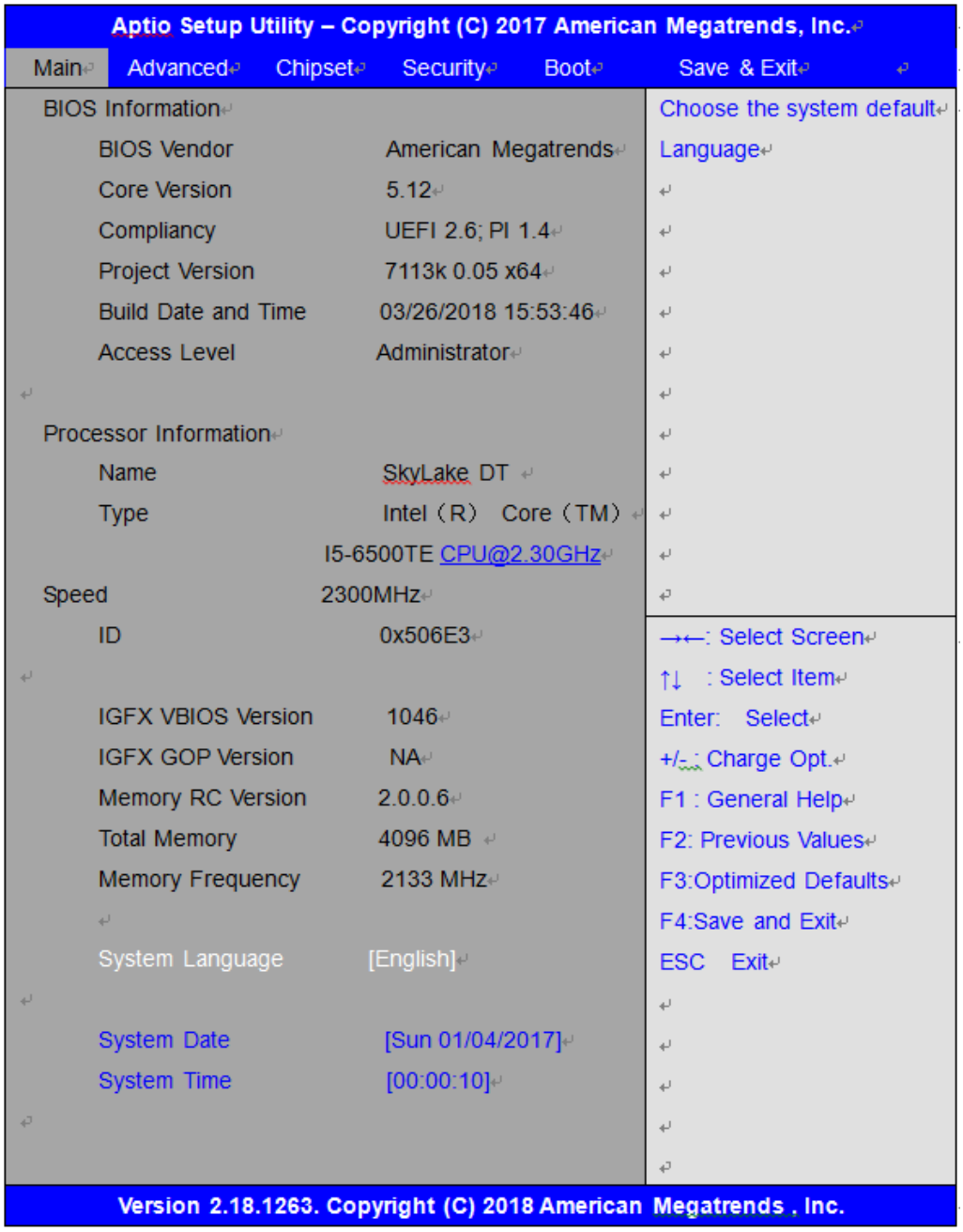
After CMOS discharge or BIOS flashing operation,.Press [Delete] key to enter CMOS Setup.

After optimizing and exiting CMOS Setup

3.2 BIOS SETUP UTILITY

Press [Delete] key to enter BIOS Setup utility during POST, and then a main menu containing system summary information will appear.

3.3 MAIN SETTING



System Time:

Set the system time, the time format is:

Hour : 0 to 23

Minute : 0 to 59

Second : 0 to 59

System Date:

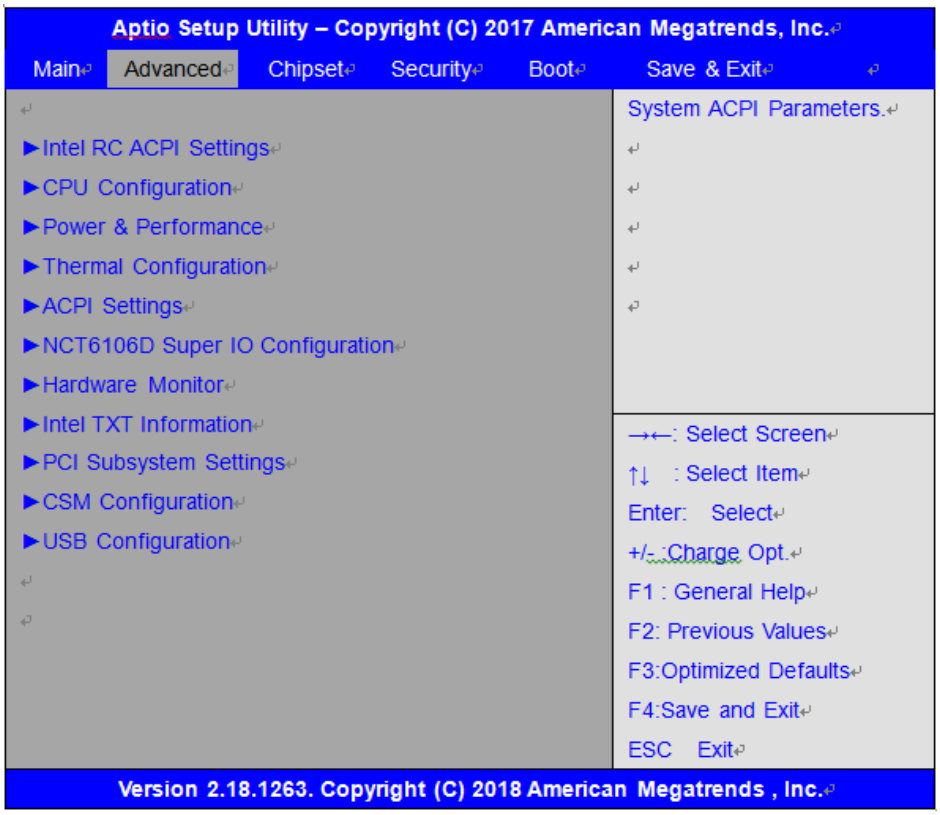
Set the system date, the date format is:

Day: Note that the 'Day' automatically changes when you set the date.

Month: 01 to 12

Date: 01 to 31

3.4 Advanced Settings



3.4.1 Intel RC ACPI Settings

PTID Support **[Enabled]**

[Disabled]

PECI Access Method **[Direct I/O]**

[ACPI]

Native PCIE Enable **[Enabled]**

[Disabled]

Native ASPM **[Auto]**

[Enabled]

[Disabled]

BDAT ACPI Table Support **[Disabled]**

[Enabled]

Wake system from S5 **[Disabled]**

[Enabled]

ACPI Debug **[Disabled]**

	[Enabled]
Low Power S0 Idle Capability	**[Disabled]**
	[Enabled]
Lpit Recidency Counter	**[SLP S0]**
	[C10]
Interl Ready Mode Technology	**[Disabled]**
	[Enabled]
PCI Delay Optimization	**[Disabled]**
	[Enabled]
ZpODD Support	**[Disabled]**
	[Enabled]

3.4.2 CPU Configuration

CPU Configuration

Type	Intel(R) Core(TM) i5-6500TE CPU @ 2.30GHz
ID	0x506E3
Speed	2300 MHz
L1 Date Cache	32 KB x 4
L1 Instruction Cache	32 KB x 4
L2 Cache	256 KB x 4
L3 Cache	6 MB
L4 Cache	NA
VMX	Supported
SMX/TXT	Supported
SW Guard Extensions(SGX)	**[Software Controlled]**
Select Owner EPOCH input type	**[No Change In Owner EPOCHS]**
PRMRR Size	[INVALID PRMRR]
CPU Flex Ratio Override	**[Disabled]**
CPU Flex Ratio Settings	23
Hardware Prefetcher	**[Enabled]**
Adjacent Cache Line Prefetch	**[Enabled]**
Intel (VMX)Virtualization Technology	**[Enabled]**
PECI	**[Enabled]**
Active Processor Cores	**[All]**

BIST	**[Disabled]**
JTAG C10 Power	**[Disabled]**
AP threads Idle Manner	**[MWAIT Loop]**
AP threads Handoff Manner	**[MWAIT Loop]**
AES	**[Enabled]**
MachineCheck	**[Enabled]**
MonitorMWait	**[Enabled]**
Intel Trusted Execution Technology	**[Disabled]**
Alias Check Reqest	[Disabled]
DPR Memory Size (MB)	4
Reset AUX Content	**[no]**
Flash Wear Out Protection	**[Disabled]**
Current Debug Interface Status	Disabled
Debug Interface	**[Disabled]**
Debug Interface Lock	**[Enabled]**
FCLK Frequency for Early Power On	**[1GHz]**
Voltage Optimization	**[Auto]**

►CPU SMM Enhancement

SMM Code Access Check	**[Enabled]**
SMM Use Delay Indication	**[Enabled]**
SMM Use Block Indication	**[Enabled]**

3.4.3 Power & Performance

►CPU – Power Management Control

Boot performance mode	**[Max Non-Turbo Performance]**
Intel(R) SpeedStep(tm)	**[Enabled]**
Race To Halt (RTH)	**[Enabled]**
Intel(R) Speed Shift Technology	**[Enabled]**
HDC Control	**[Enabled]**
Turbo Mode	**[Enabled]**
Platform PL1 Enable	**[Disabled]**
Platform PL2 Enable	**[Disabled]**
Power Limit 4 Override	**[Disabled]**
C states	**[Enabled]**
Enhanced C-states	**[Enabled]**
C-State Auto Demotion	**[C1 and C3]**
C-State Un-demotion	**[C1 and C3]**

Package C-State Demotion	**[Auto]**
Package C-State Un-Demotion	**[Auto]**
CState Pre-Wake	**[Enabled]**
IO MWAIT Readirection	**[Disabled]**
Package C State Limit	**[Auto]**
C3 Latency Control(MSR 0x60A)	
Time Unit	**[1024 ns]**
Latency	**78**
C6/C7 Short Latency Control(MSR 0x60B)	
Time Unit	**[1024 ns]**
Latency	**118**
C6/C7 Short Latency Control(MSR 0x60C)	
Time Unit	**[1024 ns]**
Latency	**148**
Thermal Monitor	**[Enabled]**
Interrupt Redirection Mode	**[PAIR with Fixde Priority]**
Timed MWAIT	**[Disabled]**
Energy Performance Gain	**[Disabled]**
EPG DIMM Idd3N	**26**
EPG DIMM Idd3P	**11**

►View/Configure Turbo Options

Current Turbo Settings

Max Turbo Power Limit	4095.875
Min Turbo Power Limit	0.0
Package TDP Limit	35.0
Power Limit 1	35.0
Power Limit 2	43.750
1-Core Turbo Ration	33
2-Core Turbo Ration	32
3-Core Turbo Ration	31
4-Core Turbo Ration	30

Energy Efficient P-state	**[Enabled]**
Package Power Limit MSR Lock	**[Disabled]**
Power Limit 1 Override	**[Disabled]**
Power Limit 2 Override	**[Enabled]**

Power Limit 2	**0**
1-Core Ration Limit Override	**0**
2-Core Ration Limit Override	**0**
3-Core Ration Limit Override	**0**
4-Core Ration Limit Override	**0**
Energy Efficient Turbo	**[Enabled]**
►CP U VR Settings	
PSYS Slope	**0**
PSYS offset	**0**
PSYS PMax Power	**0**
VR Mailbox Command options	**0**
►Acoustic Noise Settings	
Acoustic Noise Mitigation	**[Disabled]**
►Core/IA VR Settings	
VR Config Enable	**[Enabled]**
VR Config Enable	**[Enabled]**
AC Loadline	**0**
DC Loadline	**0**
PS Current Threshould1	**80**
PS Current Threshould2	**20**
PS Current Threshould3	**4**
PS3 Enable	**[Enabled]**
PS4 Enable	**[Enabled]**
IMON Slope	**0**
IMON Offset	**0**
IMON Prefix	**[+]**
VR Config Enable	**0**
VR Voltage Enable	**0**
TDC Enable	**[Disabled]**
TDC Lock	**[Disabled]**
►VR-Sliced VR Settings	
VR Config Enable	**[Enabled]**
AC Loadline	**0**
DC Loadline	**0**
PS Current Threshould1	**80**

PS Current Threshould2 **20**

PS Current Threshould3 **4**

PS3 Enable **[Enabled]**

PS4 Enable **[Enabled]**

IMON Slope **0**

IMON Offset **0**

IMON Prefix **[+]**

VR Config Enable **0**

VR Voltage Enable **0**

TDC Enable **[Disabled]**

TDC Lock **[Disabled]**

►Custom P-state Table

Number of P states **0**

►Power Limit 3 Settings

Power Limit 3 Override **[Disabled]**

►CPU Lock Configuration

CFG Lock **[Enabled]**

Overclocking Lock **[Disabled]**

►GT – Power Management Control

RC6(Render Standby) **[Enabled]**

Maximum GT frequency **[Default Max Frequency]**

3.4.4 Thermal Configuration

►CPU Thermal Configuration

DTS SMM **[Disabled]**

Tcc Activation Offset **0**

Tcc offset Time Window **[Disabled]**

Tcc offset Clamp Enable **[Disabled]**

Tcc offset Lock Enable **[Disabled]**

Bi-directional PROCHOT# **[Enabled]**

Disable PROCHOT# Output **[Enabled]**

Disable VR Thermal Alert **[Disabled]**

PROCHOT Response **[Disabled]**

PROCHOT Lock **[Disabled]**

ACPI T-States **[Disabled]**

PECI Reset **[Disabled]**

PECI C10 Reset **[Disabled]**

►Platform Thermal Configuration

Automatic Thermal Reporting **[Disabled]**

Critical Trip Point **[119 C (POR)]**

Active Trip Point 0 **[71 C]**

Active Trip Point 0 Fan Speed **100**

Active Trip Point 1 **[55 C]**

Active Trip Point 1 Fan Speed **75**

Passive Trip Point **[95 C]**

Passive TC1 Value **1**

Passive TC2 Value **5**

Passive TSP Value **10**

Active Trip Points **[Enabled]**

Passive Trip Poinst **[Disabled]**

Critical Trip Points **[Enabled]**

PCH Thermal Device **[Enabled in PCI mode]**

PCH Temp Read **[Enabled]**

CPU Energy Read **[Enabled]**

CPU Temp Read **[Enabled]**

Alert Enable Lock **[Disabled]**

CPU Temp **72**

CPU Fan Speed **65**

►DPTF Configuration

3.4.5 ACPI Settings

Enable ACPI Auto Configuration:

[Disabled]

[Enabled]

Enable Hibernation:

[Enabled]

[Disabled]

ACPI Sleep State:

[S3 (Suspend to RAM)]

[Suspend Disabled]

Lock Legacy Resources:

[Disabled]

[Enabled]

S3 Video Repost:

[Disabled]

[Enabled]

3.4.6 T6106 Super IO Configuration

►Serial Port 1 Configuration

Serial port **[Enabled]**

[Disabled]

Device Settings IO=3F8h； IRQ=4；

Change Settings **[Auto]**

F75111 COM1 Config

[RS-232 Mode]

[RS-485 Mode]

[RS-422 Mode]

►Serial Port 2 Configuration

Serial port **[Enabled]**

[Disabled]

Device Settings IO=2F8h； IRQ=3；

Change Settings **[Auto]**

F75111 COM2 Config

[RS-232 Mode]

[RS-485 Mode]

[RS-422 Mode]

►Serial Port 3 Configuration

Serial port **[Enabled]**

[Disabled]

Device Settings IO=3E8h； IRQ=7；

Change Settings **[Auto]**

►Serial Port 4 Configuration

Serial port **[Enabled]**

[Disabled]

Device Settings IO=2E8h； IRQ=7；

Change Settings **[Auto]**

►Serial Port 5 Configuration

Serial port **[Enabled]**

[Disabled]

Device Settings IO=2F0h； IRQ=7；

Change Settings **[Auto]**

F75111 COM5 Config

[RS-232 Mode]

[RS-485 Mode]

[RS-422 Mode]

►Serial Port 6 Configuration

Serial port **[Enabled]**

[Disabled]

Device Settings IO=2E0h； IRQ=7；

Change Settings **[Auto]**

F75111 COM6 Config

[RS-232 Mode]

[RS-485 Mode]

[RS-422 Mode]

►Parallel Port Configuration

Parallel Port **[Enabled]**

Device Settings IO=378h； IRQ=5；

Change Settings **[Auto]**

Device Mode **[EPP-1.7 and SPP Mode]**

[STD Printer Mode]

[STD Mode]

[EPP-1.9 and SPP Mode]

3.4.7 Hardware Monitor

Pc Health Status

CPU temperature ：+31 C

Fan2 Speed ：1262 RPM(波动值)

Vcore ：+0.936 V

12V ：	：+11.960 V
5V ：	：+5.160 V
1.5C ：	：+1.552 V

3.4.8 Intel TXT Information

Chipset	Production Fused
BiosAcm	Production Fused
Chipset Txt	Supported
Cput Txt	Supported
Error Code	None
Class Code	None
Major Code	None
Minor Code	None

3.4.9 PCI Subsystem Settings

AMI PCI Driver Version : A5.01.12

PCI Settings Common for all Devices:

Above 4G Decoding	**[Disabled]**
Hot-Piug Support	**[Enabled]**

Change Settings of the Following PCI Devices:

WARNING: Changing PCI Device(s) settings may
Have unwanted side effects! System may HANG!
PROCEED WITH CAUTION.

3.4.10 CSM Configuration

Compatibility Support Module Configuration

CSM Support	[Enabled]
CSM16 Module Version	07.81
GateA20 Active	**[Upon Request]**
Option ROM Messages	**[Force BIOS]**
INT19 Trap Response	**[Immediate]**

Boot option filter **[UEFI and Legacy]**

Option ROM execution

Network **[Do not launch]**
Storage **[UEFI]**
Video **[Legacy]**
Other PCI devices **[UEFI]**

3.4.11 USB Configuration

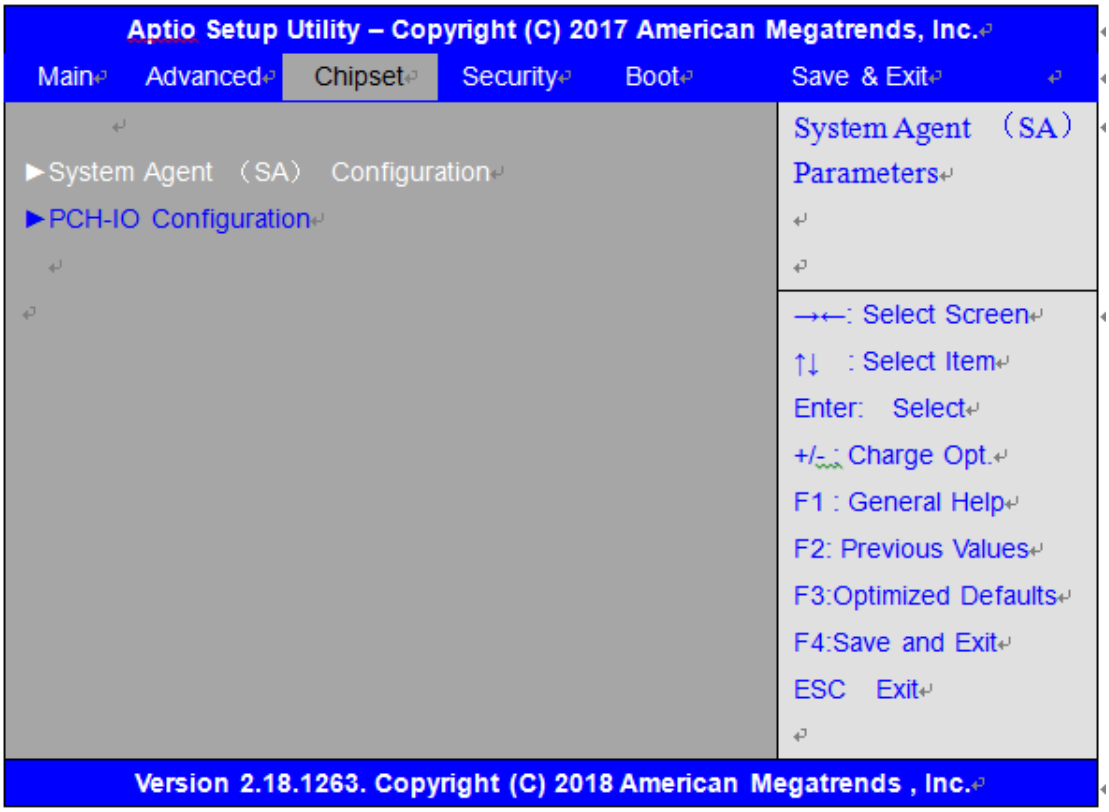
USB Module Version 19

USB Controllers:
1XHCI
USB Devices:
1 Keyboard,1 Mouse

Legacy USB Support **[Enabled]**
XHCI Hand-off **[Enabled]**
USB Mass Storage Driver Support **[Enabled]**
Port 60/64 Emulation **[Disabled]**

USB Hardware delays and time-outs:
USB transfer time-out **[20 sec]**
Device reset time-out **[20 sec]**
Device power-up delay **[Auto]**

3.5 Chipset Settings



3.5.1 System Agent （SA） Configuration

SA PCIe Code Version	1.9.0.0
VT-d	Supported
Stop Grant Configuration	**[Auto]**
VT-d	**[Enabled]**

►Memory Configuration

Memory RC Version	2.0.0.6
Memory Frequency	2133MHz
Memory Timings (Tcl-Trcd-TRP-TRAS)	13-13-13-35
Channel 0 Slot 0	Populated & Enabled
Size	4096 MB (DDR4)
Number of Ranks	1
Manufacturer	Kingston
Channel 0 Slot 1	Not Present & Disabled
Channel 1 Slot 0	Not Present/& Disabled

Channel 1 Slot 1	Not Present / Disabled

Memory ratio/reference clock
Options moved to
Overclock->Menmory->Custom Profile
menu

MRC ULT Safe Conifg	**[Disabled]**
Maximum Memory Frequency	**[Auto]**
HOB Buffer Size	**[Auto]**
ECC Support	**[Enabled]**
Max TOLUD	**[Dynamic]**
SA GV	**[Enabled]**
SA GV Low Freq	**[MRC default]**
Retrain on Fast fail	**[Enabled]**
Command Tristate	**[Enabled]**
Enable RH Prevention	**[Enabled]**
Row Hammer Solution	**[Hardware RHP]**
RH Activation Probability	**[1/2^11]**
Exit On Failure(MRC)	**[Enabled]**
MC Lock	**[Enabled]**
Probeless Trace	**[Disabled]**
Enable/Disable IED(Intel Enhanced Debug)	**[Disabled]**
Ch Hash Support	**[Enabled]**
Ch Hash Mask	**12488**
Ch Hash Interleaved Bit	**[BIT8]**
VC1 Read Metering	**[Enabled]**
VC1 RdMeter Time Window	8**00**
VC1 RdMeter Threshold	**280**
Strong Weak Leaker	**7**
Memory Scrambler	**[Enabled]**
Force ColdReset	**[Disabled]**
Channel A DIMM Control	**[Enable both DIMMS]**
Channel B DIMM Control	**[Enable both DIMMS]**
Force Single Rank	**[Disabled]**
Memory Remap	**[Enabled]**
Time Measure	**[Disabled]**
DLL Weak Lock Support	**[Enabled]**
Pwr Down Idle Timer	**0**

Mrc Fast Boot	**[Enabled]**
Lpddr Mem WL Set	**[Set B]**
EV Loader	**[Disabled]**
EV Loader Delay	**[Enabled]**

►Memory Thermal Configuration

►Memory Power and Thermal Throttling

DDR PowerDown and idle counter	**[BIOS]**
For LPDDR Only:DDR PowerDown and idle counter	**[BIOS]**
REFRESH_2X_MODE	**[Disabled]**
LPDDR Thermal Sensor	**[Enabled]**
SelfRefresh Enable	**[Enabled]**
SelfRefresh IdleTimer	512
Throttler CKEMin Defeature	**[Enabled]**
Throttler CKEMin Timer	48

►Dram Power Meter

Use user provided power weights, scale factor,and channel power floor values	[Disabled]
Energy Scale factor	4
Idle Energy Ch0Dimm0	10
PowerDown Energy Ch0Dimm0	6
Activate Energy Ch0Dimm0	172
Read Energy Ch0Dimm0	212
Write Energy Ch0Dimm0	221
Idle Energy Ch0Dimm1	10
PowerDown Energy Ch0Dimm1	6
Activate Energy Ch0Dimm1	172
Read Energy Ch0Dimm1	212
Write Energy Ch0Dimm1	221
Idle Energy Ch1Dimm0	10
PowerDown Energy Ch1Dimm0	6
Activate Energy Ch1Dimm0	172

Read Energy Ch1Dimm0 212
Write Energy Ch1Dimm0 221

Idle Energy Ch1Dimm1 10
PowerDown Energy Ch1Dimm1 6
Activate Energy Ch1Dimm1 172
Read Energy Ch1Dimm1 212
Write Energy Ch1Dimm1 221

►**Memory Thermal Reporting**
Lock Thermal:Management Registers **[Enabled]**

Memory Thermal Reporting

Extern Therm Status **[Disabled]**
Closed Loop Therm Manage **[Disabled]**
Open Loop Therm Manage **[Disabled]**

Thermal Threshold Settings

Warm Threshold Ch0 Dimm0 255
Warm Threshold Ch0 Dimm1 255
Hot Threshold Ch0 Dimm0 255
Hot Threshold Ch0 Dimm1 255
Warm Threshold Ch1 Dimm0 255
Warm Threshold Ch1 Dimm1 255
Hot Threshold Ch1 Dimm0 255
Hot Threshold Ch1 Dimm1 255

Thermal Throttle Budget Settings
Warm Budget Ch0 Dimm0 255
Warm Budget Ch0 Dimm1 255
Hot Budget Ch0 Dimm0 255
Hot Budget Ch0 Dimm1 255
Warm Budget Ch1 Dimm0 255
Warm Budget Ch1 Dimm1 255
Hot Budget Ch1 Dimm0 255
Hot Budget Ch1 Dimm1 255

►**Memory RAPL**

Rapl Power Floor Ch0	0
Rapl Power Floor Ch1	0
RAPL PL Lock	**[Disabled]**
RAPL PL 1 enable	**[Disabled]**
RAPL PL 1 Power	0
RAPL PL 1 WindowX	0
RAPL PL 1 WindowY	0
RAPL PL 2 enable	**[Disabled]**
RAPL PL 2 Power	222
RAPL PL 2 WindowX	1
RAPL PL 2 WindowY	10
Memory Thermal Management	**[Disabled]**

►**Memory Training Algorithms**

Early Command Training	**[Disabled]**
SenseAmp Offset Training	**[Enabled]**
Early ReadMPR Timing Centering 2D	**[Enabled]**
Read MPR Training	**[Enabled]**
Receive Enable Training	**[Enabled]**
Jedec Write Leveling	**[Enabled]**
Early Write Time Centering 2D	**[Enabled]**
Early Write Drive Strength/Equalization	**[Enabled]**
Early Read Time Centering 2D	**[Enabled]**
Write Timing Centering 1D	**[Enabled]**
Write Voltage Centering 1D	**[Enabled]**
Read Timing Centering 1D	**[Enabled]**
Dimm ODT Training*	**[Enabled]**
Max RTT_WR	**[ODT Off]**
DIMM RON Training*	**[Enabled]**
Write Drive Strength/Equalization 2D*	**[Disabled]**
Write Slew Rate Training*	**[Enabled]**

Read ODT Training*	**[Enabled]**
Read Equalization Training*	**[Enabled]**
Read Amplifier Training*	**[Enabled]**
Write Timing Centering 2D	**[Enabled]**
Read Timing Centering 2D	**[Enabled]**
Command Voltage Centering	**[Enabled]**
Write Voltage Centering 2D	**[Enabled]**
Read Voltage Centering 2D	**[Enabled]**
Late Command Training	**[Enabled]**
Round Trip Latency	**[Enabled]**
Turn Around Timing Training	**[Enabled]**
Rank Margin Tool	**[Disabled]**
Memory Test	**[Disabled]**
DIMM SPD Alias Test	**[Enabled]**
Receive Enable Centering 1D	**[Enabled]**
Retrain Margin Check	**[Enabled]**
Write Drive Strength Up/Dn Independently	**[Disabled]**
CMD Slew Rate Traning	**[Enabled]**
CMD Drive Strength / Tx Equalization	**[Enabled]**
CMD Normalization	**[Enabled]**

► **Graphics Configuration**

Graphics Turbo IMON Current	31
Skip Scaning of External GFx Card	**[Disabled]**
Primary Diispiay	**[Auto]**
Select PCIE Card	**[Auto]**
Internal Graphics	**[Auto]**
GTT Size	**[8MB]**
Aperture Size	**[256MB]**
DVMT Pre-Allocated	**[32]**
DVMT Total GFx Mem	**[256]**
GFx Low Power Mode	**[Enabled]**
VDD Enable	**[Enabled]**
HDCP Support	**[Enabled]**
Algorithm	**[One-time]**

PM Support	**[Enabled]**
Cdynmax Clamping Enable	**[Enabled]**
Cd Clock Frequency	**[675Mhz]**
IUER Button Enable	**[Disabled]**

►External GFx Primary Dispiay Configuration

Primary PEG	**[Auto]**
Primary PCIE	**[Auto]**

►LCD Control

Primary IGFX Boot Dispaly	**[HDMI]**
Secondary IGFX Boot Dispaly	**[VGA]**
LCD Panel Type	**[VBIOS Default]**
Panel Scanling	**[Auto]**
Backlight Control	**[PWM Normal]**
Active LFP	**[EDP Port-A]**
Panel Color Depth	**[18 Bit]**
Backlight Brightness	**255**

►DMI/OPI Configuration

DMI	X4 Gen3
DMI Max Link Speed	**[Auto]**
DMI Gen3 Eq Phase 2	**[Auto]**
DMI Gen3 Eq Phase 3 Method	**[Auto]**
DMI Vc1 Control	**[Disabled]**
DMI Vcm Control	**[Enabled]**
Program Static Phase1 Eq	**[Enabled]**
DMI Link ASPM Control	**[L1]**
DMI Extended Sync Control	**[Disabled]**
DMI De-emphasis Control	**[-3.5 dB]**
DMI IOT	**[Disabled]**

► Gen3 Root Port Preset value for each Lane

Lane 0	**4**
Lane 1	**4**
Lane 2	**4**

Lane 3	**4**

► **Gen3 Endpoint Preset value for each Lane**

Lane 0	**7**
Lane 1	**7**
Lane 2	**7**
Lane 3	**7**

► **Gen3 Endpoint Hint value for each Lane**

Lane 0	**2**
Lane 1	**2**
Lane 2	**2**
Lane 3	**2**

► **Gen3 RxCTLE Control**

Bundle0	**3**
Bundle1	**3**

►**PEG Port Configuration**

PEG 0：1:0	Not Present
Enable Root Port	**[Auto]**
Max Link Speed	**[Auto]**
PEG0 Slot Power Limit Value	**75**
PEG0 Slot Power Limit Scale	**[1.0x]**
PEG0 Slot Power Limit Number	**1**
PEG 0：1:1	Not Present
Enable Root Port	**[Auto]**
Max Link Speed	**[Auto]**
PEG0 Slot Power Limit Value	**75**
PEG0 Slot Power Limit Scale	**[1.0x]**
PEG0 Slot Power Limit Number	**2**
PEG 0：1:2	Not Present
Enable Root Port	**[Auto]**
Max Link Speed	**[Auto]**
PEG0 Slot Power Limit Value	**75**
PEG0 Slot Power Limit Scale	**[1.0x]**
PEG0 Slot Power Limit Number	**3**

Program PCIe ASPM after opROM	**[Disabled]**

Program Static Phase1 Eq	**[Enabled]**
Gen3 Adaptive Software Equalization	
Always Attempt SW EQ	**[Disabled]**
Nimber of Presets to test	**[Auto]**
Allow PERST# GPIO Usage	**[Enabled]**
SW EQ Enable VOC	**[Auto]**
Jitter Dwell Time	**3000**
Jitter Error Target	**2**
VOC Dwell Time	**10000**
Jitter Error Target	**2**
Generate BDAT PEG Margin Date	**[Disabled]**
PCIe Rx CEM Test Mode	**[Disabled]**
PCIe Spread Spectrum Clocking	**[Enabled]**
►PEG Port Feature Configuration	
Detect Non-Compliance Device	**[Disabled]**
►Gen3 Root Port Preset value for each Lane	
Lane 0	**7**
Lane 1	**7**
Lane 2	**7**
Lane 3	**7**
Lane 5	**7**
Lane 6	**7**
Lane 7	**7**
Lane 8	**7**
Lane 9	**7**
Lane 10	**7**
Lane 11	**7**
Lane 12	**7**
Lane 13	**7**
Lane 14	**7**
Lane 15	**7**
► Gen3 Endpoint Preset value for each Lane	
Lane 0	**7**
Lane 1	**7**

Lane 2	**7**
Lane 3	**7**
Lane 5	**7**
Lane 6	**7**
Lane 7	**7**
Lane 8	**7**
Lane 9	**7**
Lane 10	**7**
Lane 11	**7**
Lane 12	**7**
Lane 13	**7**
Lane 14	**7**
Lane 15	**7**

► **Gen3 Endpoint Hint value for each Lane**

Lane 0	**2**
Lane 1	**2**
Lane 2	**2**
Lane 3	**2**
Lane 5	**2**
Lane 6	**2**
Lane 7	**2**
Lane 8	**2**
Lane 9	**2**
Lane 10	**2**
Lane 11	**2**
Lane 12	**2**
Lane 13	**2**
Lane 14	**2**
Lane 15	**2**

► **Gen3 RxCTLE Control**

Bundle0	**0**
Bundle2	**0**
Bundle3	**0**
Bundle4	**0**
Bundle5	**0**
Bundle6	**0**

Bundle7 **0**

RxCTLE Override **[Disabled]**

3.5.2 PCH-IO Configuration

DCI enable (HDCIEN) [Disabled]

Debug Port Selection [Legacy UART]

Serial IRQ Mode [Continuous]

State After G3 [S5 state]

WiFi Control [Enabled]

F75111 GPIO20 Config [Output]

F75111 GPIO20 Output Setting [Low]

F75111 GPIO21 Config [Output]

F75111 GPIO21 Output Setting [Low]

F75111 GPIO22 Config [Output]

F75111 GPIO22 Output Setting [Low]

F75111 GPIO23 Config [Output]

F75111 GPIO23 Output Setting [Low]

F75111 GPIO24 Config [Output]

F75111 GPIO24 Output Setting [Low]

F75111 GPIO25 Config [Output]

F75111 GPIO25 Output Setting [Low]

F75111 GPIO26 Config [Output]

F75111 GPIO26 Output Setting [Low]

F75111 GPIO27 Config [Output]

F75111 GPIO27 Output Setting [Low]

F75111 COM1 Config [RS232 mode]

F75111 COM2 Config [RS232 mode]

F75111 COM5 Config [RS232 mode]

F75111 COM6 Config [RS232 mode]

Port 80h Redirecton [LPC Bus]

►PCI Express Configuration

PCI Express Clock Gating [Enabled]

Legacy IO Low Latency [Disabled]

DMI Link ASPM Control [Enabled]

PCIE Port assigned to LAN Disabled

Port8xh Decode [Disabled]

Peer Memory Write Enable [Disabled]

Compliance Test Mode [Disabled]

PCIe-USB Glitch W/A	[Disabled]
PCIe function swap	[Enabled]
►PCI Express Gen3 Eq Lanes	
PCIE1 Cm	6
PCIE1 Cp	2
PCIE2 Cm	6
PCIE2 Cp	2
PCIE3 Cm	6
PCIE3 Cp	2
PCIE4 Cm	6
PCIE4 Cp	2
PCIE5 Cp	6
PCIE5 Cm	2
PCIE6 Cp	6
PCIE6 Cm	2
PCIE7 Cp	6
PCIE7 Cm	2
PCIE8 Cp	6
PCIE8 Cm	2
PCIE9 Cp	6
PCIE9 Cm	2
PCIE10 Cp	6
PCIE10 Cm	2
PCIE11 Cp	6
PCIE11 Cm	2
PCIE12 Cp	6
PCIE12 Cm	2
PCIE13 Cp	6
PCIE13 Cm	2
PCIE14 Cp	6
PCIE14 Cm	2
PCIE15 Cp	6
PCIE15 Cm	2
PCIE16 Cp	6
PCIE16 Cm	2
PCIE17 Cp	6
PCIE17 Cm	2
PCIE18 Cp	6

PCIE18 Cm 2
PCIE19 Cp 6
PCIE19 Cm 2
PCIE20 Cp 6
PCIE20Cm 2

Override SW EQ Settings [Disabled]

►PCI Express Root Port 1

PCI Express Root Port 1 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE1 LTR [Enabled]
Snoop Latency Override [Auto]

Non Snoop Latency Override [Auto]
Force LTP Override [Disabled]

PCIE1 LTR Lock [Disabled]

PCH PCIe CLKRRQ# Configuration
PCIE CLKRRQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 2
PCI Express Root Port 2 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0

Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE2 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE2 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE2 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 3
PCI Express Root Port 3 [Enabled]
Topology [X1]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]

Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE3 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE3 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE3 CLKREQ Mapping Override [Default]

►**Extra options**
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 4
PCI Express Root Port 4 [Enabled]
Topology [X1]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]

CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE4 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE4 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE4 CLKREQ Mapping Override [Default]

►Extra options

Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 5

PCI Express Root Port 5 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]

UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Timeout	0
Extra Bus Reserved	0
Reserved Memory	10
Reserved I/O	4

PCH PCIe LTR Configuration

PCH PCIE5 LTR	[Enabled]
Snoop Latency Override	[Auto]
Non-Snoop Latency Override	[Auto]
Force LTR Override	[Disabled]
PCIE5 LTR Lock	[Disabled]

PCH PCIe CLKREQ# Configuration

PCIE5 CLKREQ Mapping Override	[Default]

►Extra options

Detect Non-Compliance Device	[Disabled]
Prefetchable Memory	10
Reseved Memory Alignment	1
Prefetchable Memory Alignment	1

►PCI Express Root Port 6

PCI Express Root Port 6	[Enabled]
Topology	[Unknown]
ASPM	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Timeout	0
Extra Bus Reserved	0
Reserved Memory	10
Reserved I/O	4

PCH PCIe LTR Configuration

PCH PCIE6 LTR	[Enabled]
Snoop Latency Override	[Auto]
Non-Snoop Latency Override	[Auto]
Force LTR Override	[Disabled]

PCIE6 LTR Lock	[Disabled]

PCH PCIe CLKREQ# Configuration

PCIE6 CLKREQ Mapping Override	[Default]

► **Extra options**

Detect Non-Compliance Device	[Disabled]
Prefetchable Memory	10
Reseved Memory Alignment	1
Prefetchable Memory Alignment	1

► **PCI Express Root Port 7**

PCI Express Root Port 7	[Enabled]
Topology	[Unknown]
ASPM	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Timeout	0
Extra Bus Reserved	7
Reserved Memory	17
Reserved I/O	8

PCH PCIe LTR Configuration	
PCH PCIE7 LTR	[Enabled]
Snoop Latency Override	[Auto]
Non-Snoop Latency Override	[Auto]
Force LTR Override	[Disabled]

PCIE7 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE7 CLKREQ Mapping Override [Default]

►Extra options

Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 8

PCI Express Root Port 8 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 7
Reserved Memory 17
Reserved I/O 4

PCH PCIe LTR Configuration

PCH PCIE8 LTR [Enabled]

Snoop Latency Override [Auto]

Non-Snoop Latency Override [Auto]

Force LTR Override [Disabled]

PCIE8 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration

PCIE8 CLKREQ Mapping Override [Default]

►Extra options

Detect Non-Compliance Device [Disabled]

Prefetchable Memory 10

Reseved Memory Alignment 1

Prefetchable Memory Alignment 1

►PCI Express Root Port 9

PCI Express Root Port 9 [Enabled]

Topology [M2]

ASPM [Auto]

L1 SubStates [L1.1&L1.2]

Gen3 Eq Phase3 Method [Software Search]

UPTP 5

DPTP 7

ACS [Enabled]

URR [Disabled]

FER [Disabled]

NFER [Disabled]

CER [Disabled]

CTO [Disabled]

SEFE [Disabled]

SENFE [Disabled]

SECE [Disabled]

PME SCI [Enabled]

Hot Plug [Disabled]

Advanced Error Reporting [Enabled]

PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE9 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE9 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE9 CLKREQ Mapping Override [Default]

►Extra options

Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 13

PCI Express Root Port 13 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]

SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE13 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE13 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE13 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 11
PCI Express Root Port 14 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7

ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE14 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE14 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE14 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 15
PCI Express Root Port 15 [Enabled]

Topology	[Unknown]
ASPM	[Auto]
L1 SubStates	[L1.1&L1.2]
Gen3 Eq Phase3 Method	[Software Search]
UPTP	5
DPTP	7
ACS	[Enabled]
URR	[Disabled]
FER	[Disabled]
NFER	[Disabled]
CER	[Disabled]
CTO	[Disabled]
SEFE	[Disabled]
SENFE	[Disabled]
SECE	[Disabled]
PME SCI	[Enabled]
Hot Plug	[Disabled]
Advanced Error Reporting	[Enabled]
PCIe Speed	[Auto]
Transmitter Half Swing	[Disabled]
Detect Timeout	0
Extra Bus Reserved	0
Reserved Memory	10
Reserved I/O	4
PCH PCIe LTR Configuration	
PCH PCIE15 LTR	[Enabled]
Snoop Latency Override	[Auto]
Non-Snoop Latency Override	[Auto]
Force LTR Override	[Disabled]
PCIE15 LTR Lock	[Disabled]
PCH PCIe CLKREQ# Configuration	
PCIE15 CLKREQ Mapping Override	[Default]

►Extra options

Detect Non-Compliance Device	[Disabled]

Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 16

PCI Express Root Port 16 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE16 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE16 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration

PCIE16 CLKREQ Mapping Override [Default]

►**Extra options**

Detect Non-Compliance Device [Disabled]

Prefetchable Memory 10

Reseved Memory Alignment 1

Prefetchable Memory Alignment 1

►**PCI Express Root Port 17**

PCI Express Root Port 17 [Enabled]

Topology [Unknown]

ASPM [Auto]

L1 SubStates [L1.1&L1.2]

Gen3 Eq Phase3 Method [Software Search]

UPTP 5

DPTP 7

ACS [Enabled]

URR [Disabled]

FER [Disabled]

NFER [Disabled]

CER [Disabled]

CTO [Disabled]

SEFE [Disabled]

SENFE [Disabled]

SECE [Disabled]

PME SCI [Enabled]

Hot Plug [Disabled]

Advanced Error Reporting [Enabled]

PCIe Speed [Auto]

Transmitter Half Swing [Disabled]

Detect Timeout 0

Extra Bus Reserved 0

Reserved Memory 10

Reserved I/O 4

PCH PCIe LTR Configuration

PCH PCIE17 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE17 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE17 CLKREQ Mapping Override [Default]

►Extra options

Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 19

PCI Express Root Port 19 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]

Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE19 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE19LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE19 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 21
PCI Express Root Port 21 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]

SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE21 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE21 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE21 CLKREQ Mapping Override [Default]

►Extra options
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 22
PCI Express Root Port 22 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]

FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE22 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE22 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE22 CLKREQ Mapping Override [Default]

►Extra options

Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►PCI Express Root Port 23

PCI Express Root Port 23 [Enabled]
Topology [Unknown]
ASPM [Auto]

L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE23 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE23 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration
PCIE23 CLKREQ Mapping Override [Default]

►**Extra options**
Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1

Prefetchable Memory Alignment 1

►PCI Express Root Port 24

PCI Express Root Port 24 [Enabled]
Topology [Unknown]
ASPM [Auto]
L1 SubStates [L1.1&L1.2]
Gen3 Eq Phase3 Method [Software Search]
UPTP 5
DPTP 7
ACS [Enabled]
URR [Disabled]
FER [Disabled]
NFER [Disabled]
CER [Disabled]
CTO [Disabled]
SEFE [Disabled]
SENFE [Disabled]
SECE [Disabled]
PME SCI [Enabled]
Hot Plug [Disabled]
Advanced Error Reporting [Enabled]
PCIe Speed [Auto]
Transmitter Half Swing [Disabled]
Detect Timeout 0
Extra Bus Reserved 0
Reserved Memory 10
Reserved I/O 4

PCH PCIe LTR Configuration
PCH PCIE24 LTR [Enabled]
Snoop Latency Override [Auto]
Non-Snoop Latency Override [Auto]
Force LTR Override [Disabled]

PCIE24 LTR Lock [Disabled]

PCH PCIe CLKREQ# Configuration

PCIE24 CLKREQ Mapping Override [Default]

►Extra options

Detect Non-Compliance Device [Disabled]
Prefetchable Memory 10
Reseved Memory Alignment 1
Prefetchable Memory Alignment 1

►SATA And RST Configuration

SATA Controller(s) [Enabled]
SATA Mode Selection [AHCI]
SATA Test Mode [Disabled]
Aggressive LPM Support [Enabled]
SATA Controller Speed [Default]
Serial ATA Port 0 Empty
Software Preserve Unknown
Port 0 [Enabled]
Hot Plug [Disabled]
Configurde as ESATA Hot Plug supported
Spin Up Device [Disabled]
SATA Device Type [Hard Disk Drive]
Topology [ISATA]
SATA Port 0 DevSlp [Disabled]
DIT0 Configuration [Disabled]
DIT0 Value 625
DM Value 15
Serial ATA Port 1 Empty
Software Preserve Unknown
Port 1 [Enabled]
Hot Plug [Disabled]
Configurded as Esata Hot Plug supported
Spin Up Device [Disabled]
SATA Device Type [Hard Disk Drive]
Topology [ISATA]
SATA Port 1 DevSlp [Disabled]
DIT0 Value 625
DM Value 15
Serial ATA Port 2 Empty

Software Preserve	Unknown
Port 2	[Enabled]
Hot Plug	[Disabled]
Configurded as Esata	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[ISATA]
SATA Port 2 DevSlp	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 3	[Enabled]
Hot Plug	[Disabled]
Configurded as Esata	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[ISATA]
SATA Port 1 DevSlp	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 4	[Enabled]
Hot Plug	[Disabled]
Configurded as Esata	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
SATA Port 1 DevSlp	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 5	[Enabled]
Hot Plug	[Disabled]
Configurded as Esata	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
SATA Port 1 DevSlp	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 6	[Enabled]

Hot Plug	[Disabled]
Configurded as Esata	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
SATA Port 1 DevSlp	[Disabled]
DIT0 Value	625
DM Value	15
Serial ATA Port 7	
Hot Plug	[Disabled]
Configurded as Esata	Hot Plug supported
Spin Up Device	[Disabled]
SATA Device Type	[Hard Disk Drive]
Topology	[Unknown]
SATA Port 1 DevSlp	[Disabled]
DIT0 Value	625
DM Value	15

►USB Configuration

XHCI Disable Compliance	[FALSE]
XDCI Support	[Disabled]
USB Port Disable Override	[Disabled]

3.6 Security Settings

3.6.1 Administrator Password

3.6.2 User Password

Type the password with up to 20 characters and then press ≮Enter≯ key. This will clear all previously typed CMOS passwords. You will be requested to confirm the password. Type the password again and press ≮Enter≯ key. You may press ≮Esc≯ key to abandon password entry

operation.

To clear the password, just press ⩤Enter⩥ key when password input window pops up. A confirmation message will be shown on the screen as to whether the password will be disabled. You will have direct access to BIOS setup without typing any password after system reboot once the password is disabled.

Once the password feature is used, you will be requested to type the password each time you enter BIOS setup. This will prevent unauthorized persons from changing your system configurations.

Also, the feature is capable of requesting users to enter the password prior to system boot to control unauthorized access to your computer. Users may enable the feature in Security Option of Advanced BIOS Features. If Security Option is set to System, you will be requested to enter the password before system boot and when entering BIOS setup; if Security Option is set to Setup, you will be requested for password for entering BIOS setup.

3.6.3 Secure Boot

System Mode	Setup
Secure Boot	Not Active
Vendor Keys	Active
Attempt Secure Boot	**[Disabled]**
Secure Boot Mode	**[Custom]**

►Key Management

Provision Factory Defaults	**[Disabled]**

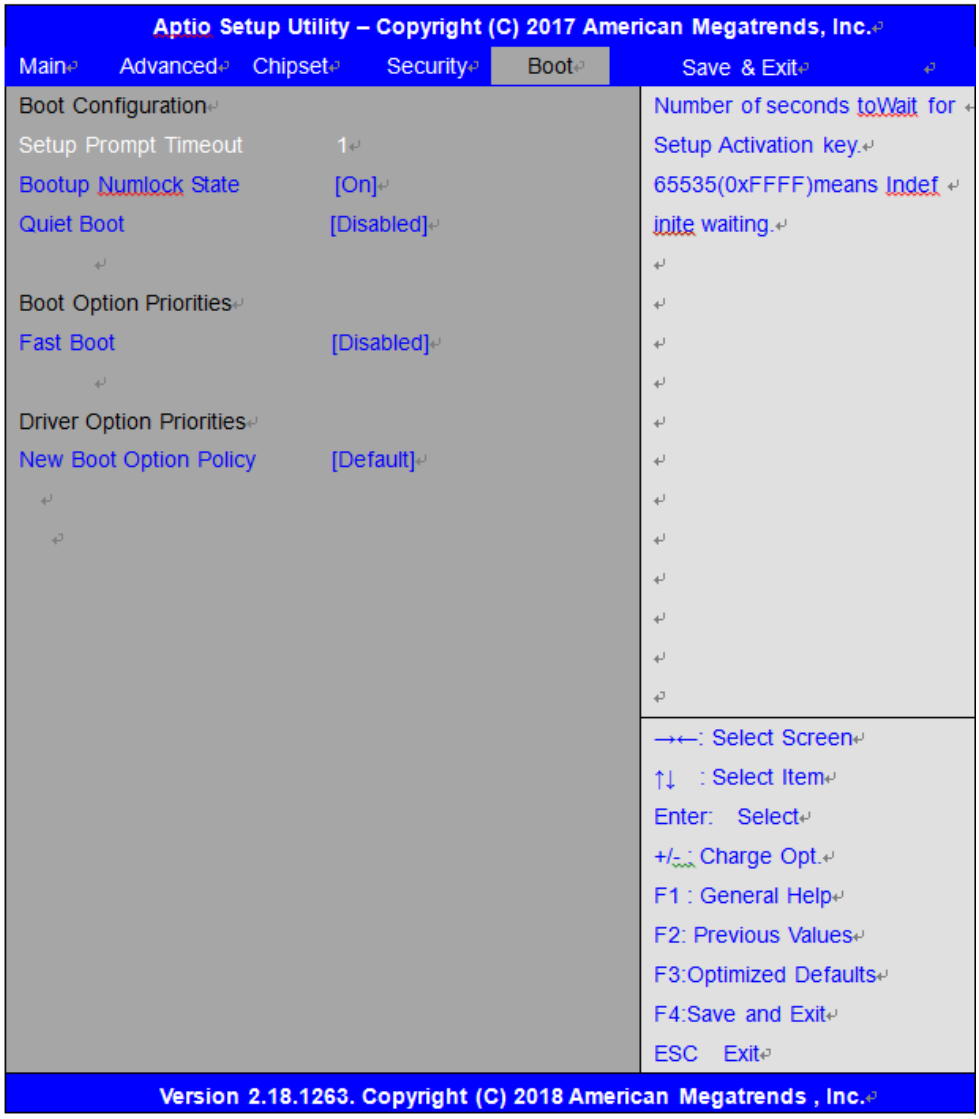
►Install Factory Default keys

►Enroll Efi Image

►Save all Secure Boot variables

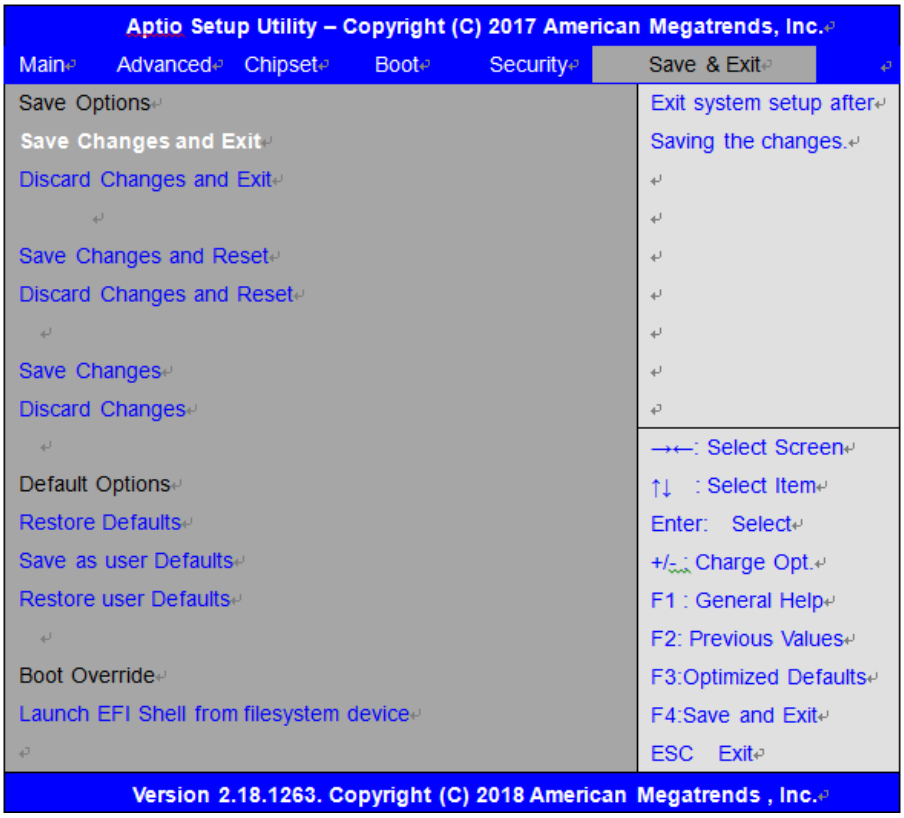
Secure Boot variables	**Size**	**Key#**	**Key Source**
►Platform Key(PK)	**0**	**0**	**No Key**
► Key Exchange Keys	**0**	**0**	**No Key**
► Authorized Signatures	**0**	**0**	**No Key**
►Forbidden Signatures	**0**	**0**	**No Key**
► Authorized TimeStamps	**0**	**0**	**No Key**
► osRecovery Signatures	**0**	**0**	**No Key**

3.7 Boot Settings



Setup Prompt Timeout	1
Bootup Numlock State	**[On]**
Quiet Boot	**[Disabled]**
Boot Option Priorities	
Fast Boot	**[Disabled]**
Driver Option Priorities	
New Boot Option Policy	**[Default]**

3.8 Save & Exit Settings



Save Changes and Exit

Save & Exit Setup save Configuration and exit ?

[Yes]

[No]

Discard Changes and Ext

Exit Without Saving Quit without saving?

[Yes]

[No]

Save Changes and Reset

Reset the system affer Saving The changes?

[Yes]

[No]

Discard Changes and Reset

Reset system setup without Saving any changes?

[Yes]

[No]

Save Changes

Save Setup done so far to any of the setup options?

[Yes]

[No]

Discard Changes

Discard Changes done so far to any of the setup options?

[Yes]

[No]

Restore Defaults

Restore /Load Defaults values for all the setup options?

[Yes]

[No]

Save as user Defaults

Save the changes done so far as User Defaults?

[Yes]

[No]

Restore user Defaults

Restore the User Defaults to all the setup options?

[Yes]

[No]

Boot Override

Launch EFI Shell from filesystem device

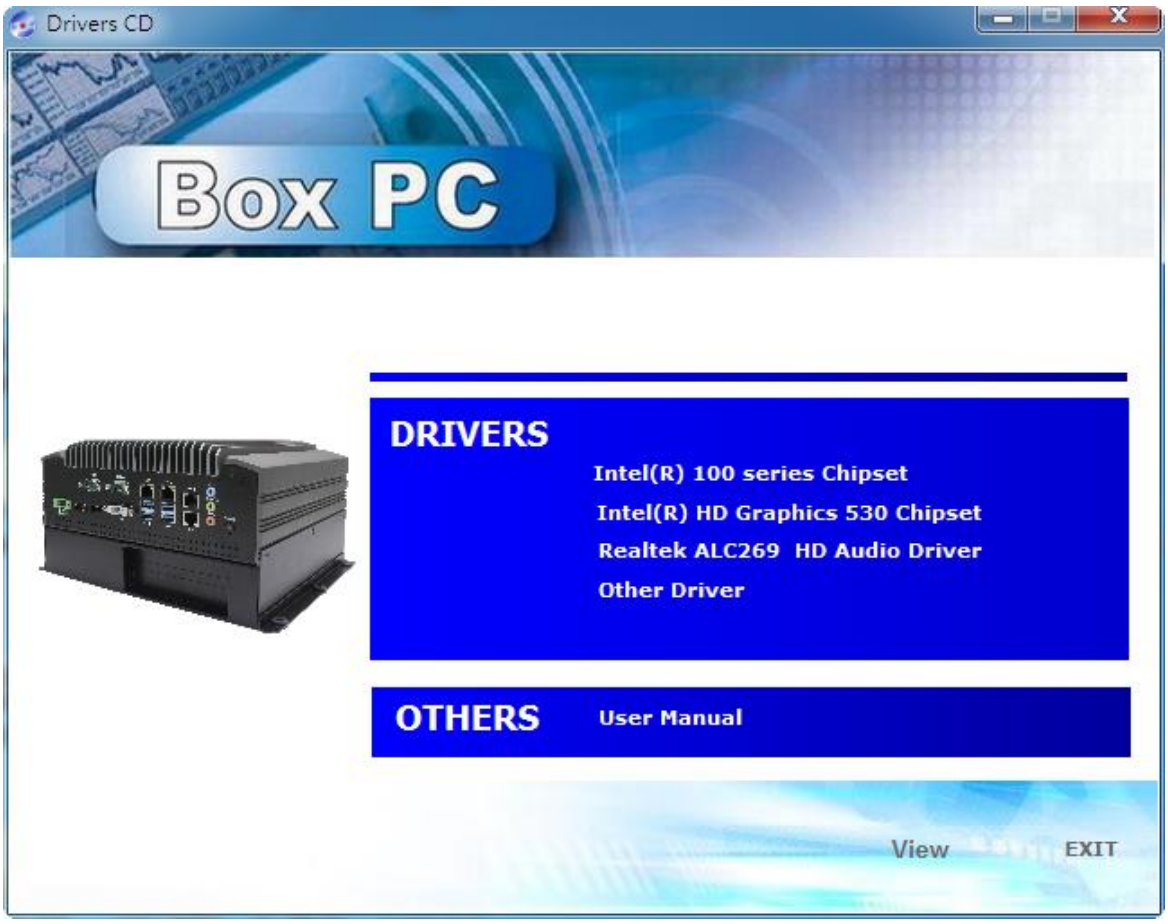
[Yes]

[No]

Chapter 4 Installation of Drivers

This chapter describes the installation procedures for software and drivers under the windows Embedded 8.1 and Windows 10 IOT. The software and drivers are included with the motherboard. The contents include **Intel(R) 100 series chipset driver, Intel(R) HD Graphics 530 chipset driver, Realtek ALC269 HD Audio Driver, and other Driver. Installation instructions are given below.**

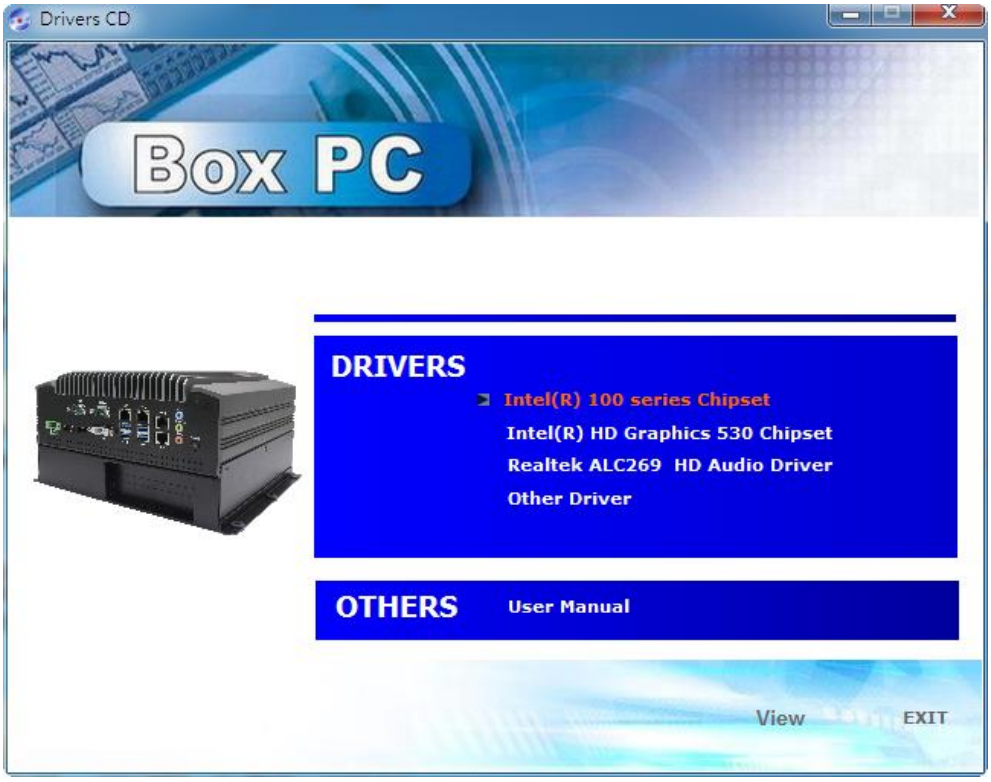
Important Note:
After installing your Windows operating system, you must install first the Intel Chipset Software Installation Utility before proceeding with the installation of drivers.



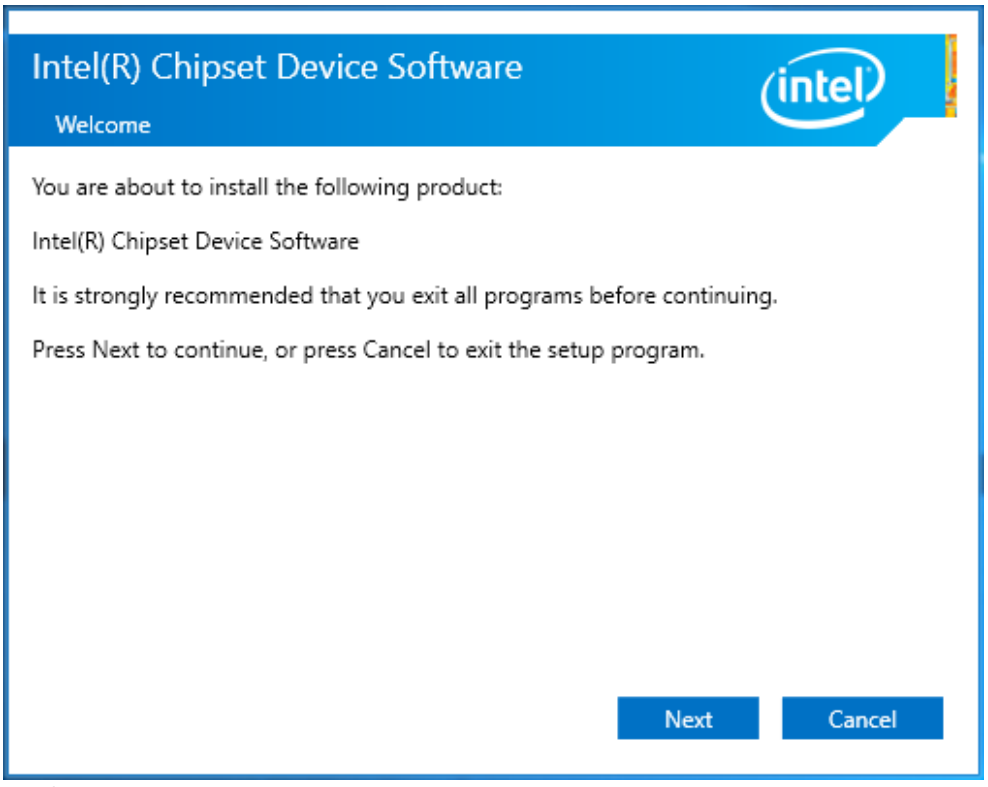
4.1 Intel(R) 100 Series Chipset Driver

To install the Intel chipset driver, please follow the steps below.

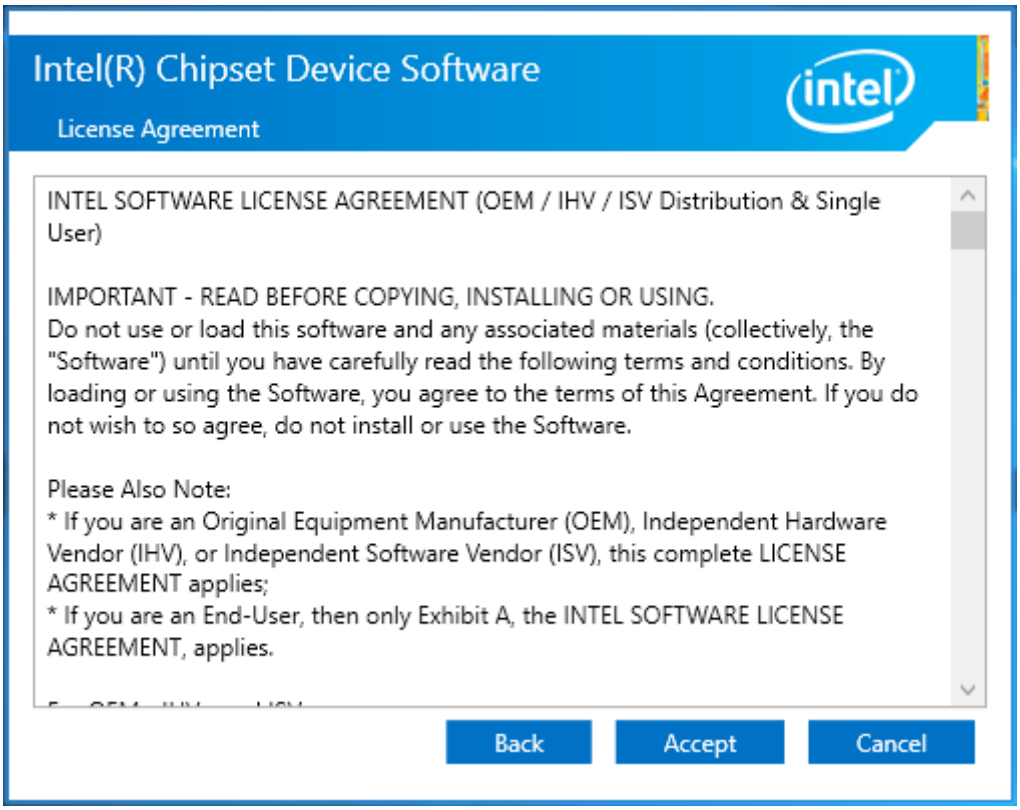
Step 1. Select 4.1 **Intel(R) 100 Series Chipset** from the list



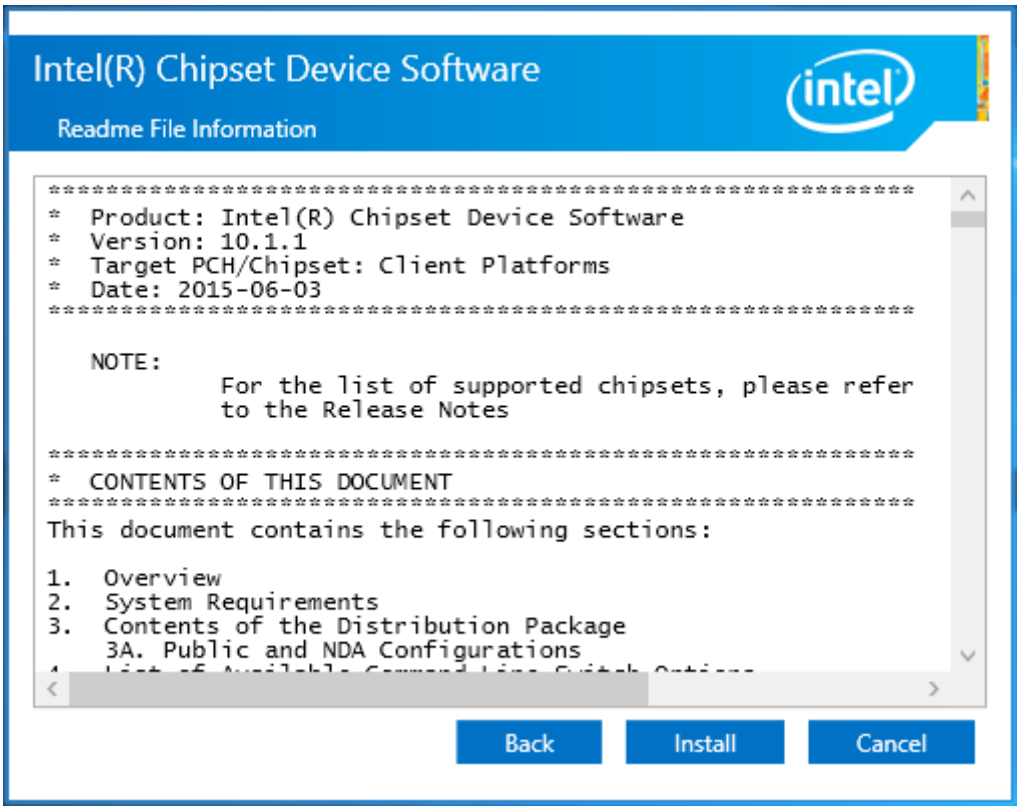
Step 2. Click **Next** to setup program.



Step 3. Read the license agreement. Click **Accept** to accept all of the terms of the license agreement.



Step 4. Click **Install** to begin the installation.



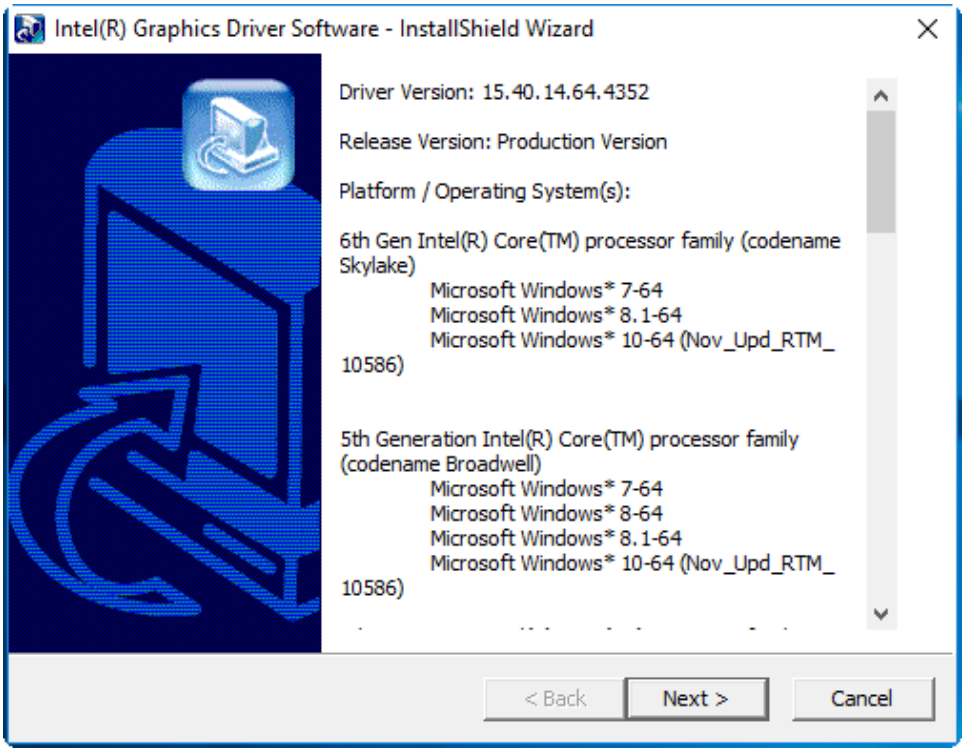
Step 5. Click **Restart Now** to complete the setup process. You must restart the computer which has been installed for the changes to take effects.

4.2 Intel(R) HD Graphics 530 Chipset Driver

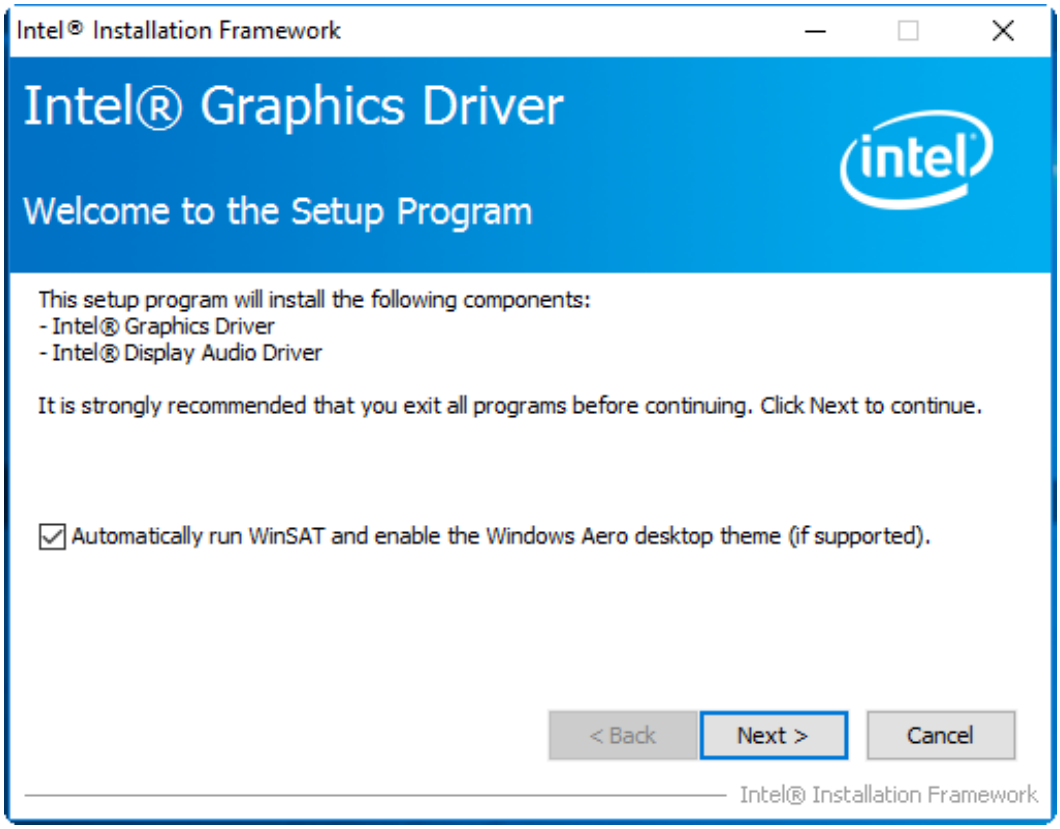
To install the HD Graphics 530 Chipset drivers, follow the steps below to proceed with the installation.

Step 1.Select **Intel(R) HD Graphics 530 Chipset** from the list.

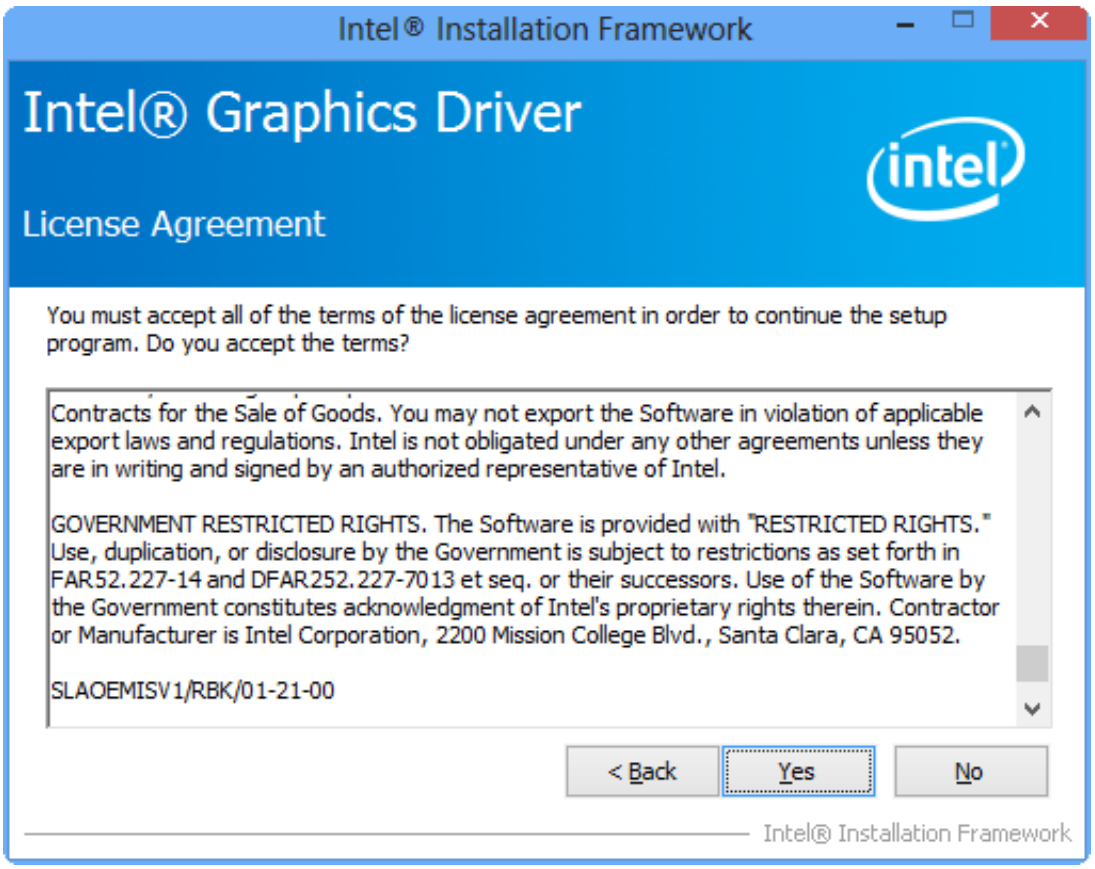
Step 2. Click **Next** to setup program**.**



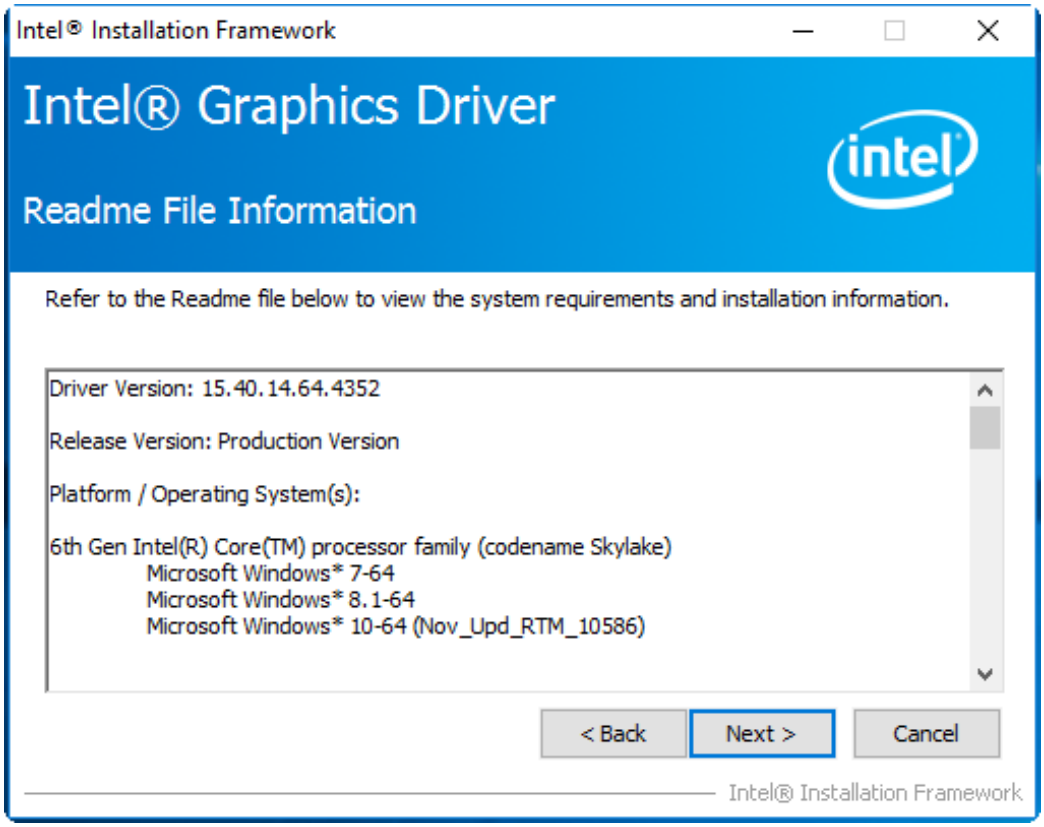
Step 3. Click **Next** to setup program**.**



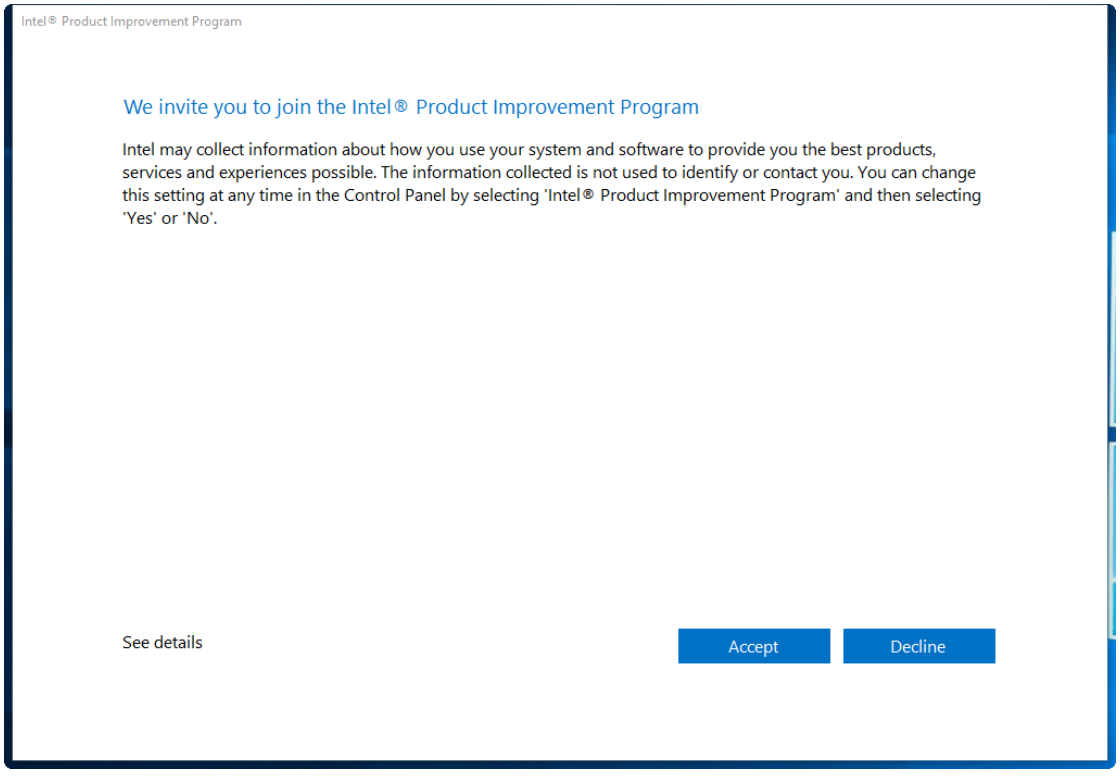
Step 4. Click **Yes** for agree the license in Intel Agreement.



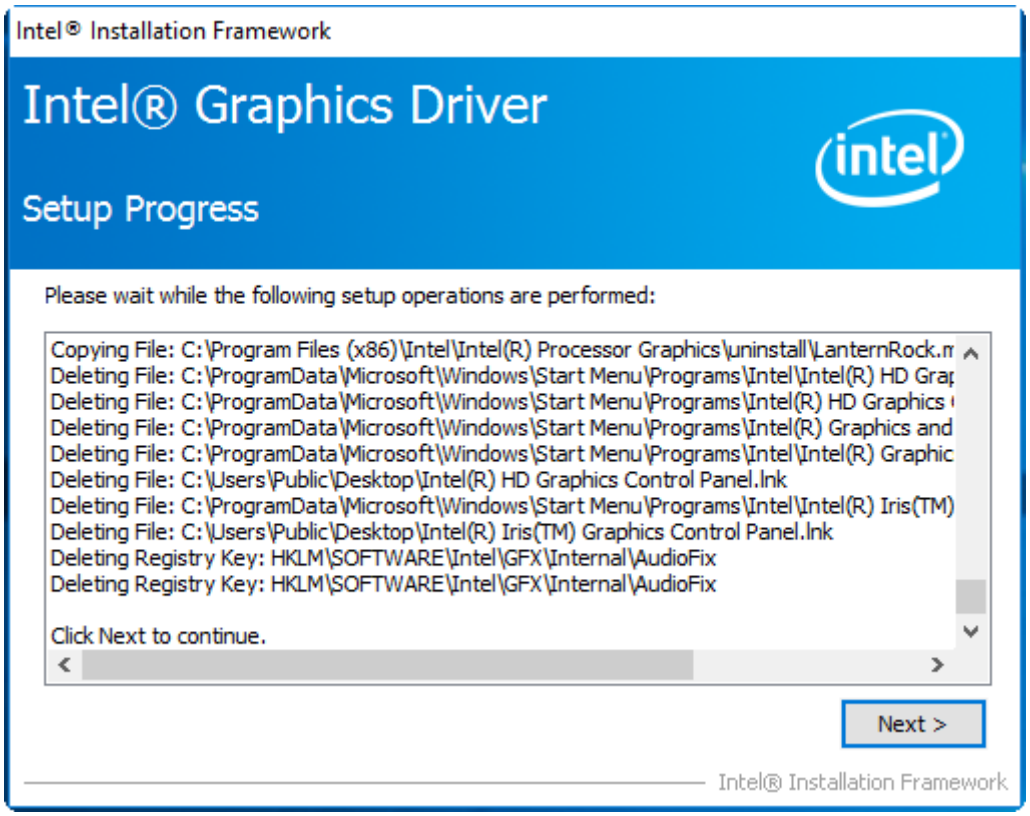
Step 5. Click **Next** to continue.



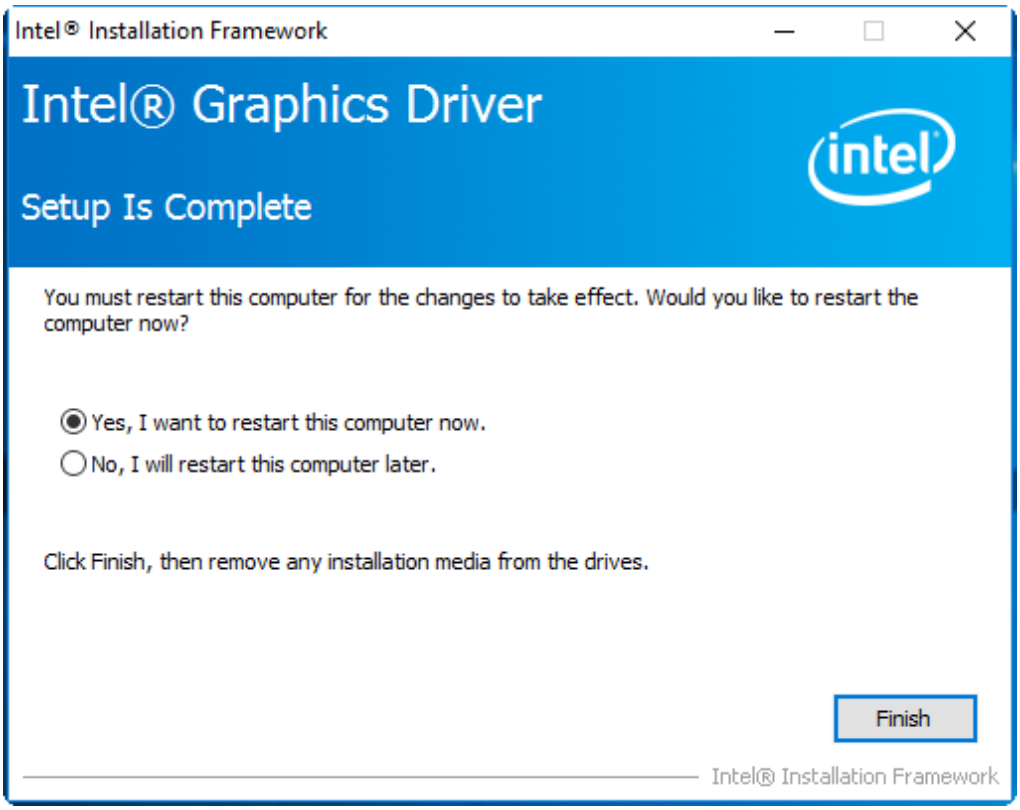
Step 6. You can choose **Accept** or **Decline** for join the intel® product improvement program. The Intel Company may collect information about how you use your system and software.



Step7. Click **Next** to continue.



Step8. Select **Yes, I want to restart this computer now.** Then click **Finish** to complete the installation.

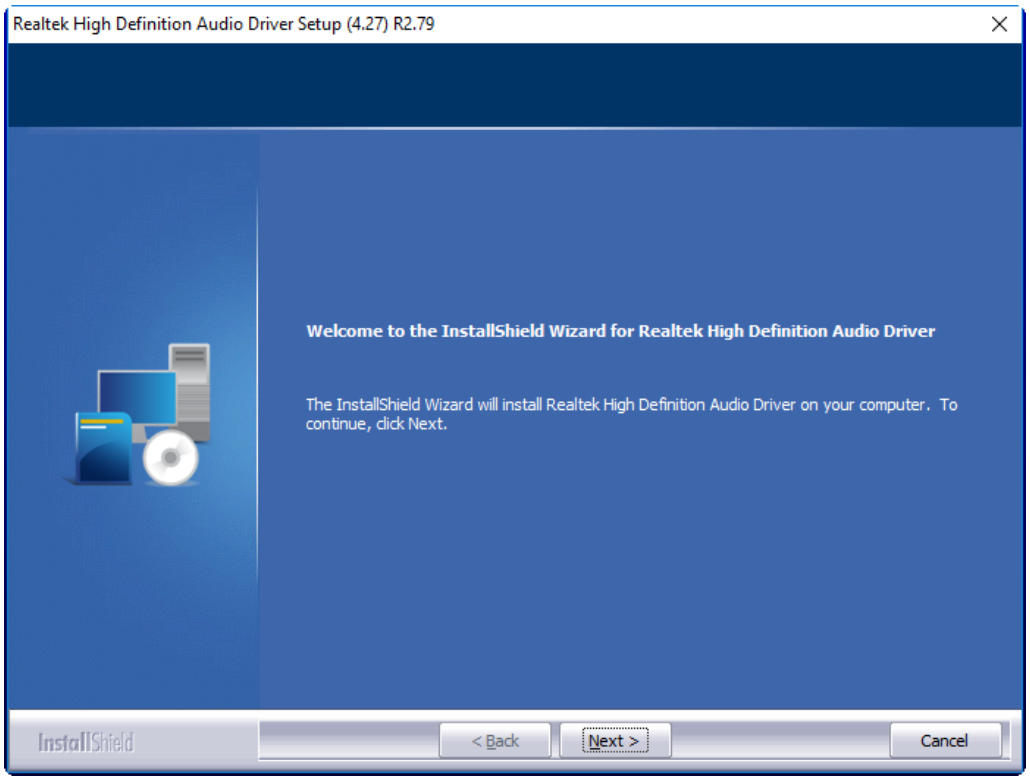


4.3 Realtek ALC269 HD Audio Driver

To install the Realtek ALC269 HD Audio Driver, please follow the steps below.

Step 1. Select **Realtek ALC269 HD Audio Driver** from the list

Step 2. Click **Next** to continue.



Step 3. Click **Yes, I want to restart my computer now**. Click **Finish** to complete the installation.