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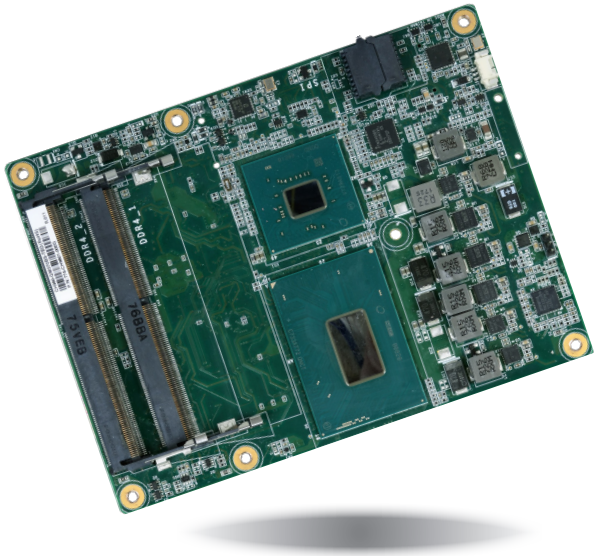

# CH960-CM246/QM370/HM370

## COM Express Basic Module
## User's Manual

A-486-M-2022

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## COM Express Specification Reference

PICMG® COM Express Module™ Base Specification.

https://www.picmg.org/

## FCC and DOC Statement on Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to Part 15 of the FCC rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and the receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio TV technician for help.

## Notice:

1. The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.
2. Shielded interface cables must be used in order to comply with the emission limits.

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## Warranty

1. Warranty does not cover damages or failures that arised from misuse of the product, inability to use the product, unauthorized replacement or alteration of components and product specifications.

2. The warranty is void if the product has been subjected to physical abuse, improper installation, modification, accidents or unauthorized repair of the product.

3. Unless otherwise instructed in this user's manual, the user may not, under any circumstances, attempt to perform service, adjustments or repairs on the product, whether in or out of warranty. It must be returned to the purchase point, factory or authorized service agency for all such work.

4. We will not be liable for any indirect, special, incidental or consequential damages to the product that has been modified or altered.

## Static Electricity Precautions

It is quite easy to inadvertently damage your PC, system board, components or devices even before installing them in your system unit. Static electrical discharge can damage computer components without causing any signs of physical damage. You must take extra care in handling them to ensure against electrostatic build-up.

1. To prevent electrostatic build-up, leave the system board in its anti-static bag until you are ready to install it.

2. Wear an antistatic wrist strap.

3. Do all preparation work on a static-free surface.

4. Hold the device only by its edges. Be careful not to touch any of the components, contacts or connections.

5. Avoid touching the pins or contacts on all modules and connectors. Hold modules or connectors by their ends.

**Important:**
Electrostatic discharge (ESD) can damage your processor, disk drive and other components. Perform the upgrade instruction procedures described at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

## Safety Measures

To avoid damage to the system:
- Use the correct AC input voltage range.

To reduce the risk of electric shock:
- Unplug the power cord before removing the system chassis cover for installation or servicing. After installation or servicing, cover the system chassis before plugging the power cord.

## About the Package

The package contains the following items. If any of these items are missing or damaged, please contact your dealer or sales representative for assistance.

- One CH960-CM246/QM370/HM370 board
- One Cooler (Height: 36.58mm)

## Optional Items

- COM332-B carrier board kit
- Heat spreader (Height: 11mm)

The board and accessories in the package may not come similar to the information listed above. This may differ in accordance with the sales region or models in which it was sold. For more information about the standard package in your region, please contact your dealer or sales representative.

## Before Using the System Board

Before using the system board, prepare basic system components.

If you are installing the system board in a new system, you will need at least the following internal components.

- Memory module
- Storage devices such as hard disk drive, etc.

You will also need external system peripherals you intend to use which will normally include at least a keyboard, a mouse and a video display monitor.

# Chapter 1 - Introduction

## Specifications

| | | |
|---|---|---|
| **SYSTEM** | Processor | 8th Generation Intel® Core™ Processors, BGA 1440<br>- Intel® Xeon® E-2176M, 6 Cores, 12M Cache, 2.7GHz (4.4GHz), 45W (CM246/QM370)<br>- Intel® Core™ i7-8850H, 6 Cores, 12M Cache, 2.6GHz (4.3GHz), 45W (CM246/QM370)<br>- Intel® Core™ i5-8400H, 4 Cores, 8M Cache, 2.5GHz (4.2GHz), 45W (CM246/QM370)<br>- Intel® Core™ i5-8400H, 4 Cores, 8M Cache, 2.5GHz (4.2GHz), 45W (HM370)<br>9th Generation Intel® Processors, BGA 1440<br>- Intel® Xeon® E-2276ML, 6 Cores, 12M Cache, 2.0GHz (4.2GHz), 25W (CM246)<br>- Intel® Xeon® E-2276ME, 6 Cores, 12M Cache, 2.8GHz (4.5GHz), 45W (CM246)<br>- Intel® Xeon® E-2254ML, 4 Cores, 8M Cache, 1.7GHz (3.5GHz), 25W (CM246)<br>- Intel® Xeon® E-2254ME, 4 Cores, 8M Cache, 2.6GHz (3.8GHz), 45W (CM246)<br>- Intel® Core™ i7-9850HL, 6 Cores, 9M Cache, 1.9GHz (4.1GHz), 25W (QM370)<br>- Intel® Core™ i7-9850HE, 6 Cores, 9M Cache, 2.7GHz (4.4GHz), 45W (QM370)<br>- Intel® Core™ i3-9100HL, 4 Cores, 6M Cache, 1.6GHz (2.9GHz), 25W (HM370)<br>- Intel® Celeron® G4930E, 2 Cores, 2M Cache, 2.4GHz (2.4GHz), 35W (CM246)<br>- Intel® Celeron® G4932E, 2 Cores, 2M Cache, 1.9GHz (1.9GHz), 25W (HM370) |
| | Chipset | Intel® CM246/QM370/HM370 Chipset |
| | Memory | CH960-CM246/QM370:<br>Two 260-pin SODIMM up to 64GB<br>Dual Channel DDR4 2666MHz (ECC Support with CM246)<br><br>CH960-HM370:<br>Two 260-pin SODIMM up to 64GB<br>Dual Channel DDR4 2666MHz |
| | BIOS | AMI SPI 128Mbit |
| **GRAPHICS** | Controller | Intel® HD Graphics |
| | Feature | OpenGL up to 4.5, DirectX 11, OpenCL 2.1<br>HW Decode: HEVC/H.265, H.264, M/JPEG, MPEG2, VC1/WMV9, VP8 (8-bit), VP9 (10-bit)<br>HW Encode: HEVC/H.265, M/JPEG, MPEG2, VP8 |
| | Display | 1 x VGA/DDI (DDI available upon request)<br>1 x LVDS/eDP (eDP available upon request)<br>2 x DDI (HDMI/DVI/DP++)<br>VGA: resolution up to 1920x1200 @ 60Hz<br>LVDS: dual channel 24-bit, resolution up to 1920x1200 @ 60Hz<br>HDMI: resolution up to 4096x2160 @ 30Hz 24bpp<br>DVI: resolution up to 1920x1200 @ 60Hz<br>DP++/eDP: resolution up to 4096x2304 @ 60Hz |
| | Triple Displays | VGA + LVDS + DDI or VGA + DDI1 + DDI2<br>eDP + 2 DDI (available upon request) |
| **EXPANSION** | Interface | 1 x PCIe x16, 8 x PCIe x1<br>1 x LPC<br>1 x I²C<br>1 x SMBus<br>2 x UART (TX/RX) |

| | | |
|---|---|---|
| **AUDIO** | Interface | HD Audio |
| **ETHERNET** | Controller | CH960-CM246/QM370:<br>1 x Intel® I219LM with iAMT12.0 PCIe (10/100/1000Mbps)<br><br>CH960-HM370:<br>1 x Intel® I219LM PCIe (10/100/1000Mbps) |
| **I/O** | USB | 4 x USB 3.1<br>8 x USB 2.0 |
| | SATA | CH960-CM246/QM370:<br>4 x SATA 3.0 (up to 6Gb/s)<br>RAID 0/1/5/10<br><br>CH960-HM370:<br>4 x SATA 3.0 (up to 6Gb/s) |
| | DIO | 1 x 8-bit DIO (Default 4 inputs and 4 outputs) |
| **WATCHDOG TIMER** | Output & Interval | System Reset, Programmable via Software from 1 to 255 Seconds |
| **SECURITY** | TPM | Available upon request |
| **POWER** | Type | 12V, 5VSB, VCC_RTC (ATX mode)<br>12V, VCC_RTC (AT mode) |
| **OS SUPPORT** | | Windows: Windows 10 IoT Enterprise 64-bit<br>Linux: Ubuntu 18.04 |
| **ENVIRONMENT** | Temperature | Operating: 0 to 60°C or -40 to 85°C (with heat spreader)<br>Storage: -40 to 85°C |
| | Humidity | Operating: 5 to 90% RH<br>Storage: 5 to 90% RH |
| **MECHANICAL** | Dimensions | COM Express® Basic<br>95mm (3.74") x 125mm (4.9") |
| | Compliance | PICMG COM Express® R2.1, Type 6 |
| **CERTIFICATION** | Certification | CE, FCC, RoHS |

**Note:** The specifications listed here may be based on previous revisions of the system. Please go to www.dfi.com for the latest specifications.

## Features

### • Watchdog Timer

The Watchdog Timer function allows your application to regularly "clear" the system at the set time interval. If the system hangs or fails to function, it will reset at the set time interval so that your system will continue to operate.

### • DDR4

DDR4 delivers increased system bandwidth and improves performance at a lower power than DDR3/DDR2.

### • Graphics

The integrated Intel® HD engine delivers an excellent blend of graphics performance and features to meet business needs. It delivers enhanced media conversion rates and higher frame rates on 4K Ultra HD videos. These enhancements deliver the performance and compatibility to meet the demand for business and home entertainment applications. The system supports 1 x VGA/DDI (DDI available upon request), 1 x LVDS/eDP (eDP available upon request) and 2 x DDI (HDMI/DVI/DP++) display outputs.

### • Serial ATA

Serial ATA is a storage interface that is compliant with SATA 1.0a specification. With speed of up to 6Gb/s (SATA 3.0), it improves hard drive performance faster than the standard parallel ATA whose data transfer rate is 100MB/s. However, the bandwidth of the SATA 3.0 will be limited by carrier board design.

### • Gigabit LAN

The Intel® I219LM Gigabit LAN PHY controller features up to 1Gbps data transmission.

### • USB

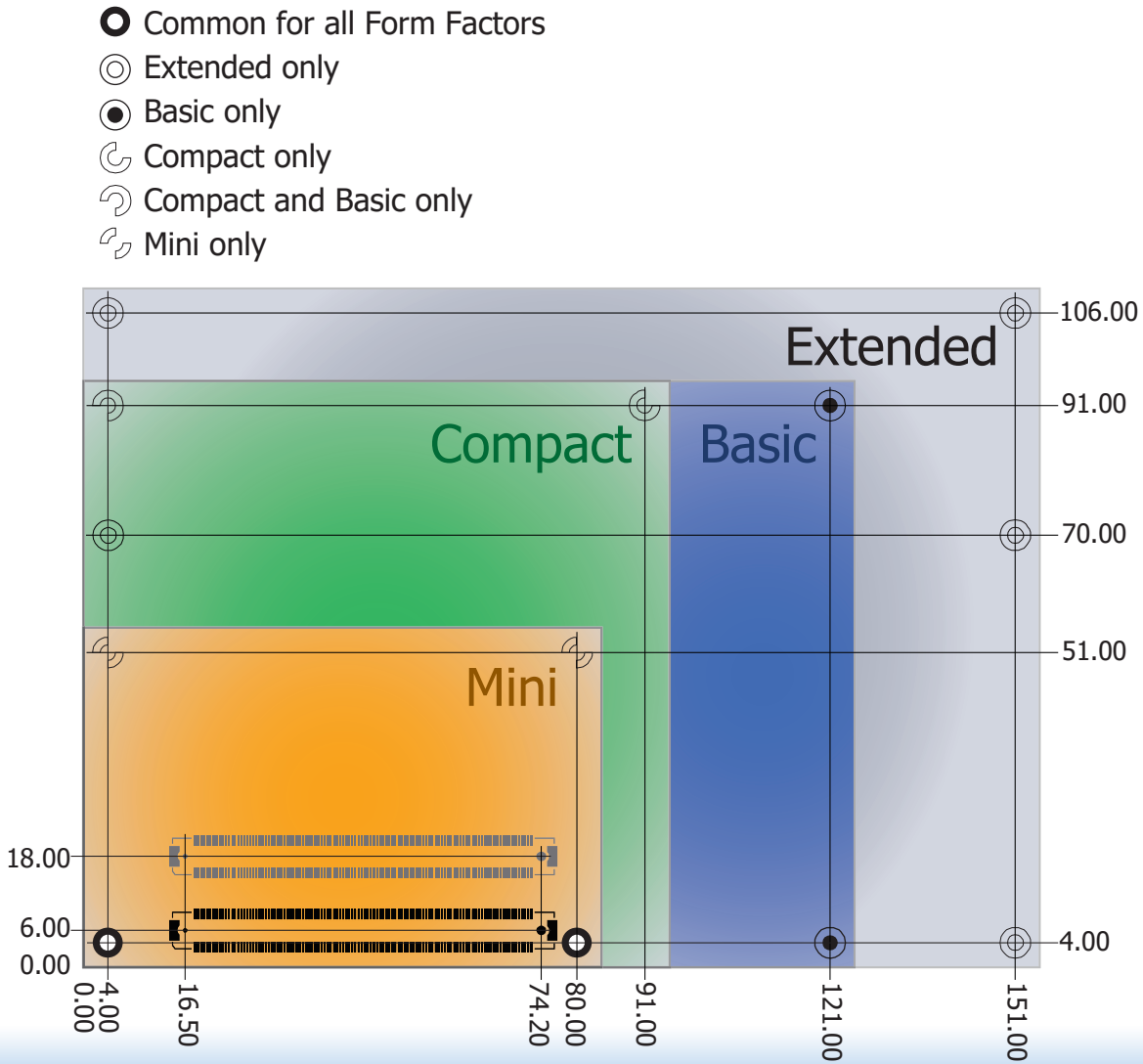
The system board supports the new USB 3.1 Gen2. It is capable of running at a maximum transmission speed of up to 10 Gbit/s (1280 MB/s) and is faster than USB 3.1 Gen1 (5 Gbit/s, or 625 MB/s), USB 2.0 (480 Mbit/s, or 60 MB/s) and USB 1.1 (12 Mbit/s). USB 3.1 reduces the time required for data transmission, reduces power consumption, and is backward compatible with USB 2.0. It is a marked improvement in device transfer speeds between your computer and a wide range of simultaneously accessible external Plug and Play peripherals.

# Chapter 2 - Concept

## COM Express Module Standards

The figure below shows the dimensions of the different types of COM Express modules.

CH960-CM246/QM370/HM370 is a COM Express Basic module. Its dimension is 95mm x 125mm.



## Specification Comparison Table

The table below shows the COM Express standard specifications and the corresponding specifications supported on the CH960-CM246/QM370/HM370 module.

Module Pin-out - Required and Optional Features A-B Connector.

| Connector | Feature | COM Express Module Base Specification Type 6 (No IDE or PCI, add DDI+ USB3) Min / Max | DFI CH960 Type 6 |
|---|---|---|---|
| A-B | **System I/O** | | |
| A-B | PCI Express Lanes 0 - 5 | 1 / 6 | 6 |
| A-B | LVDS Channel A | 0 / 1 | 1 |
| A-B | LVDS Channel B | 0 / 1 | 1 |
| A-B | eDP on LVDS CH A pins | 0 / 1 | 1 |
| A-B | VGA Port | 0 / 1 | 1 |
| A-B | TV-Out | NA | NA |
| A-B | DDI 0 | NA | NA |
| A-B[5] | Serial Ports 1 - 2 | 0 / 2 | 2 |
| A-B | CAN interface on SER1 | 0 / 1 | 0 |
| A-B | SATA / SAS Ports | 1 / 4 | 4 |
| A-B | AC'97 / HDA Digital Interface | 0 / 1 | 1 |
| A-B | USB 2.0 Ports | 4 / 8 | 8 |
| A-B | USB Client | 0 / 1 | 0 |
| A-B | USB 3.0 Ports | NA | NA |
| A-B | LAN Port 0 | 1 / 1 | 1 |
| A-B | Express Card Support | 1 / 2 | 2 |
| A-B | LPC Bus | 1 / 1 | 1 |
| A-B | SPI | 1 / 2 | 1 |
| A-B | **System Management** | | |
| A-B[6] | SDIO (muxed on GPIO) | 0 / 1 | NA |
| | General Purpose I/O | 8 / 8 | 8 |
| A-B | SMBus | 1 / 1 | 1 |
| A-B | I2C | 1 / 1 | 1 |
| A-B | Watchdog Timer | 0 / 1 | 1 |
| A-B | Speaker Out | 1 / 1 | 1 |
| A-B | External BIOS ROM Support | 0 / 2 | 1 |
| A-B | Reset Functions | 1 / 1 | 1 |

- [5] Indicates 12V-tolerant features on former VCC_12V signals.
- [6] Cells in the connected columns spanning rows provide a rough approximation of features sharing connector pins.

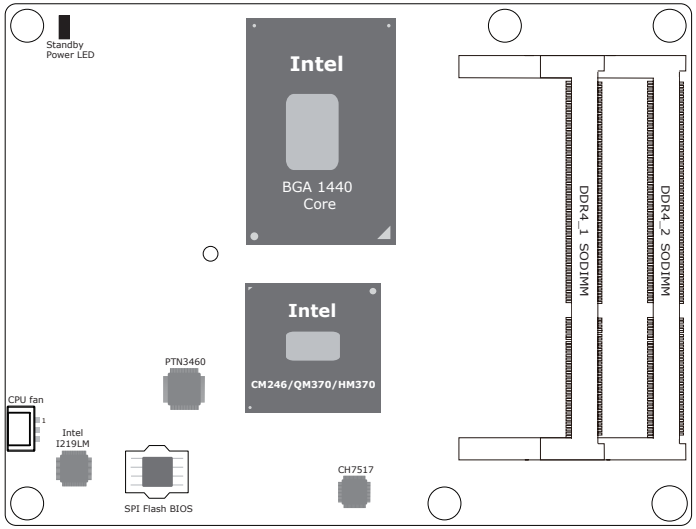
| Connector | Feature | COM Express Module Base Specification Type 6 (No IDE or PCI, add DDI+ USB3) Min / Max | DFI CH960 Type 6 |
|---|---|---|---|
| A-B | **Power Management** | | |
| A-B | Thermal Protection | 0 / 1 | 1 |
| A-B | Battery Low Alarm | 0 / 1 | 1 |
| A-B | Suspend/Wake Signals | 0 / 3 | 2 |
| A-B | Power Button Support | 1 / 1 | 1 |
| A-B | Power Good | 1 / 1 | 1 |
| A-B | VCC_5V_SBY Contacts | 4 / 4 | 4 |
| A-B[5] | Sleep Input | 0 / 1 | 1 |
| A-B[5] | Lid Input | 0 / 1 | 1 |
| A-B[5] | Fan Control Signals | 0 / 2 | 1 |
| A-B | Trusted Platform Modules | 0 / 1 | 1 (optional) |
| A-B | **Power** | | |
| A-B | VCC_12V Contacts | 12 / 12 | 12 |

Module Pin-out - Required and Optional Features C-D Connector.

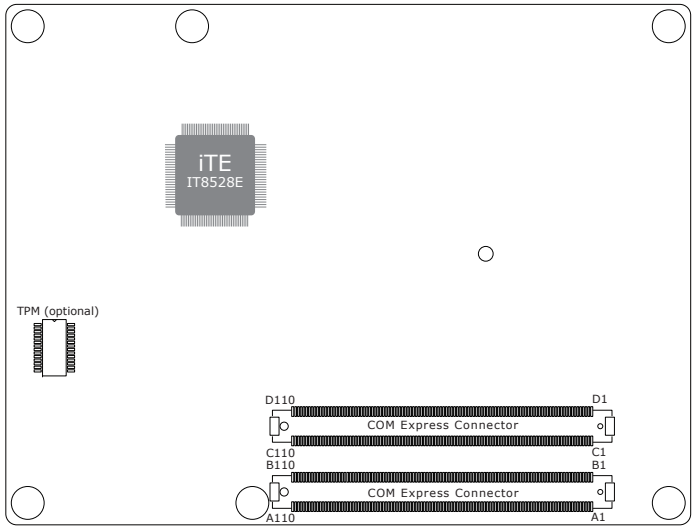
| Connector | Feature | COM Express Module Base Specification Type 6 (No IDE or PCI, add DDI+ USB3) Min / Max | DFI CH960 Type 6 |
|---|---|---|---|
| C-D | **System I/O** | | |
| | PCI Express Lanes 16 - 31 | 0 / 16 | 16 |
| | PCI Express Graphics (PEG) | 0 / 1 | 1 |
| C-D[6] | Muxed SDVO Channels 1 - 2 | NA | NA |
| | PCI Express Lanes 6 - 15 | 0 / 2 | 2 |
| | PCI Bus - 32 Bit | NA | NA |
| | PATA Port | NA | NA |
| | LAN Ports 1 - 2 | NA | NA |
| | DDIs 1 - 3 | 0 / 3 | 3 (DDI3 option) |
| C-D[6] | USB 3.1 Ports | 0 / 4 | 4 |
| C-D | **Power** | | |
| C-D | VCC_12V Contacts | 12 / 12 | 12 |

# Chapter 3 - Hardware Installation

## Board Layout

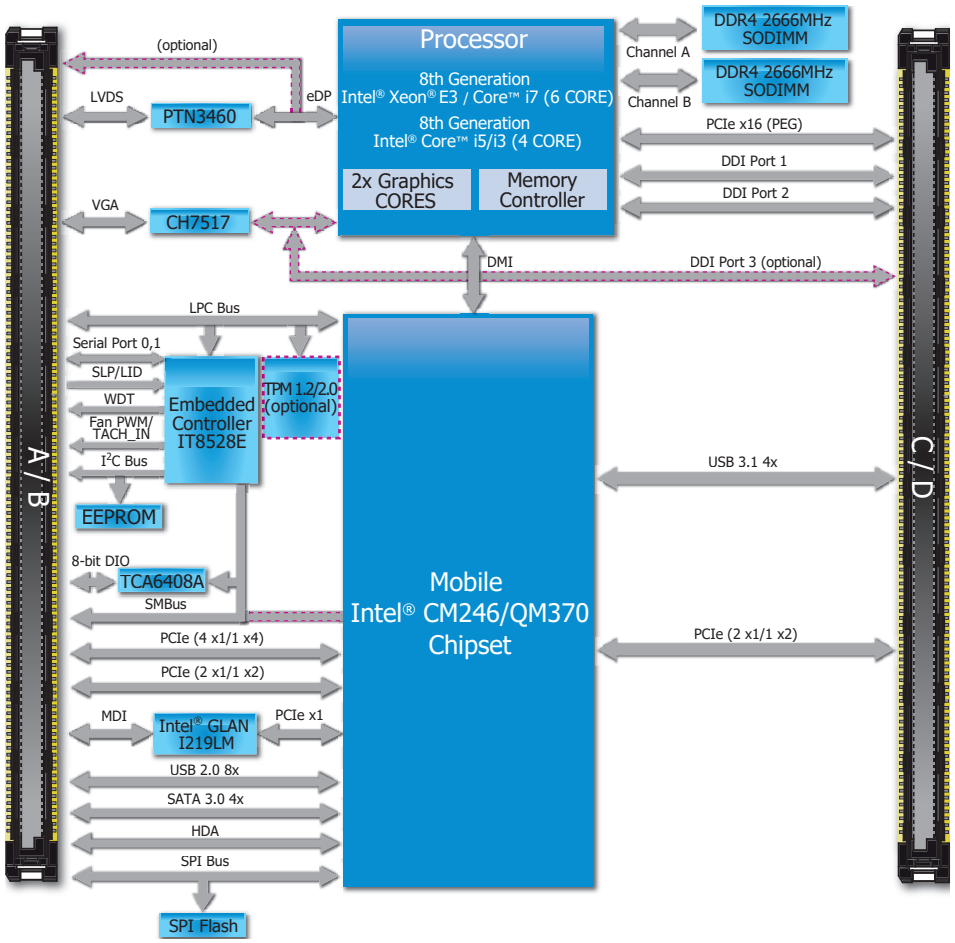



Top View

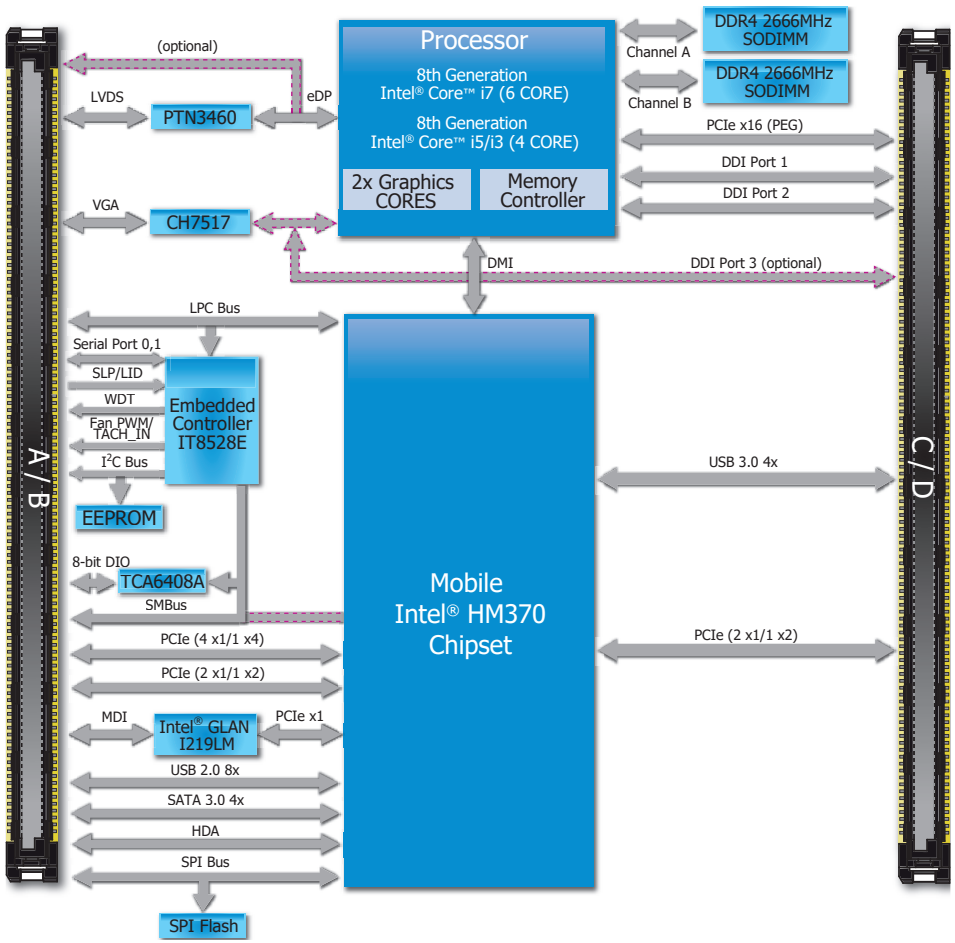



Bottom View

## Block Diagram




CH960-CM246/QM370

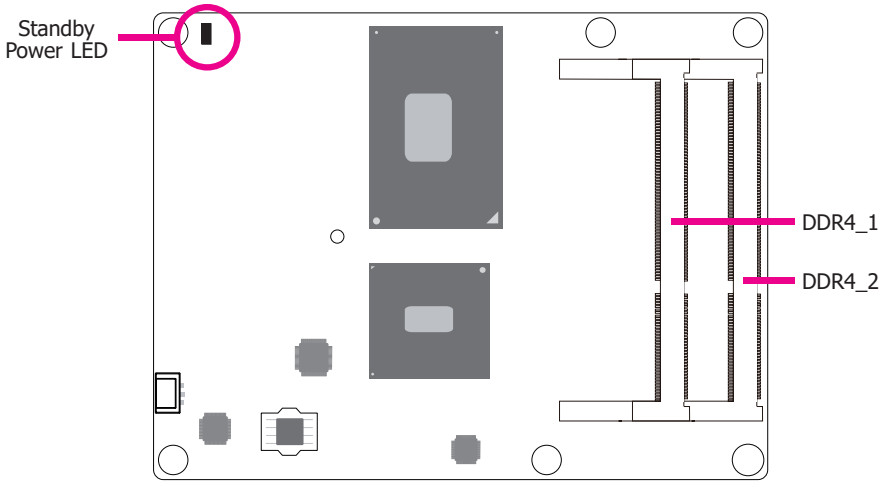



CH960-HM370

**Important:**
Electrostatic discharge (ESD) can damage your board, processor, disk drives, add-in boards, and other components. Perform installation procedures at an ESD workstation only. If such a station is not available, you can provide some ESD protection by wearing an antistatic wrist strap and attaching it to a metal part of the system chassis. If a wrist strap is unavailable, establish and maintain contact with the system chassis throughout any procedures requiring ESD protection.

## System Memory

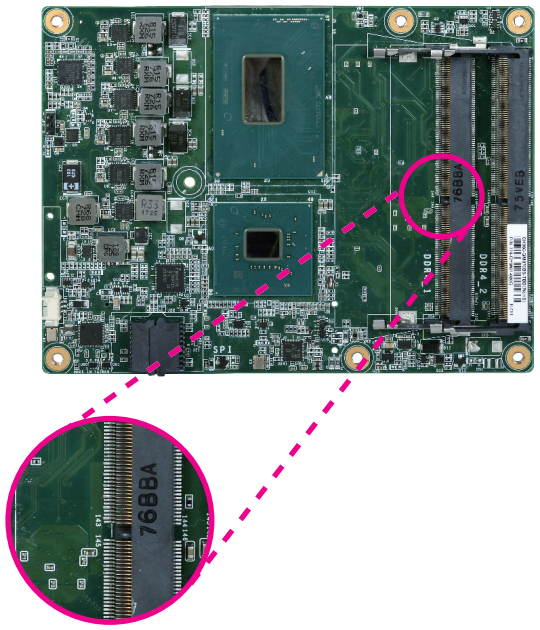
**Important:**
When the Standby Power LED is red, it indicates that there is power on the board. Power off the PC then unplug the power cord prior to installing any devices. Failure to do so will cause severe damage to the board and components.



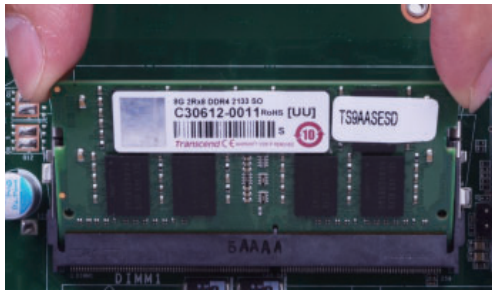

## Installing the SODIMM Module

**Note:**
The system board used in the following illustrations may not resemble the actual one. These illustrations are for reference only.

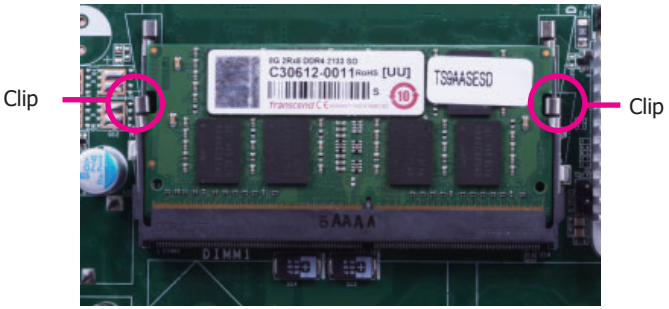
1. Make sure the PC and all other peripheral devices connected to it has been powered down.
2. Disconnect all power cords and cables.
3. Locate the SODIMM socket on the system board.
4. Note the key on the socket. The key ensures that the module can be plugged into the socket in only one direction.



5. Grasping the module by its edges, align the module into the socket at an approximately 30 degrees angle. Apply firm even pressure to each end of the module until it slips down into the socket. The contact fingers on the edge of the module will almost completely disappear inside the socket.

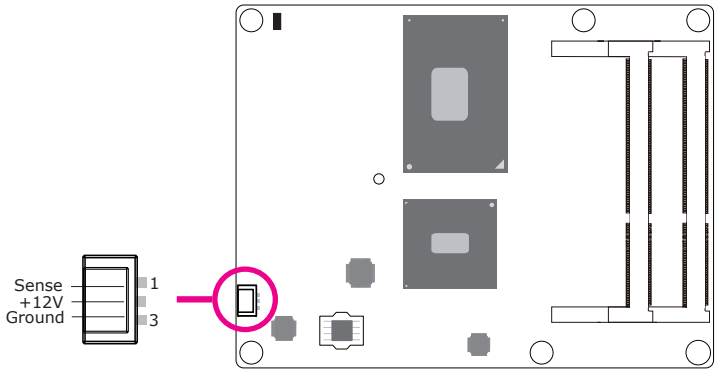



6. Push down the module until the clips at each end of the socket lock into position. You will hear a distinctive "click", indicating the module is correctly locked into position.




## Connectors

### CPU Fan Connector




Connect the CPU fan's cable connector to the CPU fan connector on the board. The cooling fan will provide adequate airflow throughout the chassis to prevent overheating the CPU and board components.

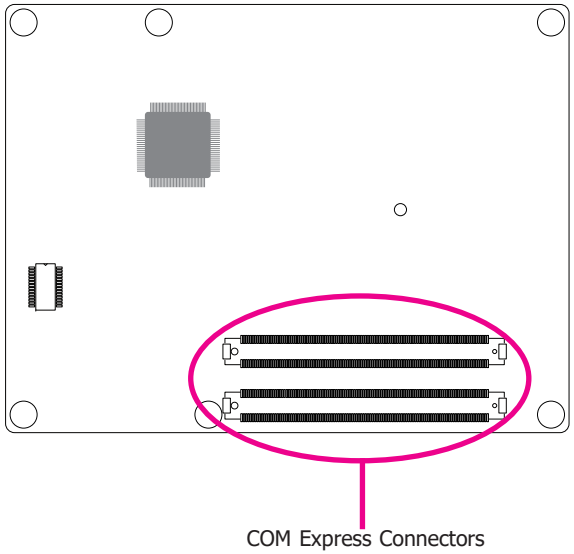
#### BIOS Setting

Configure the speed of the CPU fan in the "PC Health Status" submenu in the Advanced menu of the BIOS.

## COM Express Connectors

The COM Express connectors are used to interface the CH960-CM246/QM370/HM370 COM Express board to a carrier board. Connect the COM Express connectors (located on the solder side of the board) to the COM Express connectors on the carrier board.

Refer to the "Installing CH960-CM246/QM370/HM370 onto a Carrier Board" section for more information.




Refer to the following page for the pin functions of these connectors.

## COM Express Connectors-Continued

| Row A | | Row B | | Row A | | Row B | |
|---|---|---|---|---|---|---|---|
| A1 | GND (FIXED) | B1 | GND (FIXED) | A56 | PCIE_TX4- | B56 | PCIE_RX4- |
| A2 | GBE0_MDI3- | B2 | GBE0_ACT# | A57 | GND | B57 | GPO2 |
| A3 | GBE0_MDI3+ | B3 | LPC_FRAME# | A58 | PCIE_TX3+ | B58 | PCIE_RX3+ |
| A4 | GBE0_LINK100# | B4 | LPC_AD0 | A59 | PCIE_TX3- | B59 | PCIE_RX3- |
| A5 | GBE0_LINK1000# | B5 | LPC_AD1 | A60 | GND (FIXED) | B60 | GND (FIXED) |
| A6 | GBE0_MDI2- | B6 | LPC_AD2 | A61 | PCIE_TX2+ | B61 | PCIE_RX2+ |
| A7 | GBE0_MDI2+ | B7 | LPC_AD3 | A62 | PCIE_TX2- | B62 | PCIE_RX2- |
| A8 | GBE0_LINK# | B8 | LPC_DRQ0# | A63 | GPI1 | B63 | GPO3 |
| A9 | GBE0_MDI1- | B9 | LPC_DRQ1# | A64 | PCIE_TX1+ | B64 | PCIE_RX1+ |
| A10 | GBE0_MDI1+ | B10 | LPC_CLK | A65 | PCIE_TX1- | B65 | PCIE_RX1- |
| A11 | GND (FIXED) | B11 | GND (FIXED) | A66 | GND | B66 | WAKE0# |
| A12 | GBE0_MDI0- | B12 | PWRBTN# | A67 | GPI2 | B67 | WAKE1# |
| A13 | GBE0_MDI0+ | B13 | SMB_CK | A68 | PCIE_TX0+ | B68 | PCIE_RX0+ |
| A14 | NC | B14 | SMB_DAT | A69 | PCIE_TX0- | B69 | PCIE_RX0- |
| A15 | SUS_S3# | B15 | SMB_ALERT# | A70 | GND (FIXED) | B70 | GND (FIXED) |
| A16 | SATA0_TX+ | B16 | SATA1_TX+ | A71 | LVDS_A0+/eDP_TX2+ | B71 | LVDS_B0+ |
| A17 | SATA0_TX- | B17 | SATA1_TX- | A72 | LVDS_A0-/eDP_TX2- | B72 | LVDS_B0- |
| A18 | SUS_S4# | B18 | SUS_STAT# | A73 | LVDS_A1+/eDP_TX1+ | B73 | LVDS_B1+ |
| A19 | SATA0_RX+ | B19 | SATA1_RX+ | A74 | LVDS_A1-/eDP_TX1- | B74 | LVDS_B1- |
| A20 | SATA0_RX- | B20 | SATA1_RX- | A75 | LVDS_A2+/eDP_TX0+ | B75 | LVDS_B2+ |
| A21 | GND (FIXED) | B21 | GND (FIXED) | A76 | LVDS_A2-/eDP_TX0- | B76 | LVDS_B2- |
| A22 | SATA2_TX+ | B22 | SATA3_TX+ | A77 | LVDS_VDD_EN/eDP_VDD_EN | B77 | LVDS_B3+ |
| A23 | SATA2_TX- | B23 | SATA3_TX- | A78 | LVDS_A3+ | B78 | LVDS_B3- |
| A24 | SUS_S5# | B24 | PWR_OK | A79 | LVDS_A3- | B79 | LVDS_BKLT_EN/eDP_BKLT_EN |
| A25 | SATA2_RX+ | B25 | SATA3_RX+ | A80 | GND (FIXED) | B80 | GND (FIXED) |
| A26 | SATA2_RX- | B26 | SATA3_RX- | A81 | LVDS_A_CK+/eDP_TX3+ | B81 | LVDS_B_CK+ |
| A27 | BATLOW# | B27 | WDT | A82 | LVDS_A_CK-/eDP_TX3- | B82 | LVDS_B_CK- |
| A28 | (S)ATA_ACT# | B28 | NC | A83 | LVDS_I2C_CK/eDP_AUX+ | B83 | LVDS_BKLT_CTRL/eDP_BKLT_CTRL |
| A29 | AC/HDA_SYNC | B29 | AC/HDA _SDIN1 | A84 | LVDS_I2C_DAT/eDP_AUX- | B84 | VCC_5V_SBY |
| A30 | AC/HDA _RST# | B30 | AC/HDA _SDIN0 | A85 | GPI3 | B85 | VCC_5V_SBY |
| A31 | GND (FIXED) | B31 | GND (FIXED) | A86 | RSVD | B86 | VCC_5V_SBY |
| A32 | AC/HDA _BITCLK | B32 | SPKR | A87 | RSVD/eDP_HPD | B87 | VCC_5V_SBY |
| A33 | AC/HDA _SDOUT | B33 | I2C_CK | A88 | PCIE0_CLK_REF+ | B88 | BIOS_DIS1# |
| A34 | BIOS_DIS0# | B34 | I2C_DAT | A89 | PCIE0_CLK_REF- | B89 | VGA_RED |
| A35 | THRMTRIP# | B35 | THRM# | A90 | GND (FIXED) | B90 | GND (FIXED) |
| A36 | USB6- | B36 | USB7- | A91 | SPI_POWER | B91 | VGA_GRN |
| A37 | USB6+ | B37 | USB7+ | A92 | SPI_MISO | B92 | VGA_BLU |
| A38 | USB_6_7_OC# | B38 | USB_4_5_OC# | A93 | GPO0 | B93 | VGA_HSYNC |
| A39 | USB4- | B39 | USB5- | A94 | SPI_CLK | B94 | VGA_VSYNC |
| A40 | USB4+ | B40 | USB5+ | A95 | SPI_MOSI | B95 | VGA_I2C_CK |
| A41 | GND (FIXED) | B41 | GND (FIXED) | A96 | TPM_PP | B96 | VGA_I2C_DAT |
| A42 | USB2- | B42 | USB3- | A97 | NC | B97 | SPI_CS# |
| A43 | USB2+ | B43 | USB3+ | A98 | SER0_TX | B98 | RSVD |
| A44 | USB_2_3_OC# | B44 | USB_0_1_OC# | A99 | SER0_RX | B99 | RSVD |
| A45 | USB0- | B45 | USB1- | A100 | GND (FIXED) | B100 | GND (FIXED) |
| A46 | USB0+ | B46 | USB1+ | A101 | SER1_TX | B101 | FAN_PWMOUT |
| A47 | VCC_RTC | B47 | EXCD1_PERST# | A102 | SER1_RX | B102 | FAN_TACHIN |
| A48 | EXCD0_PERST# | B48 | EXCD1_CPPE# | A103 | LID# | B103 | SLEEP# |
| A49 | EXCD0_CPPE# | B49 | SYS_RESET# | A104 | VCC_12V | B104 | VCC_12V |
| A50 | LPC_SERIRQ | B50 | CB_RESET# | A105 | VCC_12V | B105 | VCC_12V |
| A51 | GND (FIXED) | B51 | GND (FIXED) | A106 | VCC_12V | B106 | VCC_12V |
| A52 | PCIE_TX5+ | B52 | PCIE_RX5+ | A107 | VCC_12V | B107 | VCC_12V |
| A53 | PCIE_TX5- | B53 | PCIE_RX5- | A108 | VCC_12V | B108 | VCC_12V |
| A54 | GPI0 | B54 | GPO1 | A109 | VCC_12V | B109 | VCC_12V |
| A55 | PCIE_TX4+ | B55 | PCIE_RX4+ | A110 | GND (FIXED) | B110 | GND (FIXED) |

| Row C | | Row D | | Row C | | Row D | |
|---|---|---|---|---|---|---|---|
| C1 | GND (FIXED) | D1 | GND (FIXED) | C56 | PEG_RX1- | D56 | PEG_TX1- |
| C2 | GND | D2 | GND | C57 | NC | D57 | GND |
| C3 | USB_SSRX0- | D3 | USB_SSTX0- | C58 | PEG_RX2+ | D58 | PEG_TX2+ |
| C4 | USB_SSRX0+ | D4 | USB_SSTX0+ | C59 | PEG_RX2- | D59 | PEG_TX2- |
| C5 | GND | D5 | GND | C60 | GND (FIXED) | D60 | GND (FIXED) |
| C6 | USB_SSRX1- | D6 | USB_SSTX1- | C61 | PEG_RX3+ | D61 | PEG_TX3+ |
| C7 | USB_SSRX1+ | D7 | USB_SSTX1+ | C62 | PEG_RX3- | D62 | PEG_TX3- |
| C8 | GND | D8 | GND | C63 | RSVD | D63 | RSVD |
| C9 | USB_SSRX2- | D9 | USB_SSTX2- | C64 | RSVD | D64 | RSVD |
| C10 | USB_SSRX2+ | D10 | USB_SSTX2+ | C65 | PEG_RX4+ | D65 | PEG_TX4+ |
| C11 | GND (FIXED) | D11 | GND (FIXED) | C66 | PEG_RX4- | D66 | PEG_TX4- |
| C12 | USB_SSRX3- | D12 | USB_SSTX3- | C67 | RSVD | D67 | GND |
| C13 | USB_SSRX3+ | D13 | USB_SSTX3+ | C68 | PEG_RX5+ | D68 | PEG_TX5+ |
| C14 | GND | D14 | GND | C69 | PEG_RX5- | D69 | PEG_TX5- |
| C15 | NA, no support | D15 | DDI1_CTRLCLK_AUX+ | C70 | GND (FIXED) | D70 | GND (FIXED) |
| C16 | NA, no support | D16 | DDI1_CTRLDATA_AUX- | C71 | PEG_RX6+ | D71 | PEG_TX6+ |
| C17 | RSVD | D17 | RSVD | C72 | PEG_RX6- | D72 | PEG_TX6- |
| C18 | RSVD | D18 | RSVD | C73 | GND | D73 | GND |
| C19 | PCIE_RX6+ | D19 | PCIE_TX6+ | C74 | PEG_RX7+ | D74 | PEG_TX7+ |
| C20 | PCIE_RX6- | D20 | PCIE_TX6- | C75 | PEG_RX7- | D75 | PEG_TX7- |
| C21 | GND (FIXED) | D21 | GND (FIXED) | C76 | GND | D76 | GND |
| C22 | PCIE_RX7+ | D22 | PCIE_TX7+ | C77 | RSVD | D77 | RSVD |
| C23 | PCIE_RX7- | D23 | PCIE_TX7- | C78 | PEG_RX8+ | D78 | PEG_TX8+ |
| C24 | DDI1_HPD | D24 | RSVD | C79 | PEG_RX8- | D79 | PEG_TX8- |
| C25 | NA, no support | D25 | RSVD | C80 | GND (FIXED) | D80 | GND (FIXED) |
| C26 | NA, no support | D26 | DDI1_PAIR0+ | C81 | PEG_RX9+ | D81 | PEG_TX9+ |
| C27 | RSVD | D27 | DDI1_PAIR0- | C82 | PEG_RX9- | D82 | PEG_TX9- |
| C28 | RSVD | D28 | RSVD | C83 | RSVD | D83 | RSVD |
| C29 | NA, no support | D29 | DDI1_PAIR1+ | C84 | GND | D84 | GND |
| C30 | NA, no support | D30 | DDI1_PAIR1- | C85 | PEG_RX10+ | D85 | PEG_TX10+ |
| C31 | GND (FIXED) | D31 | GND (FIXED) | C86 | PEG_RX10- | D86 | PEG_TX10- |
| C32 | DDI2_CTRLCLK_AUX+ | D32 | DDI1_PAIR2+ | C87 | GND | D87 | GND |
| C33 | DDI2_CTRLDATA_AUX- | D33 | DDI1_PAIR2- | C88 | PEG_RX11+ | D88 | PEG_TX11+ |
| C34 | DDI2_DDC_AUX_SEL | D34 | DDI1_DDC_AUX_SEL | C89 | PEG_RX11- | D89 | PEG_TX11- |
| C35 | RSVD | D35 | RSVD | C90 | GND (FIXED) | D90 | GND (FIXED) |
| C36 | DDI3_CTRLCLK_AUX+ | D36 | DDI1_PAIR3+ | C91 | PEG_RX12+ | D91 | PEG_TX12+ |
| C37 | DDI3_CTRLDATA_AUX- | D37 | DDI1_PAIR3- | C92 | PEG_RX12- | D92 | PEG_TX12- |
| C38 | DDI3_DDC_AUX_SEL | D38 | RSVD | C93 | GND | D93 | GND |
| C39 | DDI3_PAIR0+ | D39 | DDI2_PAIR0+ | C94 | PEG_RX13+ | D94 | PEG_TX13+ |
| C40 | DDI3_PAIR0- | D40 | DDI2_PAIR0- | C95 | PEG_RX13- | D95 | PEG_TX13- |
| C41 | GND (FIXED) | D41 | GND (FIXED) | C96 | GND | D96 | GND |
| C42 | DDI3_PAIR1+ | D42 | DDI2_PAIR1+ | C97 | RSVD | D97 | RSVD |
| C43 | DDI3_PAIR1- | D43 | DDI2_PAIR1- | C98 | PEG_RX14+ | D98 | PEG_TX14+ |
| C44 | DDI3_HPD | D44 | DDI2_HPD | C99 | PEG_RX14- | D99 | PEG_TX14- |
| C45 | RSVD | D45 | RSVD | C100 | GND (FIXED) | D100 | GND (FIXED) |
| C46 | DDI3_PAIR2+ | D46 | DDI2_PAIR2+ | C101 | PEG_RX15+ | D101 | PEG_TX15+ |
| C47 | DDI3_PAIR2- | D47 | DDI2_PAIR2- | C102 | PEG_RX15- | D102 | PEG_TX15- |
| C48 | RSVD | D48 | RSVD | C103 | GND | D103 | GND |
| C49 | DDI3_PAIR3+ | D49 | DDI2_PAIR3+ | C104 | VCC_12V | D104 | VCC_12V |
| C50 | DDI3_PAIR3- | D50 | DDI2_PAIR3- | C105 | VCC_12V | D105 | VCC_12V |
| C51 | GND (FIXED) | D51 | GND (FIXED) | C106 | VCC_12V | D106 | VCC_12V |
| C52 | PEG_RX0+ | D52 | PEG_TX0+ | C107 | VCC_12V | D107 | VCC_12V |
| C53 | PEG_RX0- | D53 | PEG_TX0- | C108 | VCC_12V | D108 | VCC_12V |
| C54 | NC | D54 | PEG_LANE_RV# | C109 | VCC_12V | D109 | VCC_12V |
| C55 | PEG_RX1+ | D55 | PEG_TX1+ | C110 | GND (FIXED) | D110 | GND (FIXED) |

## COM Express Connectors Signals and Descriptions

Pin Types
I Input to the Module
O Output from the Module
I/O Bi-directional input / output signal
OD Open drain output
RSVD pins are reserved for future use and should be no connect. Do not tie the RSVD pins together.

### AC97/HDA Signals Descriptions

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| AC/HDA_RST# | A30 | O CMOS | 3.3V Suspend/3.3V | series 33Ω resistor | Reset output to CODEC, active low. | CODEC Reset. |
| AC/HDA_SYNC | A29 | O CMOS | 3.3V/3.3V | series 33Ω resistor | Sample-synchronization signal to the CODEC(s). | Serial Sample Rate Synchronization. |
| AC/HDA_BITCLK | A32 | I/O CMOS | 3.3V/3.3V | series 33Ω resistor | Serial data clock generated by the external CODEC(s). | 24 MHz Serial Bit Clock for HDA CODEC. |
| AC/HDA_SDOUT | A33 | O CMOS | 3.3V/3.3V | series 33Ω resistor | Serial TDM data output to the CODEC. | Audio Serial Data Output Stream. |
| AC/HDA_SDIN0 | B30 | I/O CMOS | 3.3V Suspend/3.3V | | Serial TDM data inputs from up to 3 CODECs. | Audio Serial Data Input Stream from CODEC[0:2]. |
| AC/HDA_SDIN1 | B29 | I/O CMOS | 3.3V Suspend/3.3V | | | |
| AC/HDA_SDIN2 | B28 | I/O CMOS | 3.3V Suspend/3.3V | NC | | |

### Gigabit Ethernet Signals Descriptions

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| GBE0_MDI0+ | A13 | I/O Analog | 3.3V max Suspend | | Gigabit Ethernet Controller 0: Media Dependent Interface Differential Pairs 0,1,2,3. The MDI can operate in 1000, 100 and 10 Mbit / sec modes. Some pairs are unused in some modes, per the following:<br>1000BASE-T 100BASE-TX 10BASE-T<br>MDI[0]+/- B1_DA+/- TX+/- TX+/-<br>MDI[1]+/- B1_DB+/- RX+/- RX+/-<br>MDI[2]+/- B1_DC+/-<br>MDI[3]+/- B1_DD+/- | Media Dependent Interface (MDI) differential pair 0. |
| GBE0_MDI0- | A12 | I/O Analog | 3.3V max Suspend | | | |
| GBE0_MDI1+ | A10 | I/O Analog | 3.3V max Suspend | | | Media Dependent Interface (MDI) differential pair 1. |
| GBE0_MDI1- | A9 | I/O Analog | 3.3V max Suspend | | | |
| GBE0_MDI2+ | A7 | I/O Analog | 3.3V max Suspend | | | Media Dependent Interface (MDI) differential pair 2.<br>Only used for 1000Mbit/sec Gigabit Ethernet mode. |
| GBE0_MDI2- | A6 | I/O Analog | 3.3V max Suspend | | | |
| GBE0_MDI3+ | A3 | I/O Analog | 3.3V max Suspend | | | Media Dependent Interface (MDI) differential pair 3.<br>Only used for 1000Mbit/sec Gigabit Ethernet mode. |
| GBE0_MDI3- | A2 | I/O Analog | 3.3V max Suspend | | | |
| GBE0_ACT# | B2 | OD CMOS | 3.3V Suspend/3.3V | | Gigabit Ethernet Controller 0 activity indicator, active low. | Ethernet controller 0 activity indicator, active low. |
| GBE0_LINK# | A8 | OD CMOS | 3.3V Suspend/3.3V | | Gigabit Ethernet Controller 0 link indicator, active low. | Ethernet controller 0 link indicator, active low. |
| GBE0_LINK100# | A4 | OD CMOS | 3.3V Suspend/3.3V | | Gigabit Ethernet Controller 0 100 Mbit / sec link indicator, active low. | Ethernet controller 0 100Mbit/sec link indicator, active low. |
| GBE0_LINK1000# | A5 | OD CMOS | 3.3V Suspend/3.3V | | Gigabit Ethernet Controller 0 1000 Mbit / sec link indicator, active low. | Ethernet controller 0 1000Mbit/sec link indicator, active low. |
| GBE0_CTREF | A14 | REF | GND min 3.3V max | NC | Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. The reference voltage is determined by the requirements of the Module PHY and may be as low as 0V and as high as 3.3V.<br>The reference voltage output shall be current limited on the Module. In the case in which the reference is shorted to ground, the current shall be limited to 250 mA or less. | Reference voltage for Carrier Board Ethernet channel 0 magnetics center tap. |

### SATA Signals Descriptions

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| SATA0_TX+ | A16 | O SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 0 transmit differential pair. | Serial ATA channel 0<br>Transmit output differential pair. |
| SATA0_TX- | A17 | O SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA0_RX+ | A19 | I SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 0 receive differential pair. | Serial ATA channel 0<br>Receive input differential pair. |
| SATA0_RX- | A20 | I SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA1_TX+ | B16 | O SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 1 transmit differential pair. | Serial ATA channel 1<br>Transmit output differential pair. |
| SATA1_TX- | B17 | O SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA1_RX+ | B19 | I SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 1 receive differential pair. | Serial ATA channel 1<br>Receive input differential pair. |
| SATA1_RX- | B20 | I SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA2_TX+ | A22 | O SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 2 transmit differential pair. | Serial ATA channel 2<br>Transmit output differential pair. |
| SATA2_TX- | A23 | O SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA2_RX+ | A25 | I SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 2 receive differential pair. | Serial ATA channel 2<br>Receive input differential pair. |
| SATA2_RX- | A26 | I SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA3_TX+ | B22 | O SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 3 transmit differential pair. | Serial ATA channel 3<br>Transmit output differential pair. |
| SATA3_TX- | B23 | O SATA | AC coupled on Module | AC Coupling capacitor | | |
| SATA3_RX+ | B25 | I SATA | AC coupled on Module | AC Coupling capacitor | Serial ATA or SAS Channel 3 receive differential pair. | Serial ATA channel 3<br>Receive input differential pair. |
| SATA3_RX- | B26 | I SATA | AC coupled on Module | AC Coupling capacitor | | |
| (S)ATA_ACT# | A28 | I/O CMOS | 3.3V / 3.3V | PU 10KΩ to 3.3V | ATA (parallel and serial) or SAS activity indicator, active low. | Serial ATA activity LED. Open collector output pin driven during SATA command activity. |

| PCI Express Lanes Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| PCIE_TX0+ | A68 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 0 | PCIe channel 0. Transmit Output differential pair. |
| PCIE_TX0- | A69 | | | AC Coupling capacitor | | |
| PCIE_RX0+ | B68 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 0 | PCIe channel 0. Receive Input differential pair. |
| PCIE_RX0- | B69 | | | | | |
| PCIE_TX1+ | A64 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 1 | PCIe channel 1. Transmit Output differential pair. |
| PCIE_TX1- | A65 | | | AC Coupling capacitor | | |
| PCIE_RX1+ | B64 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 1 | PCIe channel 1. Receive Input differential pair. |
| PCIE_RX1- | B65 | | | | | |
| PCIE_TX2+ | A61 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 2 | PCIe channel 2. Transmit Output differential pair. |
| PCIE_TX2- | A62 | | | AC Coupling capacitor | | |
| PCIE_RX2+ | B61 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 2 | PCIe channel 2. Receive Input differential pair. |
| PCIE_RX2- | B62 | | | | | |
| PCIE_TX3+ | A58 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 3 | PCIe channel 3. Transmit Output differential pair. |
| PCIE_TX3- | A59 | | | AC Coupling capacitor | | |
| PCIE_RX3+ | B58 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 3 | PCIe channel 3. Receive Input differential pair. |
| PCIE_RX3- | B59 | | | | | |
| PCIE_TX4+ | A55 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 4 | PCIe channel 4. Transmit Output differential pair. |
| PCIE_TX4- | A56 | | | AC Coupling capacitor | | |
| PCIE_RX4+ | B55 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 4 | PCIe channel 4. Receive Input differential pair. |
| PCIE_RX4- | B56 | | | | | |
| PCIE_TX5+ | A52 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 5 | PCIe channel 5. Transmit Output differential pair. |
| PCIE_TX5- | A53 | | | AC Coupling capacitor | | |
| PCIE_RX5+ | B52 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 5 | PCIe channel 5. Receive Input differential pair. |
| PCIE_RX5- | B53 | | | | | |
| PCIE_TX6+ | D19 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 6 | PCIe channel 6. Transmit Output differential pair. |
| PCIE_TX6- | D20 | | | AC Coupling capacitor | | |
| PCIE_RX6+ | C19 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 6 | PCIe channel 6. Receive Input differential pair. |
| PCIE_RX6- | C20 | | | | | |
| PCIE_TX7+ | D22 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Differential Transmit Pairs 7 | PCIe channel 7. Transmit Output differential pair. |
| PCIE_TX7- | D23 | | | AC Coupling capacitor | | |
| PCIE_RX7+ | C22 | I PCIE | AC coupled off Module | | PCI Express Differential Receive Pairs 7 | PCIe channel 7. Receive Input differential pair. |
| PCIE_RX7- | C23 | | | | | |
| PCIE_CLK_REF+ | A88 | O PCIE | PCIE | | Reference clock output for all PCI Express and PCI Express Graphics lanes. | PCIe Reference Clock for all COM Express PCIe lanes, and for PEG lanes. |
| PCIE_CLK_REF- | A89 | | | | | |

| PEG Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| PEG_TX0+ | D52 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 0 | PEG channel 0, Transmit Output differential pair. |
| PEG_TX0- | D53 | | | AC Coupling capacitor | | |
| PEG_RX0+ | C52 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 0 | PEG channel 0, Receive Input differential pair. |
| PEG_RX0- | C53 | | | | | |
| PEG_TX1+ | D55 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 1 | PEG channel 1, Transmit Output differential pair. |
| PEG_TX1- | D56 | | | AC Coupling capacitor | | |
| PEG_RX1+ | C55 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 1 | PEG channel 1, Receive Input differential pair. |
| PEG_RX1- | C56 | | | | | |
| PEG_TX2+ | D58 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 2 | PEG channel 2, Transmit Output differential pair. |
| PEG_TX2- | D59 | | | AC Coupling capacitor | | |
| PEG_RX2+ | C58 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 2 | PEG channel 2, Receive Input differential pair. |
| PEG_RX2- | C59 | | | | | |
| PEG_TX3+ | D61 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 3 | PEG channel 3, Transmit Output differential pair. |
| PEG_TX3- | D62 | | | AC Coupling capacitor | | |
| PEG_RX3+ | C61 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 3 | PEG channel 3, Receive Input differential pair. |
| PEG_RX3- | C62 | | | | | |
| PEG_TX4+ | D65 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 4 | PEG channel 4, Transmit Output differential pair. |
| PEG_TX4- | D66 | | | AC Coupling capacitor | | |
| PEG_RX4+ | C65 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 4 | PEG channel 4, Receive Input differential pair. |
| PEG_RX4- | C66 | | | | | |
| PEG_TX5+ | D68 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 5 | PEG channel 5, Transmit Output differential pair. |
| PEG_TX5- | D69 | | | AC Coupling capacitor | | |
| PEG_RX5+ | C68 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 5 | PEG channel 5, Receive Input differential pair. |
| PEG_RX5- | C69 | | | | | |

| PEG Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| PEG_TX6+ | D71 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 6 | PEG channel 6, Transmit Output differential pair. |
| PEG_TX6- | D72 | | | AC Coupling capacitor | | |
| PEG_RX6+ | C71 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 6 | PEG channel 6, Receive Input differential pair. |
| PEG_RX6- | C72 | | | | | |
| PEG_TX7+ | D74 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 7 | PEG channel 7, Transmit Output differential pair. |
| PEG_TX7- | D75 | | | AC Coupling capacitor | | |
| PEG_RX7+ | C74 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 7 | PEG channel 7, Receive Input differential pair. |
| PEG_RX7- | C75 | | | | | |
| PEG_TX8+ | D78 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 8 | PEG channel 8, Transmit Output differential pair. |
| PEG_TX8- | D79 | | | AC Coupling capacitor | | |
| PEG_RX8+ | C78 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 8 | PEG channel 8, Receive Input differential pair. |
| PEG_RX8- | C79 | | | | | |
| PEG_TX9+ | D81 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 9 | PEG channel 9, Transmit Output differential pair. |
| PEG_TX9- | D82 | | | AC Coupling capacitor | | |
| PEG_RX9+ | C81 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 9 | PEG channel 9, Receive Input differential pair. |
| PEG_RX9- | C82 | | | | | |
| PEG_TX10+ | D85 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 10 | PEG channel 10, Transmit Output differential pair. |
| PEG_TX10- | D86 | | | AC Coupling capacitor | | |
| PEG_RX10+ | C85 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 10 | PEG channel 10, Receive Input differential pair. |
| PEG_RX10- | C86 | | | | | |
| PEG_TX11+ | D88 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 11 | PEG channel 11, Transmit Output differential pair. |
| PEG_TX11- | D89 | | | AC Coupling capacitor | | |
| PEG_RX11+ | C88 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 11 | PEG channel 11, Receive Input differential pair. |
| PEG_RX11- | C89 | | | | | |
| PEG_TX12+ | D91 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 12 | PEG channel 12, Transmit Output differential pair. |
| PEG_TX12- | D92 | | | AC Coupling capacitor | | |
| PEG_RX12+ | C91 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 12 | PEG channel 12, Receive Input differential pair. |
| PEG_RX12- | C92 | | | | | |
| PEG_TX13+ | D94 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 13 | PEG channel 13 Transmit Output differential pair. |
| PEG_TX13- | D95 | | | AC Coupling capacitor | | |
| PEG_RX13+ | C94 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 13 | PEG channel 13, Receive Input differential pair. |
| PEG_RX13- | C95 | | | | | |
| PEG_TX14+ | D98 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 14 | PEG channel 14, Transmit Output differential pair. |
| PEG_TX14- | D99 | | | AC Coupling capacitor | | |
| PEG_RX14+ | C98 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 14 | PEG channel 14, Receive Input differential pair. |
| PEG_RX14- | C99 | | | | | |
| PEG_TX15+ | D101 | O PCIE | AC coupled on Module | AC Coupling capacitor | PCI Express Graphics transmit differential pairs 15 | PEG channel 15, Transmit Output differential pair. |
| PEG_TX15- | D102 | | | AC Coupling capacitor | | |
| PEG_RX15+ | C101 | I PCIE | AC coupled off Module | | PCI Express Graphics receive differential pairs 15 | PEG channel 15, Receive Input differential pair. |
| PEG_RX15- | C102 | | | | | |
| PEG_LANE_RV# | D54 | I CMOS | 3.3V / 3.3V | PU 10KΩ to 3V3 | PCI Express Graphics lane reversal input strap.<br>Pull low on the Carrier board to reverse lane order. | PCI Express Graphics lane reversal input strap.<br>Pull low on the carrier board to reverse lane order. |

| ExpressCard Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| EXCD0_CPPE# | A49 | I CMOS | 3.3V /3.3V | PU 10k to 3.3V | PCI ExpressCard: PCI Express capable card request, active low, one per card | PCI ExpressCard0: PCI Express capable card request, active low, one per card |
| EXCD0_PERST# | A48 | O CMOS | 3.3V /3.3V | | PCI ExpressCard: reset, active low, one per card | PCI ExpressCard0: reset, active low, one per card |
| EXCD1_CPPE# | B48 | I CMOS | 3.3V /3.3V | PU 10k to 3.3V | PCI ExpressCard: PCI Express capable card request, active low, one percard | PCI ExpressCard1: PCI Express capable card request, active low, one per card |
| EXCD1_PERST# | B47 | O CMOS | 3.3V /3.3V | | PCI ExpressCard: reset, active low, one per card | PCI ExpressCard1: reset, active low, one per card |

| USB Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| USB0+ | A46 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 0 | USB Port 0, data + or D+ |
| USB0- | A45 | | | | | USB Port 0, data - or D- |
| USB1+ | B46 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 1 | USB Port 1, data + or D+ |
| USB1- | B45 | | | | | USB Port 1, data - or D- |

| USB Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| USB2+ | A43 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 2 | USB Port 2, data + or D+ |
| USB2- | A42 | | | | | USB Port 2, data - or D- |
| USB3+ | B43 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 3 | USB Port 3, data + or D+ |
| USB3- | B42 | | | | | USB Port 3, data - or D- |
| USB4+ | A40 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 4 | USB Port 4, data + or D+ |
| USB4- | A39 | | | | | USB Port 4, data - or D- |
| USB5+ | B40 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 5 | USB Port 5, data + or D+ |
| USB5- | B39 | | | | | USB Port 5, data - or D- |
| USB6+ | A37 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 6 | USB Port 6, data + or D+ |
| USB6- | A36 | | | | | USB Port 6, data - or D- |
| USB7+ | B37 | I/O USB | 3.3V Suspend/3.3V | | USB differential pairs, channel 7.<br>USB7 may be configured as a USB client or as a host, or both, at the Module designer's discretion. (CH960 default set as a host) | USB Port 7, data + or D+ |
| USB7- | B36 | | | | | USB Port 7, data - or D- |
| USB_0_1_OC# | B44 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | USB over-current sense, USB channels 0 and 1. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. | USB over-current sense, USB ports 0 and 1. |
| USB_2_3_OC# | A44 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | USB over-current sense, USB channels 2 and 3. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. | USB over-current sense, USB ports 2 and 3. |
| USB_4_5_OC# | B38 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | USB over-current sense, USB channels 4 and 5. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. | USB over-current sense, USB ports 4 and 5. |
| USB_6_7_OC# | A38 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | USB over-current sense, USB channels 6 and 7. A pull-up for this line shall be present on the Module. An open drain driver from a USB current monitor on the Carrier Board may drive this line low. Do not pull this line high on the Carrier Board. | USB over-current sense, USB ports 6 and 7. |
| USB_SSTX0+ | D4 | O PCIE | AC coupled on Module | AC Coupling capacitor | Additional transmit signal differential pairs for the SuperSpeed USB data path. | USB Port 0, SuperSpeed TX + |
| USB_SSTX0- | D3 | | | AC Coupling capacitor | | USB Port 0, SuperSpeed TX - |
| USB_SSRX0+ | C4 | I PCIE | AC coupled off Module | | Additional receive signal differential pairs for the SuperSpeed USB data path. | USB Port 0, SuperSpeed RX + |
| USB_SSRX0- | C3 | | | | | USB Port 0, SuperSpeed RX - |
| USB_SSTX1+ | D7 | O PCIE | AC coupled on Module | AC Coupling capacitor | Additional transmit signal differential pairs for the SuperSpeed USB data path. | USB Port 1, SuperSpeed TX + |
| USB_SSTX1- | D6 | | | AC Coupling capacitor | | USB Port 1, SuperSpeed TX - |
| USB_SSRX1+ | C7 | I PCIE | AC coupled off Module | | Additional receive signal differential pairs for the SuperSpeed USB data path. | USB Port 1, SuperSpeed RX + |
| USB_SSRX1- | C6 | | | | | USB Port 1, SuperSpeed RX - |
| USB_SSTX2+ | D10 | O PCIE | AC coupled on Module | AC Coupling capacitor | Additional transmit signal differential pairs for the SuperSpeed USB data path. | USB Port 2, SuperSpeed TX + |
| USB_SSTX2- | D9 | | | AC Coupling capacitor | | USB Port 2, SuperSpeed TX - |

**USB Signals Descriptions**

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| USB_SSRX2+ | C10 | I PCIE | AC coupled off Module | | Additional receive signal differential pairs for the SuperSpeed USB data path. | USB Port 2, SuperSpeed RX + |
| USB_SSRX2- | C9 | | | | | USB Port 2, SuperSpeed RX - |
| USB_SSTX3+ | D13 | O PCIE | AC coupled on Module | AC Coupling capacitor | Additional transmit signal differential pairs for the SuperSpeed USB data path. | USB Port 3, SuperSpeed TX + |
| USB_SSTX3- | D12 | | | AC Coupling capacitor | | USB Port 3, SuperSpeed TX - |
| USB_SSRX3+ | C13 | I PCIE | AC coupled off Module | | Additional receive signal differential pairs for the SuperSpeed USB data path. | USB Port 3, SuperSpeed RX + |
| USB_SSRX3- | C12 | | | | | USB Port 3, SuperSpeed RX - |

**LVDS Signals Descriptions**

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| LVDS_A0+/eDP_TX2+ | A71 | O LVDS | LVDS<br>EDP: AC coupled off Module | | LVDS Channel A differential pairs<br>Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board.<br><br>eDP: eDP differential pairs | LVDS channel A differential signal pair 0<br>eDP lane 2, TX± differential signal pair |
| LVDS_A0-/eDP_TX2- | A72 | | | | | |
| LVDS_A1+/eDP_TX1+ | A73 | O LVDS | LVDS<br>EDP: AC coupled off Module | | | LVDS channel A differential signal pair 1<br>eDP lane 1, TX± differential signal pair |
| LVDS_A1-/eDP_TX1- | A74 | | | | | |
| LVDS_A2+/eDP_TX0+ | A75 | O LVDS | LVDS<br>EDP: AC coupled off Module | | | LVDS channel A differential signal pair 2<br>eDP lane 0, TX ± differential signal pair |
| LVDS_A2-/eDP_TX0- | A76 | | | | | |
| LVDS_A3+ | A78 | O LVDS | LVDS<br>EDP: AC coupled off Module | | | LVDS channel A differential signal pair 3 |
| LVDS_A3- | A79 | | | | | |
| LVDS_A_CK+/eDP_TX3+ | A81 | O LVDS | LVDS | | LVDS Channel A differential clock | LVDS channel A differential clock pair<br>eDP lane 3, TX± differential pair |
| LVDS_A_CK-/eDP_TX3- | A82 | | | | | |
| LVDS_B0+ | B71 | O LVDS | LVDS | | LVDS Channel B differential pairs<br>Ther LVDS flat panel differential pairs (LVDS_A[0:3]+/-, LVDS_B[0:3]+/-. LVDS_A_CK+/-, LVDS_B_CK+/-) shall have 100Ω terminations across the pairs at the destination. These terminations may be on the Carrier Board if the Carrier Board implements a LVDS deserializer on-board. | LVDS channel B differential signal pair 0 |
| LVDS_B0- | B72 | | | | | |
| LVDS_B1+ | B73 | O LVDS | LVDS | | | LVDS channel B differential signal pair 1 |
| LVDS_B1- | B74 | | | | | |
| LVDS_B2+ | B75 | O LVDS | LVDS | | | LVDS channel B differential signal pair 2 |
| LVDS_B2- | B76 | | | | | |
| LVDS_B3+ | B77 | O LVDS | LVDS | | | LVDS channel B differential signal pair 3 |
| LVDS_B3- | B78 | | | | | |
| LVDS_B_CK+ | B81 | O LVDS | LVDS | | LVDS Channel B differential clock | LVDS channel B differential clock pair |
| LVDS_B_CK- | B82 | | | | | |
| LVDS_VDD_EN/eDP_VDD_EN | A77 | O CMOS | 3.3V / 3.3V | LVDS/eDP: PD 100KΩ | LVDS panel power enable | LVDS flat panel power enable.<br>eDP power enable |
| LVDS_BKLT_EN/eDP_BKLT_EN | B79 | O CMOS | 3.3V / 3.3V | LVDS/eDP: PD 100KΩ | LVDS panel backlight enable | LVDS flat panel backlight enable high active signal<br>eDP backlight enable |
| LVDS_BKLT_CTRL/eDP_BKLT_CTRL | B83 | O CMOS | 3.3V / 3.3V | LVDS/eDP: PD 100KΩ | LVDS panel backlight brightness control | LVDS flat panel backlight brightness control<br>EDP backlight brightness control |
| LVDS_I2C_CK/eDP_AUX+ | A83 | I/O OD CMOS | 3.3V / 3.3V | PU 4.7KΩ to 3.3V | I2C clock output for LVDS display use | DDC I2C clock signal used for flat panel detection and control.<br>eDP auxiliary lane + |
| LVDS_I2C_DAT/eDP_AUX- | A84 | I/O OD CMOS | 3.3V / 3.3V | PU 4.7KΩ to 3.3V | I2C data line for LVDS display use | DDC I2C data signal used for flat panel detection and control.<br>eDP auxiliary lane - |
| RSVD/eDP_HPD | A87 | I CMOS | 3.3V / 3.3V | LVDS: RSV series resistor to PCH EDP HPD<br>eDP: Connect to PCH EDP HPD w/PD 100KΩ | eDP_HPD:Detection of Hot Plug / Unplug and notification of the link layer | eDP_HPD: Detection of Hot Plug / Unplug and notification of the link layer |

| LPC Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| LPC_AD0 | B4 | I/O CMOS | 3.3V / 3.3V | | LPC multiplexed address, command and data bus. | LPC multiplexed command, address and data. |
| LPC_AD1 | B5 | | | | | |
| LPC_AD2 | B6 | | | | | |
| LPC_AD3 | B7 | | | | | |
| LPC_FRAME# | B3 | O CMOS | 3.3V / 3.3V | | LPC frame indicates the start of an LPC cycle | LPC frame indicates start of a new cycle or termination of a broken cycle. |
| LPC_DRQ0# | B8 | I CMOS | 3.3V / 3.3V | PU 10K to 3.3V, not support. | LPC serial DMA request | LPC encoded DMA/Bus master request. |
| LPC_DRQ1# | B9 | | | PU 10K to 3.3V, not support. | | |
| LPC_SERIRQ | A50 | I/O CMOS | 3.3V / 3.3V | PU 10K to 3.3V | LPC serial interrupt | LPC serialized IRQ. |
| LPC_CLK | B10 | O CMOS | 3.3V / 3.3V | series 22Ω resistor | LPC clock output - 33MHz nominal | LPC clock output 33MHz. |

| SPI Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| SPI_CS# | B97 | O CMOS | 3.3V Suspend/3.3V | | Chip select for Carrier Board SPI - may be sourced from chipset SPI0 or SPI1 | Chip select for Carrier Board SPI – may be sourced from chipset SPI0 or SPI1 |
| SPI_MISO | A92 | I CMOS | 3.3V Suspend/3.3V | | Data in to Module from Carrier SPI | Data in to Module from Carrier SPI |
| SPI_MOSI | A95 | O CMOS | 3.3V Suspend/3.3V | | Data out from Module to Carrier SPI | Data out from Module to Carrier SPI |
| SPI_CLK | A94 | O CMOS | 3.3V Suspend/3.3V | | Clock from Module to Carrier SPI | Clock from Module to Carrier SPI |
| SPI_POWER | A91 | O | 3.3V Suspend/3.3V | | Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier Board. | Power supply for Carrier Board SPI – sourced from Module – nominally 3.3V. The Module shall provide a minimum of 100mA on SPI_POWER. Carriers shall use less than 100mA of SPI_POWER. SPI_POWER shall only be used to power SPI devices on the Carrier. |
| BIOS_DIS0# | A34 | I CMOS | NA | PU 10KΩ to 3V3 Suspend. | Selection straps to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to COM Express Module Base Specification Revision 2.1 for strapping options of BIOS disable signals. | Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low, please refer to for strapping options of BIOS disable signals. |
| BIOS_DIS1# | B88 | | | PU 10KΩ to 3V3 Suspend. | | Selection strap to determine the BIOS boot device. The Carrier should only float these or pull them low. |

| VGA Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| VGA_RED | B89 | O Analog | Analog | PD 150Ω to GND | Red for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load. | Red component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load. |
| VGA_GRN | B91 | O Analog | Analog | PD 150Ω to GND | Green for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load. | Green component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load. |
| VGA_BLU | B92 | O Analog | Analog | PD 150Ω to GND | Blue for monitor. Analog DAC output, designed to drive a 37.5Ω equivalent load. | Blue component of analog DAC monitor output, designed to drive a 37.5Ω equivalent load. |
| VGA_HSYNC | B93 | O CMOS | 3.3V / 3.3V | | Horizontal sync output to VGA monitor | Horizontal sync output to VGA monitor. |
| VGA_VSYNC | B94 | O CMOS | 3.3V / 3.3V | | Vertical sync output to VGA monitor | Vertical sync output to VGA monitor. |
| VGA_I2C_CK | B95 | I/O OD CMOS | 3.3V / 3.3V | PU 2.2KΩ to 3.3V | DDC clock line (I2C port dedicated to identify VGA monitor capabilities) | DDC clock line (I2C port dedicated to identify VGA monitor capabilities). |
| VGA_I2C_DAT | B96 | I/O OD CMOS | 3.3V / 3.3V | PU 2.2KΩ to 3.3V | DDC data line. | DDC data line. |

| DDI Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| DDI1_PAIR0+ | D26 | O PCIE | AC coupled off Module | | DDI for Display Port: DP1_LANE 0 differential pairs<br>DDI for SDVO: SDVO1_RED± differential pair (Serial Digital Video red output)<br>DDI for HDMI/DVI: TMDS1_DATA lanes 2 differential pairs | DP1_LANE0+ for DP / TMDS1_DATA2+ for HDMI or DVI |
| DDI1_PAIR0- | D27 | | | | | DP1_LANE0- for DP / TMDS1_DATA2- for HDMI or DVI |
| DDI1_PAIR1+ | D29 | O PCIE | AC coupled off Module | | DDI for Display Port: DP1_LANE 1 differential pairs<br>DDI for SDVO: SDVO1_GRN± differential pair (Serial Digital Video green output)<br>DDI for HDMI/DVI: TMDS1_DATA lanes 1 differential pairs | DP1_LANE1+ for DP / TMDS1_DATA1+ for HDMI or DVI |
| DDI1_PAIR1- | D30 | | | | | DP1_LANE1- for DP / TMDS1_DATA1- for HDMI or DVI |

| DDI Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| DDI1_PAIR2+ | D32 | O PCIE | AC coupled off Module | | DDI for Display Port: DP1_LANE 2 differential pairs<br>DDI for SDVO: SDVO1_BLU± differential pair (Serial Digital Video blue output)<br>DDI for HDMI/DVI: TMDS1_DATA lanes 0 differential pairs | DP1_LANE2+ for DP / TMDS1_DATA0+ for HDMI or DVI |
| DDI1_PAIR2- | D33 | | | | | DP1_LANE2- for DP / TMDS1_DATA0- for HDMI or DVI |
| DDI1_PAIR3+ | D36 | O PCIE | AC coupled off Module | | DDI for Display Port: DP1_LANE 3 differential pairs<br>DDI for SDVO: SDVO1_CK± differential pair (Serial Digital Video clock output)<br>DDI for HDMI/DVI: TMDS1_CLK differential pairs | DP1_LANE3+ for DP / TMDS1_CLK+ |
| DDI1_PAIR3- | D37 | | | | | DP1_LANE3- for DP / TMDS1_CLK- |
| DDI1_PAIR4+ | C25 | I PCIE | AC coupled off Module | NA,no spport | DDI for SDVO: SDVO1_INT± differential pair<br>(Serial Digital Video B interrupt input differential pair) | NA |
| DDI1_PAIR4- | C26 | | | NA,no spport | | NA |
| DDI1_PAIR5+ | C29 | I PCIE | AC coupled off Module | NA,no spport | DDI for SDVO: SDVO1_TVCLKIN± differential pair<br>(Serial Digital Video TVOUT synchronization clock input differential pair.) | NA |
| DDI1_PAIR5- | C30 | | | NA,no spport | | NA |
| DDI1_PAIR6+ | C15 | I PCIE | AC coupled off Module | NA,no spport | DDI for SDVO: SDVO1_FLDSTALL± differential pair<br>(Serial Digital Video Field Stall input differential pair.) | NA |
| DDI1_PAIR6- | C16 | | | NA,no spport | | NA |
| DDI1_CTRLCLK_AUX+ | D15 | I/O PCIE | AC coupled on Module | PD 100K to GND<br>**(S/W IC between Rpu/PCH)** | DDI for Display Port: DP1_AUX+ Differetial pairs<br>(DP AUX+ function if DDI1_DDC_AUX_SEL is no connect)<br>Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access | DP1_AUX+ for DP |
| | | I/O OD CMOS | 3.3V / 3.3V | PU 2.2K to 3.3V, PD 100K to GND<br>**(S/W IC between Rpu/Rpd resistor)** | DDI for SDVO: SDVO1_CTRLCLK (SDVO I2C clock line - to set up SDVO peripherals.)<br>DDI for HDMI/DVI: HDMI1_CTRLCLK<br>(HDMI/DVI I2C CTRLCLK if DDI1_DDC_AUX_SEL is pulled high) | HDMI1_CTRLCLK for HDMI or DVI |
| DDI1_CTRLDATA_AUX- | D16 | I/O PCIE | AC coupled on Module | PU 100K to 3.3V<br>**(S/W IC between Rpu/PCH)** | DDI for Display Port: DP1_AUX- Differetial pairs<br>(DP AUX- function if DDI1_DDC_AUX_SEL is no connect)<br>Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access | DP1_AUX- for DP |
| | | I/O OD CMOS | 3.3V / 3.3V | PU 2.2K to 3.3V/PU 100K to 3.3V<br>**(S/W IC between 2.2K/100K resistor)** | DDI for SDVO: SDVO1_CTRLDATA (SDVO I2C data line - to set up SDVO peripherals.)<br>DDI for HDMI/DVI: HDMI1_CTRLDATA<br>(HDMI/DVI I2C CTRLDATA if DDI1_DDC_AUX_SEL is pulled high) | HDMI1_CTRLDATA for HDMI or DVI |
| DDI1_HPD | C24 | I CMOS | 3.3V / 3.3V | PD 1M to GND | DDI for Display Port: DP1_HPD (DP Hot-Plug Detect)<br>DDI for HDMI/DVI: HDMI1_HPD (HDMI Hot-Plug Detect) | DP1_HPD for DP / HDMI1_HPD for HDMI or DVI |
| DDI1_DDC_AUX_SEL | D34 | I CMOS | 3.3V / 3.3V | PD 1M to GND | Selects the function of DDI1_CTRLCLK_AUX+ and DDI1_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals. | Selects the function of DP1 AUX±(Low) or HDMI1 DDC CLK/DATA(High)<br>The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode.<br>When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels. |
| DDI2_PAIR0+ | D39 | O PCIE | AC coupled off Module | | DDI for Display Port: DP2_LANE 0 differential pairs<br>DDI for HDMI/DVI: TMDS2_DATA lanes 2 differential pairs | DP2_LANE0+ for DP / TMDS2_DATA2+ for HDMI or DVI |
| DDI2_PAIR0- | D40 | | | | | DP2_LANE0- for DP / TMDS2_DATA2- for HDMI or DVI |
| DDI2_PAIR1+ | D42 | O PCIE | AC coupled off Module | | DDI for Display Port: DP2_LANE 1 differential pairs<br>DDI for HDMI/DVI: TMDS2_DATA lanes 1 differential pairs | DP2_LANE1+ for DP / TMDS2_DATA1+ for HDMI or DVI |
| DDI2_PAIR1- | D43 | | | | | DP2_LANE1- for DP / TMDS2_DATA1- for HDMI or DVI |
| DDI2_PAIR2+ | D46 | O PCIE | AC coupled off Module | | DDI for Display Port: DP2_LANE 2 differential pairs<br>DDI for HDMI/DVI: TMDS2_DATA lanes 0 differential pairs | DP2_LANE2+ for DP / TMDS2_DATA0+ for HDMI or DVI |
| DDI2_PAIR2- | D47 | | | | | DP2_LANE2- for DP / TMDS2_DATA0- for HDMI or DVI |
| DDI2_PAIR3+ | D49 | O PCIE | AC coupled off Module | | DDI for Display Port: DP2_LANE 3 differential pairs<br>DDI for HDMI/DVI: TMDS2_CLK differential pairs | DP2_LANE3+ for DP / TMDS2_CLK+ |
| DDI2_PAIR3- | D50 | | | | | DP2_LANE3- for DP / TMDS2_CLK- |
| DDI2_CTRLCLK_AUX+ | C32 | I/O PCIE | AC coupled on Module | PD 100K to GND<br>**(S/W IC between Rpu/PCH)** | DDI for Display Port: DP2_AUX+ Differetial pairs<br>(DP AUX+ function if DDI2_DDC_AUX_SEL is no connect)<br>Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access | DP2_AUX+ for DP |
| | | I/O OD CMOS | 3.3V / 3.3V | PU 2.2K to 3.3V, PD 100K to GND<br>**(S/W IC between Rpu/Rpd resistor)** | DDI for HDMI/DVI: HDMI2_CTRLCLK<br>(HDMI/DVI I2C CTRLCLK if DDI2_DDC_AUX_SEL is pulled high) | HDMI2_CTRLCLK for HDMI or DVI |

| DDI Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| DDI2_CTRLDATA_AUX- | C33 | I/O PCIE | AC coupled on Module | PU 100K to 3.3V **(S/W IC between Rpu/PCH)** | DDI for Display Port: DP2_AUX- Differetial pairs (DP AUX- function if DDI2_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access | DP2_AUX- for DP |
| | | I/O OD CMOS | 3.3V / 3.3V | PU 2.2K to 3.3V/PU 100K to 3.3V **(S/W IC between 2.2K/100K resistor)** | DDI for HDMI/DVI: HDMI2_CTRLDATA (HDMI/DVI I2C CTRLDATA if DDI2_DDC_AUX_SEL is pulled high) | HDMI2_CTRLDATA for HDMI or DVI |
| DDI2_HPD | D44 | I CMOS | 3.3V / 3.3V | PD 1M to GND | DDI for Display Port: DP2_HPD (DP Hot-Plug Detect) DDI for HDMI/DVI: HDMI2_HPD (HDMI Hot-Plug Detect) | DP2_HPD for DP / HDMI1_HPD for HDMI or DVI |
| DDI2_DDC_AUX_SEL | C34 | I CMOS | 3.3V / 3.3V | PD 1M to GND | Selects the function of DDI2_CTRLCLK_AUX+ and DDI2_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals. | Selects the function of DP2 AUX±(Low) or HDMI2 DDC CLK/DATA(High) The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels. |
| DDI3_PAIR0+ | C39 | O PCIE | AC coupled off Module | | DDI for Display Port: DP3_LANE 0 differential pairs | DP3_LANE0+ for DP / TMDS3_DATA2+ for HDMI or DVI |
| DDI3_PAIR0- | C40 | | | | DDI for HDMI/DVI: TMDS3_DATA lanes 2 differential pairs | DP3_LANE0- for DP / TMDS3_DATA2- for HDMI or DVI |
| DDI3_PAIR1+ | C42 | O PCIE | AC coupled off Module | | DDI for Display Port: DP3_LANE 1 differential pairs | DP3_LANE1+ for DP / TMDS3_DATA1+ for HDMI or DVI |
| DDI3_PAIR1- | C43 | | | | DDI for HDMI/DVI: TMDS3_DATA lanes 1 differential pairs | DP3_LANE1- for DP / TMDS3_DATA1- for HDMI or DVI |
| DDI3_PAIR2+ | C46 | O PCIE | AC coupled off Module | | DDI for Display Port: DP3_LANE 2 differential pairs | DP3_LANE2+ for DP / TMDS3_DATA0+ for HDMI or DVI |
| DDI3_PAIR2- | C47 | | | | DDI for HDMI/DVI: TMDS3_DATA lanes 0 differential pairs | DP3_LANE2- for DP / TMDS3_DATA0- for HDMI or DVI |
| DDI3_PAIR3+ | C49 | O PCIE | AC coupled off Module | | DDI for Display Port: DP3_LANE 3 differential pairs | DP3_LANE3+ for DP / TMDS3_CLK+ |
| DDI3_PAIR3- | C50 | | | | DDI for HDMI/DVI: TMDS3_CLK differential pairs | DP3_LANE3- for DP / TMDS3_CLK- |
| DDI3_CTRLCLK_AUX+ | C36 | I/O PCIE | AC coupled on Module | PD 100K to GND **(S/W IC between Rpu/PCH)** | DDI for Display Port: DP3_AUX+ Differetial pairs (DP AUX+ function if DDI3_DDC_AUX_SEL is no connect) Half-duplex bi-directional AUX channel for services such as link configuration or maintenance and EDID access | DP3_AUX+ for DP |
| | | I/O OD CMOS | 3.3V / 3.3V | PU 2.2K to 3.3V, PD 100K to GND **(S/W IC between Rpu/Rpd resistor)** | DDI for HDMI/DVI: HDMI3_CTRLCLK (HDMI/DVI I2C CTRLCLK if DDI3_DDC_AUX_SEL is pulled high) | HDMI3_CTRLCLK for HDMI or DVI |
| DDI3_CTRLDATA_AUX- | C37 | I/O PCIE | AC coupled on Module | PU 100K to 3.3V **(S/W IC between Rpu/PCH)** | DDI for Display Port: DP3_AUX- Differetial pairs (DP AUX- function if DDI3_DDC_AUX_SEL is no connect) | DP3_AUX- for DP |
| | | I/O OD CMOS | 3.3V / 3.3V | PU 2.2K to 3.3V/PU 100K to 3.3V **(S/W IC between 2.2K/100K resistor)** | DDI for HDMI/DVI: HDMI3_CTRLDATA (HDMI/DVI I2C CTRLDATA if DDI3_DDC_AUX_SEL is pulled high) | HDMI3_CTRLDATA for HDMI or DVI |
| DDI3_HPD | C44 | I CMOS | 3.3V / 3.3V | PD 1MΩ to GND | DDI for Display Port: DP3_HPD (DP Hot-Plug Detect) DDI for HDMI/DVI: HDMI3_HPD (HDMI Hot-Plug Detect) | DP3_HPD for DP / HDMI1_HPD for HDMI or DVI |
| DDI3_DDC_AUX_SEL | C38 | I CMOS | 3.3V / 3.3V | PD 1MΩ to GND | Selects the function of DDI3_CTRLCLK_AUX+ and DDI3_CTRLDATA_AUX-. This pin shall have a 1M pull-down to logic ground on the Module. If this input is floating the AUX pair is used for the DP AUX+/- signals. If pulled-high the AUX pair contains the CRTLCLK and CTRLDATA signals. | Selects the function of DP3 AUX±(Low) or HDMI3 DDC CLK/DATA(High) The DDC_AUX_SEL pin should be routed to pin 13 of the DisplayPort connector, to enable Dual-Mode. When HDMI/DVI is directly done on the Carrier Board, this pin shall be pulled to 3.3V with a 100k Ohm resistor to configure the AUX pairs as DDC channels. |

| Serial Interface Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| SER0_TX | A98 | O CMOS | 5V/12V | | General purpose serial port 0 transmitter | Transmit Line for Serial Port 0 ; PD 4.7KΩ |
| SER0_RX | A99 | I CMOS | 5V/12V | PU 10KΩ to 3.3V | General purpose serial port 0 receiver | Receive Line for Serial Port 0 |
| SER1_TX | A101 | O CMOS | 5V/12V | | General purpose serial port 1 transmitter | Transmit Line for Serial Port 1 ; PD 4.7KΩ |
| SER1_RX | A102 | I CMOS | 5V/12V | PU 10KΩ to 3.3V | General purpose serial port 1 receiver | Receive Line for Serial Port 1 |

**I2C Signal Descriptions**

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| I2C_CK | B33 | I/O OD CMOS | 3.3V Suspend/3.3V | PU 2.2K to 3.3V Suspend | General purpose I2C port clock output | General Purpose I2C Clock output |
| I2C_DAT | B34 | I/O OD CMOS | 3.3V Suspend/3.3V | PU 2.2K to 3.3V Suspend | General purpose I2C port data I/O line | General Purpose I2C data I/O line. |

**Miscellaneous Signal Descriptions**

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| SPKR | B32 | O CMOS | 3.3V / 3.3V | | Output for audio enunciator - the "speaker" in PC-AT systems. This port provides the PC beep signal and is mostly intended for debugging purposes. | Output used to control an external FET or a logic gate to drive an external PC speaker. |
| WDT | B27 | O CMOS | 3.3V / 3.3V | PD 100KΩ | Output indicating that a watchdog time-out event has occurred. | Output indicating that a watchdog time-out event has occurred. |
| FAN_PWMOUT | B101 | O CMOS | 3.3V / 12V | RSV PD 100KΩ to GND | Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. | Fan speed control. Uses the Pulse Width Modulation (PWM) technique to control the fan's RPM. |
| FAN_TACHIN | B102 | I OD CMOS | 3.3V / 12V | PU 47KΩ to 3.3V | Fan tachometer input for a fan with a two pulse output. | Fan tachometer input for a fan with a two pulse output. |
| TPM_PP | A96 | I CMOS | 3.3V / 3.3V | PD 100KΩ to GND. | Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. This signal is used to indicate Physical Presence to the TPM. | Trusted Platform Module (TPM) Physical Presence pin. Active high. TPM chip has an internal pull down. Thissignal is used to indicate Physical Presence to the TPM. |

**Power and System Management Signals Descriptions**

| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
|---|---|---|---|---|---|---|
| PWRBTN# | B12 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | A falling edge creates a power button event. Power button events can be used to bring a system out of S5 soft off and other suspend states, as well as powering the system down. | Power button low active signal used to wake up the system from S5 state (soft off). This signal is triggered on the falling edge. |
| SYS_RESET# | B49 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. | Reset button input. Active low request for Module to reset and reboot. May be falling edge sensitive. For situations when SYS_RESET# is not able to reestablish control of the system, PWR_OK or a power cycle may be used. |
| CB_RESET# | B50 | O CMOS | 3.3V Suspend/3.3V | PD 100KΩ to GND | Reset output from Module to Carrier Board. Active low. Issued by Module chipset and may result from a low SYS_RESET# input, a low PWR_OK input, a VCC_12V power input that falls below the minimum specification, a watchdog timeout, or may be initiated by the Module software. | Reset output signal from Module to Carrier Board. This signal may be driven low by the Module to reset external components located on the Carrier Board. |
| PWR_OK | B24 | I CMOS | 3.3V / 3.3V | Both PU 10KΩ to 5V and PD20K | Power OK from main power supply. A high value indicates that the power is good. This signal can be used to hold off Module startup to allow Carrier based FPGAs or other configurable devices time to be programmed. | Power OK status signal generated by the ATX power supply to notify the Module that the DC operating voltages are within the ranges required for proper operation. |
| SUS_STAT# | B18 | O CMOS | 3.3V Suspend/3.3V | PD 100KΩ to GND | Indicates imminent suspend operation; used to notify LPC devices. | Suspend status signal to indicate that the system will be entering a low power state soon. It can be used by other peripherals on the Carrier Board as an indication that they should go into power-down mode. |
| SUS_S3# | A15 | O CMOS | 3.3V Suspend/3.3V | PD 100KΩ to GND | Indicates system is in Suspend to RAM state. Active low output. An inverted copy of SUS_S3# on the Carrier Board may be used to enable the non-standby power on a typical ATX supply. | S3 Sleep control signal indicating that the system resides in S3 state (Suspend to RAM). |
| SUS_S4# | A18 | O CMOS | 3.3V Suspend/3.3V | PD 100KΩ to GND | Indicates system is in Suspend to Disk state. Active low output. | S4 Sleep control signal indicating that the system resides in S4 state (Suspend to Disk). |
| SUS_S5# | A24 | O CMOS | 3.3V Suspend/3.3V | PD 100KΩ to GND | Indicates system is in Soft Off state. | S5 Sleep Control signal indicating that the system resides in S5 State (Soft Off). |
| WAKE0# | B66 | I CMOS | 3.3V Suspend/3.3V | PU 1KΩ to 3.3V Suspend | PCI Express wake up signal. | PCI Express wake-up event signal. |
| WAKE1# | B67 | I CMOS | 3.3V Suspend/3.3V | PU 10KΩ to 3.3V Suspend | General purpose wake up signal. May be used to implement wake-up on PS2 keyboard or mouse activity. | General purpose wake-up signal. |
| BATLOW# | A27 | I CMOS | 3.3V Suspend/ 3.3V | PU 10KΩ to 3.3V Suspend | Indicates that external battery is low. This port provides a battery-low signal to the Module for orderly transitioning to power saving or power cut-off ACPI modes. | Battery low input. This signal may be driven low by external circuitry to signal that the system battery is low. It also can be used to signal some other external power management event. |
| LID# | A103 | I OD CMOS | 3.3V Suspend/12V | PU 47KΩ to 3.3V Suspend | LID switch. Low active signal used by the ACPI operating system for a LID switch. | LID switch. Low active signal used by the ACPI operating system for a LID switch. |
| SLEEP# | B103 | I OD CMOS | 3.3V Suspend/12V | PU 47KΩ to 3.3V Suspend | Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. | Sleep button. Low active signal used by the ACPI operating system to bring the system to sleep state or to wake it up again. |

| Thermal Protection Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| THRM# | B35 | I CMOS | 3.3V / 3.3V | PU 10KΩ to 3.3V | Input from off-Module temp sensor indicating an over-temp situation. | Thermal Alarm active low signal generated by the external hardware to indicate an over temperature situation. This signal can be used to initiate thermal throttling. |
| THRMTRIP# | A35 | O CMOS | 3.3V / 3.3V | PU 10KΩ to 3.3V | Active low output indicating that the CPU has entered thermal shutdown. | Thermal Trip indicates an overheating condition of the processor. If 'THRMTRIP#' goes active the system immediately transitions to the S5 State (Soft Off). |

| SMBUS Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| SMB_CK | B13 | I/O OD CMOS | 3.3V Suspend/3.3V | PU 2.2KΩ to 3.3V Suspend | System Management Bus bidirectional clock line. | System Management Bus bidirectional clock line |
| SMB_DAT | B14 | I/O OD CMOS | 3.3V Suspend/3.3V | PU 2.2KΩ to 3.3V Suspend | System Management Bus bidirectional data line. | System Management bidirectional data line. |
| SMB_ALERT# | B15 | I CMOS | 3.3V Suspend/3.3V | PU 2.2KΩ to 3.3V Suspend | System Management Bus Alert – active low input can be used to generate an SMI# (System Management Interrupt) or to wake the system. | System Management Bus Alert |

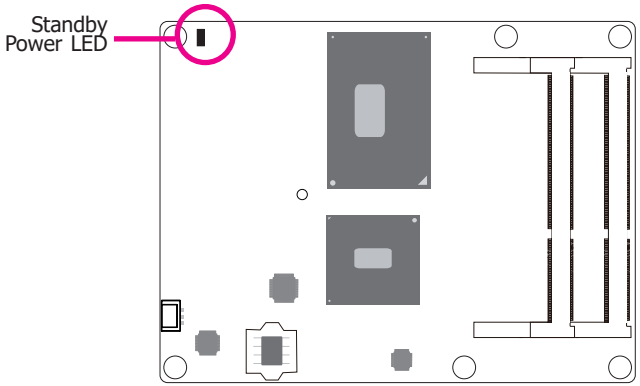
| GPIO Signals Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| GPO0 | A93 | O CMOS | 3.3V / 3.3V | | General purpose output pins. Upon a hardware reset, these outputs should be low. | General Purpose Outputs for system specific usage. |
| GPO1 | B54 | | | | | |
| GPO2 | B57 | | | | | |
| GPO3 | B63 | | | | | |
| GPI0 | A54 | I CMOS | 3.3V / 3.3V | PU 47KΩ to 3.3V | General purpose input pins. Pulled high internally on the Module. | General Purpose Input for system specific usage. The signals are pulled up by the Module. |
| GPI1 | A63 | | | PU 47KΩ to 3.3V | | |
| GPI2 | A67 | | | PU 47KΩ to 3.3V | | |
| GPI3 | A85 | | | PU 47KΩ to 3.3V | | |

| Power and GND Signal Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| VCC_12V | A104~A109<br>B104~B109<br>C104~C109<br>D104~D109 | Power | | | Primary power input: +12V nominal. All available VCC_12V pins on the connector(s) shall be used. | |
| VCC_5V_SBY | B84~B87 | Power | | | Standby power input: +5.0V nominal. If VCC5_SBY is used, all available VCC_5V_SBY pins on the connector(s) shall be used. Only used for standby and suspend functions. May be left unconnected if these functions are not used in the system design. | |
| VCC_RTC | A47 | Power | | | Real-time clock circuit-power input. Nominally +3.0V. | |

| Power and GND Signal Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| GND | A1, A11, A21, A31, A41, A51, A57, A60, A66, A70, A80, A90, A100, A110, B1, B11, B21 ,B31, B41, B51, B60, B70, B80, B90, B100, B110, C1, C2, C5, C8, C11, C14, C21, C31, C41, C51, C60, C70, C73, C76, C80, C84, C87, C90, C93, C96, C100, C103, C110, D1, D2, D5, D8, D11, D14, D21, D31, D41, D51, D60, D67, D70, D73, D76, D80, D84, D87, D90, D93, D96, D100, D103, D110 | Power | | | Ground - DC power and signal and AC signal return path.<br>All available GND connector pins shall be used and tied to Carrier Board GND plane. | |

| Module type Signal Descriptions | | | | | | |
|---|---|---|---|---|---|---|
| Signal | Pin# | Pin Type | Pwr Rail /Tolerance | CH960 PU/PD | Module Base Specification R2.1 Description | COM Express Carrier Design Guide R2.0 Description |
| TYPE0# | C54 | PDS | | N.C. | TYPE2# TYPE1# TYPE0#<br>X X X pin out Type 1<br>NC NC NC pin out Type 2<br>NC NC GND pin out Type 3 (no IDE)<br>NC GND NC pin out Type 4 (no PCI)<br>NC GND GND pin out Type 5 (no IDE, no PCI)<br>GND NC NC pin out Type 6 (no IDE, no PCI) | The Type pins indicate the COM Express pin-out type of the Module. To indicate the Module's pin-out type, the pins are either not connected or strapped to ground on the Module. The Carrier Board has to implement additional logic, which prevents the system to switch power on, if a Module with an incompatible pin-out type is detected. |
| TYPE1# | C57 | PDS | | N.C. | | |
| TYPE2# | D57 | PDS | | PD 0Ω to GND | | |
| TYPE10# | A97 | PDS | | N.C. | Dual use pin. Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier that a Rev 1.0/2.0 Module is installed<br>TYPE10#<br>NC Pin-out R2.0<br>PD Pin-out Type 10 pull down to ground with 47K resistor<br>12V Pin-out R1.0<br>This pin is reclaimed from the VCC_12V pool. In R1.0 Modules this pin will connect to other VCC_12V pins. In R2.0 this pin is defined as a no connect for types 1-6. A Carrier can detect a R1.0 Module by the presence of 12V on this pin. R2.0 Module types 1-6 will no connect this pin. Type 10 Modules shall pull this pin to ground through a 47K resistor. | Indicates to the Carrier Board that a Type 10 Module is installed. Indicates to the Carrier Board, that a Rev 1.0/2.0 Module is installed.<br>TYPE10#<br>NC Pin-out R2.0<br>PD Pin-out Type 10 pull down to ground with 47k<br>12V Pin-out R1.0 |

## Standby Power LED



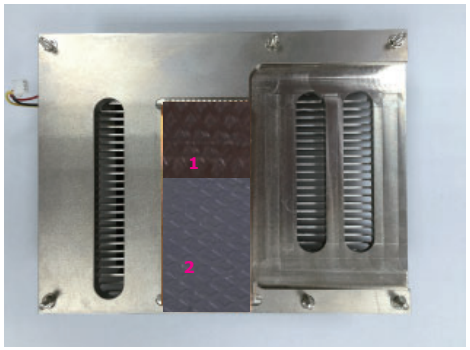

This LED will light when the system is in the standby mode.

## Cooling Option

### Heat Sink with Fan

**Note:**
The system board used in the following illustrations may not resemble the actual board. These illustrations are for reference only.

Top View of the Heat Sink




Bottom View of the Heat Sink

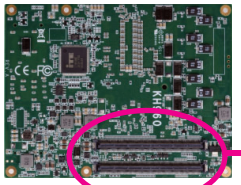
- "1" and "2" denote the locations of the thermal pads designed to contact the corresponding components on CH960-CM246/QM370/HM370.

**Important:**
Remove the plastic covering from the thermal pads prior to mounting the heat sink onto CH960-CM246/QM370/HM370.

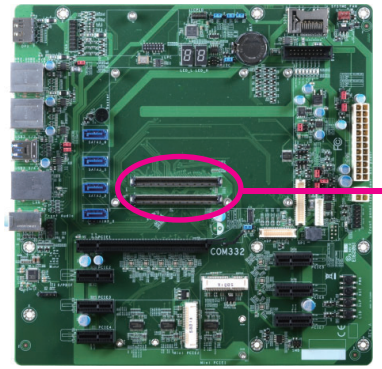
## Installing CH960-CM246/QM370/HM370 onto a Carrier Board

**Important:**
The carrier board used in this section is for reference purpose only and may not resemble your carrier board. These illustrations are mainly to guide you on how to install CH960-CM246/QM370/HM370 onto the carrier board of your choice.

1. Grasp CH960-CM246/QM370/HM370 by its edges and position it on top of the carrier board with its mounting holes aligned with the standoffs on the carrier board. This helps align the COM Express connectors of the two boards to each other.

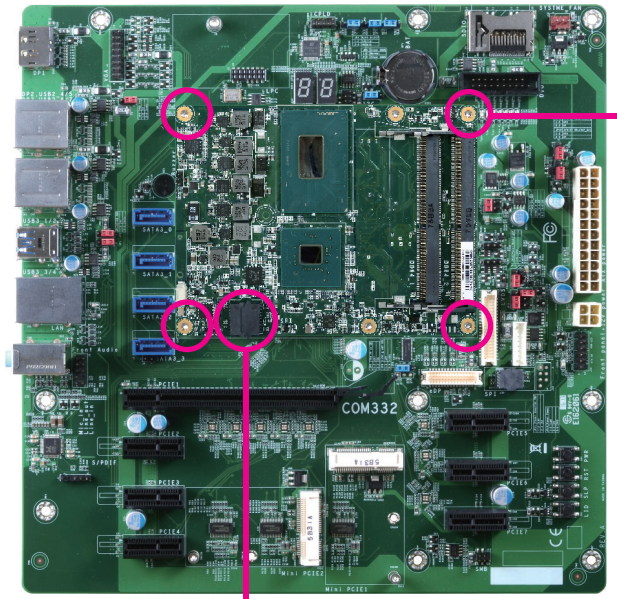


COM Express connectors on CH960-CM246/QM370/HM370




COM Express connectors on the carrier board

2. Apply firm even pressure to the side with the COM Express connectors first and push down the entire board. You will hear a "click", indicating the module is correctly seated in the COM Express connectors of the carrier board.

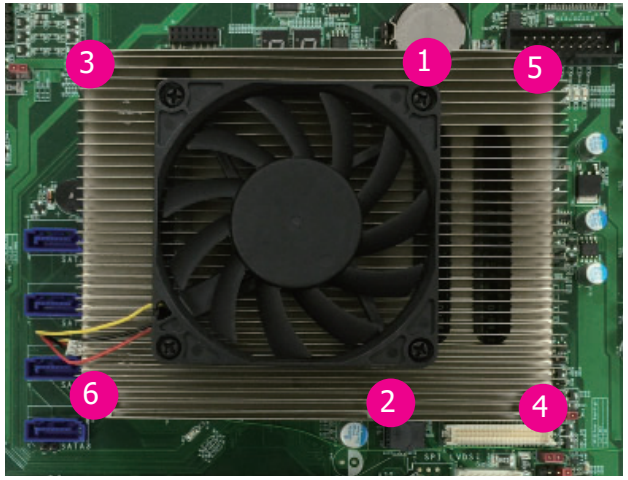



Pressing points

BIOS ROM socket

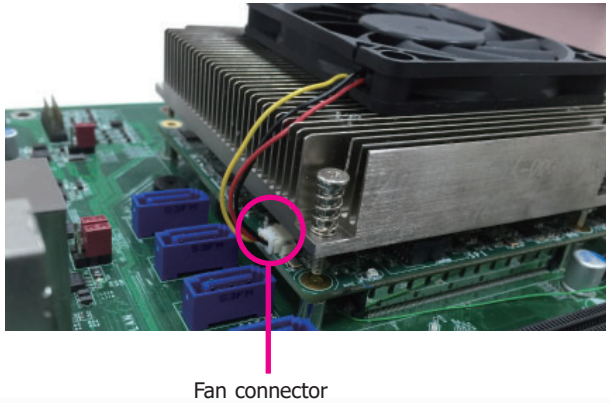
**Note:**
The illustrations above show the pressing points of the module onto the carrier board. Be careful when pressing the module, it may damage the socket.

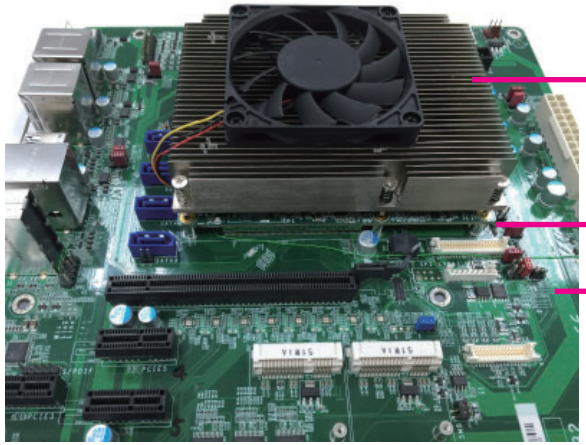
3. Install a heat sink onto the CH960 with the carrier board. First align the mounting holes of the heat sink with the mounting holes of the module.




**Note:**
Install the heat sink according to the sequence of the screws shown in the image above to avoid damages to the CPU. Turn each screw half way down first to initially stabilize the heat sink onto the board, then finally tighten each screw. This is to avoid imbalance which might cause cracks or fractures to the CPU and/or heatsink assembly.

4. Connect the heat sink and fan's cable to the fan connector on CH960.




**Side View of the Heat sink, Module, and Carrier Board**

# Chapter 4 - BIOS Setup

## Overview

The BIOS is a program that takes care of the basic level of communication between the CPU and peripherals. It contains codes for various advanced features found in this system board. The BIOS allows you to configure the system and save the configuration in a battery-backed CMOS so that the data retains even when the power is off. In general, the information stored in the CMOS RAM of the EEPROM will stay unchanged unless a configuration change has been made such as a hard drive replaced or a device added.

It is possible that the CMOS battery will fail causing CMOS data loss. If this happens, you need to install a new CMOS battery and reconfigure the BIOS settings.

**Note:**
The BIOS is constantly updated to improve the performance of the system board; therefore the BIOS screens in this chapter may not appear the same as the actual one. These screens are for reference purpose only.

## Default Configuration

Most of the configuration settings are either predefined according to the Load Optimal Defaults settings which are stored in the BIOS or are automatically detected and configured without requiring any actions. There are a few settings that you may need to change depending on your system configuration.

## Entering the BIOS Setup Utility

The BIOS Setup Utility can only be operated from the keyboard and all commands are keyboard commands. The commands are available at the right side of each setup screen.

The BIOS Setup Utility does not require an operating system to run. After you power up the system, the BIOS message appears on the screen and the memory count begins. After the memory test, the message "Press DEL to run setup" will appear on the screen. If the message disappears before you respond, restart the system or press the "Reset" button. You may also restart the system by pressing the <Ctrl> <Alt> and <Del> keys simultaneously.

## Legends

| KEYs | Function |
|---|---|
| Right and Left Arrows | Moves the highlight left or right to select a menu. |
| Up and Down Arrows | Moves the highlight up or down between submenus or fields. |
| <Enter> | Press <Enter> to enter the highlighted submenu |
| + (plus key) | Scrolls forward through the values or options of the hightlighted field. |
| - (minus key) | Scolls backward through the values or options of the hightlighted field. |
| <F1> | Displays general help |
| <F2> | Displays previous values |
| <F9> | Optimized defaults |
| <F10> | Saves and reset the setup program. |
| <Esc> | Exits to the BIOS setup utility |

## Scroll Bar

When a scroll bar appears to the right of the setup screen, it indicates that there are more available fields not shown on the screen. Use the up and down arrow keys to scroll through all the available fields.

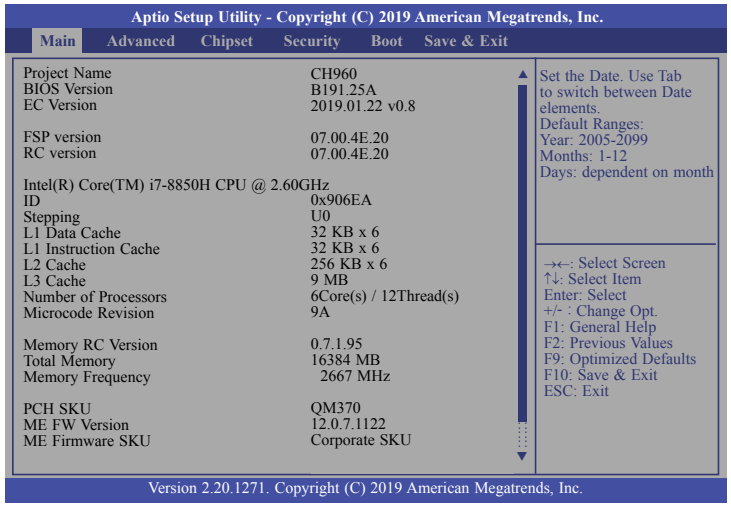
## Submenu

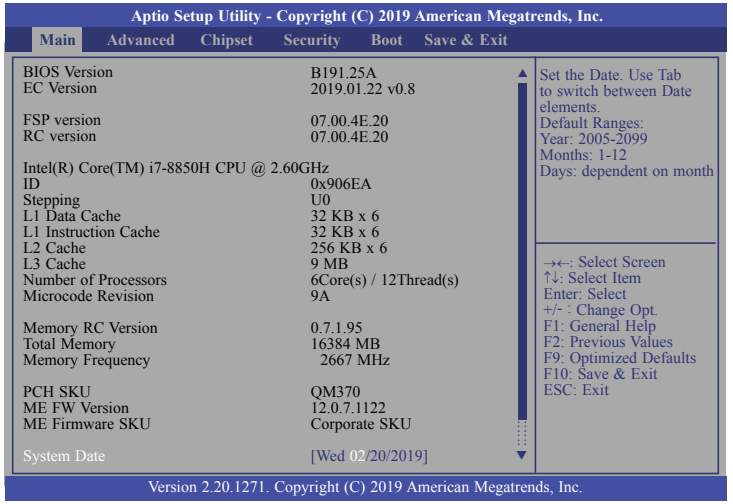
When "▶" appears on the left of a particular field, it indicates that a submenu which contains additional options are available for that field. To display the submenu, move the highlight to that field and press <Enter>.

# AMI BIOS Setup Utility

## Main

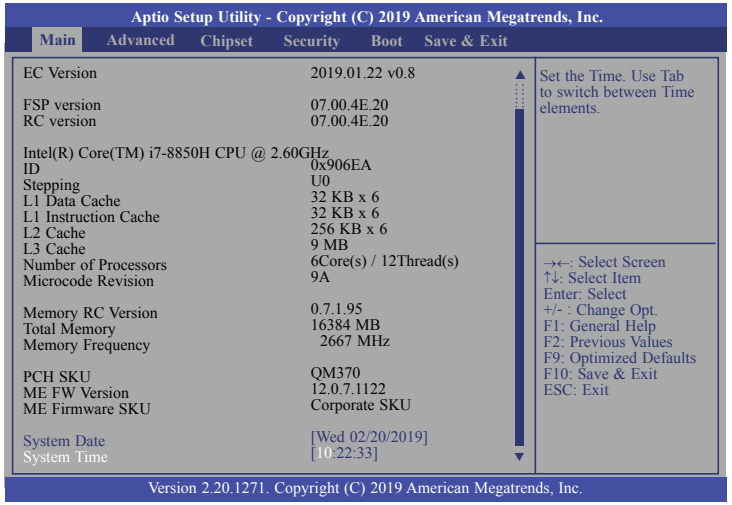
The Main menu is the first screen that you will see when you enter the BIOS Setup Utility.




### System Date

The date format is <day>, <month>, <date>, <year>. Day displays a day, from Sunday to Saturday. Month displays the month, from 01 to 12. Date displays the date, from 01 to 31. Year displays the year, from 2005 to 2099.



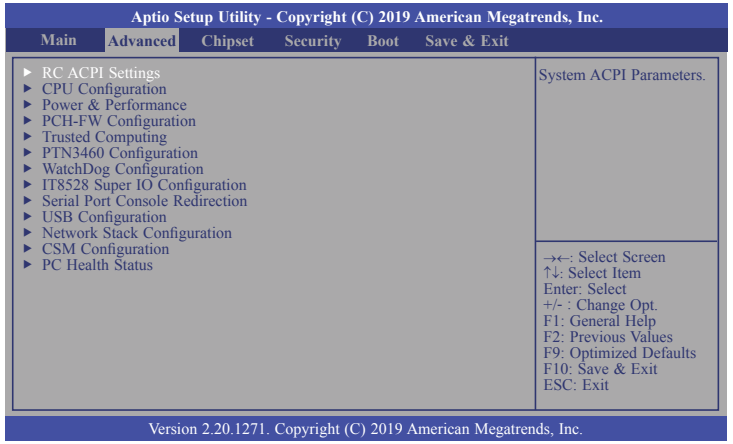

### System Time

The time format is <hour>, <minute>, <second>. The time is based on the 24-hour military-time clock. For example, 1 p.m. is 13:00:00. Hour displays hours from 00 to 23. Minute displays minutes from 00 to 59. Second displays seconds from 00 to 59.

## Advanced

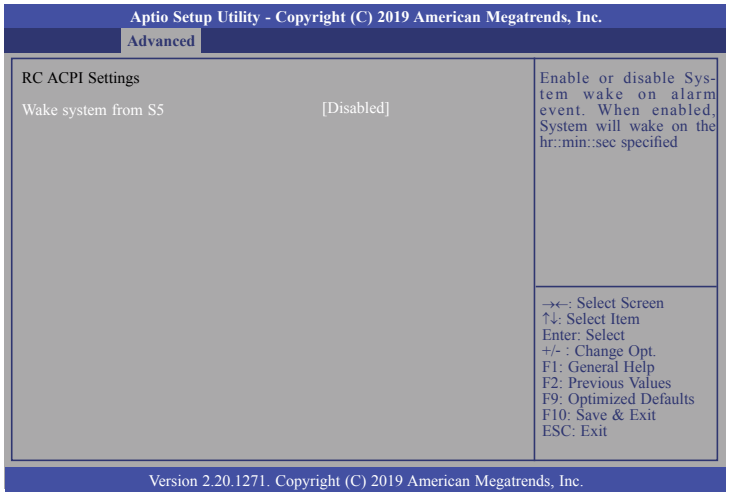
The Advanced menu allows you to configure your system for basic operation. Some entries are defaults required by the system board, while others, if enabled, will improve the performance of your system or let you set some features according to your preference.

**Important:**
Setting incorrect field values may cause the system to malfunction.



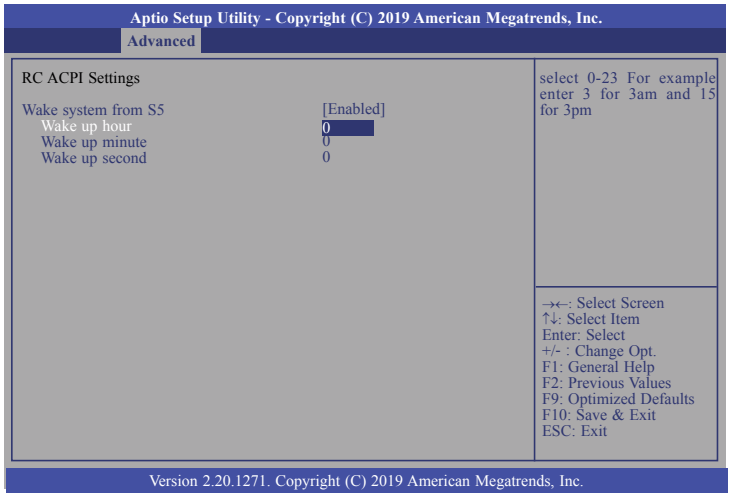

### RC ACPI Settings

This section is used to configure the system ACPI parameters.




#### Wake system from S5

When Enabled, the system uses the RTC to generate a wakeup event.




### Wake up hour

Select hour from 0 to 23.

### Wake up minute

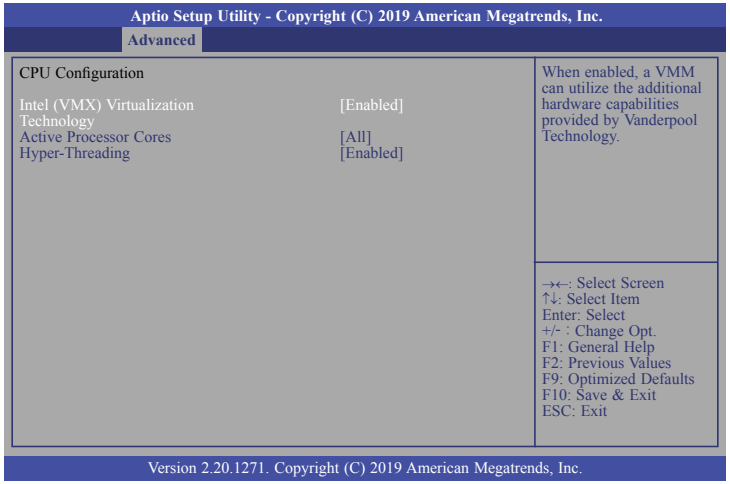
Select minute from 0 to 59.

### Wake up second

Select second from 0 to 59.

## CPU Configuration

This section is used to configure the CPU.




### Intel (VMX) Virtualization Technology

When this field is set to Enabled, the VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.

### Active Processor Cores

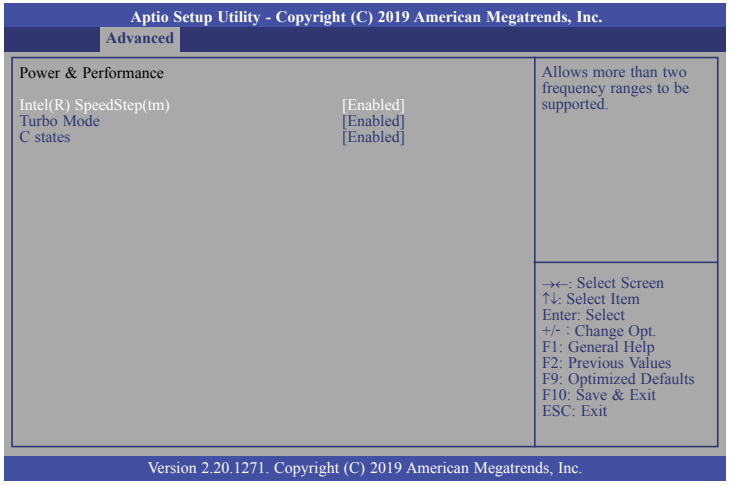
Select number of cores to enable in each processor package: all, 1, 2, 3, 4 or 5.

### Hyper-threading

Enables this field for Windows XP and Linux which are optimized for Hyper-Threading technology. Select disabled for other OSes not optimized for Hyper-Threading technology. When disabled, only one thread per enabled core is enabled.

## Power & Performance

This section is used to configure the power & performance options.




### Intel(R) SpeedStep(tm)

This field is used to enable or disable the Intel Enhanced SpeedStep Technology. If enabled, Turbo Mode will appear for configuration.

### Turbo Mode

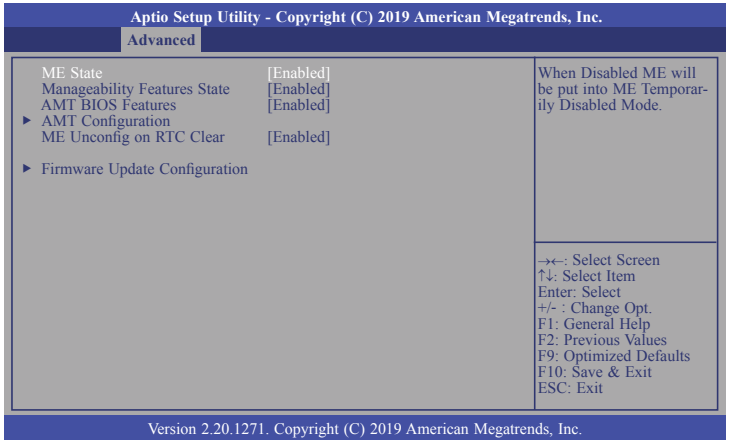
This field is used to enable or disable processor turbo mode (requires that Intel(R) SpeedStep(tm) is enabled too), which allows the processor core to automatically run faster than the base frequency when the processor's power, temperature, and specification are within the limits of TDP.

### C states

Enable or disable CPU Power Management. It allows CPU to go to C states when it's not 100% utilized.

## PCH-FW Configuration

This section configures the parameters of Management Engine Technology.




### ME State

When this field is set to Disabled, ME will be put into ME Temporarily Disabled Mode.

### Manageability Features State

Enable or disable Intel(R) Manageability features. This option disables/enables Manageability Features support in FW. To disable, support platform must be in an unprovisioned state first.

### AMT BIOS Features (for CH960-CM246/QM370 only)

When disabled, AMT BIOS features are no longer supported and user is no longer able to access MEBx Setup. This option does not disable manageability features in FW.

### AMT Configuration (for CH960-CM246/QM370 only)

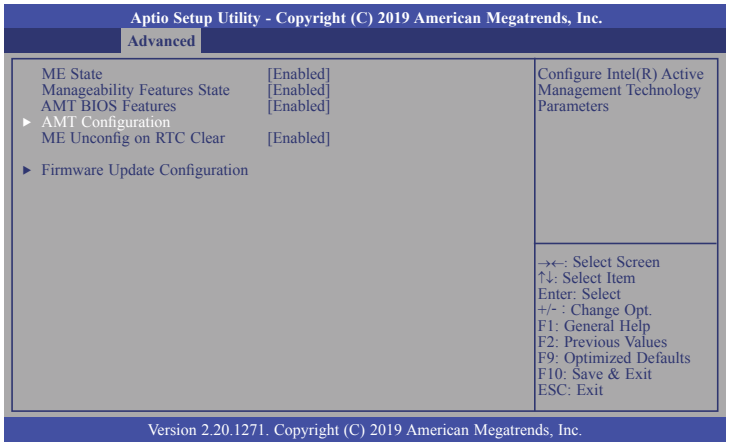
This section is used to configure Intel(R) Active Management Technology Parameters. Refer next two pages for more information.

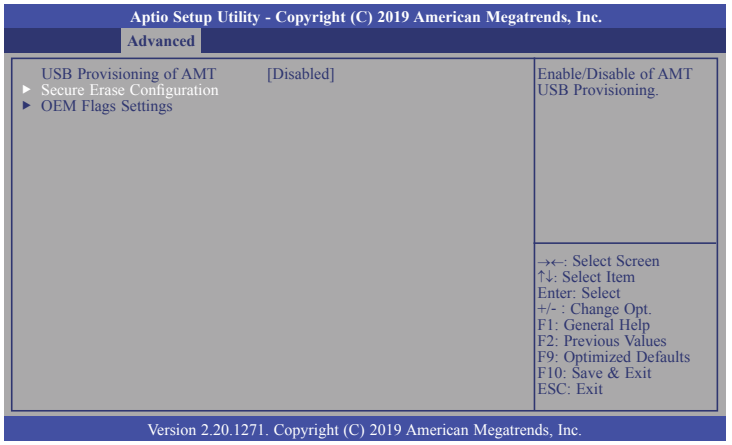
### ME Unconfig on RTC Clear

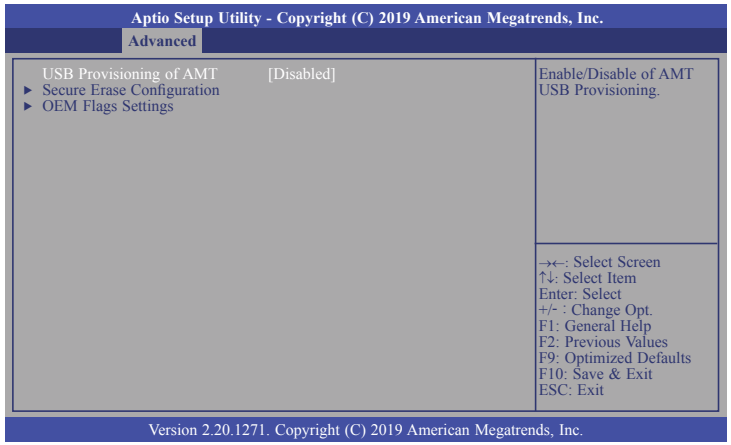
When disabled, ME will not be unconfigured on RTC Clear.

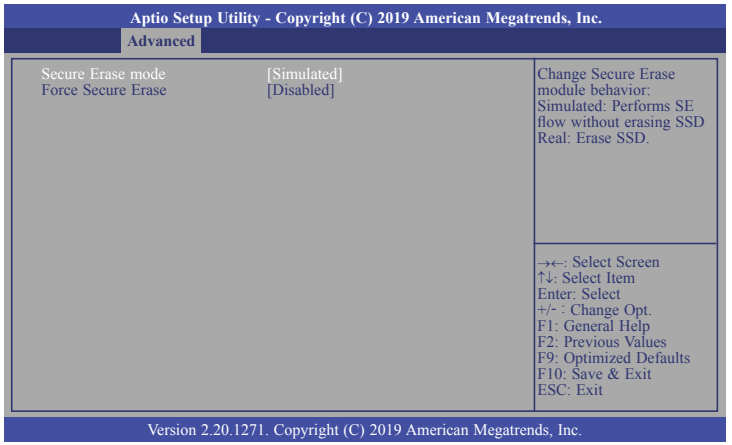
### Firmware Update Configuration

This section is used to configure Management Engine Technology Parameters. Refer page 36 for more information.




### USB Provisioning of AMT

Enable or disable AMT USB Provisioning.

### Secure Erase Configuration

This section is used to configure Secure Erase.

### OEM Flags Settings

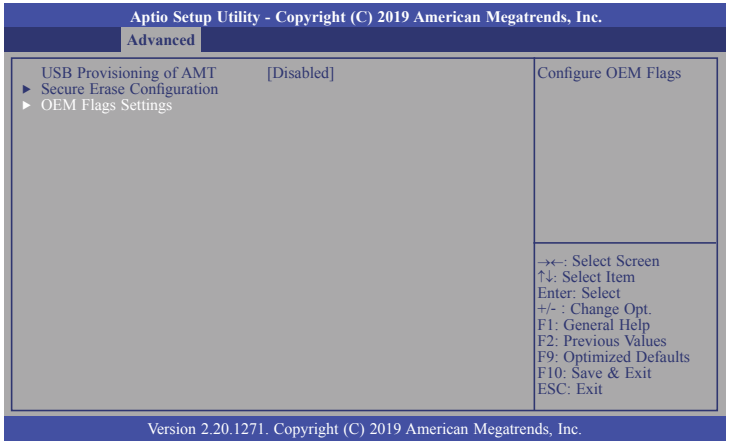
This section is used to configure OEM Flags.

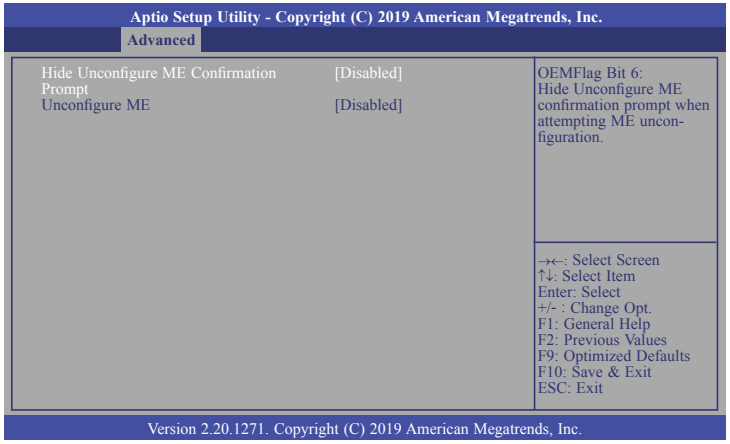
### Secure Erase Mode

Select Secure Erase module behavior: Simulated or Real.

### Force Secure Erase

Enable or disable Force Secure Erase on next boot.



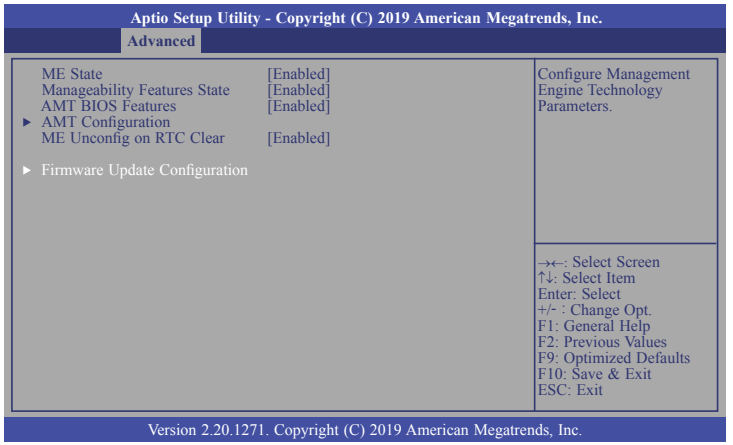



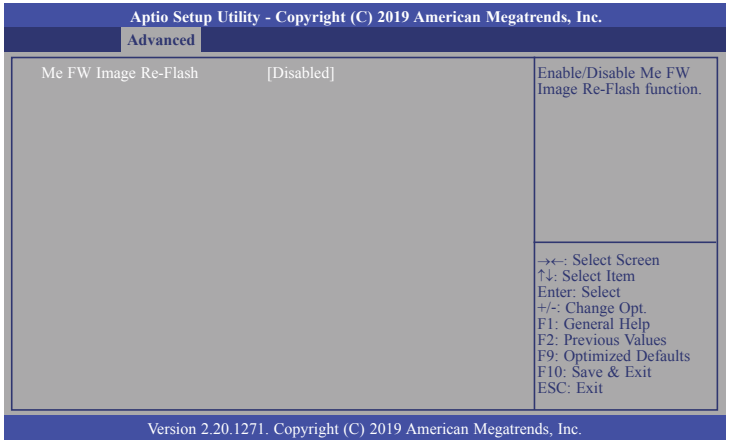

### Hide Unconfigure ME Confirmation Prompt

Enable or disable to hide unconfigure ME confirmation prompt when attempting ME unconfiguration.

### Unconfigure ME

Enable or disable to unconfigure ME with resetting MEBx password to default.



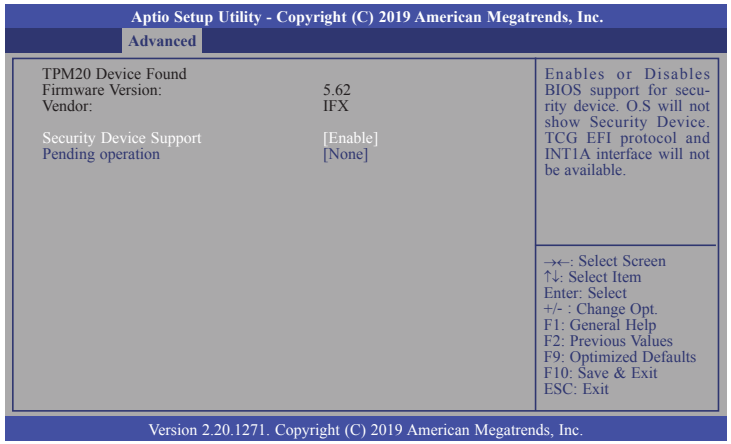




### Me Fw Image Re-Flash

This field is used to enable or disable the Me FW Image Re-Flash function.

## Trusted Computing

This section configures settings relevant to Trusted Computing innovations.




### Security Device Support

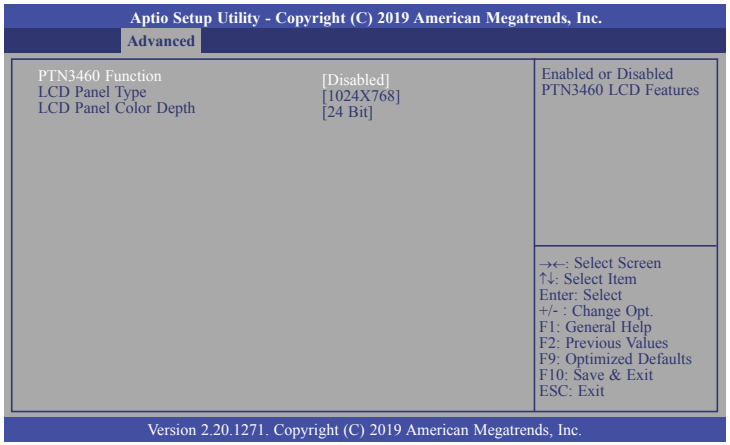
This field is used to enable or disable BIOS support for the security device. O.S will not show the security device. TCG EFI protocol and INT1A interface will not be available.

### Pending operation

This field is used to schedule an operation for the Security Device. Your computer will reboot during restart in order to change State of Security Device.

## PTN3460 Configuration

This section is used to configure the PTN3460 parameters.




### PTN3460 Function

Enable or disable PTN3460 LCD features.

### LCD Panel Type

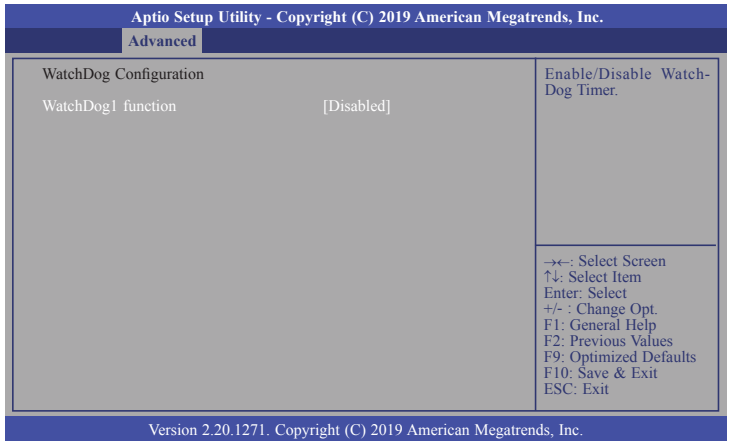
Select LCD Panel Type: 800X480, 800X600, 1024X768, 1366X768, 1280X1024, 1920X1080 or 1920X1200.

### LCD Panel Color Depth

Select LCD Panel Color Depth: 18 Bit, 24 Bit, 36 Bit or 48 Bit.

## WatchDog Configuration

This section configures WatchDog parameters.




### WatchDog1 function

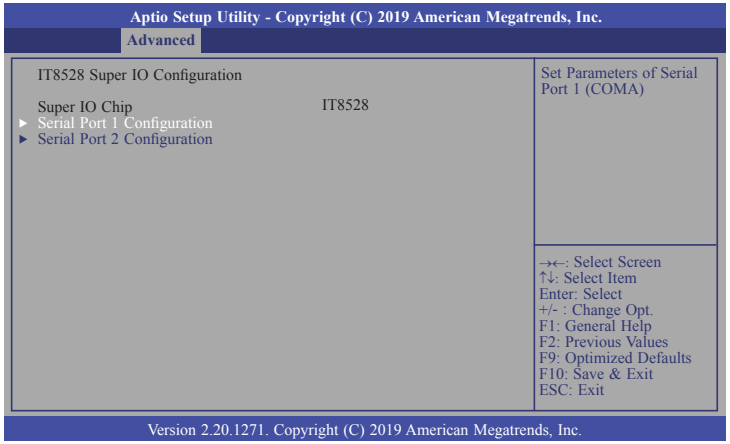
This field is used to enable or disable WatchDog Timer. When enabled, WatchDog1 Timer will show up for configuration.

### WatchDog1 Timer

Set up WatchDog1 Timer in second. The range is from 1 to 255 seconds.

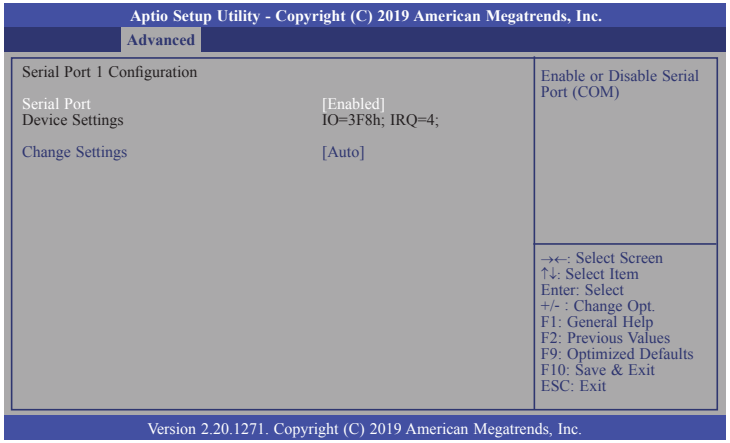
## IT8528 Super IO Configuration

This section is used to configure the I/O functions supported by the onboard Super I/O chip.




### Serial Port 1/2 Configuration

Set the parameters of serial port 1 (COMA)/serial port 2 (COMB).




### Serial Port

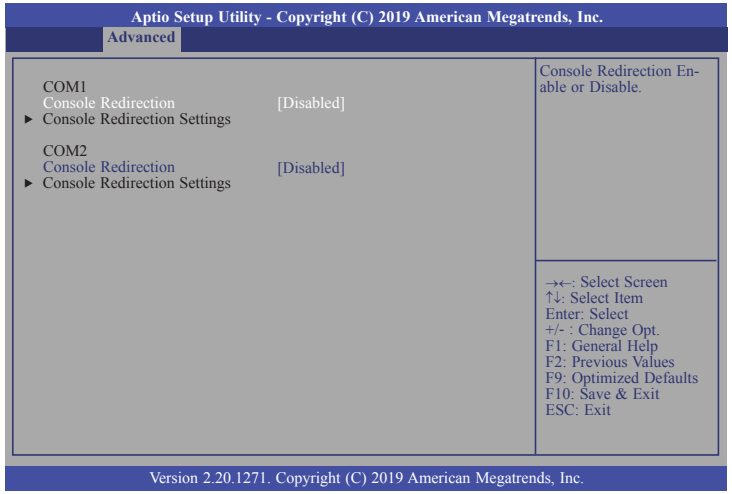
Enable or disable the serial COM port.

### Change Settings

Select an optimal settings for Super IO Device.

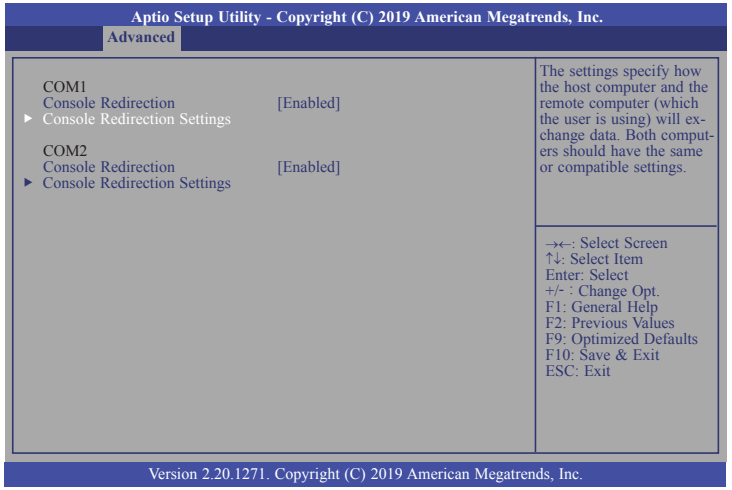
## Serial Port Console Redirection

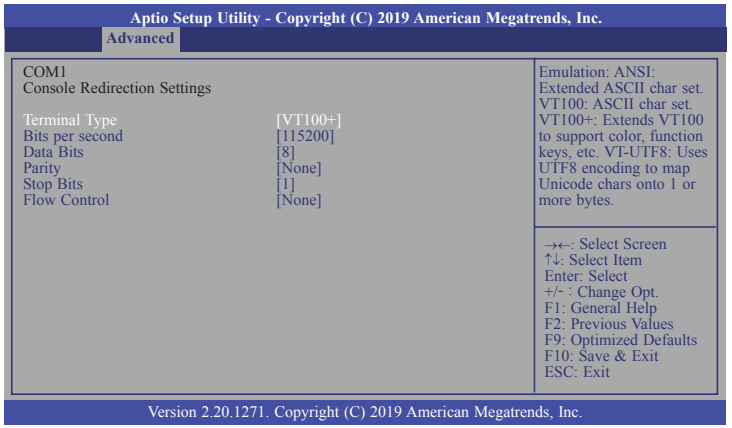
This section configures settings relevant to serial port console redirection.




### Console Redirection

This field is used to enable or disable the console redirection function. When console redirection is set to enabled, console redirection settings are available like below screen.




### Terminal Type

Select terminal type: VT100, VT100+, VT-UTF8 or ANSI.

### Bits per second

Select serial port transmission speed: 9600, 19200, 38400, 57600 or 115200.

### Data Bits

Select data bits: 7 bits or 8 bits.

### Parity

Select parity bits: None, Even, Odd, Mark or Space.

### Stop Bits

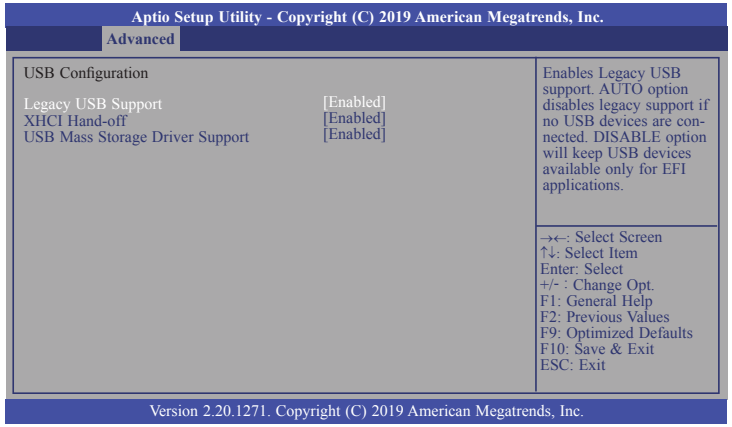
Select stop bits: 1 bit or 2 bits.

### Flow Control

Select flow control: None or Hardware RTS/CTS.

## USB Configuration

This section is used to configure the USB settings.




### Legacy USB Support

**Enabled**

Enable Legacy USB support.

**Disabled**

Keep USB devices available only for EFI applications.

**Auto**

Disable Legacy support if no USB devices are connected.

### XHCI Hand-off

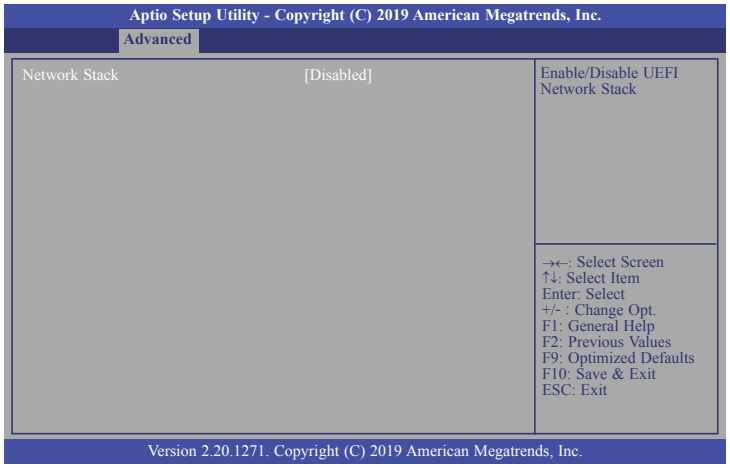
Enable or disable XHCI Hand-off.

### USB Mass Storage Driver Support

Enable or disable USB Mass Storage Driver Support.

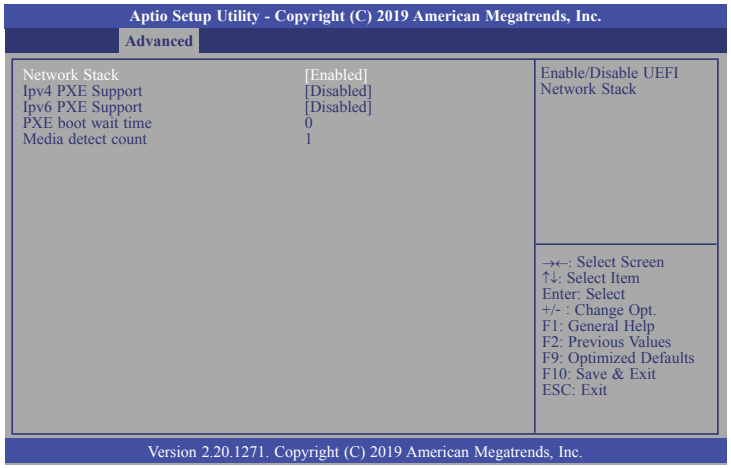
## Network Stack Configuration

This section is used to configure the Network Stack settings.




### Network Stack

This section is used to enable or disable UEFI network stack. When Network Stack is set to enabled, several options will appear for configuration.



### Ipv4 PXE Support

Enable or disable IPv4 PXE boot support. If disabled, IPv4 PXE boot support will not be available.

### Ipv6 PXE Support

Enable or disable IPv6 PXE boot support. If disabled, IPv6 PXE boot support will not be available.

### PXE boot wait time

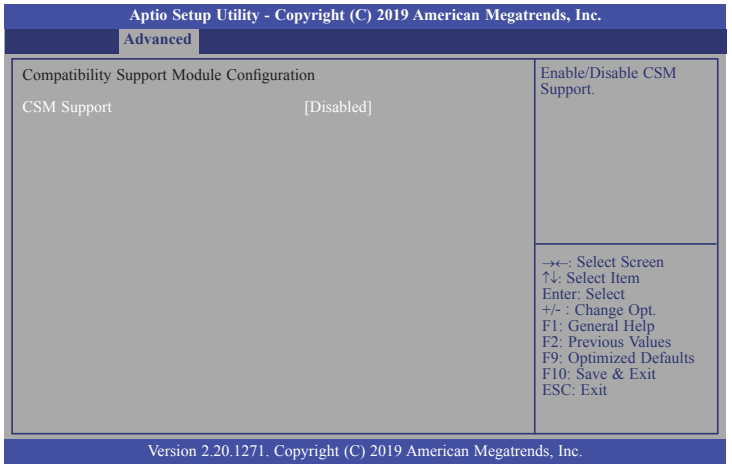
Set the wait time in seconds to press ESC key to abort the PXE boot. Use either +/- or numeric keys to set the value.

### Media detect count

Set the number of times the presence of media will be checked. Use either +/- or numeric keys to set the value.

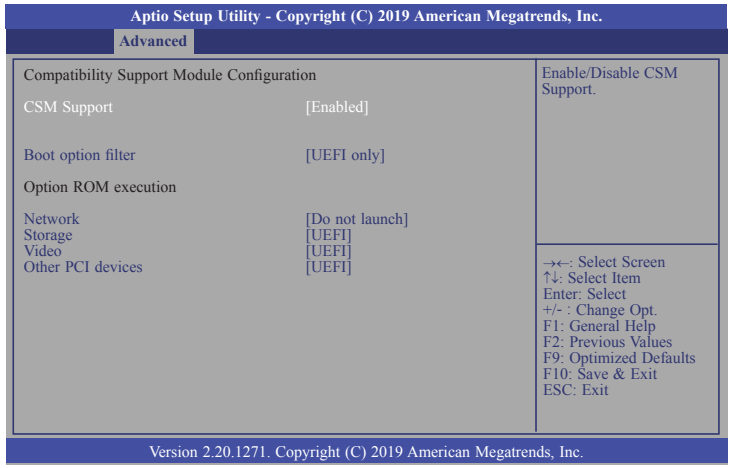
## CSM Configuration

This section is used to configure the CSM settings.




### CSM Support

This section is used to enable or disable CSM Support. When CSM Support is set to enabled, several options will appear for configuration.



### Boot option filter

This field controls Legacy/UEFI ROMs priority.

### Network

This field controls the execution of UEFI and Legacy Network OpROM.

### Storage

This field controls the execution of UEFI and Legacy Storage OpROM.

### Video

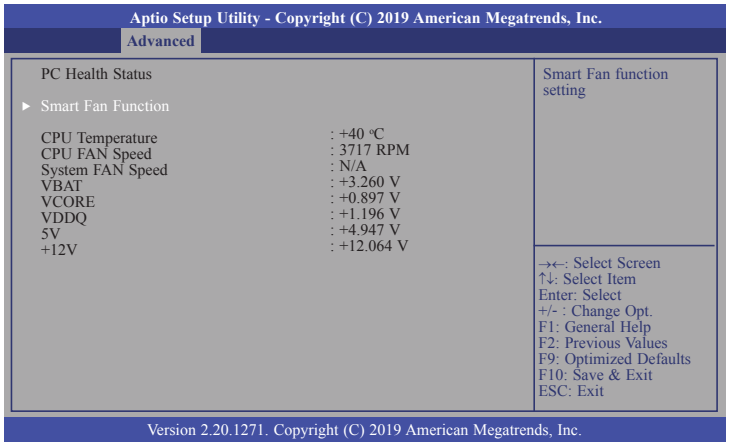
This field controls the execution of UEFI and Legacy Video OpROM.

### Other PCI devices

This field determines OpROM execution policy for devices other than Network, Storage or Video.

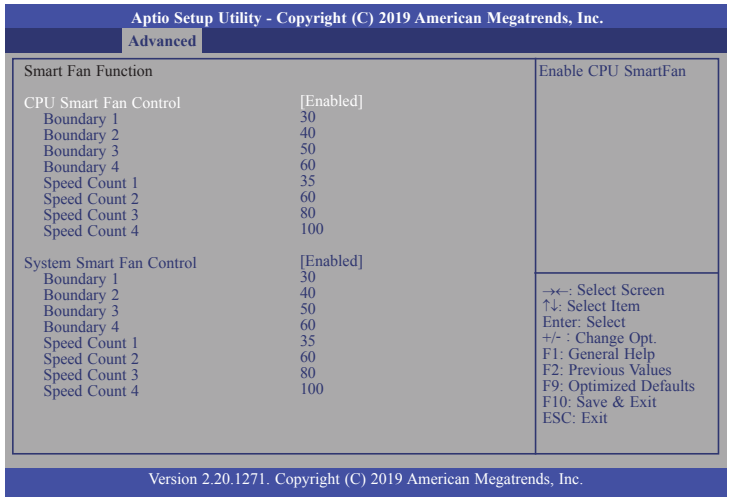
## PC Health Status

This section displays the hardware health monitor and also configures smart fans.




### Smart Fan Function

This section is for smart fan function setting. Refer next page for more information.




### CPU Smart Fan and System Smart Fan Control

Enable or disable the CPU smart fan and system smart fan.

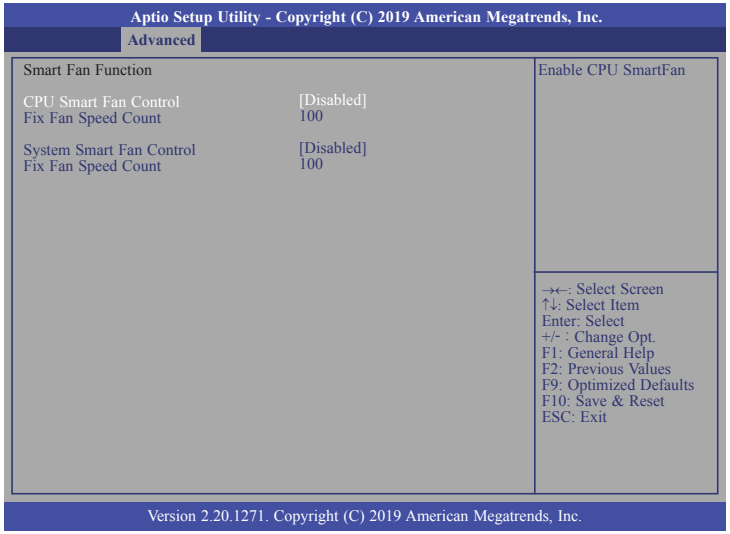
### Boundary 1 to Boundary 4

Set the boundary temperatures that determine the operation of the fan with different fan speeds accordingly. For example, when the system or the CPU temperature reaches boundary temperature 1, the system or CPU fan should be turned on and operate at the designated speed. The range is from 0-127℃.

### Speed Count 1 to Speed Count 4

Set the fan speed. The range is from 1-100% (full speed).

**Note:**
CPU Smart Fan Control and System Smart Fan Control can be switched to [Disabled]. When they are disabled, "Fix Fan Speed Count" will appear for configuration.

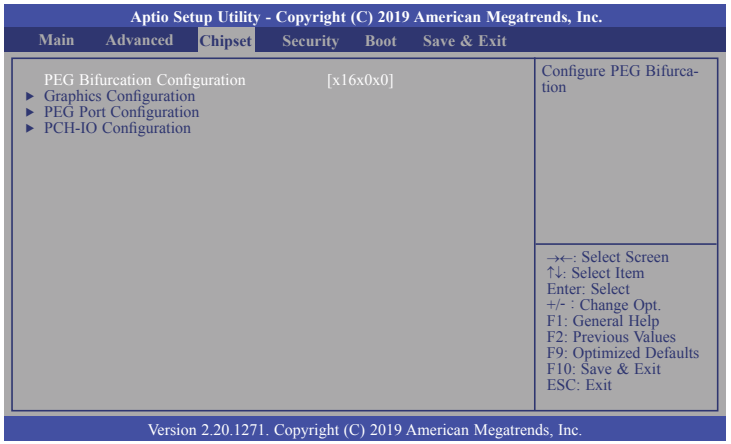



### Fix Fan Speed Count

Set the fix fan speed. The range is from 1-100% (full speed).

## Chipset

This section configures relevant chipset functions.

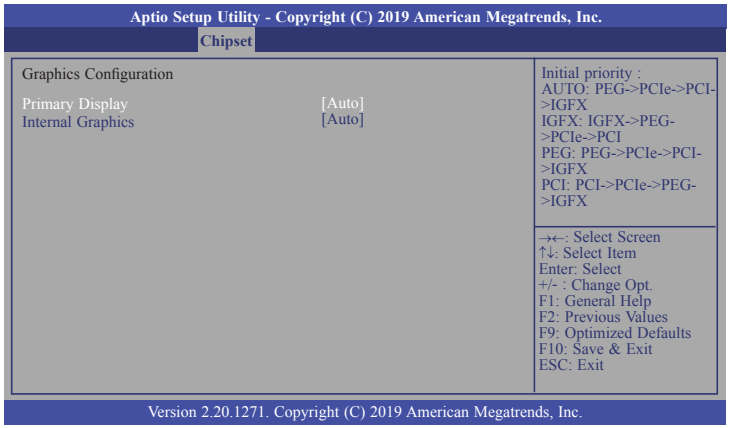



### PEG Bifurcation Configuration

Select PEG Bifurcation: x8x4x4, x8x8x0 or x16x0x0.

### Graphics Configuration

This section configures the Graphics setting.




### Primary Display

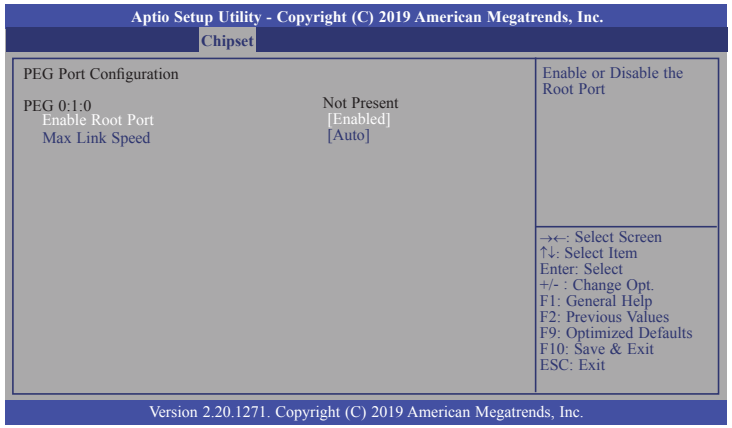
Select Auto/IGFX/PEG/PCI Graphics device to be the primary display.

### Internal Graphics

Keep IGFX enabled based on the setup options.

## PEG Port Configuration

This section configures the PEG port.




### Enable Root Port

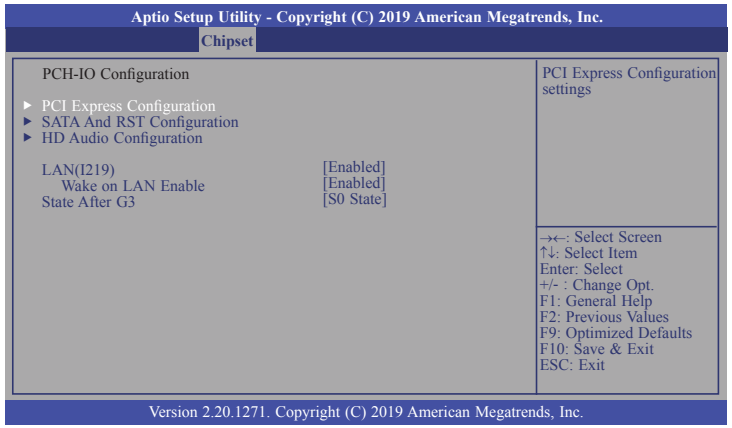
Enable or disable the root port.

### Max Link Speed

Configure PEF 0:1:0 Max Speed: Auto, Gen1, Gen2 or Gen3.

## PCH-IO Configuration

This section illustrates the PCH parameters.




### PCI Express Configuration

This section configures PCI Express settings.

### SATA And RST Configuration

This section configures SATA Device Options settings. Refer next page for more information.

### HD Audio Configuration

This section configures HD Audio Subsystem settings. Refer page 47 for more information.

### LAN(I219)

Enable or disable onboard NIC.

### Wake on LAN Enable

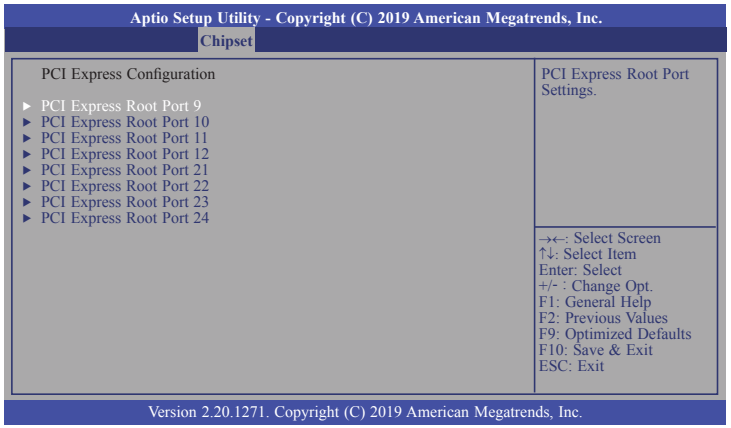
Enable or disable integrated LAN to wake the system.

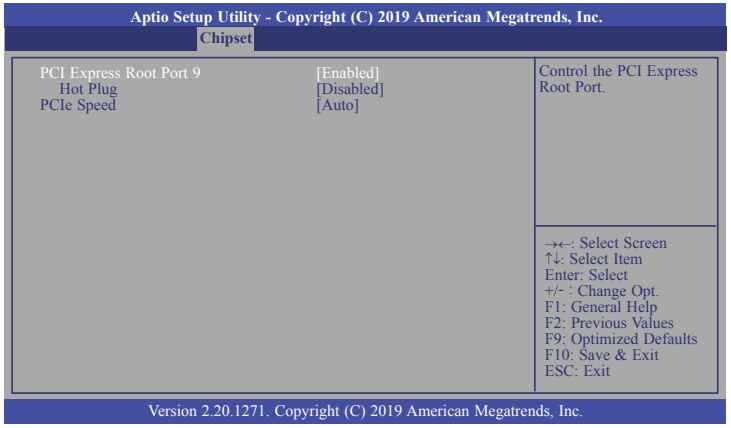
### State After G3

This field is to specify what state the system should be in when power is re-applied after a power failure (G3, the mechanical-off, state).

**S0 State** The system is in working state.

**S5 State** The system is in soft-off state, except for trickle current to devices such as the power button.




### PCI Express Root Port 9/10/11/12/21/22/23/24

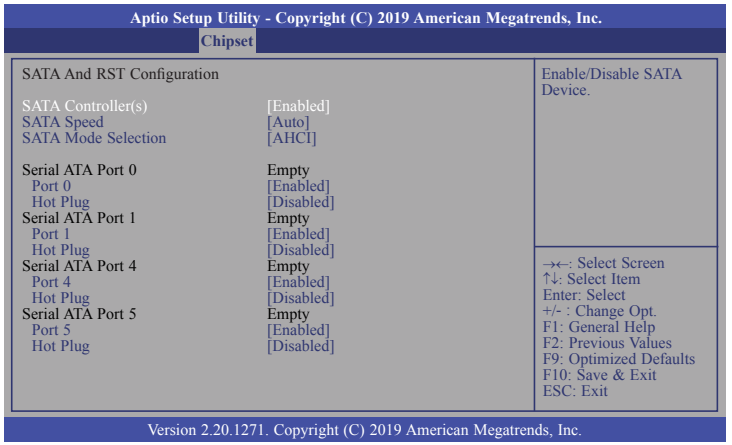
This field is used to enable or disable the PCI express root port.

### Hot Plug

Enable or disable the hot plug function of the PCI Express root port.

### PCIe Speed

Select the speed of the PCI Express root port: Auto, Gen1, Gen 2 or Gen3.




### SATA Controller(s)

This field is used to enable or disable the Serial ATA controller.

### SATA Speed

Select the SATA speed: Auto, Gen1, Gen 2 or Gen3.

### SATA Mode Selection

The mode selection determines how the SATA controller(s) operates.

**AHCI**
This option allows the Serial ATA controller(s) to use AHCI (Advanced Host Controller Interface).

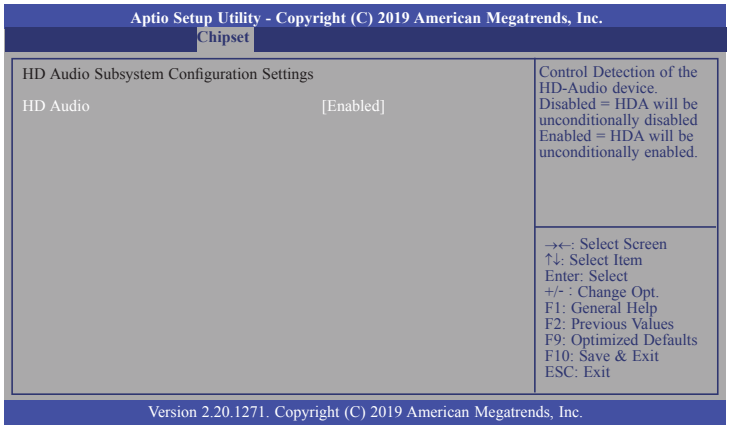
**Intel RST Premium With Intel Optane System Acceleration (for CH960-CM246/QM370 only)**
This option allows you to create RAID or Intel Rapid Storage configuration with Intel® Optane™ system acceleration on Serial ATA devices. When this mode is selected, "Use RST Legacy OROM" field will show up for configuration.

### Use RST Legacy OROM (for CH960-CM246/QM370 only)

Enable or disable to use RST Legacy OROM when CSM is enabled.

### Serial ATA Port 0/1/4/5 and Hot Plug

Enable or disable the Serial ATA port and its hot plug function.



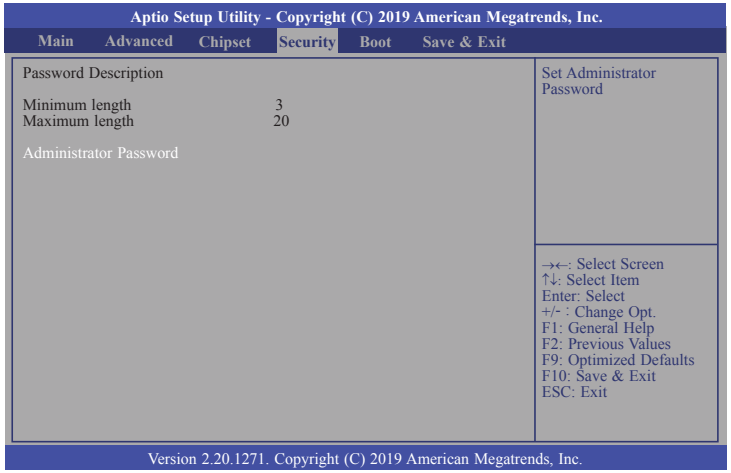

### HD Audio

Control the detection of the HD Audio device.

**Disabled**
HDA will be unconditionally disabled.

**Enabled**
HDA will be unconditionally enabled.

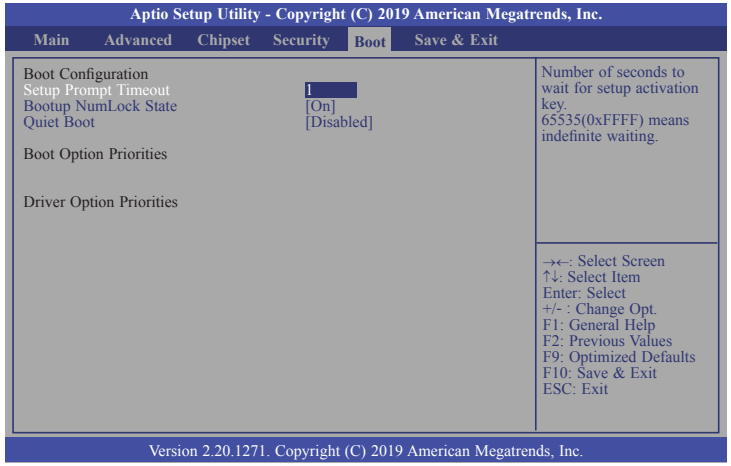
## Security




### Administrator Password

Set the administrator password.

## Boot




### Setup Prompt Timeout

Set the number of seconds to wait for the setup activation key. 65535 (0xFFFF) denotes indefinite waiting.

### Bootup NumLock State

Select the keyboard NumLock state: On or Off.

### Quiet Boot

This section is used to enable or disable quiet boot option.

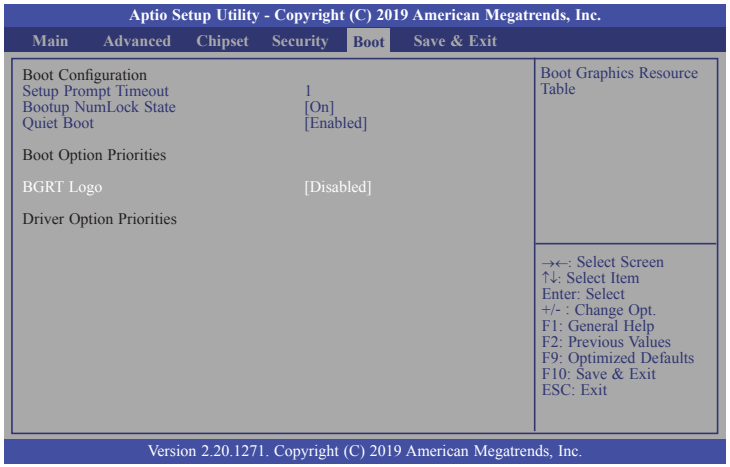
### Boot Option Priorities

Select the system boot order.

### Driver Option Priorities

Select the driver boot order.

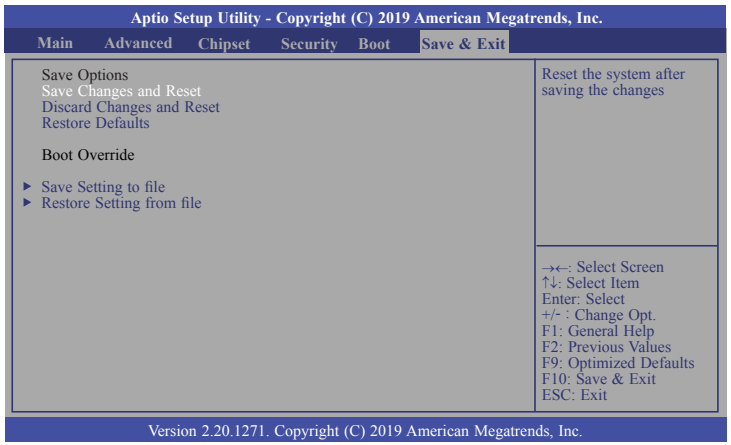
**Note:**
If "Boot option filter" is set to "UEFI and Legacy" or "UEFI only" and "Quiet Boot" is set to enabled, "BGRT Logo" field will show up for configuration. Refer to the Advanced > CSM Configuration for more information.




### BGRT Logo

It is used to enable or disable to support display logo with ACPI Boot Graphics Resource table.

## Save & Exit




### Save Changes and Reset

To save the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system after saving all changes made.

### Discard Changes and Reset

To discard the changes, select this field and then press <Enter>. A dialog box will appear. Select Yes to reset the system setup without saving any changes.

### Restore Defaults

To restore and load the optimized default values, select this field and then press <Enter>. A dialog box will appear. Select Yes to restore the default values of all the setup options.

### Save Setting to file

Select this option to save BIOS configuration settings to a USB flash device.

### Restore Setting from file

This field will appear only when a USB flash device is detected. Select this field to restore setting from the USB flash device.

## Updating the BIOS

To update the BIOS, you will need the new BIOS file and a flash utility. Please contact technical support or your sales representative for the files. You may refer to how-to-video, How to update AMI BIOS in UEFI mode on DFI products?, at https://www.dfi.com/Knowledge/Video/5 for updating the BIOS steps.

## Notice: BIOS SPI ROM

1. The Intel® Management Engine has already been integrated into this system board. Due to the safety concerns, the BIOS (SPI ROM) chip cannot be removed from this system board and used on another system board of the same model.

2. The BIOS (SPI ROM) on this system board must be the original equipment from the factory and cannot be used to replace one which has been utilized on other system boards.

3. If you do not follow the methods above, the Intel® Management Engine will not be updated and will cease to be effective.

**Note:**
a. You can take advantage of flash tools to update the default configuration of the BIOS (SPI ROM) to the latest version anytime.
b. When the BIOS IC needs to be replaced, you have to populate it properly onto the system board after the EEPROM programmer has been burned and follow the technical person's instructions to confirm that the MAC address should be burned or not.

# Chapter 5 - Supported Software

Please download drivers, utilities and software applications required to enhance the performance of the system board at https://www.dfi.com/DownloadCenter .

## Intel Chipset Software Installation Utility

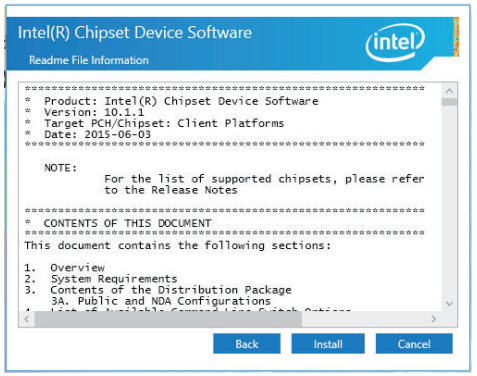
The Intel Chipset Software Installation Utility is used for updating Windows® INF files so that the Intel chipset can be recognized and configured properly in the system.

To install the utility, download "CH960 Chipset Driver" zip file at our website.

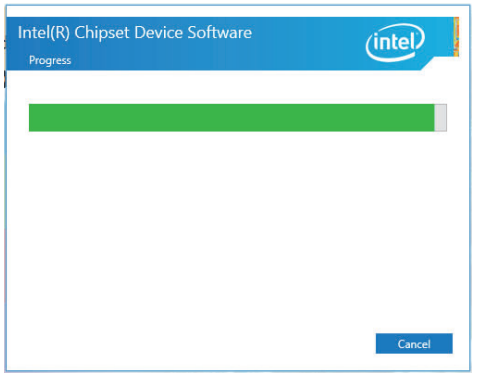
1. Setup is ready to install the utility. Click "Next".

2. Read the license agreement then click "Accept".

3. Go through the readme document for more installation tips then click "Install".




4. The step displays the installing status in the progress.



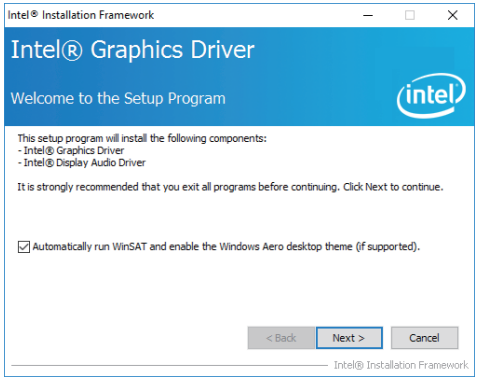

5. After completing installation, click "Restart Now" to exit setup.

   Restarting the system will allow the new software installation to take effect.

## Intel Graphics Drivers

To install the driver, download "CH960 Graphics Driver" zip file at our website.

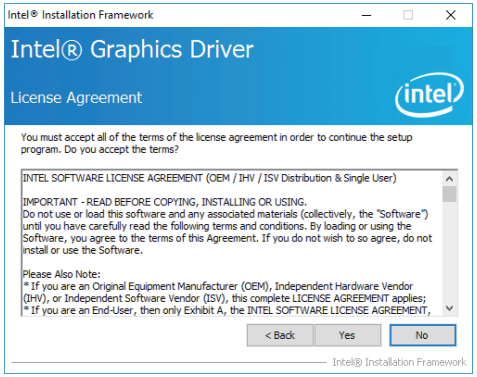
1. Setup is now ready to install the graphics driver. Click "Next".



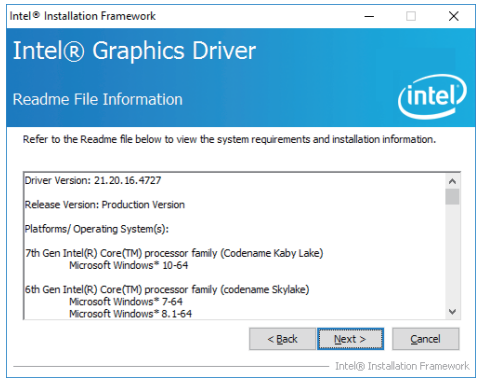

By default, the "Automatically run WinSAT and enable the Windows Aero desktop theme" is enabled. With this enabled, after installing the graphics driver and the system rebooted, the screen will turn blank for 1 to 2 minutes (while WinSAT is running) before the Windows 10 desktop appears. The "blank screen" period is the time Windows is testing the graphics performance.

We recommend that you skip this process by disabling this function then click "Next".

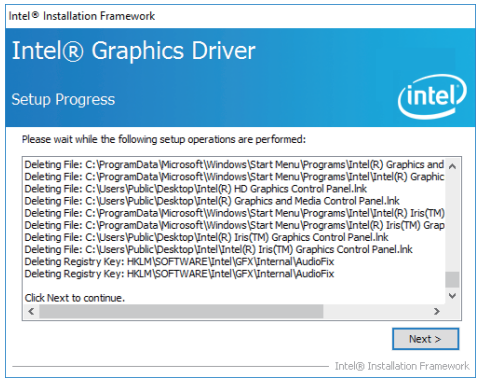
2. Read the license agreement then click "Yes".




3. Go through the readme document for system requirements and installation tips then click "Next".

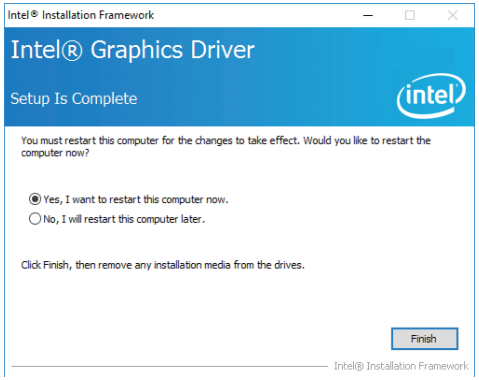



4. Setup is now installing the driver. Click "Next" to continue.




5. Click "Yes, I want to restart this computer now" then click "Finish".

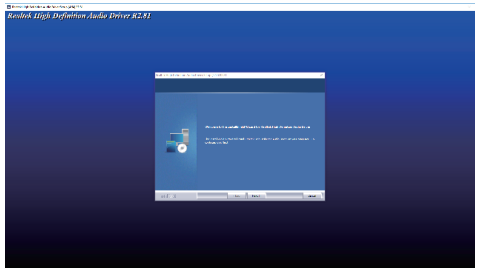
   Restarting the system will allow the new software installation to take effect.



## Audio Drivers

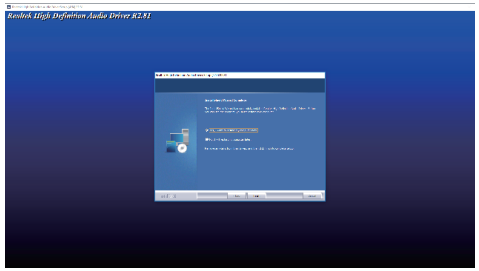
To install the driver, download "CH960 Audio Driver" zip file at our website.

1. Setup is ready to install the driver. Click "Next".




2. Click "Yes, I want to restart my computer now" then click "Finish".

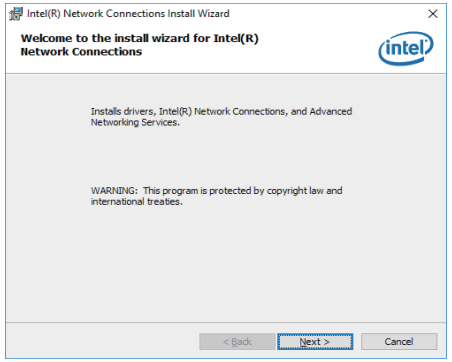
   Restarting the system will allow the new software installation to take effect.



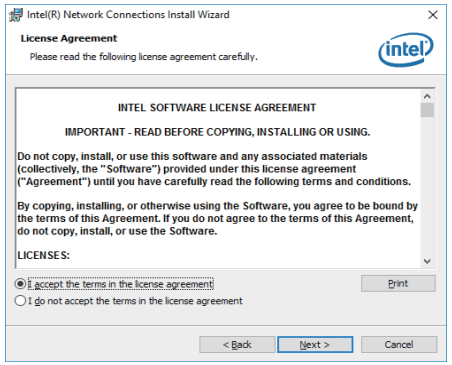

## Intel LAN Drivers

To install the driver, download "CH960 LAN Driver" zip file at our website.

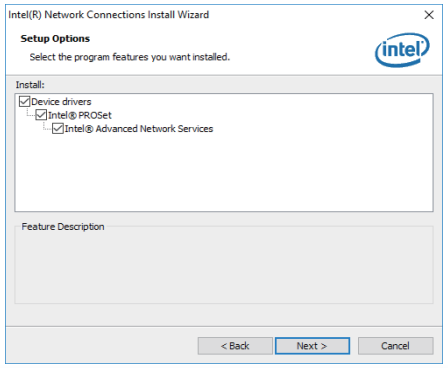
1. Setup is ready to install the driver. Click "Next".



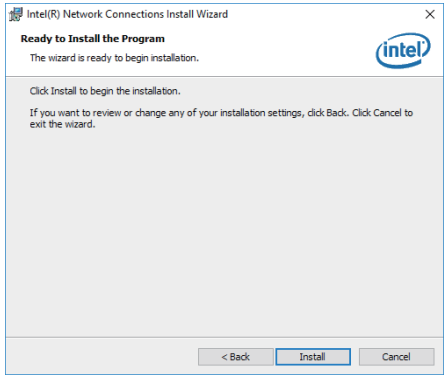

2. Click "I accept the terms in the license agreement" then click "Next".



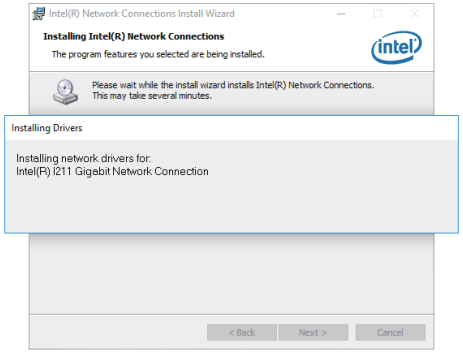

3. Select the program features you want installed then click "Next".



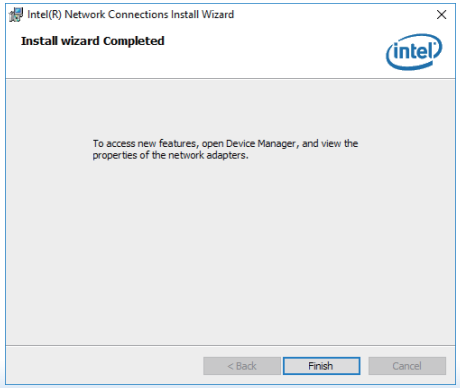
4. Click "Install" to begin the installation.




5. The step displays the installing status in the progress.



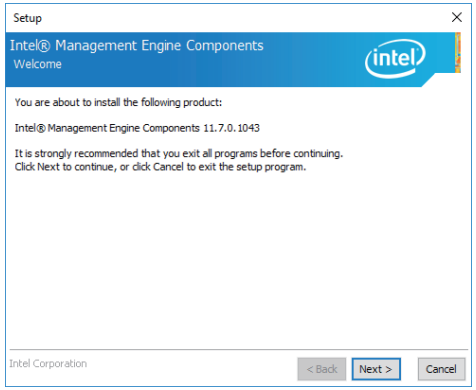

6. After completing installation, click "Finish".



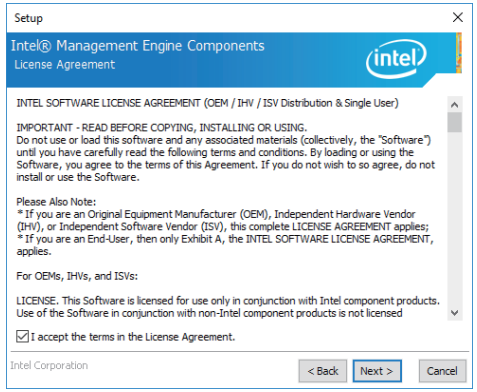

## Intel Management Engine Drivers

To install the driver, download "CH960 MEI Driver" zip file at our website.

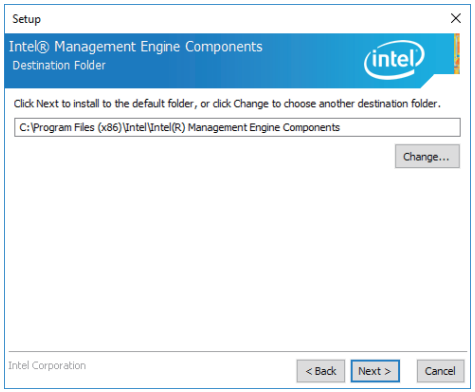
1. Setup is ready to install the driver. Click "Next".



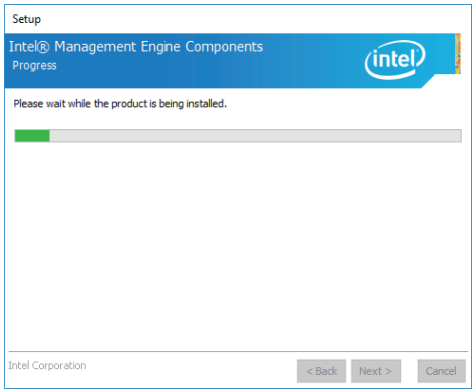

2. Read the license agreement then tick "I accept the terms in the License Agreement". Click "Next".



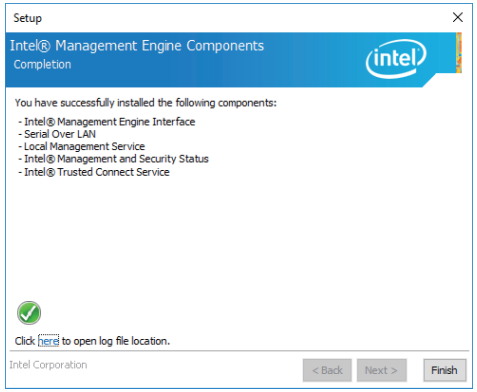
3. Click "Next" to install to the default folder, or click "Change" to choose another destination folder.




4. Please wait while the product is being installed.




5. After completing installation, click "Finish".

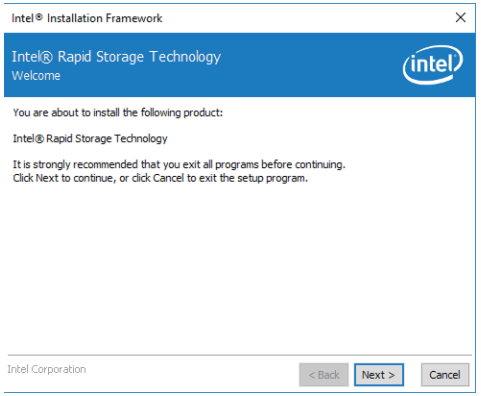



## Intel Rapid Storage Technology

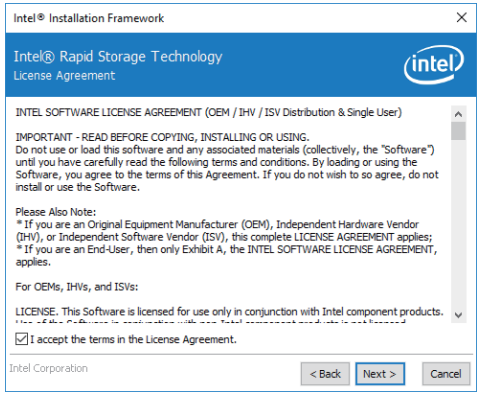
The Intel Rapid Storage Technology is a utility that allows you to monitor the current status of the SATA drives. It enables enhanced performance and power management for the storage subsystem.

To install the driver, download "CH960 IRST Driver" zip file at our website.

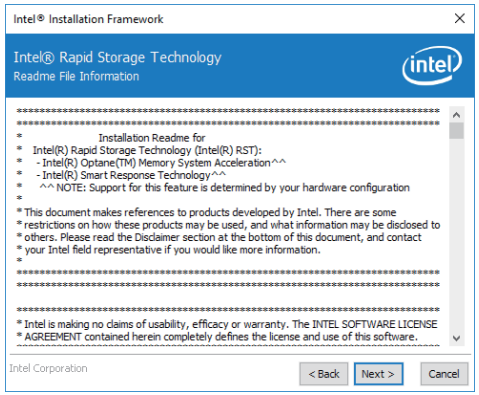
1. Setup is ready to install the utility. Click "Next".



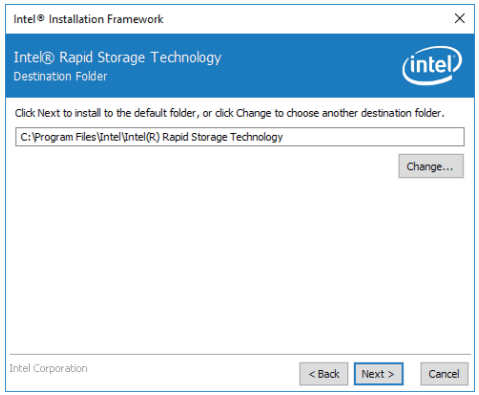

2. Read the license agreement and click "I accept the terms in the License Agreement". Then, click "Next".



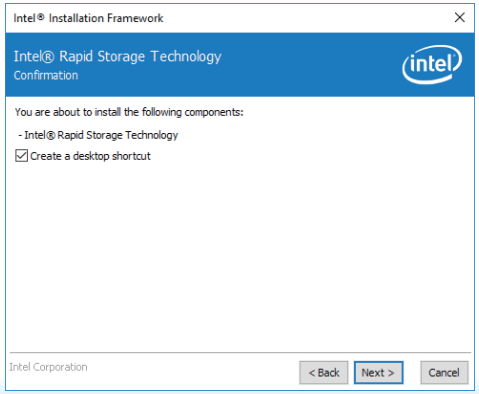
3. Go through the readme document to view system requirements and installation information then click "Next".



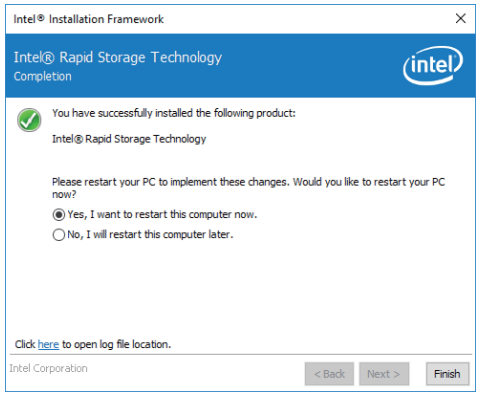

4. Click "Next" to install to the default folder or click "Change to choose another destination folder".




5. Confirm the installation and click "Next".



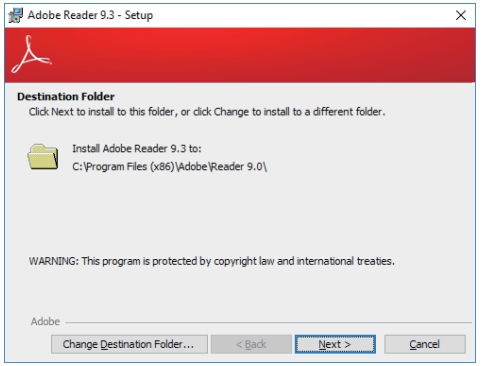

6. Click "Yes, I want to restart this computer now" to complete the installation and then click "Finish".



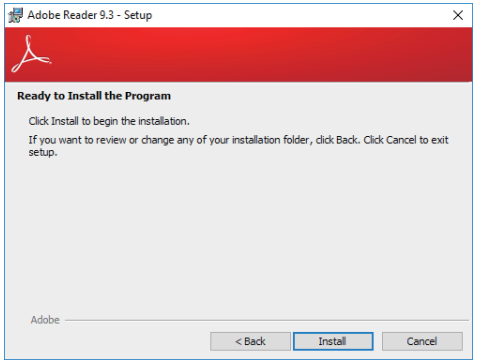
## Adobe Acrobat Reader 9.3

To install the reader, download "CH960-CM246/QM370/HM370 Driver Package" iso file at our website. Click "Adobe Acrobat Reader 9.3".

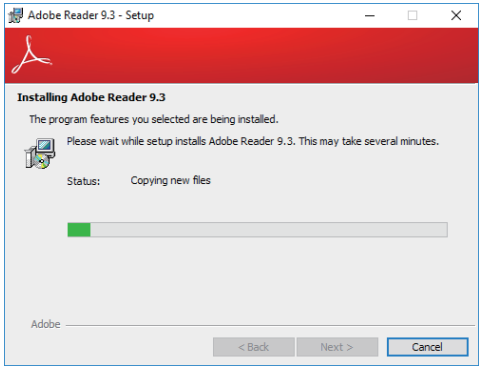
1. Click "Next" to install or click "Change Destination Folder" to select another folder.



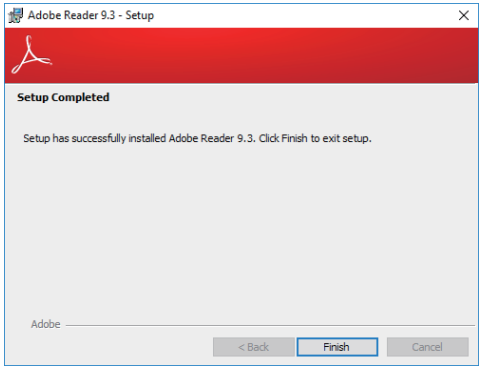

2. Click "Install" to begin installation.




3. Setup is now installing the driver.




4. Click "Finish" to exit installation.



# Chapter 6 - RAID

The system board allows configuring RAID on Serial ATA drives. It supports RAID 0, RAID 1, RAID 5 and RAID 10.

## RAID Levels

### RAID 0 (Striped Disk Array without Fault Tolerance)

RAID 0 uses two new identical hard disk drives to read and write data in parallel, interleaved stacks. Data is divided into stripes and each stripe is written alternately between two disk drives. This improves the I/O performance of the drives at different channel; however it is not fault tolerant. A failed disk will result in data loss in the disk array.

### RAID 1 (Mirroring Disk Array with Fault Tolerance)

RAID 1 copies and maintains an identical image of the data from one drive to the other drive. If a drive fails to function, the disk array management software directs all applications to the other drive since it contains a complete copy of the drive's data. This enhances data protection and increases fault tolerance to the entire system. Use two new drives or an existing drive and a new drive but the size of the new drive must be the same or larger than the existing drive.

### RAID 5

RAID 5 stripes data and parity information across hard drives. It is fault tolerant and provides better hard drive performance and more storage capacity.

### RAID 10 (Mirroring and Striping)

RAID 10 is a combination of data striping and data mirroring providing the benefits of both RAID 0 and RAID 1. Use four new drives or an existing drive and three new drives for this configuration.

| RAID Level | Min. Drives | Protection | Description |
|---|---|---|---|
| RAID 0 | 2 | None | Data striping without redundancy |
| RAID 1 | 2 | Single Drive Failure | Disk mirroring |
| RAID 5 | 3 | Single Drive Failure | Block-level data striping with distributed parity |
| RAID 10 | 4 | 1 Disk Per Mirrored Stripe (not same mirror) | Combination of RAID 0 (data striping) and RAID 1 (mirroring) |

## Settings

To enable the RAID function, the following settings are required.

1. Connect the Serial ATA drives.
2. Configure Serial ATA in the AMI BIOS.
3. Configure RAID in the RAID BIOS.
4. Install the RAID driver during OS installation.
5. Install the Intel Rapid Storage Drivers.

### Step 1: Connect the Serial ATA Drives

Refer to chapter 2 for details on connecting the Serial ATA drives.

**Important:**
1. Make sure you have installed the Serial ATA drives and connected the data cables otherwise you won't be able to enter the RAID BIOS utility.
2. Treat the cables with extreme caution especially while creating RAID. A damaged cable will ruin the entire installation process and operating system. The system will not boot and you will lost all data in the hard drives. Please give special attention to this warning because there is no way of recovering back the data.

### Step 2: Configure Serial ATA in the AMI BIOS

1. Power-on the system then press <Del> to enter the main menu of the AMI BIOS.
2. Configure Serial ATA in the appropriate fields.
3. Save the changes in the Save & Exit menu.
4. Reboot the system.

### Step 3: Configure RAID in the RAID BIOS

When the system powers-up and all drives have been detected, the Intel RAID BIOS status message screen will appear. Press the <Ctrl> and <I> keys simultaneously to enter the utility. The utility allows you to build a RAID system on Serial ATA drives.

## Step 4: Install the RAID Driver During OS Installation

The RAID driver must be installed during the Windows® XP or Windows® 2000 installation using the F6 installation method. This is required in order to install the operating system onto a hard drive or RAID volume when in RAID mode or onto a hard drive when in AHCI mode.

1. Start Windows Setup by booting from the installation CD.

2. Press <F6> when prompted in the status line with the 'Press F6 if you need to install a third party SCSI or RAID driver' message.

3. Press <S> to "Specify Additional Device".

4. At this point you will be prompted to insert a floppy disk containing the RAID driver. Insert the RAID driver diskette.

5. Locate for the drive where you inserted the diskette then select RAID or AHCI controller that corresponds to your BIOS setup. Press <Enter> to confirm.

You have successfully installed the driver. However you must continue installing the OS. Leave the floppy disk in the floppy drive until the system reboots itself because Windows setup will need to copy the files again from the floppy disk to the Windows installation folders. After Windows setup has copied these files again, remove the floppy diskette so that Windows setup can reboot as needed.

## Step 5: Install the Intel Rapid Storage Technology Utility

The Intel Rapid Storage Technology Utility can be installed from within Windows. It allows RAID volume management (create, delete, migrate) from within the operating system. It will also display useful SATA device and RAID volume information. The user interface, tray icon service and monitor service allow you to monitor the current status of the RAID volume and/or SATA drives. It enables enhanced performance and power management for the storage subsystem.

Pleaser refer chapter 5 to install the IRST driver.

# Chapter 7 - Intel AMT Settings (CH960-CM246/QM370 only)

## Overview

Intel Active Management Technology (Intel® AMT) combines hardware and software solution to provide maximum system defense and protection to networked systems.

The hardware and software information are stored in non-volatile memory. With its built-in manageability and latest security applications, Intel® AMT provides the following functions.

### • Discover

Allows remote access and management of networked systems even while PCs are powered off; significantly reducing desk-side visits.

### • Repair

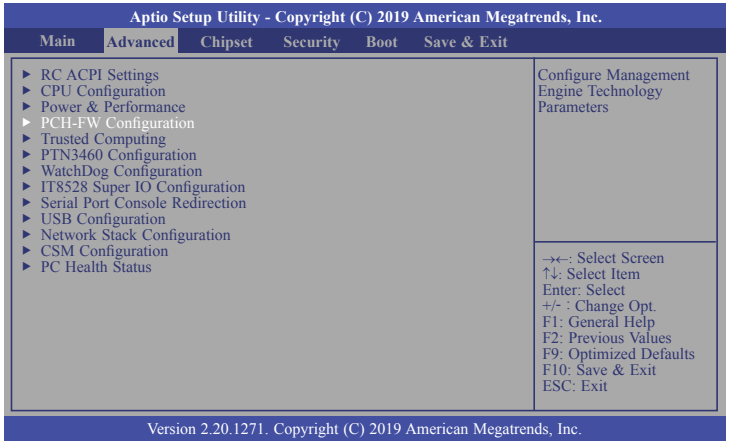
Remotely repair systems after OS failures. Alerting and event logging help detect problems quickly to reduce downtime.

### • Protect

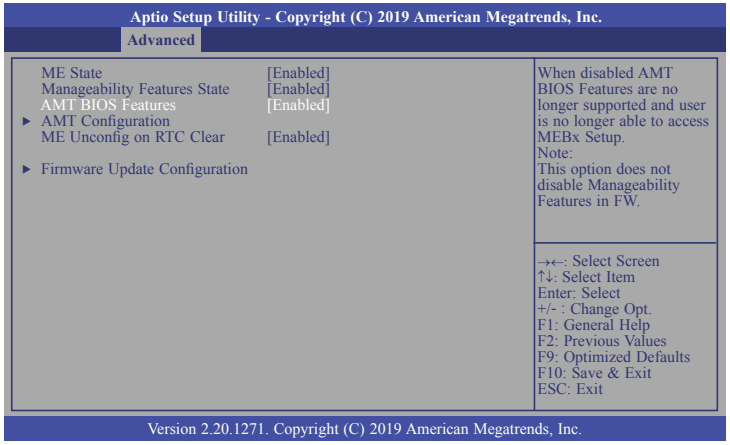
Intel AMT's System Defense capability remotely updates all systems with the latest security software. It protects the network from threats at the source by proactively blocking incoming threats, reactively containing infected clients before they impact the network, and proactively alerting when critical software agents are removed.

## Enable Intel® AMT in the AMI BIOS

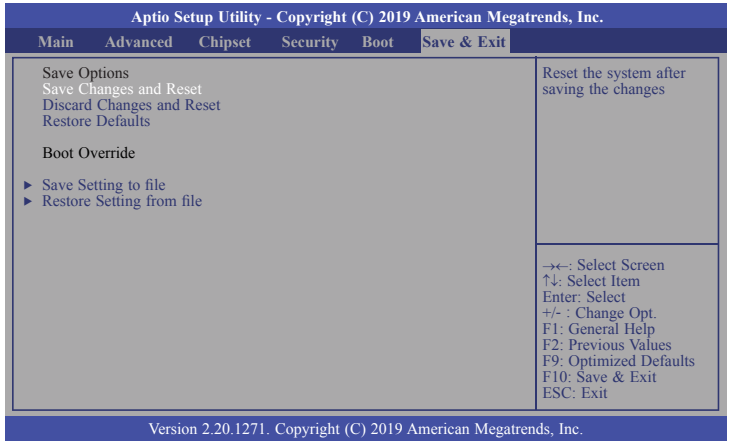
1. Power-on the system then press <Del> to enter the main menu of the Insyde BIOS.
2. In the **Advanced** menu, select **PCH-FW Configuration**.




3. Select **Enabled** in the **AMT BIOS Features** field.

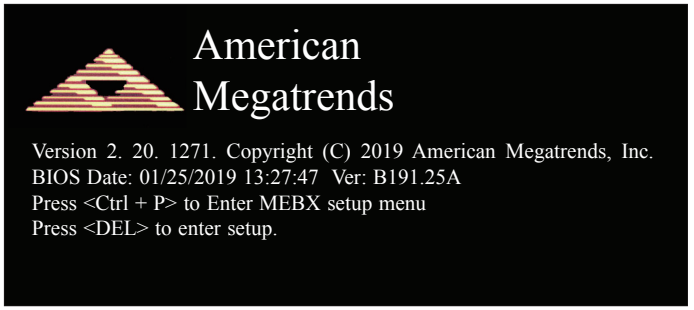


4. In the **Save & Exit** menu, select **Save Changes and Reset** and then press <Enter>. A dialog box will appear. Select **Yes** and press Enter to reset the system after saving all changes made.

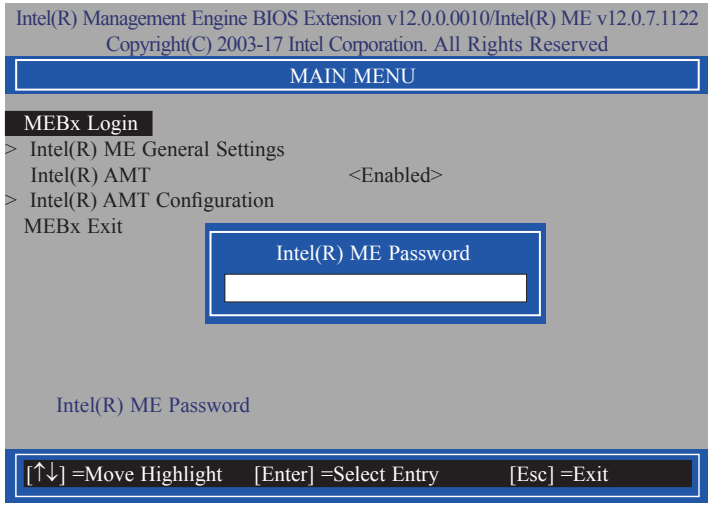



## Configure Intel® AMT in the Intel® Management Engine BIOS Extension (MEBX) Setup Menu

1. When the system reboots, the following message will be displayed. Press **<Ctrl + P>** as soon as the message is displayed; as this message will be displayed for only a few seconds.

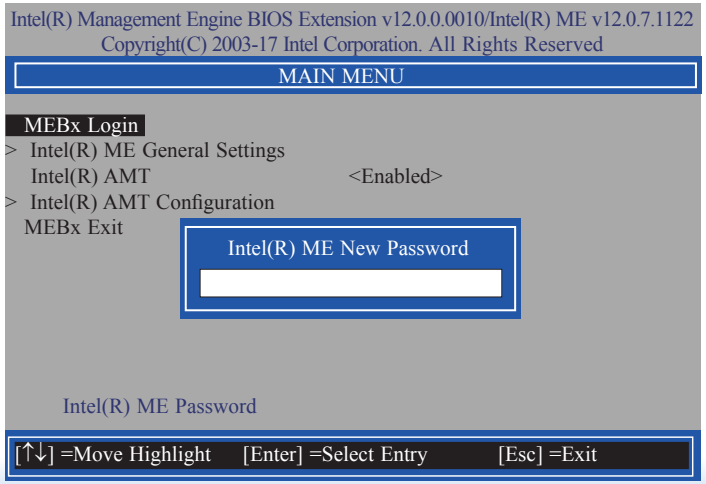


2. Select **MEBx Login** and press Enter. You will be prompted for a password. The default password is "**admin**". Enter the default password in the space provided under Intel(R) ME Password then press Enter.

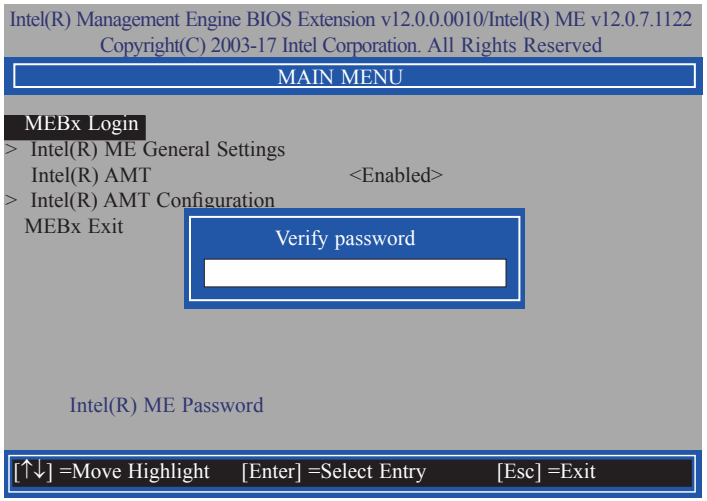



3. Enter a new password in the space provided under Intel(R) ME New Password then press Enter. The password must include:

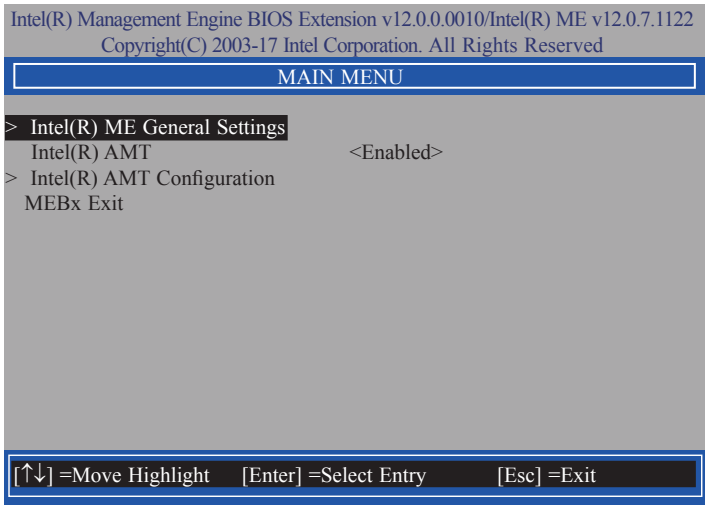
- 8-32 characters
- Strong 7-bit ASCII characters excluding **: ,** and **"** characters
- At least one digit character (0, 1, ...9)
- At least one 7-bit ASCII non alpha-numeric character, above 0x20, (e.g. !, $, ;)
- Both lower case and upper case characters




4. You will be asked to verify the new password. Enter the same new password in the space provided under Verify Password then press Enter.



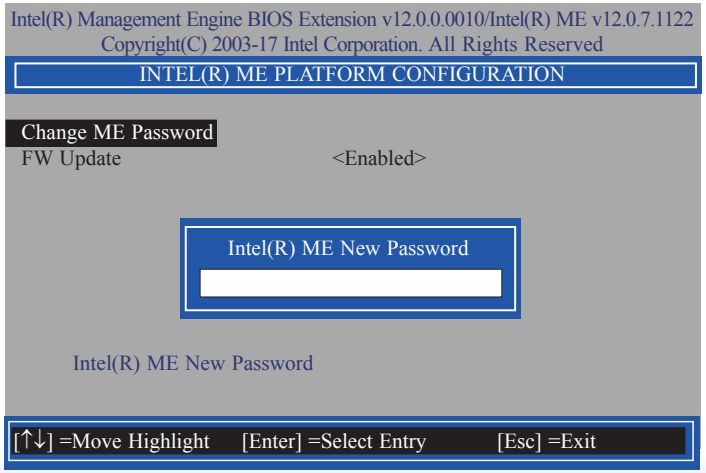

5. Select **Intel(R) ME General Settings** then press Enter.



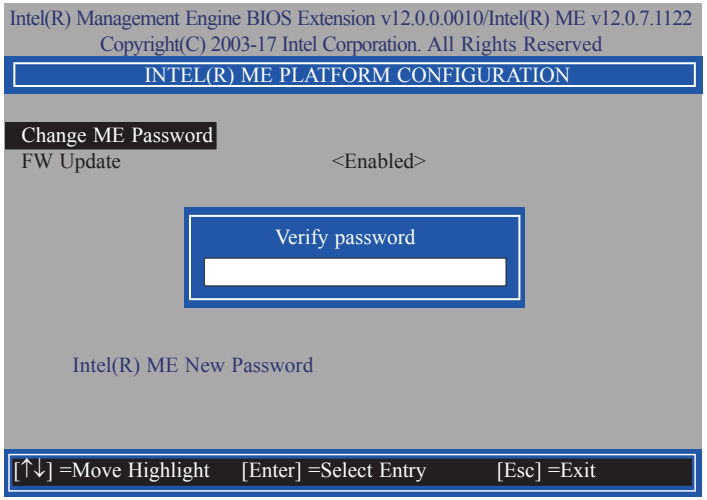
6. If you want to change ME password, select **Change ME Password** then press Enter. Enter the current password in the space provided under Intel(R) ME Password then press Enter.

7. Enter a new password in the space provided under Intel(R) ME New Password then press Enter. The password must include:

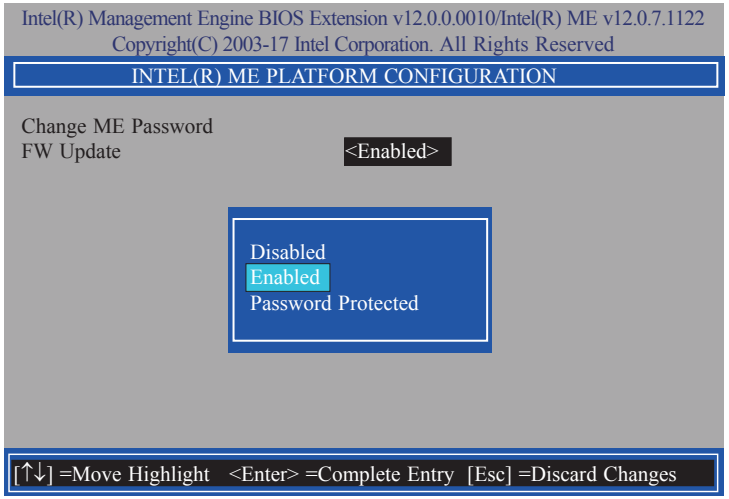
- 8-32 characters
- Strong 7-bit ASCII characters excluding **: ,** and **"** characters
- At least one digit character (0, 1, ...9)
- At least one 7-bit ASCII non alpha-numeric character, above 0x20, (e.g. !, $, ;)
- Both lower case and upper case characters



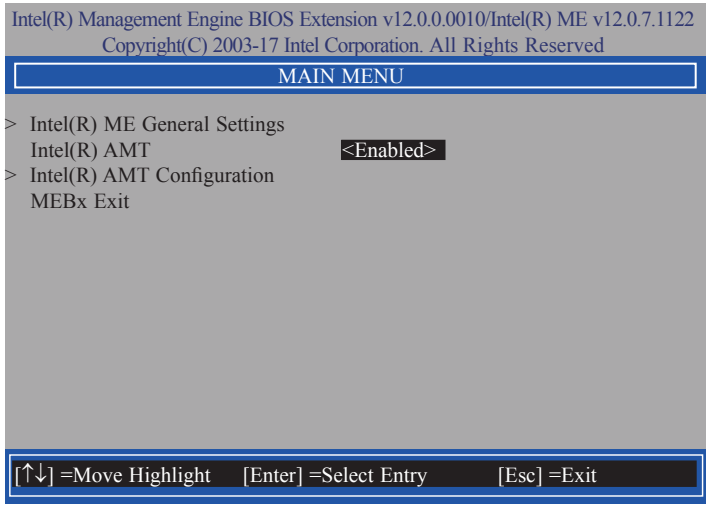

8. You will be asked to verify the new password. Enter the same new password in the space provided under Verify Password then press Enter.



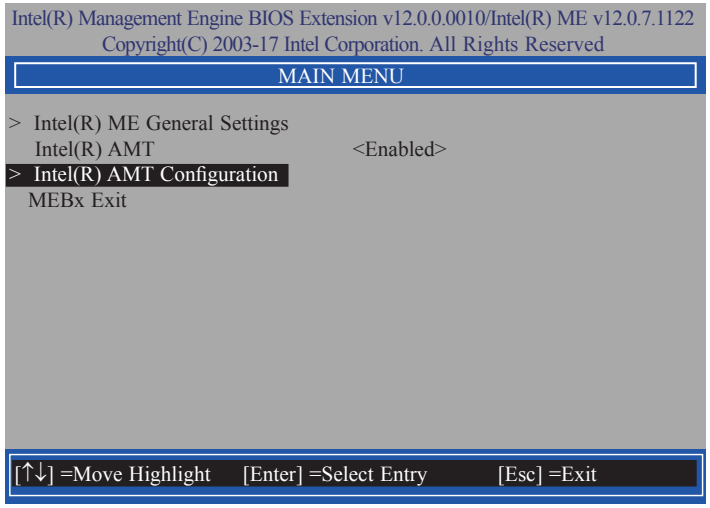

9. Select **FW Update** then press Enter. Select **Enabled** or **Disabled** or **Password Protected** then press Enter.



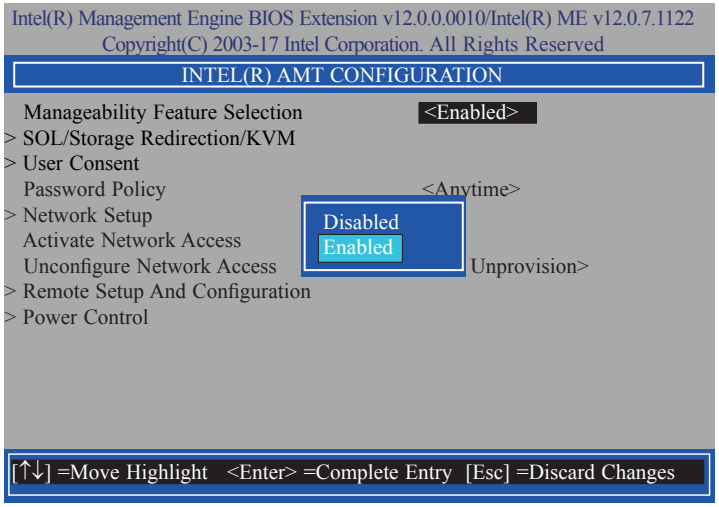
10. Press Esc until you return to the **Main Menu**. Select **Intel(R) AMT** then press Enter. Select **Enabled** or **Disabled** then press Enter.



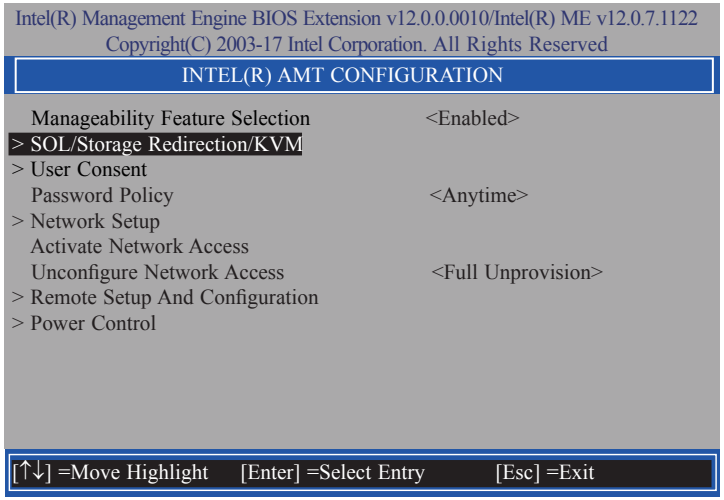

11. Select **Intel(R) AMT Configuration** then press Enter.



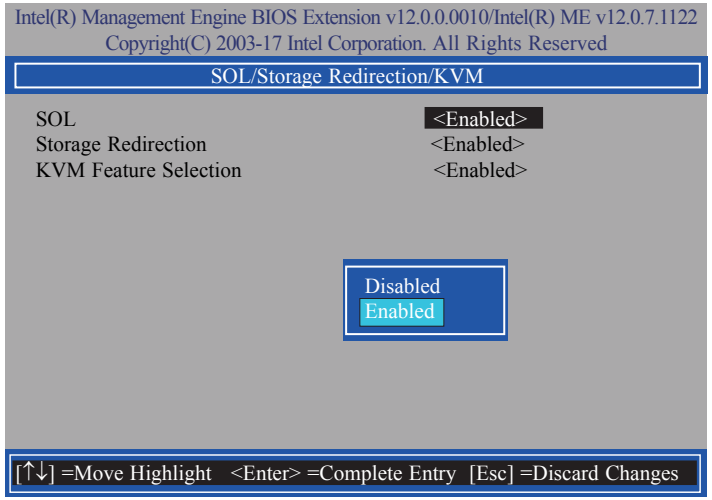

12. In the **Intel(R) AMT Configuration** menu, select **Manageability Feature Selection** then press Enter. Select **Enabled** or **Disabled** then press Enter.



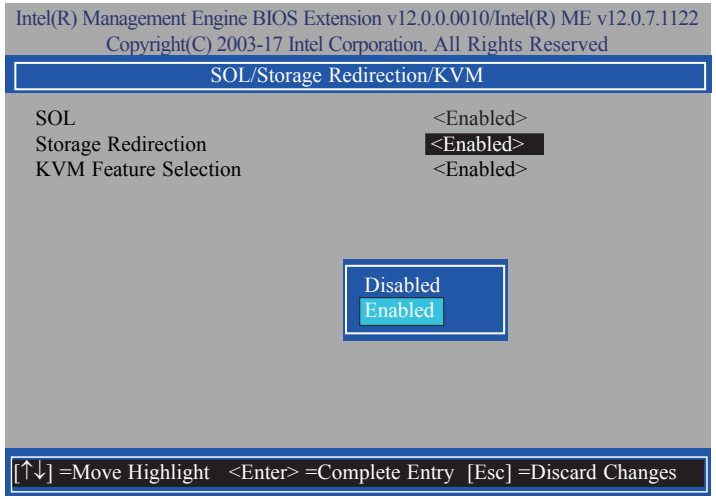

13. In the **Intel(R) AMT Configuration** menu, select **SOL/Storage Redirection/KVM** then press Enter.



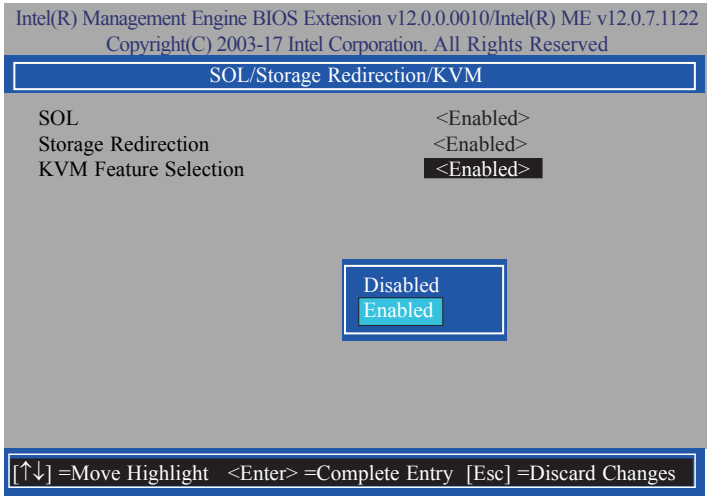
14. Select **SOL** then press Enter. Select **Enabled** or **Disabled** then press Enter.



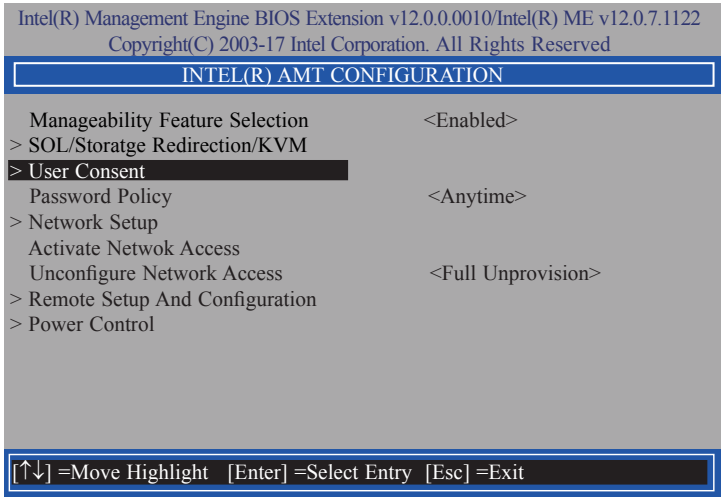

15. Select **Storage Redirection** then press Enter. Select **Enabled** or **Disabled** then press Enter.



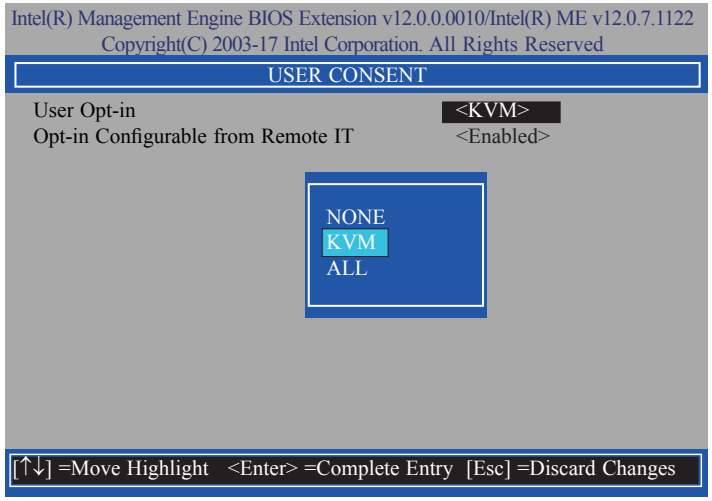

16. Select **KVM Feature Selection** then press Enter. Select **Enabled** or **Disabled** then press Enter.



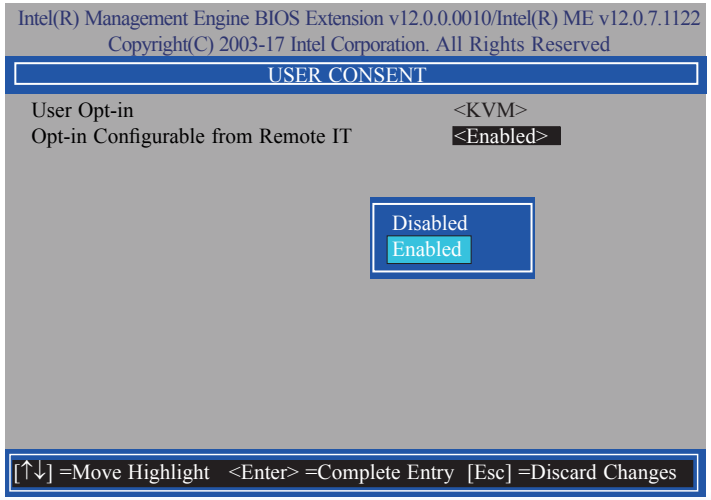

17. Press Esc until you return to the **Intel(R) AMT Configuration** menu. Select **User Consent** then press Enter.



18. In the **User Consent** menu**,** select **User Opt-in** then press Enter. Select **NONE** or **KVM** or **ALL** then press Enter.

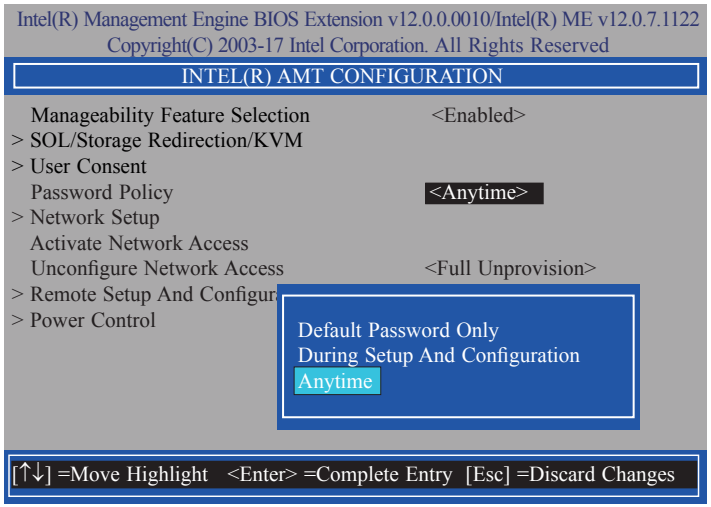



19. Select **Opt-in Configurable from Remote IT** then press Enter. Select **Enabled** or **Disabled** then press Enter.

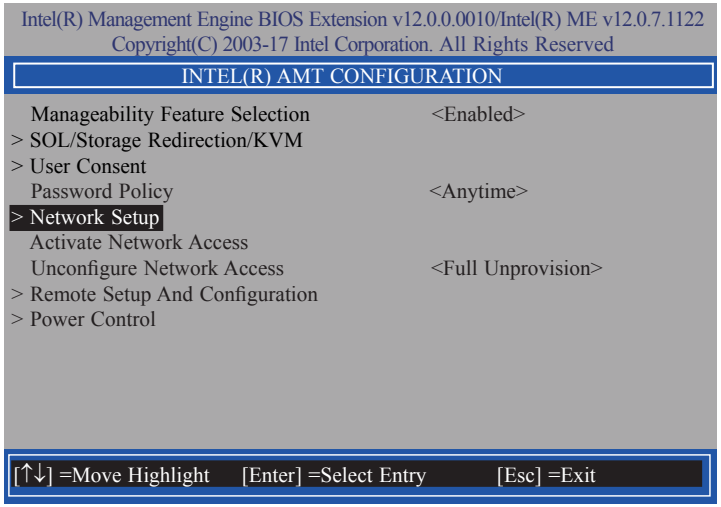



20. Press Esc until you return to the **Intel(R) AMT Configuration** menu. Select **Password Policy** then press Enter.

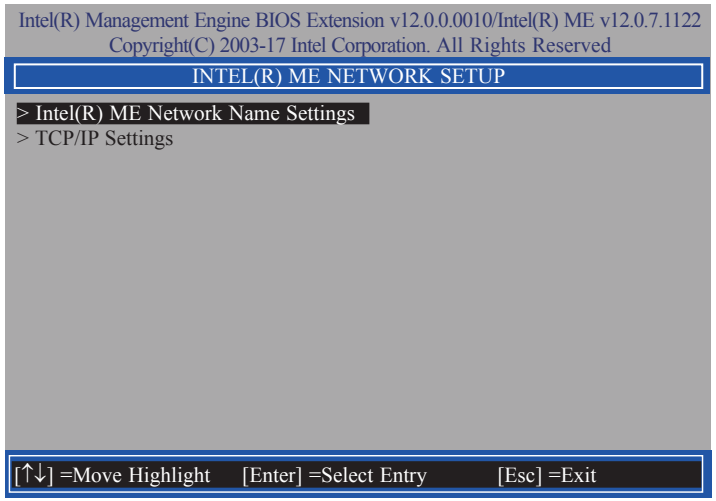
You may choose to use a password only during setup and configuration or to use a password anytime the system is being accessed.



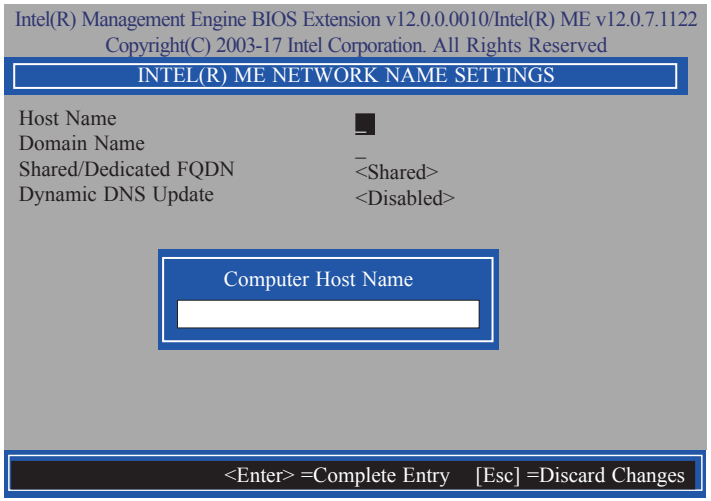

21. In the **Intel(R) AMT Configuration** menu**,** select **Network Setup** then press Enter.



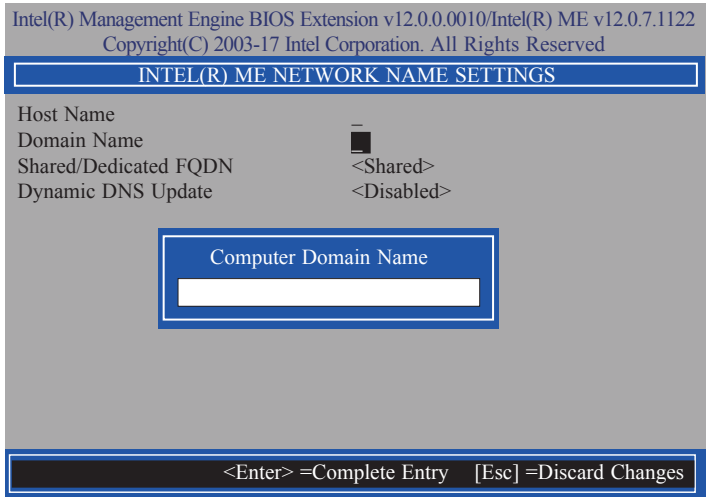
22. In the **Intel(R) ME Network Setup** menu, select **Intel(R) ME Network Name Settings** then press Enter.



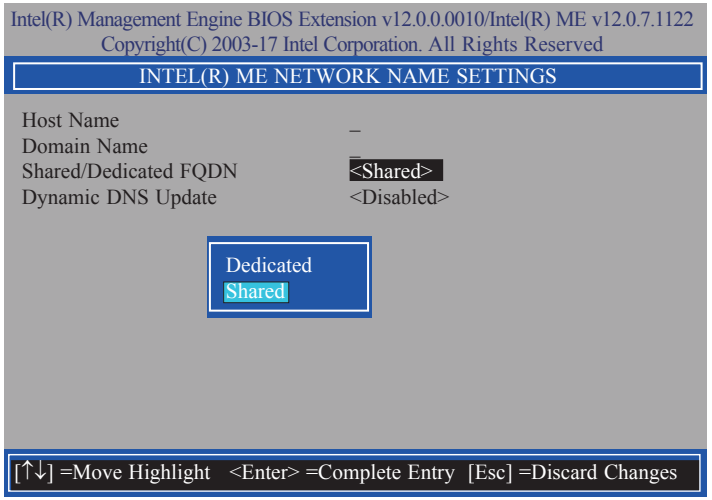

23. In the **Intel(R) ME Network Name Settings** menu, select **Host Name** then press Enter. Enter the computer's host name then press Enter.



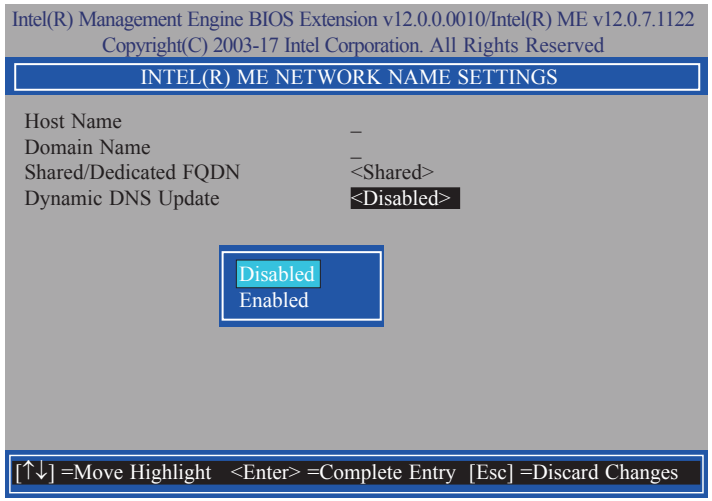

24. Select **Domain Name** then press Enter. Enter the computer's domain name then press Enter.



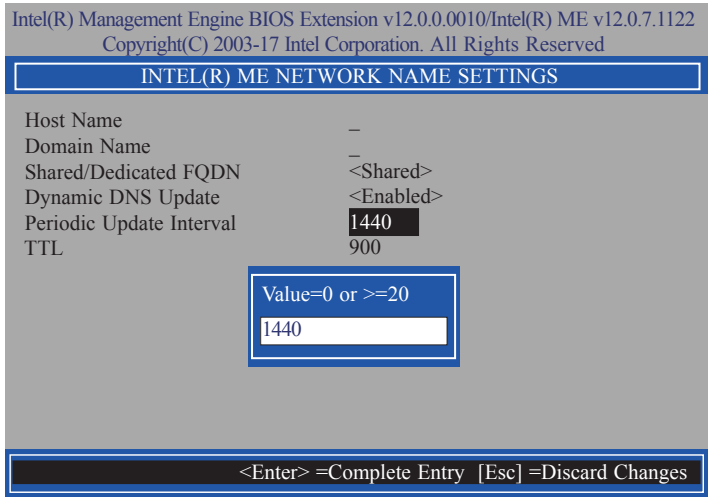

25. Select **Shared/Dedicated FQDN** then press Enter. Select **Shared** or **Dedicated** then press Enter.



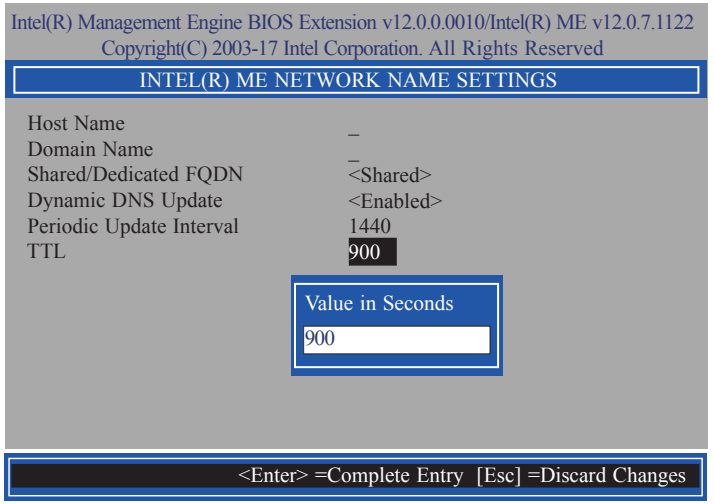
26. Select **Dynamic DNS Update** then press Enter. Select **Enabled** or **Disabled** then press Enter. If **Dynamic DNS Update** is set to **Enabled**, **Periodic Update Interval** and **TTL** fields will show up.



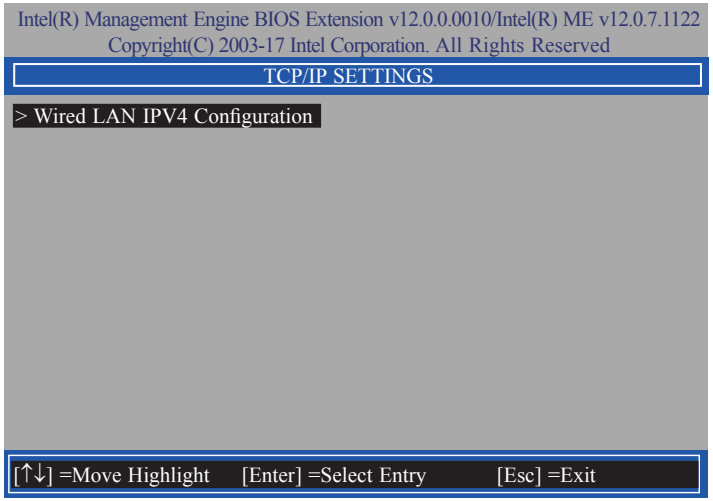

27. Select **Periodic Update Interval** then press Enter. Enter value then press Enter.



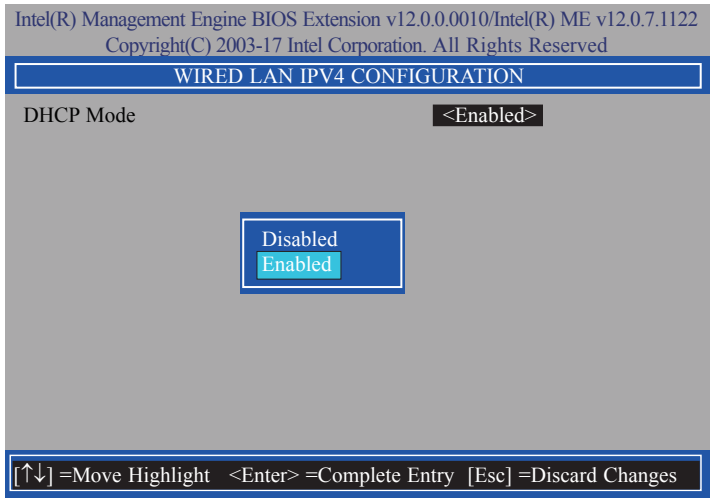

28. Select **TTL** then press Enter. Enter value then press Enter.



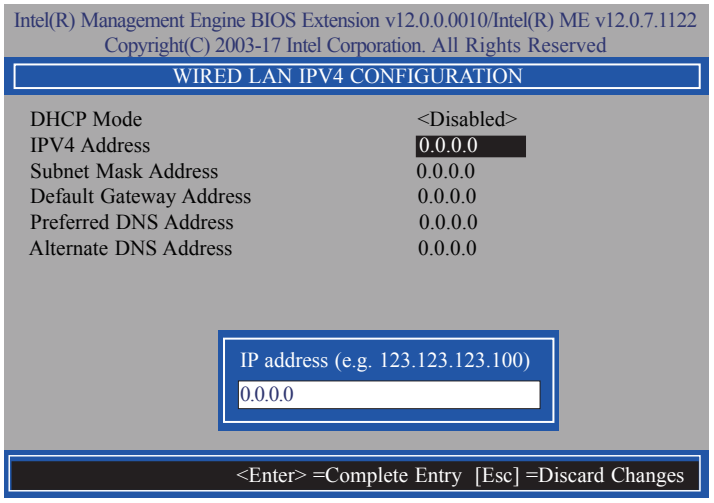

29. Press Esc until you return to the **Intel(R) ME Network Setup** menu. Select **TCP/IP Settings** then press Enter. In the **TCP/IP Settings** menu, select **Wired LAN IPV4 Configuration** then press Enter.



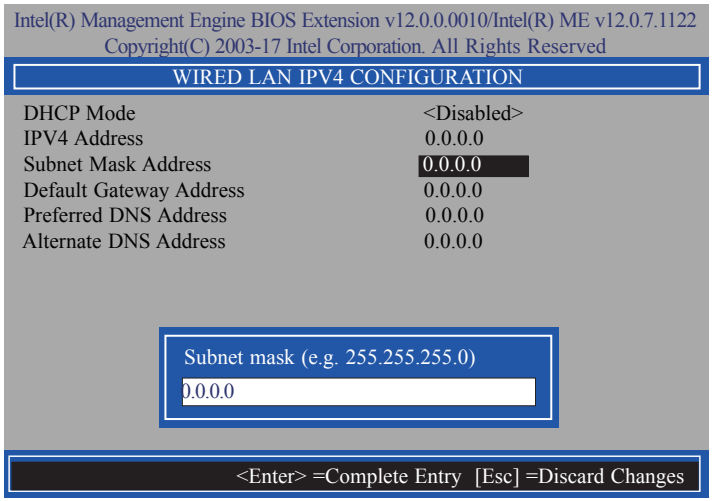
30. In the **Wired LAN IPV4 Configuration** menu, select **DHCP Mode** then press Enter. Select **Enabled** or **Disabled** then press Enter. If set to **Disabled**, **IPV4 Address**, **Subnet Mask Address**, **Default Gateway Address**, **Preferred DNS Address** and **Alternate DNS Address** will show up.



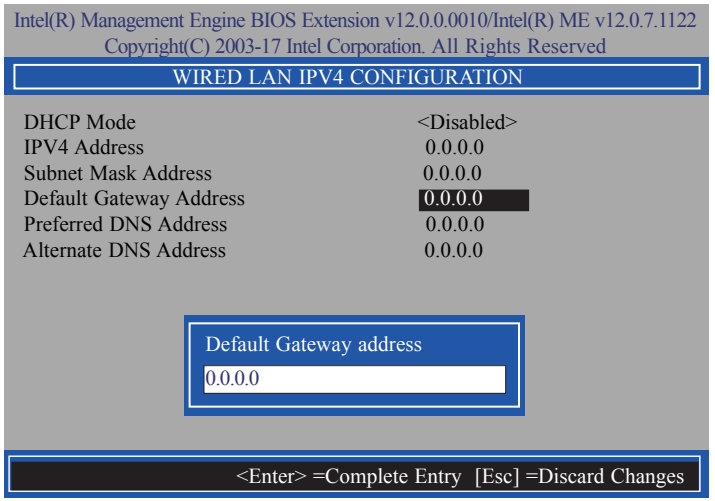

31. Select **IPV4 Address** then press Enter. Enter address then press Enter.



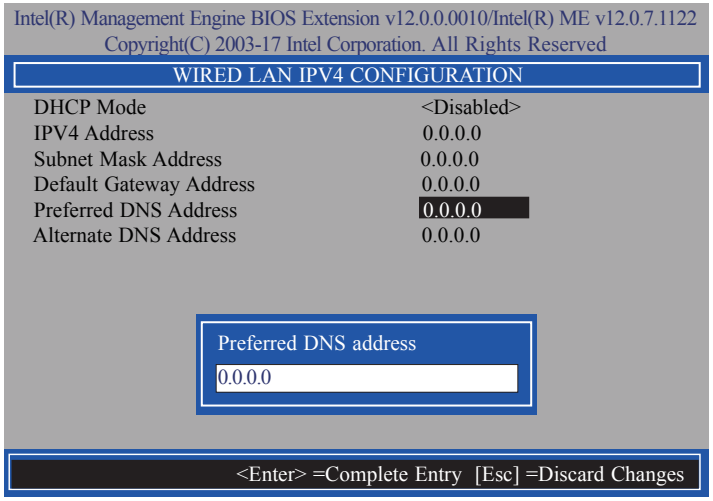

32. Select **Subnet Mask Address** then press Enter. Enter address then press Enter.



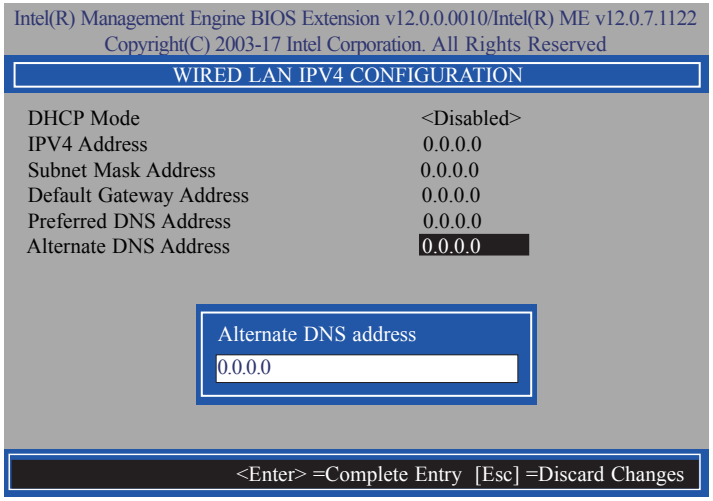

33. Select **Default Gateway Address** then press Enter. Enter address then press Enter.



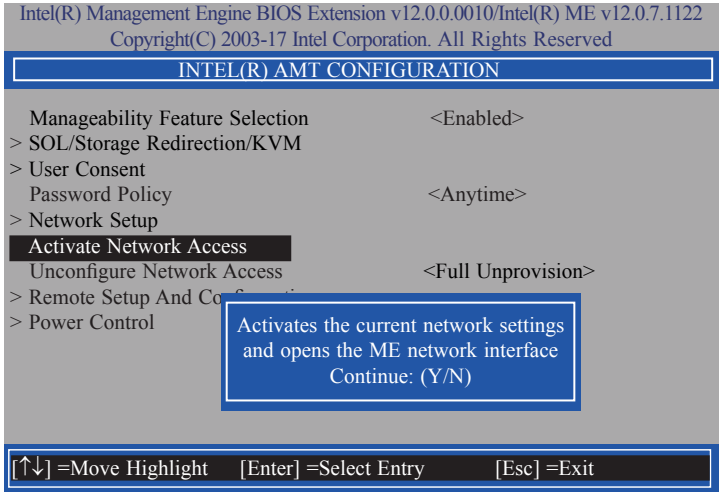
34. Select **Preferred DNS Address** then press Enter. Enter address then press Enter.



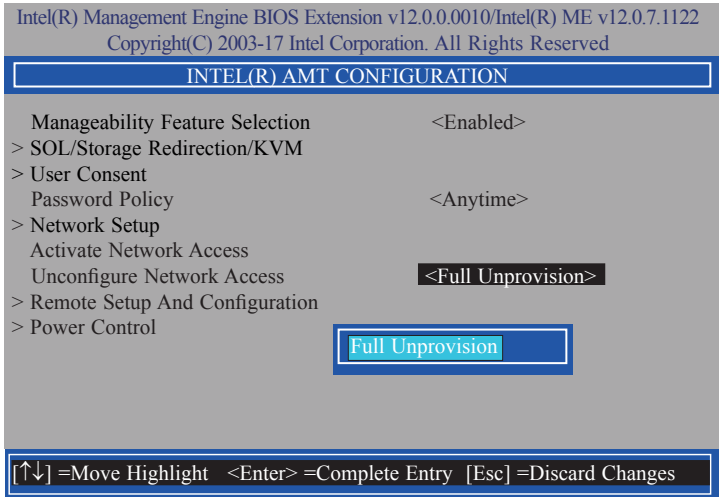

35. Select **Alternate DNS Address** then press Enter. Enter address then press Enter.



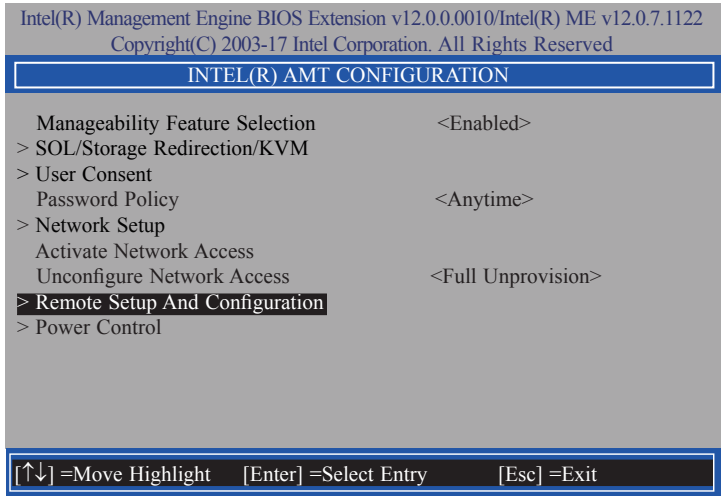

36. Press Esc until you return to the **Intel(R) AMT Configuration** menu. If you want to activate the current network settings and open the ME network inferface, select **Activate Network Access**, press Enter, then press Y.



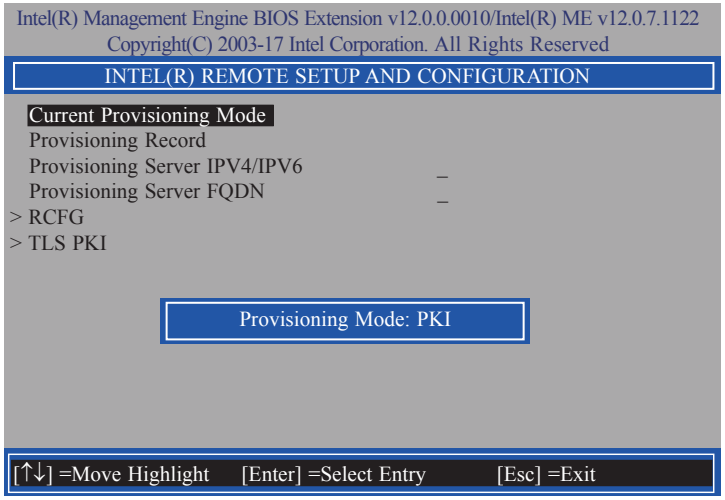

37. In the **Intel(R) AMT Configuration** menu, select **Unconfigure Network Access** then press Enter.



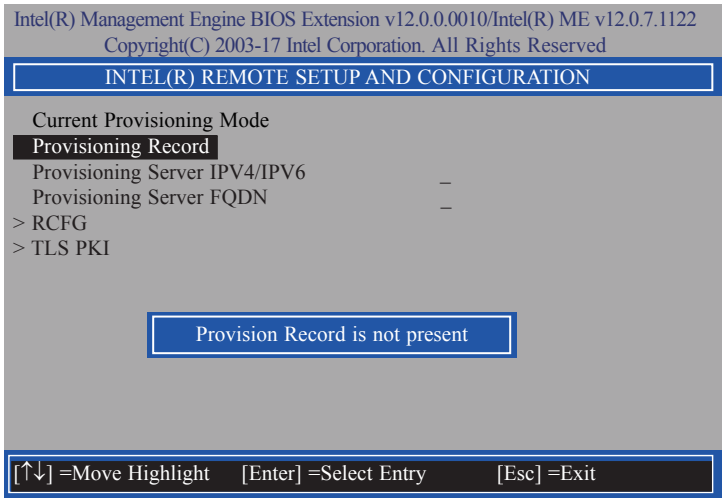
38. In the **Intel(R) AMT Configuration** menu, select **Remote Setup And Configuration** then press Enter.



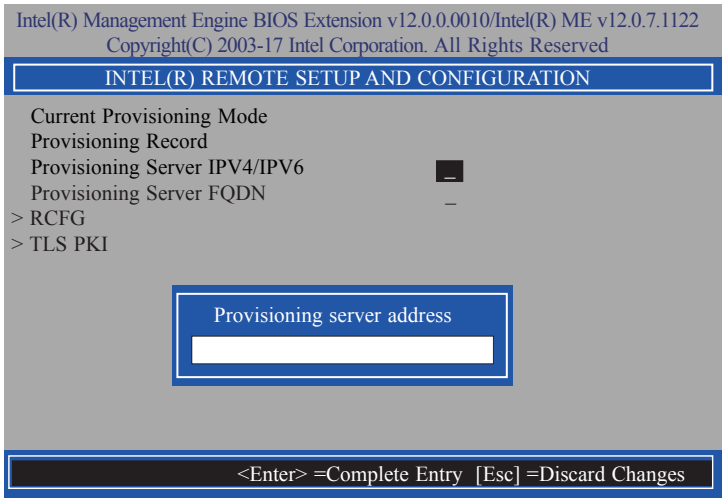

39. In the **Intel(R) Remote Setup And Configuration** menu**,** select **Current Provisioning Mode** then press Enter.



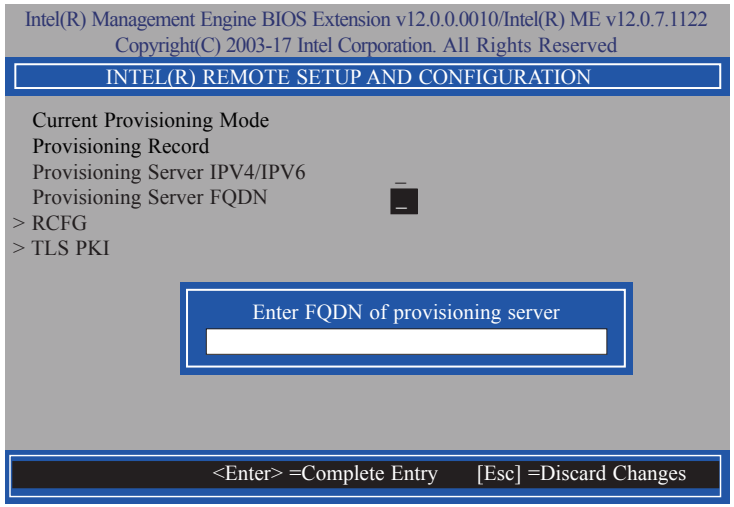

40. In the **Intel(R) Remote Setup And Configuration** menu**,** select **Provisioning Record** then press Enter.



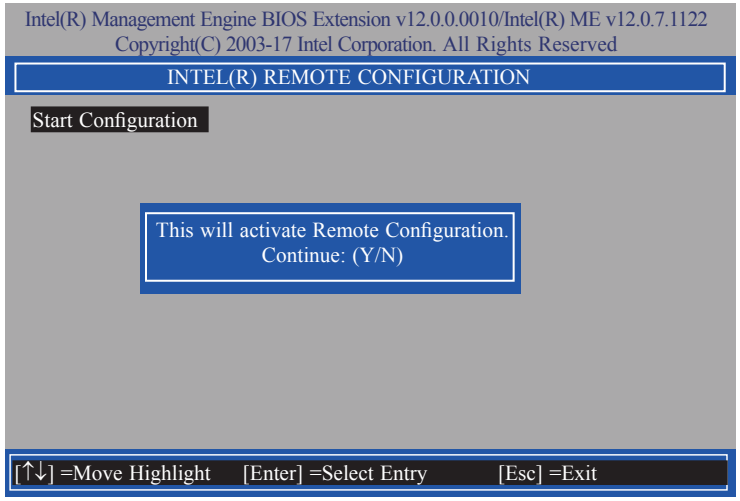

41. In the **Intel(R) Remote Setup And Configuration** menu**,** select **Provisioning Server IPV4/IPV6** then press Enter. Enter the address then press Enter.



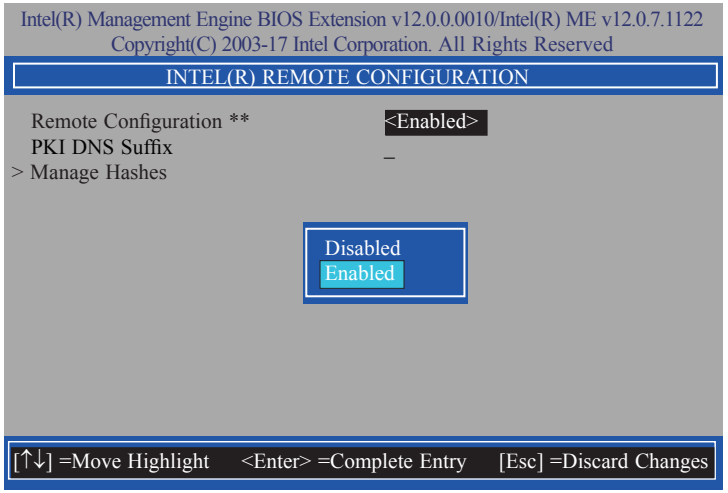
42. In the **Intel(R) Remote Setup And Configuration** menu**,** select **Provisioning Server FQDN** then press Enter. Enter the FQDN then press Enter.



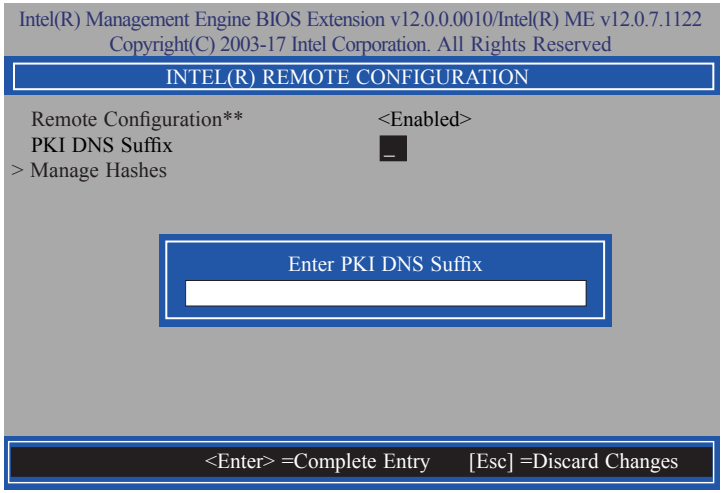

43. If you want to activate remote configuration, in the **Intel(R) Remote Setup And Configuration** menu**,** select **RCFG** then press Enter. Select **Start Configuration** then press Enter. Press Y to activate.



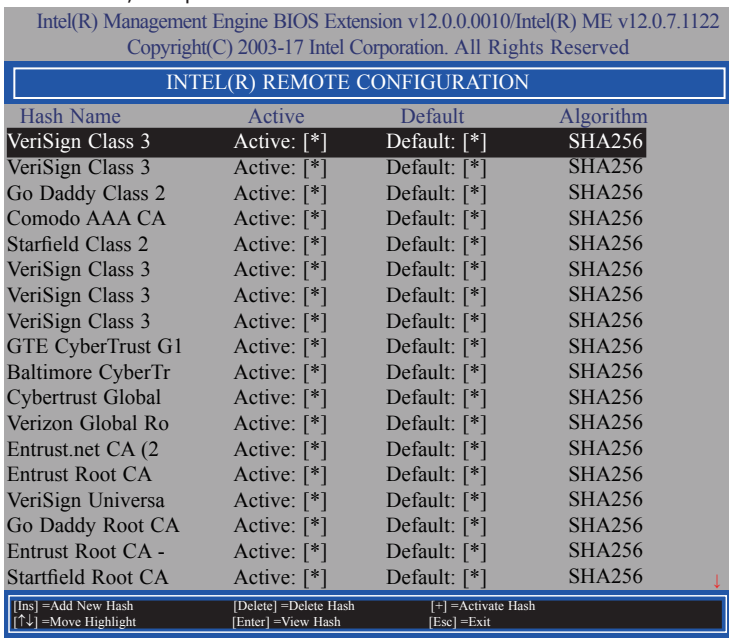

44. Press Esc until you return to the **Intel(R) Remote Setup And Configuration** menu**.** Select **TLS PKI** then press Enter. Select **Remote Configuration **** then press Enter. Select **Enabled** or **Disabled** then press Enter.



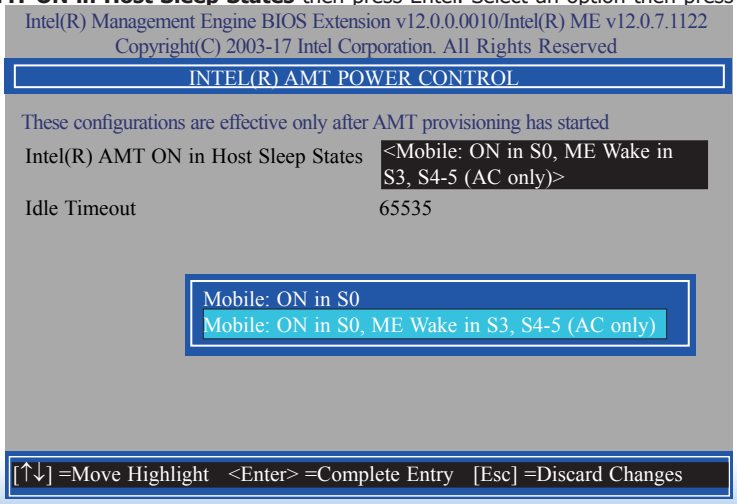

45. Select **PKI DNS Suffix** then press Enter. Enter the PKI DNS Suffix then press Enter.



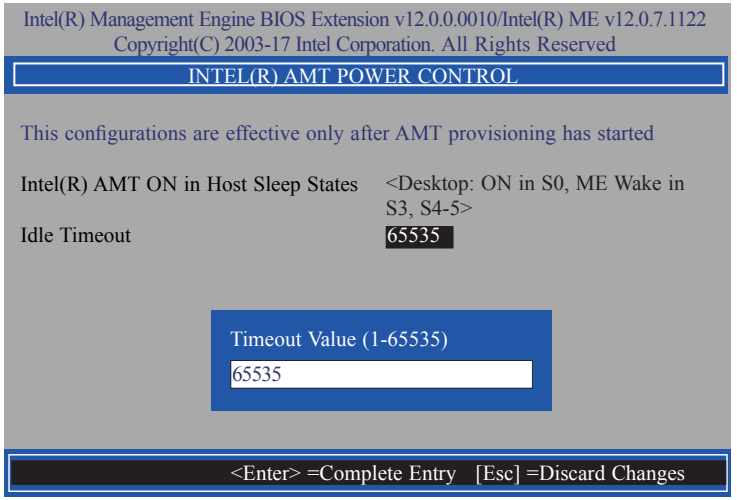
46. In the **Intel(R) Remote Configuration** menu, select **Manage Hashes** then press Enter. Select the hash name then press Insert to enter custom hash certificate name, press Delete to delete hash, press Enter to view hash information, press + to activate or deactivate hash, and press Esc to exit.

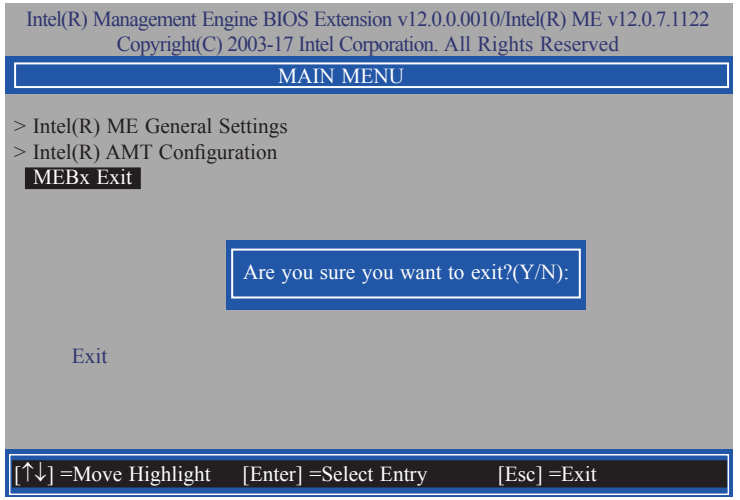



47. Press Esc until you return to the **Intel(R) AMT Configuration** menu, select **Power Control** then press Enter. In the **Intel(R) AMT Power Control** menu, select **Intel(R) AMT ON in Host Sleep States** then press Enter. Select an option then press Enter.




48. In the **Intel(R) AMT Power Control** menu, select **Idle Timeout** then press Enter. Enter the timeout value and press Enter.




49. Press Esc until you return to the **Main Menu**. Select **MEBx Exit** then press Enter. Press Y to exit.