

Approval Sheet

| | |
|------------------------------|-------------------------------------|
| Customer | |
| Product Number | M5R0-BGS2DCVP |
| Data Rate | 4800 MT/s |
| Pin | 288 pin |
| CI-tRCD-tRP | 40-39-39 |
| Operating temperature | Tc=0 to 95°C |
| Date | 23th October 2023 |

**The Total Solution For
Industrial Flash Storage**

Rev 1.0

1. Features

- 288-pin VLP Registered Dual In-Line Memory Module
- VDD=VDDQ= 1.1V (1.067V ~ 1.166V)
- VPP=1.8V (1.746V ~ 1.908V)
- VDDSPD= 1.8V
- On-die, internal, adjustable VREF generation for DQ,CA,CS
- 16n-bit prefetch
- Two independent I/O sub channels
- Programmable /CAS Latency: 22,26,28,30,32,36,40,42
- tREFI 3.9us for 0°C ≤ Tcase < 85°C, tREFI 1.95us for 85°C < Tcase ≤ 95°C
- On-Die ECC
- PMIC on DIMM, nominal supply 12V, VIN_Bulk input supply range: 4.25 V to 15 V
- Fly-by topology
- I3C/I2C support
- Terminated control and C/A bus
- SPD EEPROM Hub and Integrated Thermal Sensor
- Halogen-free

| Specification | | | | | | | |
|---------------|-----------|------------------|-------------------|--------------|----------------|------|-----|
| Density | Data Rate | IC Configuration | DIMM Organization | Number of IC | Number of rank | Side | ECC |
| 32GB | 4800 MT/s | 2Gx8 (16Gb) | 4Gx80 | 20 | 2 | 2 | Y |

| Key timing parameters | | | | |
|-----------------------|--------------|-------------|--------------|-------------|
| tCK (ns) | tRCD (ns) | tRP (ns) | tRAS (ns) | tRC (ns) |
| 0.416 | 16.00 | 16.00 | 32 | 48.00 |

| tRFC parameter by IC Configuration | | | | | |
|------------------------------------|------------------|------|------|------|------|
| Parameter | IC Configuration | | | | Unit |
| | 8Gb | 16Gb | 24Gb | 32Gb | |
| tRFC1,min | 195 | 295 | TBD | TBD | ns |
| tRFC2,min | 130 | 160 | TBD | TBD | ns |
| tRFCsb,min | 115 | 130 | TBD | TBD | ns |

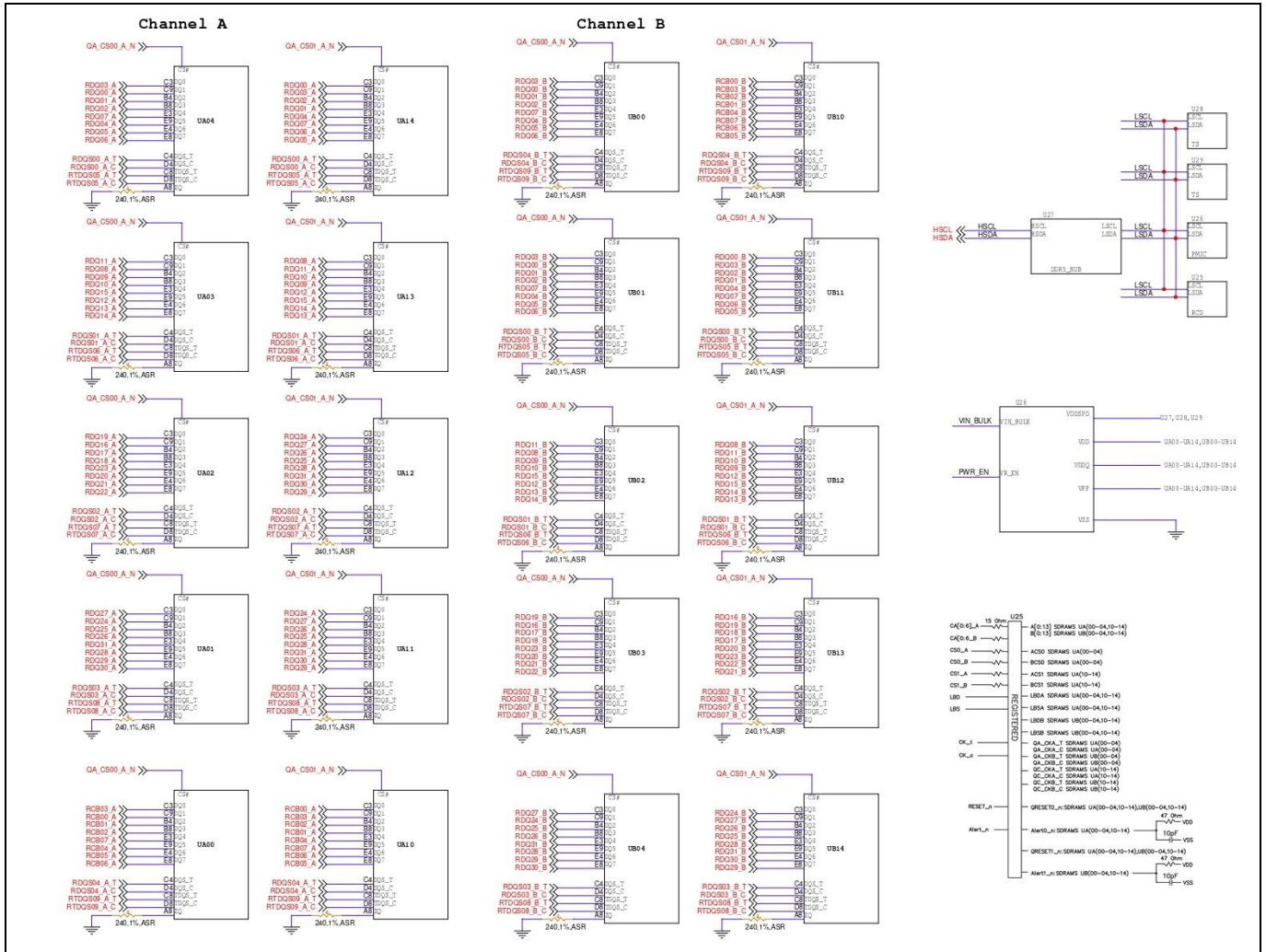
2. Pin Assignments

| 288-Pin DDR5 RDIMM Front | | | | | | | | 288-Pin DDR5 RDIMM Back | | | | | | | |
|--------------------------|----------|-----|----------|-----|-------------------------------------|-----|----------|-------------------------|---------------------------------------------------|-----|------------------------|-----|------------------------|-----|------------------------|
| Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol | Pin | Symbol |
| 1 | VIN_BULK | 37 | Vss | 73 | Vss | 109 | DQ5_B | 145 | VIN_BULK | 181 | DQ22_A | 217 | CK_t | 253 | Vss |
| 2 | RFU | 38 | DQ21_A | 74 | PAR_A | 110 | Vss | 146 | VIN_BULK | 182 | Vss | 218 | CK_c | 254 | DQ7_B |
| 3 | VIN_MGMT | 39 | Vss | 75 | Vss | 111 | DQ8_B | 147 | PWR_GOOD, D,FAL_n | 183 | DQ23_A | 219 | Vss | 255 | Vss |
| 4 | SCL | 40 | DQ24_A | 76 | CA0_B | 112 | Vss | 148 | SAA | 184 | Vss | 220 | RFU | 256 | DQ10_B |
| 5 | SDA | 41 | Vss | 77 | Vss | 113 | DQ9_B | 149 | RFU | 185 | DQ26_A | 221 | CA1_B | 257 | Vss |
| 6 | Vss | 42 | DQ25_A | 78 | CA2_B | 114 | Vss | 150 | RFU | 186 | Vss | 222 | Vss | 258 | DQ11_B |
| 7 | DQ0_A | 43 | Vss | 79 | Vss | 115 | DQS1_B_t | 151 | Vss | 187 | DQ27_A | 223 | CA3_B | 259 | Vss |
| 8 | Vss | 44 | DQS3_A_t | 80 | CA4_B | 116 | DQS1_B_c | 152 | DQ2_A | 188 | Vss | 224 | Vss | 260 | DQS6_B_c, TDQS6_B_c |
| 9 | DQ1_A | 45 | DQS3_A_c | 81 | Vss | 117 | Vss | 153 | Vss | 189 | DQS8_A_c, TDQS8_A_c | 225 | CA5_B | 261 | DQS6_B_t, TDQS6_B_t |
| 10 | Vss | 46 | Vss | 82 | CA6_B | 118 | DQ12_B | 154 | DQ3_A | 190 | DQS8_A_t, TDQS8_A_t | 226 | Vss | 262 | Vss |
| 11 | DQS0_A_t | 47 | DQ28_A | 83 | Vss | 119 | Vss | 155 | Vss | 191 | Vss | 227 | PAR_B | 263 | DQ14_B |
| 12 | DQS0_A_c | 48 | Vss | 84 | CS0_B_n | 120 | DQ13_B | 156 | DQS5_A_c, TDQS5_A_c, DQS5_A_t, TDQS5_A_t | 192 | DQ30_A | 228 | Vss | 264 | Vss |
| 13 | Vss | 49 | DQ29_A | 85 | Vss | 121 | Vss | 157 | DQS5_A_t, TDQS5_A_t | 193 | Vss | 229 | CS1_B_n | 265 | DQ15_B |
| 14 | DQ4_A | 50 | Vss | 86 | LBDRSP_A_n | 122 | DQ16_B | 158 | Vss | 194 | DQ31_A | 230 | Vss | 266 | Vss |
| 15 | Vss | 51 | CB0_A | 87 | LBDRSP_B_n | 123 | Vss | 159 | DQ6_A | 195 | Vss | 231 | RFU | 267 | DQ18_B |
| 16 | DQ5_A | 52 | Vss | 88 | Vss | 124 | DQ17_B | 160 | Vss | 196 | CB2_A | 232 | RFU | 268 | Vss |
| 17 | Vss | 53 | CB1_A | 89 | CB4_B | 125 | Vss | 161 | DQ7_A | 197 | Vss | 233 | Vss | 269 | DQ19_B |
| 18 | DQ8_A | 54 | Vss | 90 | Vss | 126 | DQS2_B_t | 162 | Vss | 198 | CB3_A | 234 | CB6_B | 270 | Vss |
| 19 | Vss | 55 | DQS4_A_t | 91 | CB5_B | 127 | DQS2_B_c | 163 | DQ10_A | 199 | Vss | 235 | Vss | 271 | DQS7_B_c, TDQS7_B_c |
| 20 | DQ9_A | 56 | DQS4_A_c | 92 | Vss | 128 | Vss | 164 | Vss | 200 | DQS9_A_c, TDQS9_A_c | 236 | CB7_B | 272 | DQS7_B_t, TDQS7_B_t |
| 21 | Vss | 57 | Vss | 93 | DQS9_B_t, TDQS9_B_t, DBI4_B_n | 129 | DQ20_B | 165 | DQ11_A | 201 | DQS9_A_t, TDQS9_A_t | 237 | Vss | 273 | Vss |
| 22 | DQS1_A_t | 58 | CB4_A | 94 | DQS9_B_c, TDQS9_B_c | 130 | Vss | 166 | Vss | 202 | Vss | 238 | DQS4_B_c | 274 | DQ22_B |
| 23 | DQS1_A_c | 59 | Vss | 95 | Vss | 131 | DQ21_B | 167 | DQS6_A_c, TDQS6_A_c, DQS6_A_t, TDQS6_A_t | 203 | CB6_A | 239 | DQS4_B_t | 275 | Vss |
| 24 | Vss | 60 | CB5_A | 96 | CB0_B | 132 | Vss | 168 | DQS6_A_t, TDQS6_A_t | 204 | Vss | 240 | Vss | 276 | DQ23_B |
| 25 | DQ12_A | 61 | Vss | 97 | Vss | 133 | DQ24_B | 169 | Vss | 205 | CB7_A | 241 | CB2_B | 277 | Vss |
| 26 | Vss | 62 | ALERT_n | 98 | CB1_B | 134 | Vss | 170 | DQ14_A | 206 | Vss | 242 | Vss | 278 | DQ26_B |
| 27 | DQ13_A | 63 | Vss | 99 | Vss | 135 | DQ25_B | 171 | Vss | 207 | RESET_n | 243 | CB3_B | 279 | Vss |
| 28 | Vss | 64 | CS0_A_n | 100 | DQ0_B | 136 | Vss | 172 | DQ15_A | 208 | Vss | 244 | Vss | 280 | DQ27_B |
| 29 | DQ16_A | 65 | Vss | 101 | Vss | 137 | DQS3_B_t | 173 | Vss | 209 | CS1_A_n | 245 | DQ2_B | 281 | Vss |
| 30 | Vss | 66 | CA0_A | 102 | DQ1_B | 138 | DQS3_B_c | 174 | DQ18_A | 210 | Vss | 246 | Vss | 282 | DQS8_B_c, TDQS8_B_c |
| 31 | DQ17_A | 67 | Vss | 103 | Vss | 139 | Vss | 175 | Vss | 211 | CA1_A | 247 | DQ3_B | 283 | DQS8_B_t, TDQS8_B_t |
| 32 | Vss | 68 | CA2_A | 104 | DQS0_B_t | 140 | DQ28_B | 176 | DQ19_A | 212 | Vss | 248 | Vss | 284 | Vss |
| 33 | DQS2_A_t | 69 | Vss | 105 | DQS0_B_c | 141 | Vss | 177 | Vss | 213 | CA3_A | 249 | DQS5_B_c, TDQS5_B_c | 285 | DQ30_B |
| 34 | DQS2_A_c | 70 | CA4_A | 106 | Vss | 142 | DQ29_B | 178 | DQS7_A_c, TDQS7_A_c | 214 | Vss | 250 | DQS5_B_t, TDQS5_B_t | 286 | Vss |
| 35 | Vss | 71 | Vss | 107 | DQ4_B | 143 | Vss | 179 | DQS7_A_t, TDQS7_A_t | 215 | CA5_A | 251 | Vss | 287 | DQ31_B |
| 36 | DQ20_A | 72 | CA6_A | 108 | Vss | 144 | RFU | 180 | Vss | 216 | Vss | 252 | DQ6_B | 288 | Vss |

3. Pin Descriptions

| Symbol | Type | I/O Level | Description | Symbol | Type | I/O Level | Description |
|----------------------------|------------------|-----------|----------------------------------|--------------------------------|------------------|-----------|-----------------------------|
| CK_t, CK_c | Input | VDDQ | Clock | DQ[31:0]_A DQ[31:0]_B | Input/ Output | VDDQ | Data Input/Output |
| CA[6:0]_A CA[6:0]_B | Input | VDDQ | Command/Address Inputs | CB[7:0]_A CB[7:0]_B | Input/ Output | VDDQ | ECC Check Bits Input/Output |
| CS[1:0]_A CS[1:0]_B | Input | VDDQ | Chip Select | DQS[9:0]_A_t DQS[9:0]_B_t | Input/ Output | VDDQ | Data Strobe |
| PAR_A PAR_B | Input | VDDQ | Command and Address Parity Input | DQS[9:0]_A_c DQS[9:0]_B_c | Input/ Output | VDDQ | Data Strobe |
| ALERT_n | Output | VDDQ | Alert | TDQS[9:0]_A_t TDQS[9:0]_B_t | Input/ Output | VDDQ | Termination Data Strobe |
| RESET_n | CMOS Input | VDDQ | Active Low Asynchronous Reset | TDQS[9:0]_A_c TDQS[9:0]_B_c | Input/ Output | VDDQ | Termination Data Strobe |
| PWR_GOOD/FAI L_n | Input/ Output | VDDQ | Power Good Indicator | VIN_BULK | Supply | | External Power Supply |
| DM[3:0]_A_n DM[3:0]_B_n | Input | VDDQ | Input Data Mask | VIN_MGMT | Supply | | External Power Supply |
| HSCL | Input | VOUT | Host Sideband Bus Clock | LBD RSP_A_n | Output | VDDQ | Loopback data output |
| HSDA | Input/Output | VOUT | Host Sideband Bus Data | LBS | Output | VDDQ | Loopback data strobe output |
| HSA | Input | GND | Host Sideband Bus Device ID | VSS | Supply | | Ground |
| RFU | | | Reserved for future use | | | | |

4. Function Block Diagram



5. Thermal Characteristics

| Symbol | Parameter | | Rating | Units | Note |
|------------------|-----------------------|------------------------|------------|-------|---------|
| T _c | Operation Temperature | Normal Operating Temp. | 0 to 85 | °C | 1,2,3 |
| | | Extended Temp. | 85 to 95 | °C | 1,2,3,4 |
| T _{STG} | Storage Temperature | | -55 to 100 | °C | 5 |

Note:

1. Maximum operating case temperature; T_c is measured in the center of the package.
2. A thermal solution must be designed to ensure the DRAM device does not exceed the maximum T_c during operation.
3. Device functionality is not guaranteed if the DRAM device exceeds the maximum T_c during operation.
4. If T_c exceeds 85°C, the DRAM must be refreshed externally at 2X refresh, which is a 1.95μs interval refresh rate.
5. Storage temperature is defined as the temperature of the top/center of the DRAM and does not reflect the storage temperatures of shipping trays.

6. IDD, IDDQ and IPP Specifications

| Symbol | Description | Value | | Units |
|--------|--------------------------------------------------|----------|----------|-------|
| | | IDD Max. | IPP Max. | |
| IDD0 | Operating One Bank Active-Precharge Current | 830 | 110 | mA |
| IDD0F | Operating Four Bank Active-Precharge Current | 1300 | 170 | mA |
| IDD2N | Precharge Standby Current | 600 | 80 | mA |
| IDD2P | Precharge Power-Down Current | 460 | 80 | mA |
| IDD3N | Active Standby Current | 920 | 100 | mA |
| IDD3P | Active Power-Down Current | 600 | 100 | mA |
| IDD4R | Operating Burst Read Current | 2200 | 120 | mA |
| IDD4W | Operating Burst Write Current | 2600 | 120 | mA |
| IDD5B | Burst Refresh Current (Normal Refresh Mode) | 2600 | 600 | mA |
| IDD5C | Burst Refresh Current (Same Bank Refresh Mode) | 1250 | 290 | mA |
| IDD6N | Self Refresh Current: Normal Temperature Range | 1240 | 240 | mA |
| IDD6E | Self Refresh Current: Extended Temperature Range | 1600 | 320 | mA |
| IDD7 | Operating Bank Interleave Read Current | 3500 | 340 | mA |
| IDD8 | Maximum Power Saving Deep Power Down Current | 320 | 80 | mA |

The above information may be change due to the update of the device specifications and is for reference only.

7. Timing Parameters

| Parameter | Symbol | 4400 | | 4800 | | 5200 | | Unit |
|-----------------------------------------------------------------------------------------|------------|-------------------------|--------|-------------------------|--------|-------------------------|--------|------|
| | | Min | Max | Min | Max | Min | Max | |
| Clock Timing | | | | | | | | |
| Average clock period | tCK,AVG | 0.454 | <0.500 | 0.416 | <0.454 | 0.384 | <0.416 | ns |
| Command and Address Timing | | | | | | | | |
| Read to Read command delay for same bank group | tCCD_L | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | nCK |
| WRITE to WRITE command delay for same bank group | tCCD_L_WR | 32nCK, 20ns (MAX) | | 32nCK, 20ns (MAX) | | 32nCK, 20ns (MAX) | | nCK |
| WRITE to WRITE command delay for same bank group, second WRITE not RMW | tCCD_L_WR2 | 16nCK, 10ns (MAX) | | 16nCK, 10ns (MAX) | | 16nCK, 10ns (MAX) | | nCK |
| Read to Read or Write to Write command delay for different bank group for BL16, BC8 OTF | tCCD_S | 8 | | 8 | | 8 | | nCK |
| ACTIVATE to ACTIVATE command delay to different bank group for 2KB page size | tRRD_S,2K | 8 | | 8 | | 8 | | nCK |
| ACTIVATE to ACTIVATE command delay to different bank group for 1KB page size | tRRD_S,1K | 8 | | 8 | | 8 | | nCK |
| ACTIVATE to ACTIVATE command delay to same bank group for 2KB page size | tRRD_L,2K | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | nCK |
| ACTIVATE to ACTIVATE command delay to same bank group for 1KB page size | tRRD_L,1K | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | 8nCK,5ns (MAX) | | nCK |
| Four activate window for | tFAW,2K | 40nCK, | | 40nCK, | | 40nCK, | | ns |

| | | | | | | | | |
|-----------------------------------------------------------------------------------------------------------------------|---------|-----------------------------|--|-----------------------------|--|-----------------------------|--|-----|
| 2KB page size | | 18.160ns (MAX) | | 16.640ns (MAX) | | 15.360ns (MAX) | | |
| Four activate window for 1KB page size | tFAW,1K | 32nCK, 14.528ns (MAX) | | 32nCK, 13.312ns (MAX) | | 32nCK, 12.288ns (MAX) | | ns |
| Delay from start of internal WRITE transaction to internal READ command for different bank group | tWTR_S | 4nCK, 2.5ns (MAX) | | 4nCK, 2.5ns (MAX) | | 4nCK, 2.5ns (MAX) | | ns |
| Delay from start of internal WRITE transaction to internal READ command for same bank group | tWTR_L | 16nCK, 10ns (MAX) | | 16nCK, 10ns (MAX) | | 16nCK, 10ns (MAX) | | ns |
| Delay from start of internal WRITE transaction to internal READ with AUTO PRECHARGE command for same bank | tWTRA | tWR-tRTP | | tWR-tRTP | | tWR-tRTP | | ns |
| Internal READ command to PRECHARGE command delay | tRTP | 12nCK, 7.5ns (MAX) | | 12nCK, 7.5ns (MAX) | | 12nCK, 7.5ns (MAX) | | ns |
| PRECHARGE to PRECHARGE delay | tPPD | 2 | | 2 | | 2 | | nCK |
| WRITE recovery time | tWR | 29.964 | | 29.952 | | 29.952 | | ns |
| DLL locking time | tDLLK | 1280 | | 1536 | | 1536 | | nCK |
| Mode Register Read/Write Timing | | | | | | | | |
| Mode register READ command period | tMRR | 14ns, 16nCK (MAX) | | 14ns, 16nCK (MAX) | | 14ns, 16nCK (MAX) | | |
| Mode register READ pattern to mode register READ pattern command spacing | tMRR_p | 8 | | 8 | | 8 | | nCK |
| Mode register WRITE command period | tMRW | 5ns,8nCK (MAX) | | 5ns,8nCK (MAX) | | 5ns,8nCK (MAX) | | |
| Mode register SET command delay | tMRD | 14ns, 16nCK | | 14ns, 16nCK | | 14ns, 16nCK | | |

| | | | | | | | | |
|-----------------------------------------------------------------------------------------------------------------------------|-------------------|-----------------------|------------------|-------------------|------------------|-------------------|------------------|-----|
| | | (MAX) | | (MAX) | | (MAX) | | |
| DFE mode register WRITE update delay time | tDFE | 80 | | 80 | | 80 | | ns |
| Data Strobe Timing | | | | | | | | |
| DQS_t, DQS_c differential READ preamble | tRPRE | TBD | | TBD | | TBD | | tCK |
| DQS_t, DQS_c differential READ postamble | tRPST | TBD | | TBD | | TBD | | tCK |
| DQS_t, DQS_c rising edge output timing location from rising CK_t, CK_c | tDQSCK | -0.286 | 0.286 | -0.3 | 0.3 | TBD | TBD | tCK |
| DQS_t, DQS_c rising edge output variance window | tDQSKI | | 0.475 | | 0.49 | | TBD | tCK |
| Data Strobe Timing | | | | | | | | |
| 2-tCK WRITE preamble enable window | tWPRE_EN_2 tCK | 1.5 | | 1.5 | | 1.5 | | tCK |
| 3-tCK WRITE preamble enable window | tWPRE_EN_3 tCK | 2.5 | | 2.5 | | 2.5 | | tCK |
| 4-tCK WRITE preamble enable window | tWPRE_EN_4 tCK | 2.5 | | 2.5 | | 2.5 | | tCK |
| DQS_t, DQS_c differential WRITE postamble | tWPST | TBD | | TBD | | TBD | | tCK |
| Final trained value of host DQS_t-DQS_c timing relative to CWL CK_t-CK_c edge | tDQSoffset | -0.5 | 0.5 | -0.5 | 0.5 | -0.5 | 0.5 | tCK |
| Write leveling setup time | tWLS | -80 | 80 | -80 | 80 | -80 | 80 | ps |
| Write leveling hold time | tWLH | -80 | 80 | -80 | 80 | -80 | 80 | ps |
| Voltage/temperature drift window of first rising DQS_t preamble edge relative to CWL CK_t-CK_c edge (x4/x8/x16) | tDQSD | -0.25 x N_ntCK | 0.25 x N_ntCK | -0.25 x N_ntCK | 0.25 x N_ntCK | -0.25 x N_ntCK | 0.25 x N_ntCK | tCK |
| Host and system voltage/ temperature drift window of first rising DQS_t preamble edge relative to | tDQSS | -0.25 x tWPRE_EN_ntCK | | | | | | tCK |

| | | | | | | | | |
|--------------------------------------------------------------------|------------------|-------------------------|------|-------------------------|------|-------------------------|------|-----|
| CWL CK_t-CK_c edge (x4/x8/x16) | | | | | | | | |
| MPSM Timing | | | | | | | | |
| MPSM exit to first valid command delay | tMPSMX | tMRD | | tMRD | | tMRD | | ns |
| ZQ Calibration Timing | | | | | | | | |
| ZQ calibration time | tZQCAL | 1 | | 1 | | 1 | | µs |
| ZQ calibration latch time | tZQLAT | 30ns, 8nCK (MIN) | | 30ns, 8nCK (MIN) | | 30ns, 8nCK (MIN) | | |
| Reset Timing | | | | | | | | |
| RESET_n low time for reset initialization with stable power | tPW_RESET | 1 | | 1 | | 1 | | µs |
| Time after RESET_n assertion to ODT off | tRST_ADC | | 50 | | 50 | | 50 | ns |
| Self Refresh Timing | | | | | | | | |
| Command pass disable delay | tCPDED | 5ns,8nCK (MAX) | | 5ns,8nCK (MAX) | | 5ns,8nCK (MAX) | | |
| Self refresh CS_n low pulse width | tCSL | 10 | | 10 | | 10 | | ns |
| Self refresh exit CS_n high pulse width | tCSH_Srexit | 13 | 30 | 13 | 30 | 13 | 30 | ns |
| Self refresh exit CS_n low pulse width | tCSL_Srexit | 3nCK | 30ns | 3nCK | 30ns | 3nCK | 30ns | |
| Self refresh exit CS_n low pulse width with frequency change | tCSL_FreqCh g | VREFOCA_ time | | VREFOCA_ time | | VREFOCA_ time | | ns |
| Valid clock requirement before SRX | tCKSRX | 3.5ns, 8nCK (MAX) | | 3.5ns, 8nCK (MAX) | | 3.5ns, 8nCK (MAX) | | ns |
| Valid clock requirement after SRE | tCKLCS | tCPDED + 1nCK | | tCPDED + 1nCK | | tCPDED + 1nCK | | nCK |
| Self refresh exit CS_n HIGH | tCASRX | 0 | | 0 | | 0 | | ns |
| Exit self refresh to commands not requiring a | tXS | tRFC1 | | tRFC1 | | tRFC1 | | ns |

| | | | | | | | | |
|---------------------------------------------------------------------|----------|-----------------------------------------|-------------------------------------|-----------------------------------------|-------------------------------------|-----------------------------------------|-------------------------------------|-----|
| locked DLL | | | | | | | | |
| Exit self refresh to commands requiring a locked DLL | tXS_DLL | tDLLK | | tDLLK | | tDLLK | | ns |
| Power-Down Timing | | | | | | | | |
| Command pass disable delay | tCPDED | 5ns,8nCK (MAX) | | 5ns,8nCK (MAX) | | 5ns,8nCK (MAX) | | ns |
| Power-down time | tPD | 7.5ns, 8nCK (MAX) | 5*tREFI1 (normal) 9*tREFI2 (FGR) | 7.5ns, 8nCK (MAX) | 5*tREFI1 (normal) 9*tREFI2 (FGR) | 7.5ns, 8nCK (MAX) | 5*tREFI1 (normal) 9*tREFI2 (FGR) | ns |
| Exit power-down to next valid command | tXP | 7.5ns, 8nCK (MAX) | | 7.5ns, 8nCK (MAX) | | 7.5ns, 8nCK (MAX) | | ns |
| Timing of ACT command to POWER DOWN ENTRY command | tACTPDEN | 2 | | 2 | | 2 | | nCK |
| Timing of PREab, PREsb or PREpb command to POWER DOWN ENTRY command | tPRPDEN | 2 | | 2 | | 2 | | nCK |
| Timing of READ or READ w/ AP command to POWER DOWN ENTRY command | tRDPDEN | CL +RBL/2+1 | | CL +RBL/2+1 | | CL +RBL/2+1 | | nCK |
| Timing of WRITE command to POWER DOWN ENTRY command | tWRPDEN | CWL +WBL/ 2+ (tWR/ tCK(avg)) +1 | | CWL +WBL/ 2+ (tWR/ tCK(avg)) +1 | | CWL +WBL/ 2+ (tWR/ tCK(avg)) +1 | | nCK |
| Timing of WRITE w/ AP command to POWER DOWN ENTRY command | tWRAPDEN | CWL +WBL/ 2+-0.25 x tWPRES_EN_n tCKWR+1 | | CWL +WBL/ 2+-0.25 x tWPRES_EN_n tCKWR+1 | | CWL +WBL/ 2+-0.25 x tWPRES_EN_n tCKWR+1 | | nCK |
| Timing of REFab or REFSb command to POWER DOWN ENTRY command | tREFPDEN | 2 | | 2 | | 2 | | nCK |
| Timing of MRR command | tMRPDEN | CL+8+1 | | CL+8+1 | | CL+8+1 | | nCK |

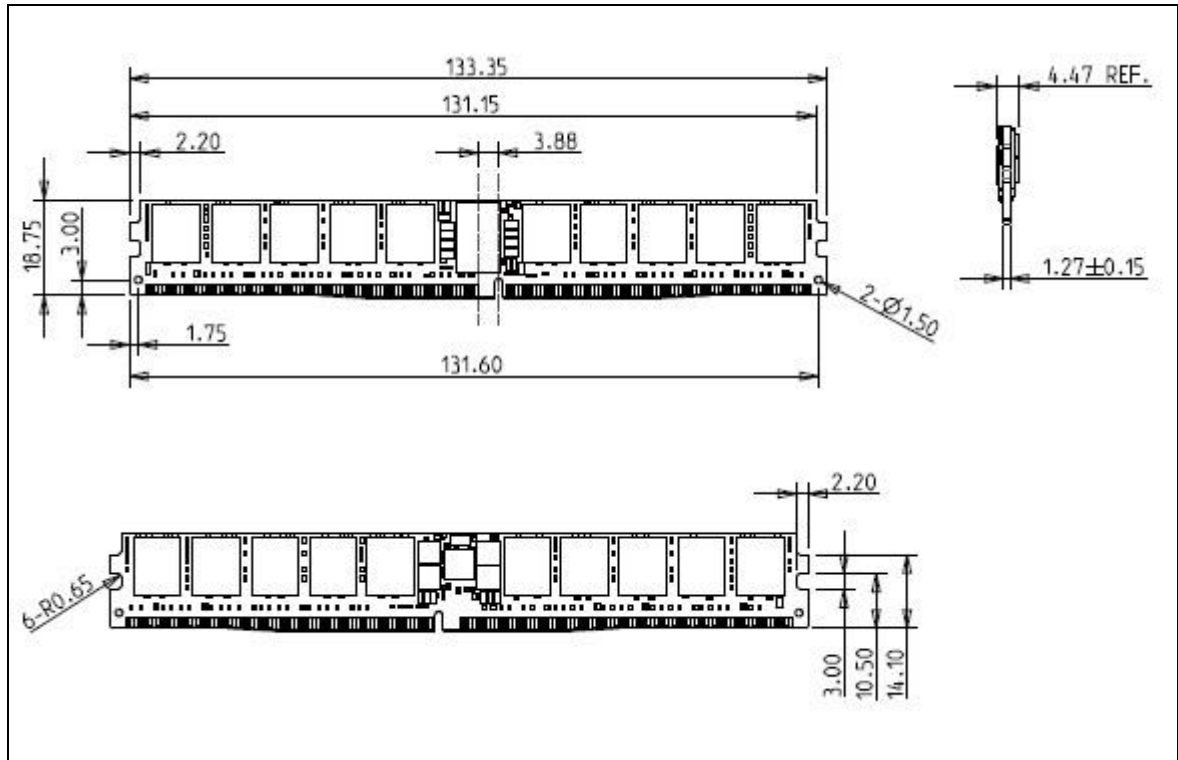
| | | | | | | | | |
|----------------------------------------------------------------------------------|----------------------|-------------------------------------------------|-----------------|-------------------------------------------------|----|-----------------|-----------------|-----|
| to POWER DOWN ENTRY command | | | | | | | | |
| Timing of MRW command to POWER DOWN ENTRY command | tMRWPDEN | tMRD (MIN) | | tMRD (MIN) | | tMRD (MIN) | | nCK |
| Timing of MPC command to POWER DOWN ENTRY command | tMPCPDEN | tMPC_delay | | tMPC_delay | | tMPC_delay | | nCK |
| MPC Command Timing | | | | | | | | |
| MPC to any other valid command | tMPC_Delay | tMRD | | tMRD | | tMRD | | nCK |
| Time between stable MPC command and first falling CS edge (setup) | tMC_MPC_Se tup | 3 | | 3 | | 3 | | nCK |
| Time between first rising CS edge and stable MPC command (HOLD) | tMC_MPC_H old | 3 | | 3 | | 3 | | nCK |
| Time CS_n is held LOW to register MPC command | tMPC_CS | 3.5 | 8 | 3.5 | 8 | 3.5 | 8 | nCK |
| PDA Timing | | | | | | | | |
| PDA ENUMERATE ID command to any other command cycle | tPDA_DELAY | tPDA_DQ S_DELAY (MAX) + BL/2 + 19ns | | tPDA_DQ S_DELAY (MAX) + BL/2 + 19ns | | TBD | | ns |
| Delay to rising strobe edge used for sampling DQ during PDA operation | tPDA_DQS_D ELAY | 5 | 18 | 5 | 18 | TBD | TBD | ns |
| DQS setup time during PDA operation | tPDA_S | 3 | | 3 | | TBD | | nCK |
| DQS hold time during PDA operation | tPDA_H | 3 | | 3 | | TBD | | nCK |
| Read Training Timing | | | | | | | | |
| Registration of MRW continuous burst mode exit to next valid command delay | tCont_Exit_ Delay | | tCont_Exit + | tCont_Exit + | | tCont_Exit + | tCont_Exit + | ns |
| Registration of MRW continuous | tCont_Exit | | CL+BL/ | | | CL+BL/ | | ns |

| | | | | | | | | |
|---------------------------------------------------------------------------------------------------------------------------|---------------------------|----|-------------------------|----|-------------------------|----|-------------------------|-----|
| burst mode exit to end of training mode | | | 2+10nCK | | 2+10nCK | | 2+10nCK | |
| Read Preamble Timing | | | | | | | | |
| Delay from MRW command to DQS driven | tSDOn | | 12nCK, 20ns (MAX) | | 12nCK, 20ns (MAX) | | 12nCK, 20ns (MAX) | |
| Delay from MRW command to DQS disabled | tSDOff | | 12nCK, 20ns (MAX) | | 12nCK, 20ns (MAX) | | 12nCK, 20ns (MAX) | |
| CA Training Mode Timing | | | | | | | | |
| Registration of CATM entry command to start of training samples time | tCATM_Entry | 20 | | 20 | | 20 | | ns |
| Registration of CATM exit CS_n assertion to end of training mode (when DQ is no longer driven by the device). | tCATM_Exit | | 14 | | 14 | | 14 | ns |
| Registration of CATM exit to next valid command delay | tCATM_Exit_ Delay | 20 | | 20 | | 20 | | ns |
| Time from sample evaluation to output on DQ bus | tCATM_Valid | | 20 | | 20 | | 20 | ns |
| Time output is available on DQ bus | tCATM_DQ_ Window | 2 | | 2 | | 2 | | nCK |
| CS_n assertion duration to exit CATM | tCATM_CS_E xit | 2 | 8 | 2 | 8 | 2 | 8 | nCK |
| Registration of CSTM entry command to start of training samples time | tCSTM_Entry | 20 | | 20 | | 20 | | ns |
| Min time between last CS_n pulse and first pulse of MPC command to exit CSTM | tCSTM_Min_ to_MPC_exit | 4 | | 4 | | 4 | | nCK |
| Registration of CSTM exit command to end of training mode | tCSTM_Exit | | 20 | | 20 | | 20 | ns |
| Time from sample evaluation | tCSTM_Valid | | 20 | | 20 | | 20 | ns |

| | | | | | | | | |
|--------------------------------------------------------------------------------------------------------------------------------------|--------------------------------|----------------------|-----|----------------------|-----|----------------------|-----|-----|
| to output on DQ bus | | | | | | | | |
| Time output is available on DQ bus | tCSTM_DQ_ Window | 2 | | 2 | | 2 | | nCK |
| Registration of CSTM exit to next valid command delay | tCSTM_Exit_ Delay | 20 | | 20 | | 20 | | ns |
| Write Leveling Timing | | | | | | | | |
| Write leveling pulse enable: time from write leveling training enable MRW to when internal write leveling pulse logic level is valid | tWLPEN | 0 | 15 | 0 | 15 | 0 | 15 | ns |
| Write leveling output delay | tWLO | 0 | 9.5 | 0 | 9.5 | 0 | 9.5 | ns |
| Write leveling output error | tWLOE | 0 | 2 | 0 | 2 | 0 | 2 | ns |
| Width of write leveling internal pulse | tWL_Pulse_ Width | 2 | | 2 | | 2 | | tCK |
| VREFC/VREFCs Timing | | | | | | | | |
| VREFC/VREFCs command to any other valid command delay | tVREFC_Delay/ tVREFCs_Delay | tMRD | | tMRD | | tMRD | | nCK |
| Time CS_n is held LOW to register VREFC/VREFCs command | tVREFC_CS/ tVREFCs_CS | 3.5 | 8 | 3.5 | 8 | 3.5 | 8 | nCK |
| hPPR/sPPR Timing | | | | | | | | |
| hPPR programming time (x4/x8) | tPGMa | 1000 | | 1000 | | 1000 | | ms |
| hPPR programming time (x16) | tPGMb | 2000 | | 2000 | | 2000 | | ms |
| sPPR programming time | tPGM_sPPR | CWL +8tCK +tWR | | CWL +8tCK +tWR | | CWL +8tCK +tWR | | tCK |
| hPPR/sPPR recognition time | tPGM_Exit | tRP | | tRP | | tRP | | ns |
| hPPR program exit and new address setting time | tPGMPST | 50 | | 50 | | 50 | | μs |
| sPPR program exit and new address setting time | tPGMPST_sP PR | tMRD | | tMRD | | tMRD | | ns |

| DQS Interval Oscillator Readout Timing | | | | | | | | |
|-----------------------------------------------------------------------|------------------|-----------------------------------------|----|---------------------------|----|---------------------------|----|-----|
| Delay time from DQS interval oscillator stop to mode register readout | tOSCO | tMPC_De lay | | tMPC_De lay | | tMPC_De lay | | nCK |
| DQS interval oscillator start gap in automatic stop mode | tOSCS | tMPC_Delay + DQS interval timer runtime | | | | | | nCK |
| ECS Timing | | | | | | | | |
| ECS operation time | tECS | 176nCK, 110ns (MAX) | | 176nCK, 110ns (MAX) | | 176nCK, 110ns (MAX) | | |
| CRC Error Reporting Timing | | | | | | | | |
| CRC error to ALERT_n_latency | tCRC_ALERT | 3 | 13 | 3 | 13 | 3 | 13 | ns |
| CRC ALERT_n pulse width | CRC_ALERT_ PW | 12 | 20 | 12 | 20 | 12 | 20 | nCK |

8. Module Dimensions



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ± 0.15 (6), unless otherwise specified.

9. RoHS Declaration

| | | |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------|----------|
|  | 宜鼎國際股份有限公司 Innodisk Corporation | Page 1/2 |
| Tel:(02)7703-3000 Internet: https://www.innodisk.com/ | | |
| RoHS 自我宣告書 (RoHS Declaration of Conformity) | | |
| Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products | | |
| <p>一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及 (EU) 2015/863 關於 RoHS 之規範要求。 Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.</p> <p>二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。 Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.</p> <p>三、 本公司聲明我們的產品符合 RoHS 指令的附件中 7(a)、7(c)-I、6(c) 允許豁免。 We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.</p> <p>※ 7(a) Lead in high melting temperature type solders (i. e. lead-based alloys containing 85% by weight or more lead).</p> <p>※ 7(c)-I Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.</p> <p>※ 6(c) Copper alloy containing up to 4% lead by weight. (This exemption applies to products that use antennas)</p> | | |
| Name of hazardous substance | Limited of RoHS ppm (mg/kg) | |
| 鉛 (Pb) | < 1000 ppm | |
| 汞 (Hg) | < 1000 ppm | |
| 鎘 (Cd) | < 100 ppm | |
| 六價鉻 (Cr 6+) | < 1000 ppm | |
| 多溴聯苯 (PBBs) | < 1000 ppm | |
| 多溴二苯醚 (PBDEs) | < 1000 ppm | |
| 鄰苯二甲酸二(2-乙基己基)酯 (DEHP) | < 1000 ppm | |
| 鄰苯二甲酸丁酯苯甲酯 (BBP) | < 1000 ppm | |
| 鄰苯二甲酸二丁酯 (DBP) | < 1000 ppm | |

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宜鼎國際股份有限公司
Innodisk Corporation

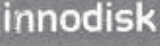


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|------------------|------------|
| 鄰苯二甲酸二異丁酯 (DIBP) | < 1000 ppm |
|------------------|------------|

立 保 證 書 人 (Guarantor)

Company name 公司名稱: Innodisk Corporation 宜鼎國際股份有限公司Company Representative 公司代表人: Randy Chien 簡川勝Company Representative Title 公司代表人職稱: Chairman 董事長Date 日期: 2021 / 06 / 09

10. REACH Declaration

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|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------------------------------------------------------------------|
|  | <p style="text-align: center;">宜鼎國際股份有限公司 Innodisk Corporation REACH Declaration</p> |
| <p style="text-align: right;">Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: https://www.innodisk.com/</p> | |
| <p>Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006). We hereby confirm that the product(s),</p> | |
| <p>Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.</p> | |
| <ul style="list-style-type: none"> ■ The standard products of not listed in the <u>Appendix2</u> meet the requirements of REACH SVHC regulations(SVHCs < 0.1% in Article), as described in the candidate list table currently including 224 substances and shown on the ECHA website. (http://echa.europa.eu/de/candidate-list-table). ■ The standard products listed in the <u>Appendix2</u> contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table. Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs > 0.1% in Article). ■ Comply with REACH Annex XVII. | |
| <p style="text-align: center;">Guarantor</p> | |
| <p>Company name 公司名稱： <u>Innodisk Corporation 宜鼎國際股份有限公司</u></p> | |
| <p>Company Representative 公司代表人： <u> 陳怡全</u></p> | |
| <p>Company Representative Title 公司代表人職稱： <u>QA Manager 品保經理</u></p> | |
| <p>Date 日期： <u>2022 / 06 / 14</u></p> | |
|  | |

Revision Log

| Rev | Date | Modification |
|-----|-------------------------------|---------------------|
| 0.1 | 23 th October 2023 | Preliminary Edition |
| 1.0 | 23 th October 2023 | Change key timing |