MS-98F7

COM Express Compact Module

Copyright Notice

Trademarks

Revision History

Revision	Date
V1.0	2017/08

Technical Support

If a problem arises with your system and no solution can be obtained from the user's manual, please contact your place of purchase or local distributor. Alternatively, please visit the MSI website for technical guide, BIOS updates, driver updates and other information, or contact our technical staff via http://www.msi.com/support/

Safety Instructions

- Always read the safety instructions carefully.
- Keep this User's Manual for future reference.
- Keep this equipment away from humidity.
- Lay this equipment on a reliable flat surface before setting it up.
- The openings on the enclosure are for air convection hence protects the equipment from overheating. DO NOT COVER THE OPENINGS.
- Make sure the voltage of the power source and adjust properly 110/220V before connecting the equipment to the power inlet.
- Place the power cord such a way that people can not step on it. Do not place anything over the power cord.
- Always Unplug the Power Cord before inserting any add-on card or module.
- All cautions and warnings on the equipment should be noted.
- Never pour any liquid into the opening that could damage or cause electrical shock.
- If any of the following situations arises, get the equipment checked by service personnel:
  - The power cord or plug is damaged.
  - Liquid has penetrated into the equipment.
  - The equipment has been exposed to moisture.
  - The equipment does not work well or you can not get it work according to User's Manual.
  - The equipment has dropped and damaged.
  - The equipment has obvious sign of breakage.
- DO NOT LEAVE THIS EQUIPMENT IN AN ENVIRONMENT UNCONDITIONED, STORAGE TEMPERATURE ABOVE 60°C (140°F), IT MAY DAMAGE THE EQUIPMENT.

Chemical Substances Information

In compliance with chemical substances regulations, such as the EU REACH Regulation (Regulation EC No. 1907/2006 of the European Parliament and the Council), MSI provides the information of chemical substances in products at:

http://www.msi.com/html/popup/csr/evmtprtt_pcm.html

Battery Information

European Union:

Batteries, battery packs, and accumulators should not be disposed of as unsorted household waste. Please use the public collection system to return, recycle, or treat them in compliance with the local regulations.

廢電池請回收

Taiwan:

For better environmental protection, waste batteries should be collected separately for recycling or special disposal.

California, USA:

The button cell battery may contain perchlorate material and requires special handling when recycled or disposed of in California.

For further information please visit:

http://www.dtsc.ca.gov/hazardouswaste/perchlorate/

Danger of explosion if battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer.

CE Conformity

Hereby, Micro-Star International CO., LTD declares that this device is in compliance with the essential safety requirements and other relevant provisions set out in the European Directive.

FCC-A Radio Frequency Interference Statement

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference, in which case the user will be required to correct the interference at his own expense.

Notice 1

The changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

Notice 2

Shielded interface cables and AC power cord, if any, must be used in order to comply with the emission limits.

This device complies with Part 15 of the FCC Rules. Operation is subject to the following two conditions:

1) this device may not cause harmful interference, and
2) this device must accept any interference received, including interference that may cause undesired operation.

WEEE Statement

Under the European Union ("EU") Directive on Waste Electrical and Electronic Equipment, Directive 2002/96/EC, which takes effect on August 13, 2005, products of "electrical and electronic equipment" cannot be discarded as municipal waste anymore and manufacturers of covered electronic equipment will be obligated to take back such products at the end of their useful life.

CONTENTS

1 Overview

Thank you for choosing the MS-98F7, an excellent COM (computer-on-module) Express Compact Module. Integrating core CPU and memory functionality, it is the entry-level model for applications looking to transition from other small form factor solutions to COM Express® and offers full PCI Express, USB, SATA, graphics and network support.

Specifications

Processor (Optional)

- Intel® Kaby Lake/ Skylake Embedded Mobile Core™ i7/ i5/ i3/ Celeron® Processor
  - Kaby Lake Core™ i7-7600U/ Skylake Core™ i7-6600U
  - Kaby Lake Core™ i5-7300U/ Skylake Core™ i5-6300U
  - Kaby Lake Core™ i3-7100U/ Skylake Core™ i3-6100U
  - Kaby Lake Celeron® 3965U/ Skylake Celeron® 3955U

Memory

- 2 * DDR4 SO-DIMM slots
- Supports non-ECC DDR4 2133 MHz SO-DIMMs
- Up to 32 GB

LAN

- PCH Integrated Gigabit LAN controller
- Intel® I219LM GbE-PHY LAN

Graphics

- Graphics integrated in Intel® processor
- 1 * LVDS 18/24-Bit Dual Channel
  - LVDS shared with eDP signal (default is LVDS)
  - LVDS resolution up to 1920x1200 @ 60 Hz
- 2 * DDI ports support HDMI1.4 or DP multiplexed (BIOS modification needed), DDI1/2 support Video out
  - HDMI1.4 up to 4096x2160 @ 24 Hz
  - DP up to 4096x2304 @ 60Hz
- 1 * VGA shared with DDI2 signal (optional)
  - Resolution up to 1920 x 1080
- 2 Independent Displays supported
  - DDI1 + LVDS
  - DDI1 + DDI2/VGA
  - DDI2/VGA + LVDS
- 3 Independent Displays supported
  - LVDS + DDI1 + DDI2/VGA

EC

- ITE IT8528 controller chip providing all PC-compatible I/O

Storage

- Controller integrated in Intel® processor
- Supports 3 Serial ATA interfaces
  - 3 * SATA 6Gb/s ports
  - Integrated Advanced Host Controller Interface (AHCI) controller

USB

- Controller integrated in Intel® processor
- 4 * USB3.0 (to carrier board)
- 8 * USB2.0 (to carrier board)

PCI Express Interface

- PEG
  - 1 * PCIe x2 (shared signal with PCIe 5 & 6)
- PCIe (supports up to 5 devices and 8 lanes)
  - 5 * PCIe x1 or
  - 4 * PCIe x1 + 1 * PCIe x4 or
  - 3 * PCIe x1 + 2 * PCIe x2

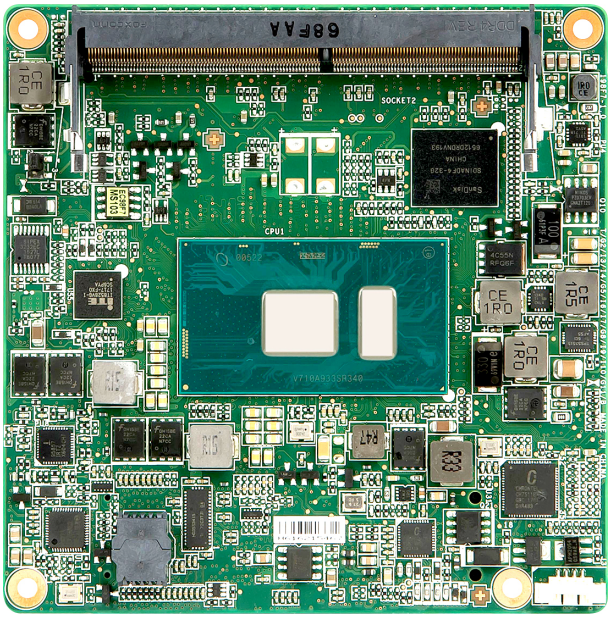
Form Factor

- COM Express Compact: 95mm x 95mm

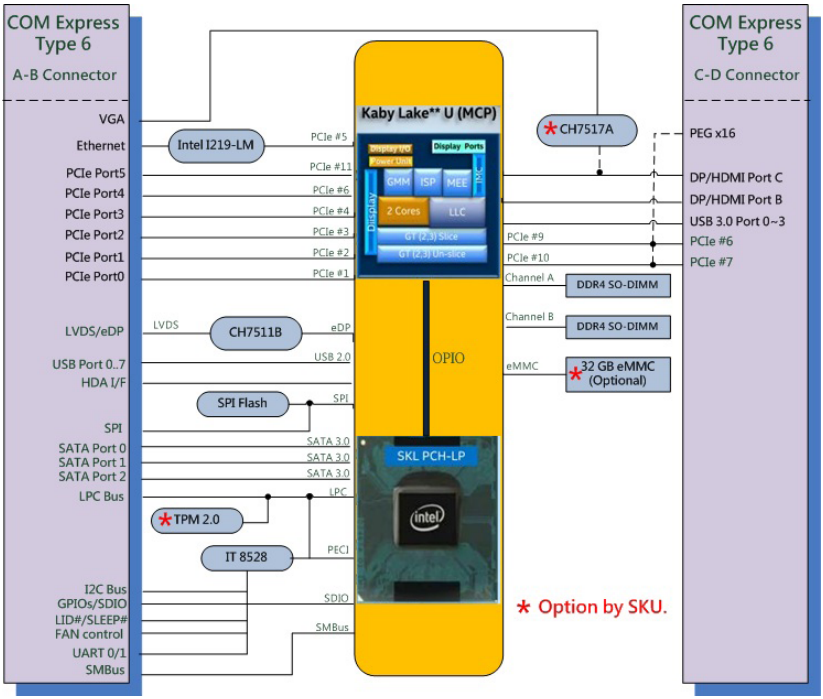
Environment

- Operating Temperature: -20 ~ 70°C
- Storage Temperature: -20 ~ 80°C
- Humidity: 10% ~ 90% RH, non-condensing

Layout



Block Diagram



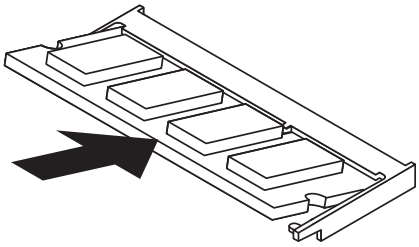
2 Hardware Setup

This chapter provides you with the information about hardware setup procedures. While doing the installation, be careful in holding the components and follow the installation procedures. For some components, if you install in the wrong orientation, the components will not work properly.
Use a grounded wrist strap before handling computer components. Static electricity may damage the components.

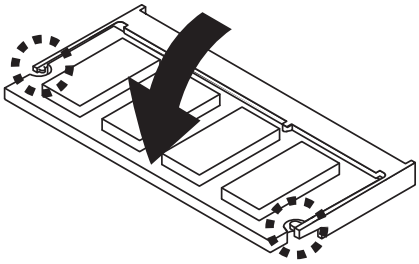
Memory

The SO-DIMM slot is intended for memory modules.

1. Locate the SO-DIMM slot. Align the notch on the DIMM with the key on the slot and insert the DIMM into the slot.



2. Push the DIMM gently downwards until the slot levers click and lock the DIMM in place.



3. To uninstall the DIMM, flip the slot levers outwards and the DIMM will be released instantly.

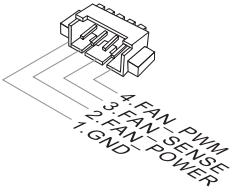
Important

You can barely see the golden finger if the DIMM is properly inserted in the DIMM slot.

Connector

Fan Power Connector: CPUFAN1

The fan power connectors support system cooling fan with +12V. When connecting the wire to the connectors, always note that the red wire is the positive and should be connected to the +12V; the black wire is Ground and should be connected to GND. If the motherboard has a System Hardware Monitor chipset onboard, you must use a specially designed fan with speed sensor to take advantage of the CPU fan control.

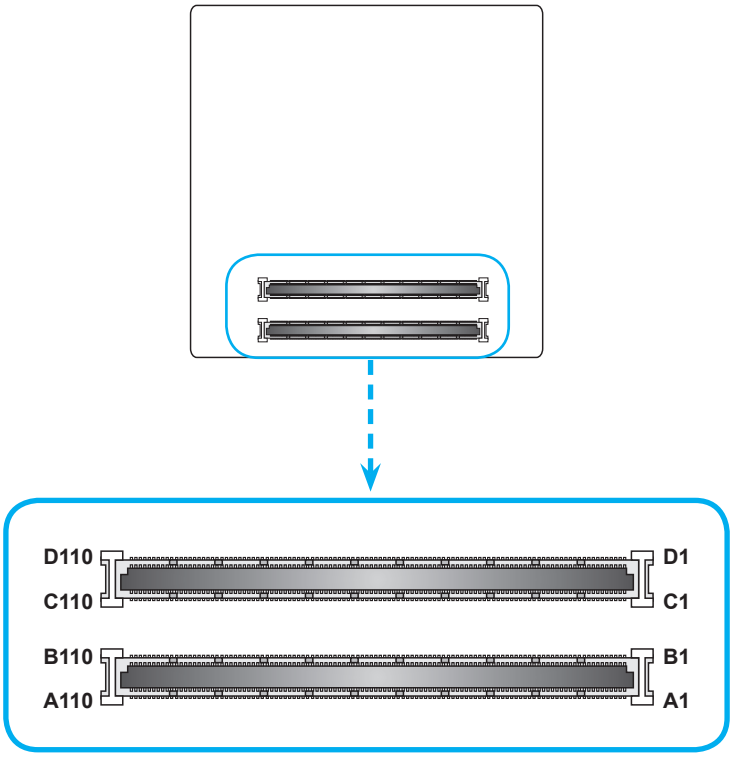


Important

Please refer to the recommended CPU fans at processor's official website or consult the vendors for proper CPU cooling fan.

COM Express Connectors

The COM Express connectors are used to interface the COM Express module board to a carrier board. Connect the COM Express connectors located on the solder side of the module board (as indicated below) to the COM Express connectors on the carrier board.



Row A		Row B		Row C		Row D	
A1	GND (FIXED)	B1	GND (FIXED)	C1	GND (FIXED)	D1	GND (FIXED)
A2	GBE0_MDI3-	B2	GBE0_ACT#	**C2**	**GND**	**D2**	**GND**
A3	GBE0_MDI3+	B3	LPC_FRAME#	**C3**	**USB_SSRX0-**	**D3**	**USB_SSTX0-**
A4	GBE0_LINK100#	B4	LPC_AD0	**C4**	**USB_SSRX0+**	**D4**	**USB_SSTX0+**
A5	GBE0_LINK1000#	B5	LPC_AD1	**C5**	**GND**	**D5**	**GND**
A6	GBE0_MDI2-	B6	LPC_AD2	**C6**	**USB_SSRX1-**	**D6**	**USB_SSTX1-**
A7	GBE0_MDI2+	B7	LPC_AD3	**C7**	**USB_SSRX1+**	**D7**	**USB_SSTX1+**
A8	GBE0_LINK#	B8		**C8**	**GND**	**D8**	**GND**
A9	GBE0_MDI1-	B9		**C9**	**USB_SSRX2-**	**D9**	**USB_SSTX2-**
A10	GBE0_MDI1+	B10	LPC_CLK	**C10**	**USB_SSRX2+**	**D10**	**USB_SSTX2+**
A11	GND (FIXED)	B11	GND (FIXED)	C11	GND (FIXED)	D11	GND (FIXED)
A12	GBE0_MDI0-	B12	PWRBTN#	**C12**	**USB_SSRX3-**	**D12**	**USB_SSTX3-**
A13	GBE0_MDI0+	B13	SMB_CK	**C13**	**USB_SSRX3+**	**D13**	**USB_SSTX3+**
A14	GBE0_CTREF	B14	SMB_DAT	**C14**	**GND**	**D14**	**GND**
A15	SUS_S3#	B15	SMB_ALERT#	**C15**		**D15**	**DDI1_CTRLCLK_AUX+**
A16	SATA0_TX+	B16	SATA1_TX+	**C16**		**D16**	**DDI1_CTRLDATA_AUX-**
A17	SATA0_TX-	B17	SATA1_TX-	**C17**	**RSVD***	**D17**	**RSVD***
A18	SUS_S4#	B18	SUS_STAT#	**C18**	**RSVD***	**D18**	**RSVD***
A19	SATA0_RX+	B19	SATA1_RX+	**C19**	**PCIE_RX6+**	**D19**	**PCIE_TX6+**
A20	SATA0_RX-	B20	SATA1_RX-	**C20**	**PCIE_RX6-**	**D20**	**PCIE_TX6-**
A21	GND (FIXED)	B21	GND (FIXED)	C21	GND (FIXED)	D21	GND (FIXED)
A22	SATA2_TX+	B22		**C22**	**PCIE_RX7+**	**D22**	**PCIE_TX7+**
A23	SATA2_TX-	B23		**C23**	**PCIE_RX7-**	**D23**	**PCIE_TX7-**
A24	SUS_S5#	B24	PWR_OK	**C24**	**DDI1_HPD**	**D24**	**RSVD***
A25	SATA2_RX+	B25		**C25**		**D25**	**RSVD***
A26	SATA2_RX-	B26		**C26**		**D26**	**DDI1_PAIR0+**
A27	BATLOW#	B27	WDT	**C27**	**RSVD***	**D27**	**DDI1_PAIR0-**
A28	**(S)ATA_ACT#**	B28		**C28**	**RSVD***	**D28**	**RSVD***
A29	**AC/HDA_SYNC**	B29	**AC/HDA_SDIN1**	**C29**		**D29**	**DDI1_PAIR1+**
A30	**AC/HDA_RST#**	B30	**AC/HDA_SDIN0**	**C30**		**D30**	**DDI1_PAIR1-**
A31	GND (FIXED)	B31	GND (FIXED)	C31	GND (FIXED)	D31	GND (FIXED)
A32	**AC/HDA_BITCLK**	B32	SPKR	**C32**	**DDI2_CTRLCLK_AUX+**	**D32**	**DDI1_PAIR2+**
A33	**AC/HDA_SDOUT**	B33	I2C_CK	**C33**	**DDI2_CTRLDATA_AUX-**	**D33**	**DDI1_PAIR2-**
A34	**BIOS_DIS0#**	B34	I2C_DAT	**C34**	**DDI2_DDC_AUX_SEL**	**D34**	**DDI1_DDC_AUX_SEL**
A35	THRMTRIP#	B35	THRM#	**C35**	**RSVD***	**D35**	**RSVD***
A36	USB6-	B36	USB7-	**C36**		**D36**	**DDI1_PAIR3+**
A37	USB6+	B37	USB7+	**C37**		**D37**	**DDI1_PAIR3-**
A38	USB_6_7_OC#	B38	USB_4_5_OC#	**C38**		**D38**	**RSVD***
A39	USB4-	B39	USB5-	**C39**		**D39**	**DDI2_PAIR0+**
A40	USB4+	B40	USB5+	**C40**		**D40**	**DDI2_PAIR0-**
A41	GND (FIXED)	B41	GND (FIXED)	C41	GND (FIXED)	D41	GND (FIXED)
A42	USB2-	B42	USB3-	**C42**		**D42**	**DDI2_PAIR1+**
A43	USB2+	B43	USB3+	**C43**		**D43**	**DDI2_PAIR1-**
A44	USB_2_3_OC#	B44	USB_0_1_OC#	**C44**		**D44**	**DDI2_HPD**
A45	USB0-	B45	USB1-	**C45**	**RSVD***	**D45**	**RSVD***
A46	USB0+	B46	USB1+	**C46**		**D46**	**DDI2_PAIR2+**
A47	VCC_RTC	B47	EXCD1_PERST#	**C47**		**D47**	**DDI2_PAIR2-**
A48	EXCD0_PERST#	B48	EXCD1_CPPE#	**C48**	**RSVD***	**D48**	**RSVD***
A49	EXCD0_CPPE#	B49	SYS_RESET#	**C49**		**D49**	**DDI2_PAIR3+**
A50	LPC_SERIRQ	B50	CB_RESET#	**C50**		**D50**	**DDI2_PAIR3-**
A51	GND (FIXED)	B51	GND (FIXED)	C51	GND (FIXED)	D51	GND (FIXED)
A52	PCIE_TX5+	B52	PCIE_RX5+	C52	PEG_RX0+	D52	PEG_TX0+
A53	PCIE_TX5-	B53	PCIE_RX5-	C53	PEG_RX0-	D53	PEG_TX0-
A54	GPI0	B54	GPO1	C54		D54	
A55	PCIE_TX4+	B55	PCIE_RX4+	C55	PEG_RX1+	D55	PEG_TX1+
A56	PCIE_TX4-	B56	PCIE_RX4-	C56	PEG_RX1-	D56	PEG_TX1-
A57	GND	B57	GPO2	C57		D57	TYPE2#
A58	PCIE_TX3+	B58	PCIE_RX3+	C58		D58	
A59	PCIE_TX3-	B59	PCIE_RX3-	C59		D59	
A60	GND (FIXED)	B60	GND (FIXED)	C60	GND (FIXED)	D60	GND (FIXED)
A61	PCIE_TX2+	B61	PCIE_RX2+	C61		D61	
A62	PCIE_TX2-	B62	PCIE_RX2-	C62		D62	
A63	GPI1	B63	GPO3	C63	RSVD*	D63	RSVD*

Row A		Row B		Row C		Row D	
A64	PCIE_TX1+	B64	PCIE_RX1+	C64	RSVD*	D64	RSVD*
A65	PCIE_TX1-	B65	PCIE_RX1-	C65		D65	
A66	GND	B66	WAKE0#	C66		D66	
A67	GPI2	B67	WAKE1#	C67	RSVD*	D67	GND
A68	PCIE_TX0+	B68	PCIE_RX0+	C68		D68	
A69	PCIE_TX0-	B69	PCIE_RX0-	C69		D69	
A70	GND (FIXED)	B70	GND (FIXED)	C70	GND (FIXED)	D70	GND (FIXED)
A71	LVDS_A0+	B71	LVDS_B0+	C71		D71	
A72	LVDS_A0-	B72	LVDS_B0-	C72		D72	
A73	LVDS_A1+	B73	LVDS_B1+	**C73**	**GND**	**D73**	**GND**
A74	LVDS_A1-	B74	LVDS_B1-	C74		D74	
A75	LVDS_A2+	B75	LVDS_B2+	C75		D75	
A76	LVDS_A2-	B76	LVDS_B2-	C76	GND	D76	GND
A77	LVDS_VDD_EN	B77	LVDS_B3+	C77	RSVD*	**D77**	**RSVD***
A78	LVDS_A3+	B78	LVDS_B3-	C78		D78	
A79	LVDS_A3-	B79	LVDS_BKLT_EN	C79		D79	
A80	GND (FIXED)	B80	GND (FIXED)	C80	GND (FIXED)	D80	GND (FIXED)
A81	LVDS_A_CK+	B81	LVDS_B_CK+	C81		D81	
A82	LVDS_A_CK-	B82	LVDS_B_CK-	C82		D82	
A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL	C83	RSVD*	D83	RSVD*
A84	LVDS_I2C_DAT	B84	VCC_5V_SBY	C84	GND	D84	GND
A85	GPI3	B85	VCC_5V_SBY	C85		D85	
A86	**RSVD***	B86	VCC_5V_SBY	C86		D86	
A87	**RSVD***	B87	VCC_5V_SBY	C87	GND	D87	GND
A88	**PCIE_CLK_REF+**	B88	BIOS_DIS1#	C88		D88	
A89	**PCIE_CLK_REF-**	B89	VGA_RED	C89		D89	
A90	GND (FIXED)	B90	GND (FIXED)	C90	GND (FIXED)	D90	GND (FIXED)
A91	**SPI_POWER**	B91	VGA_GRN	C91		D91	
A92	**SPI_MISO**	B92	VGA_BLU	C92		D92	
A93	GPO0	B93	VGA_HSYNC	C93	GND	D93	GND
A94	**SPI_CLK**	B94	VGA_VSYNC	C94		D94	
A95	**SPI_MOSI**	B95	VGA_I2C_CK	C95		D95	
A96	**TPM_PP**	B96	VGA_I2C_DAT	C96	GND	D96	GND
A97		B97	**SPI_CS#**	C97	RSVD*	D97	**RSVD***
A98	**SER0_TX**	B98	**RSVD***	C98		D98	
A99	**SER0_RX**	B99	**RSVD***	C99		D99	
A100	GND (FIXED)	B100	GND (FIXED)	C100	GND (FIXED)	D100	GND (FIXED)
A101	**SER1_TX**	**B101**	**FAN_PWMOUT**	C101		D101	
A102	**SER1_RX**	**B102**	**FAN_TACHIN**	C102		D102	
A103	**LID#**	**B103**	**SLEEP#**	C103	GND	D103	GND
A104	VCC_12V	B104	VCC_12V	C104	VCC_12V	D104	VCC_12V
A105	VCC_12V	B105	VCC_12V	C105	VCC_12V	D105	VCC_12V
A106	VCC_12V	B106	VCC_12V	C106	VCC_12V	D106	VCC_12V
A107	VCC_12V	B107	VCC_12V	C107	VCC_12V	D107	VCC_12V
A108	VCC_12V	B108	VCC_12V	C108	VCC_12V	D108	VCC_12V
A109	VCC_12V	B109	VCC_12V	C109	VCC_12V	D109	VCC_12V
A110	GND (FIXED)	B110	GND (FIXED)	C110	GND (FIXED)	D110	GND (FIXED)

** RSVD pins are reserved for future use and **should** be no connect. Do not tie the RSVD pins together.*

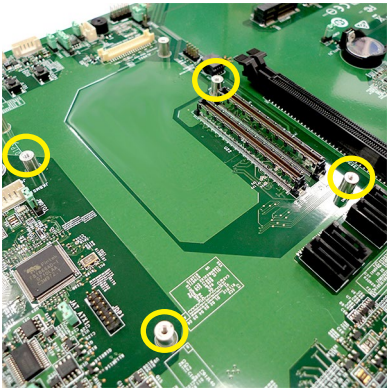
Hardware Installation

➤ Installing Module Board onto Carrier Board

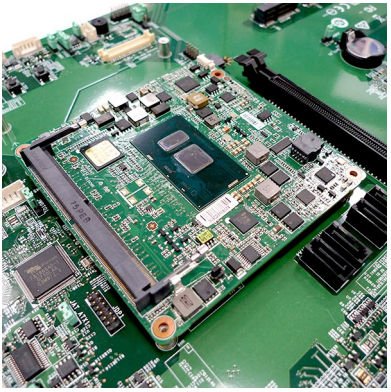
Important

The illustrations are provided to guide users on how to install the module board onto the carrier board of their choice and should be held for reference only.

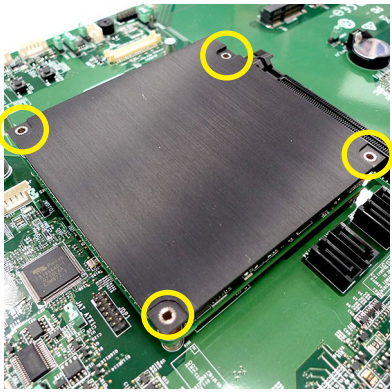
1. Locate the threaded standoffs on the carrier board.



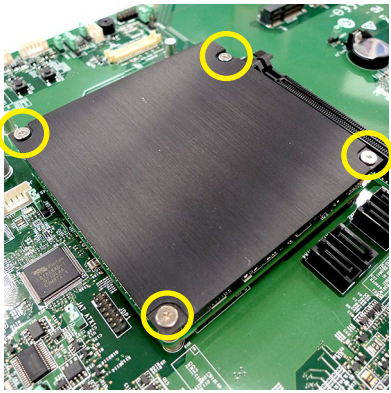
2. Position the module board on top of the carrier board with its mounting holes aligned with the standoffs on the carrier board and the COM Express connectors of both boards aligned to each other. Press the module board down firmly until it is securely seated on the COM Express connectors of the carrier board.



3. Flip the heat spreader over and remove the protective film from its thermal paste. Mount the heat spreader onto the module board with mounting holes aligned.



4. Use the provided mounting screws to secure the heat spreader to the module board and the carrier board.



3 BIOS Setup

This chapter provides information on the BIOS Setup program and allows users to configure the system for optimal use.

Users may need to run the Setup program when:

- An error message appears on the screen at system startup and requests users to run SETUP.
- Users want to change the default settings for customized features.

Important

- *Please note that BIOS update assumes technician-level experience.*
- *As the system BIOS is under continuous update for better system performance, the illustrations in this chapter should be held for reference only.*

Entering Setup

Power on the computer and the system will start POST (Power On Self Test) process. When the message below appears on the screen, press <DEL> key to enter Setup.

Press <DEL> to enter SETUP

If the message disappears before you respond and you still wish to enter Setup, restart the system by turning it OFF and On or pressing the RESET button. You may also restart the system by simultaneously pressing <Ctrl>, <Alt>, and <Delete> keys.

Important

The items under each BIOS category described in this chapter are under continuous update for better system performance. Therefore, the description may be slightly different from the latest BIOS and should be held for reference only.

Control Keys

← →	Select Screen
↑ ↓	Select Item
Enter	Select
+ -	Change Option
F1	General Help
F7	Previous Values
F9	Optimized Defaults
F10	Save & Reset
Esc	Exit

Getting Help

After entering the Setup menu, the first menu you will see is the Main Menu.

Main Menu

The main menu lists the setup functions you can make changes to. You can use the arrow keys (↑↓) to select the item. The on-line description of the highlighted setup function is displayed at the bottom of the screen.

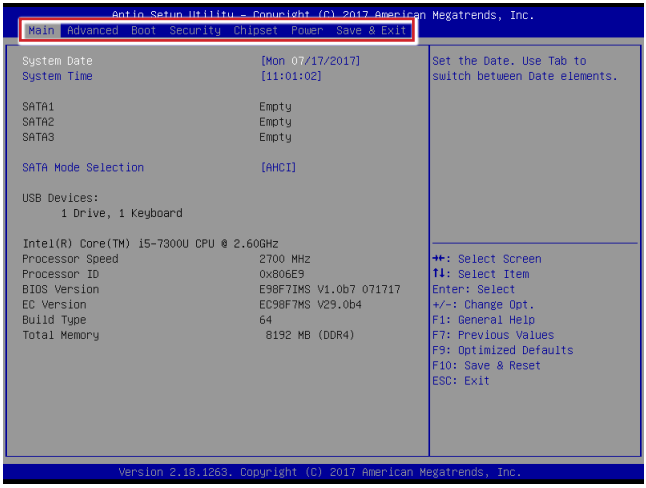
Sub-Menu

If you find a right pointer symbol appears to the left of certain fields that means a sub-menu can be launched from this field. A sub-menu contains additional options for a field parameter. You can use arrow keys (↑↓) to highlight the field and press <Enter> to call up the sub-menu. Then you can use the control keys to enter values and move from field to field within a sub-menu. If you want to return to the main menu, just press the <Esc >.

General Help <F1>

The BIOS setup program provides a General Help screen. You can call up this screen from any menu by simply pressing <F1>. The Help screen lists the appropriate keys to use and the possible selections for the highlighted item. Press <Esc> to exit the Help screen.

The Menu Bar



▸ **Main**

Use this menu for basic system configurations, such as time, date, etc.

▸ **Advanced**

Use this menu to set up the items of special enhanced features.

▸ **Boot**

Use this menu to specify the priority of boot devices.

▸ **Security**

Use this menu to set supervisor and user passwords.

▸ **Chipset**

This menu controls the advanced features of the onboard chipsets.

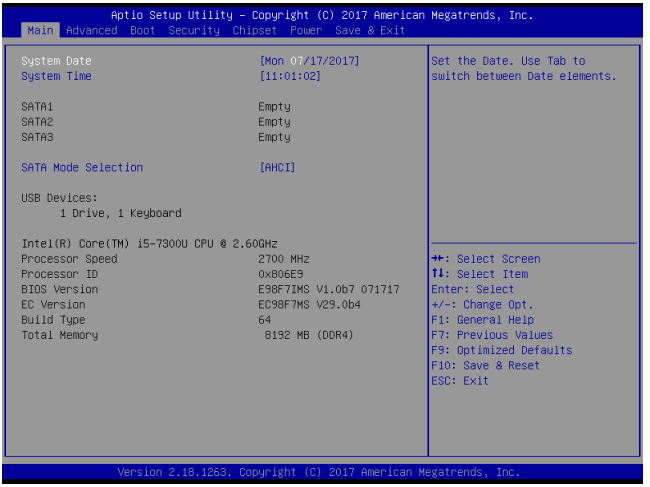
▸ **Power**

Use this menu to specify your settings for power management.

▸ **Save & Exit**

This menu allows you to load the BIOS default values or factory default settings into the BIOS and exit the BIOS setup utility with or without changes.

Main



▸System Date

This setting allows you to set the system date. The date format is <Day>, <Month> <Date> <Year>.

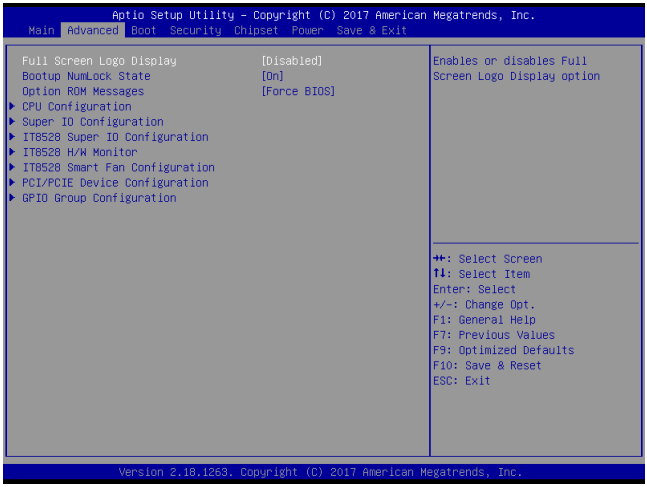
▸System Time

This setting allows you to set the system time. The time format is <Hour> <Minute> <Second>.

▸SATA Mode Selection

This setting specifies the SATA controller mode.

Advanced



▸Full Screen Logo Display

This BIOS feature determines if the BIOS should hide the normal POST messages with the motherboard or system manufacturer's full-screen logo.

When it is enabled, the BIOS will display the full-screen logo during the boot-up sequence, hiding normal POST messages.

When it is disabled, the BIOS will display the normal POST messages, instead of the full-screen logo.

Please note that enabling this BIOS feature often adds 2-3 seconds of delay to the booting sequence. This delay ensures that the logo is displayed for a sufficient amount of time. Therefore, it is recommended that you disable this BIOS feature for a faster boot-up time.

▸Bootup NumLock State

This setting is to set the Num Lock status when the system is powered on. Setting to [On] will turn on the Num Lock key when the system is powered on. Setting to [Off] will allow users to use the arrow keys on the numeric keypad.

▸Option ROM Messages

This item is used to determine the display mode when an optional ROM is initialized during POST. When set to [Force BIOS], the display mode used by AMI BIOS is used. Select [Keep Current] if you want to use the display mode of optional ROM.

▸CPU Configuration

▸Intel Virtualization Technology

Virtualization enhanced by Intel Virtualization Technology will allow a platform to run multiple operating systems and applications in independent partitions. With virtualization, one computer system can function as multiple “Virtual” systems.

▸Active Processor Cores

This setting specifies the number of active processor cores.

▸Hyper-Threading

The processor uses Hyper-Threading technology to increase transaction rates and reduces end-user response times. The technology treats the two cores inside the processor as two logical processors that can execute instructions simultaneously. In this way, the system performance is highly improved. If you disable the function, the processor will use only one core to execute the instructions. Please disable this item if your operating system doesn’t support HT Function, or unreliability and instability may occur.

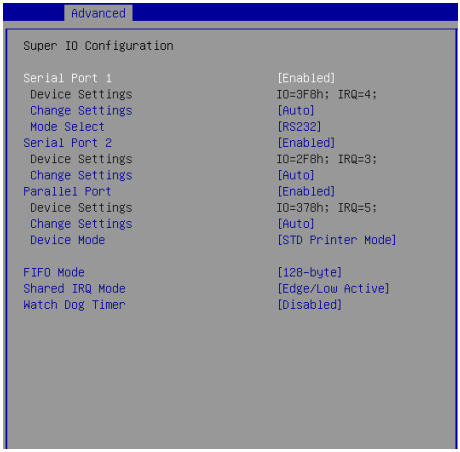
▸Intel(R) SpeedStep(TM)

EIST (Enhanced Intel SpeedStep Technology) allows the system to dynamically adjust processor voltage and core frequency, which can result in decreased average power consumption and decreased average heat production. When disabled, the processor will return the actual maximum CPUID input value of the processor when queried.

▸C States

C-state performance indicates the ability to run the processor in lower power states when the PC is idle. This setting enables/disables the C-State Configuration for power saving purposes.

▸**Super IO Configuration** *(the Carrier Board)*



▸**Serial Port 1, Serial Port 2**

This setting enables/disables the specified serial port.

▸**Change Settings**

This setting is used to change the address & IRQ settings of the specified serial port.

▸**Mode Select**

Select an operation mode for the serial port 1.

▸**Parallel Port**

This setting enables/disables the parallel port.

▸**Change Settings**

This setting is used to change the address & IRQ settings of the parallel port.

▸**Device Mode**

Select an operation mode for the parallel port.

▸**FIFO Mode**

This setting controls the FIFO data transfer mode.

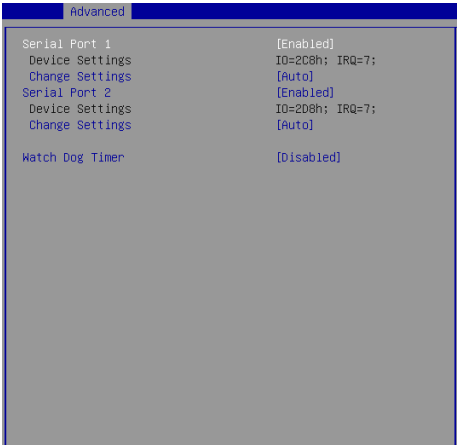
▸**Shared IRQ Mode**

This setting provides the system with the ability to share interrupts among its serial ports.

▸ **Watch Dog Timer**

You can enable the system watch-dog timer, a hardware timer that generates a reset when the software that it monitors does not respond as expected each time the watch dog polls it.

▸IT8528 Super IO Configuration



▸Serial Port 1, Serial Port 2

This setting enables/disables the specified serial port.

▸Change Settings

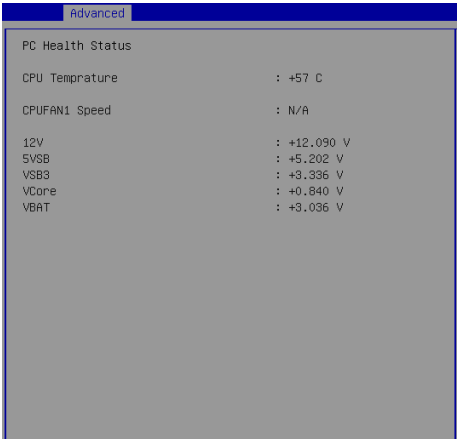
This setting is used to change the address & IRQ settings of the specified serial port.

▸Watch Dog Timer

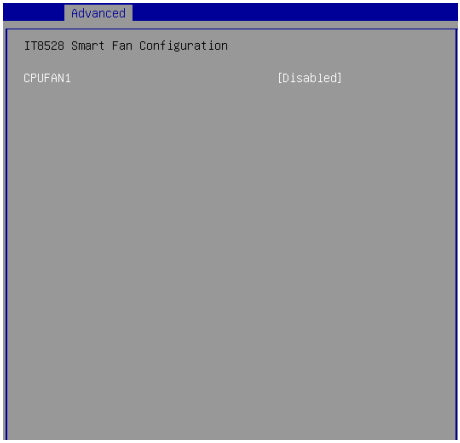
You can enable the system watch-dog timer, a hardware timer that generates a reset when the software that it monitors does not respond as expected each time the watch dog polls it.

▸IT8528 H/W Monitor *(the Compact Module)*

These items display the current status of all monitored hardware devices/ components such as voltages, temperatures and all fans' speeds.



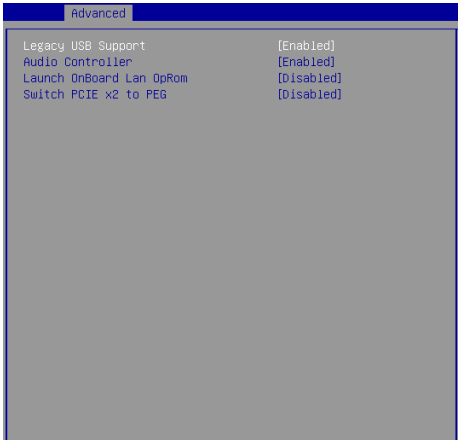
▸**IT8528 Smart Fan Configuration** *(the Compact Module)*



▸**CPUFAN1**

These settings enable/disable the Smart Fan function. Smart Fan is an excellent feature which will adjust the CPU/system fan speed automatically depending on the current CPU/system temperature, avoiding the overheating to damage your system.

▸**PCI/PCIE Device Configuration**



▸**Legacy USB Support**

Set to [Enabled] if you need to use any USB 1.1/2.0 device in the operating system that does not support or have any USB 1.1/2.0 driver installed, such as DOS and SCO Unix.

▸**Audio Controller**

This setting enables/disables the onboard audio controller.

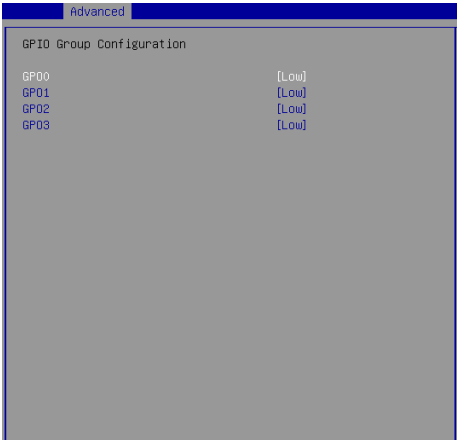
▸**Launch Onboard LAN OpROM**

This setting enables/disables the initialization of the specified LAN Boot ROM during bootup. Selecting [Disabled] will speed up the boot process.

▸**Switch PCIE x2 to PEG**

This setting allows users to switch PCIE x2 to PEG.

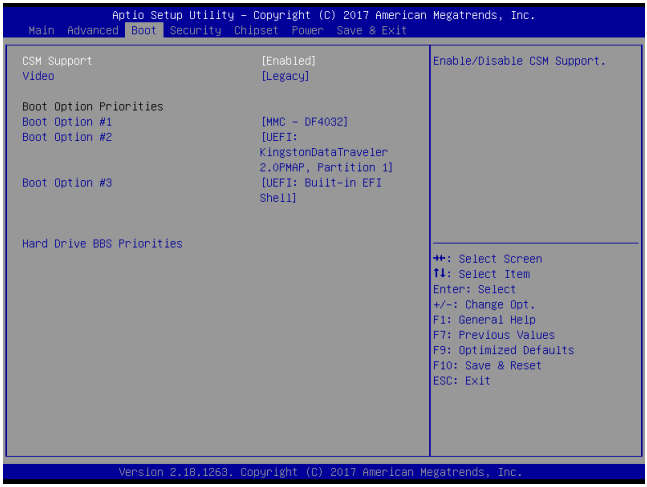
▸**GPIO Group Configuration** *(the Carrier Board)*



▸**GPO0 ~ GPO3**

These settings control the operation mode of the specified GPIO.

Boot



▸CSM Support

This setting enables/disables the support for Compatibility Support Module, a part of the Intel Platform Innovation Framework for EFI providing the capability to support legacy BIOS interfaces.

▸ Video

Select the type of primary video for your system.

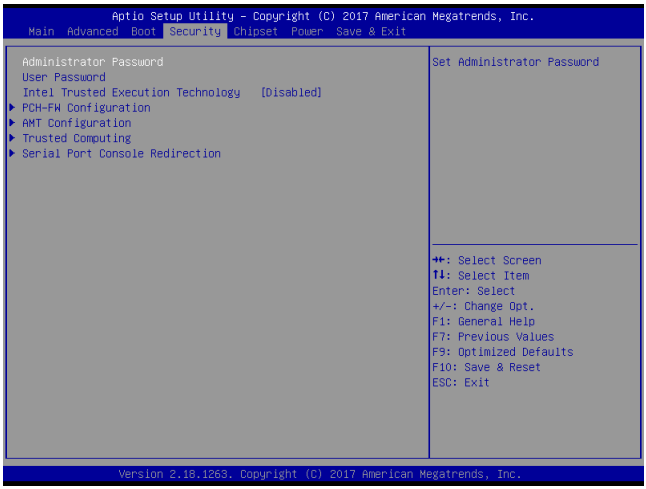
▸Boot Option Priorities

This setting allows users to set the sequence of boot devices where BIOS attempts to load the disk operating system.

▸Hard Drive BBS Priorities

This setting allows users to set the priority of the specified devices. First press <Enter> to enter the sub-menu. Then you may use the arrow keys (↑↓) to select the desired device, then press <+>, <-> or <PageUp>, <PageDown> key to move it up/down in the priority list.

Security



▸Administrator Password

Administrator Password controls access to the BIOS Setup utility.

▸User Password

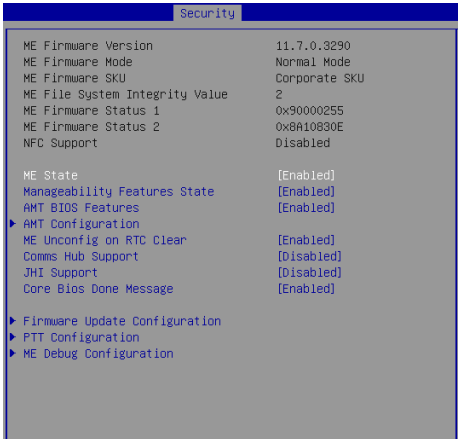
User Password controls access to the system at boot and to the BIOS Setup utility.

▸Intel Trusted Execution Technology

Intel Trusted Execution Technology provides highly scalable platform security in physical and virtual infrastructures.

▸PCH-FW Configuration

This menu provides settings for PCH-FW Configuration.



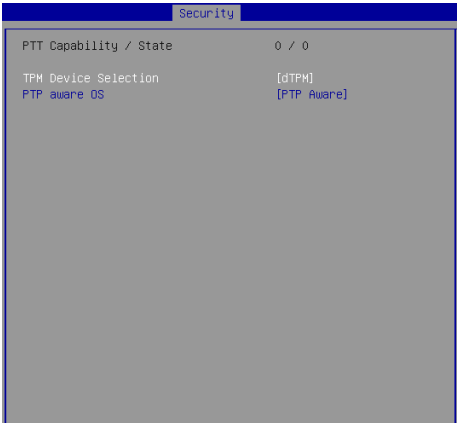
▸Firmware Update Configuration

▸ME FW Image Re-Flash

This setting enables/disables the ME FW image reflash.

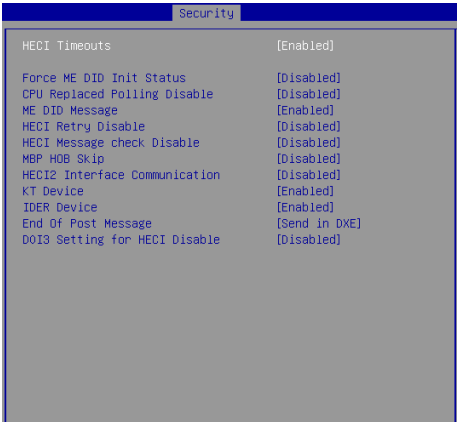
▸PTT Configuration

Intel Platform Trust Technology (PTT) is a platform functionality for credential storage and key management used by Microsoft Windows.



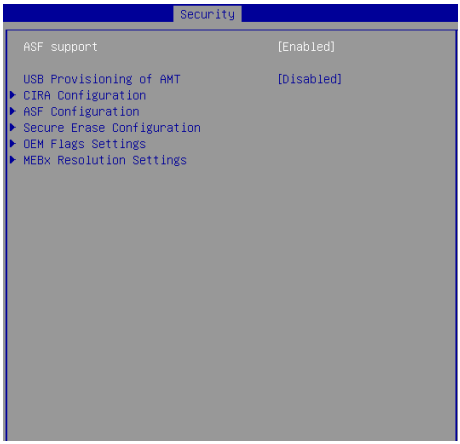
▸ME Debug Configuration

This menu provides settings for ME Debug Configuration.

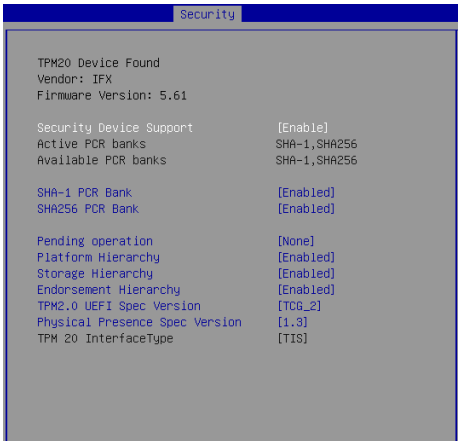


▸AMT Configuration

Intel Active Management Technology (AMT) is hardware-based technology for remotely managing and securing PCs out-of-band.



▸Trusted Computing



▸Security Device Support

This setting enables/disables BIOS support for security device. When set to [Disable], the OS will not show security device. TCG EFI protocol and INT1A interface will not be available.

▸SHA-1 PCR Bank, SHA256 PCR Bank

These settings enable/disable the SHA-1 PCR Bank and SHA256 PCR Bank.

▸Pending Operation

This setting shows pending operation.

▸**Platform Hierarchy, Storage Hierarchy, Endorsement Hierarchy**

These settings enable/disable the Platform Hierarchy, Storage Hierarchy and Endorsement Hierarchy.

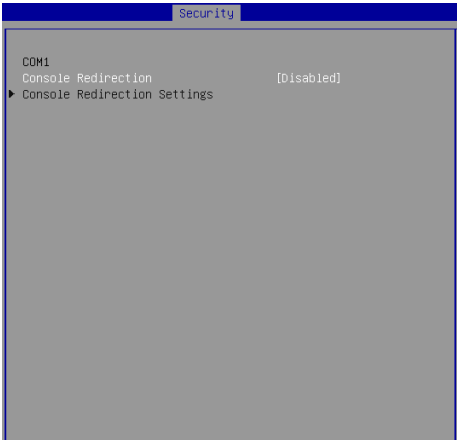
▸**TPM2.0 UEFI Spec Version, Physical Presence Spec Version**

This settings show the TPM2.0 UEFI Spec Version and Physical Presence Spec Version.

▸**TPM2.0 Interface Type**

This setting shows the TPM2.0 Interface Type.

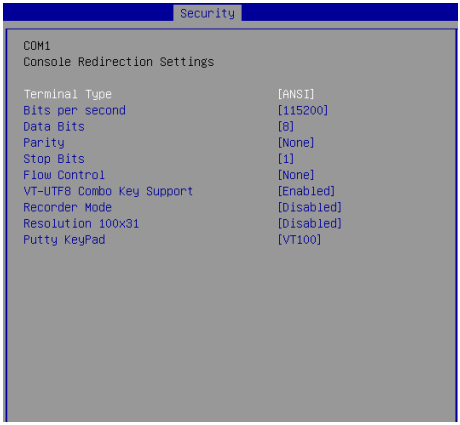
▸**Serial Port Console Redirection**



▸**Console Redirection**

Console Redirection operates in host systems that do not have a monitor and keyboard attached. This setting enables/disables the operation of console redirection. When set to [Enabled], BIOS redirects and sends all contents that should be displayed on the screen to the serial COM port for display on the terminal screen. Besides, all data received from the serial port is interpreted as keystrokes from a local keyboard.

▸Console Redirection Settings



▸Terminal Type

To operate the system's console redirection, you need a terminal supporting ANSI terminal protocol and a RS-232 null modem cable connected between the host system and terminal(s). This setting specifies the type of terminal device for console redirection.

▸ Bits per second, Data Bits, Parity, Stop Bits

This setting specifies the transfer rate (bits per second, data bits, parity, stop bits) of Console Redirection.

▸Flow Control

Flow control is the process of managing the rate of data transmission between two nodes. It's the process of adjusting the flow of data from one device to another to ensure that the receiving device can handle all of the incoming data. This is particularly important where the sending device is capable of sending data much faster than the receiving device can receive it.

▸VT-UTF8 Combo Key Support

This setting enables/disables the VT-UTF8 combination key support for ANSI/VT100 terminals.

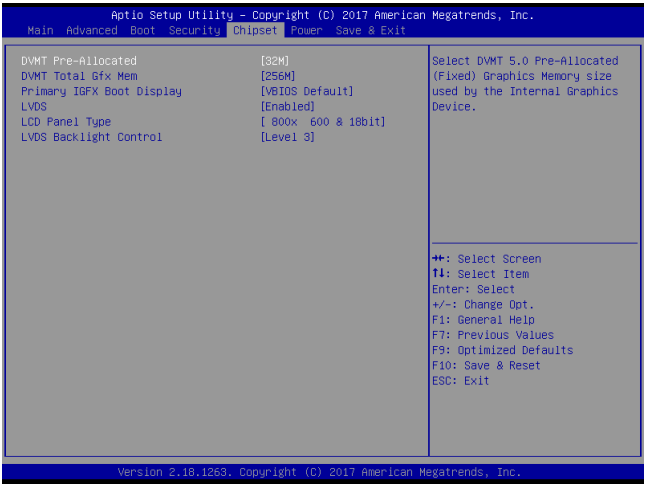
▸Recorder Mode, Resolution 100x31

These settings enable/disable the recorder mode and the resolution 100x31.

▸Putty Keypad

PuTTY is a terminal emulator for Windows. This setting controls the numeric keypad for use in PuTTY.

Chipset



▸DVMT Pre-Allocated

This setting defines the DVMT pre-allocated memory. Pre-allocated memory is the small amount of system memory made available at boot time by the system BIOS for video. Pre-allocated memory is also known as locked memory. This is because it is "locked" for video use only and as such, is invisible and unable to be used by the operating system.

▸DVMT Total Gfx Mem

This setting specifies the memory size for DVMT.

▸Primary IGFX Boot Display

Use the field to select the type of device you want to use as the display(s) of the system.

▸LVDS

This setting enables/disables the LVDS interface.

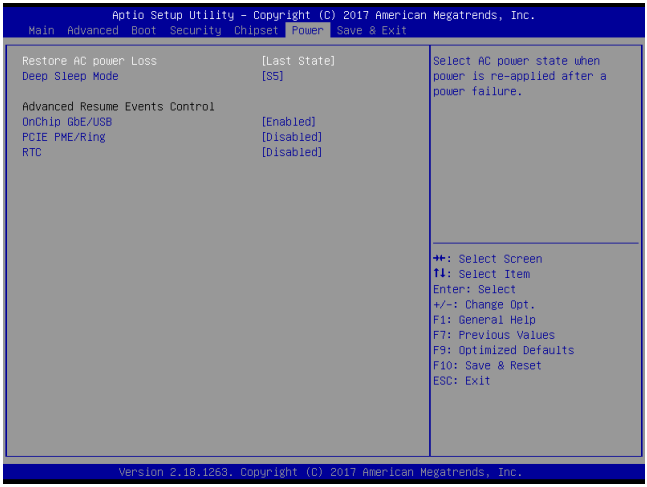
▸LCD Panel Type

This setting specifies the LCD panel type.

▸LVDS Backlight Control

This setting controls the intensity of the LVDS backlight.

Power



▸Restore AC Power Loss

This setting specifies whether your system will reboot after a power failure or interrupt occurs. Available settings are:

[Power Off]	Leaves the computer in the power off state.
[Power On]	Leaves the computer in the power on state.
[Last State]	Restores the system to the previous status before power failure or interrupt occurred.

▸Deep Sleep Mode

The setting enables/disables the Deep S5 power saving mode. S5 is almost the same as G3 Mechanical Off, except that the PSU still supplies power, at a minimum, to the power button to allow return to S0. A full reboot is required. No previous content is retained. Other components may remain powered so the computer can “wake” on input from the keyboard, clock, modem, LAN, or USB device.

**** Advanced Resume Events Control ****

▸OnChip GbE/USB

This field specifies whether the system will be awakened from power saving modes when the activity of USB devices or input signal of onchip LAN is detected.

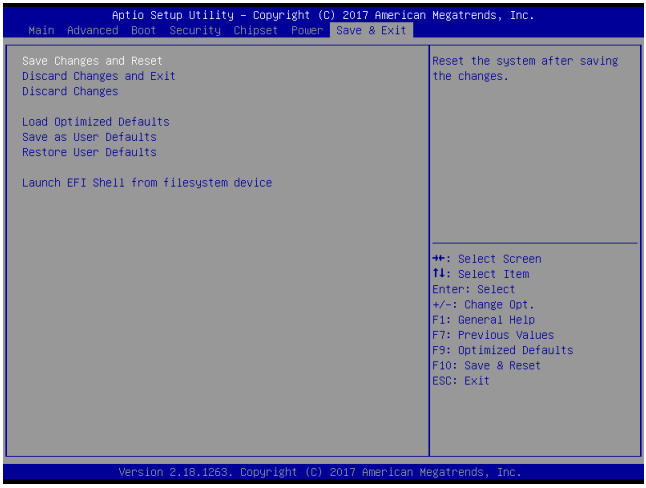
▸**PCIE PME/Ring**

This field specifies whether the system will be awakened from power saving modes when input signals on the serial Ring Indicator (RI) line or input signals of onboard PCIE PME are detected.

▸**RTC**

When [Enabled], your can set the date and time at which the RTC (real-time clock) alarm awakens the system from suspend mode.

Save & Exit



▸**Save Changes and Reset**

Save changes to CMOS and reset the system.

▸**Discard Changes and Exit**

Abandon all changes and exit the Setup Utility.

▸**Discard Changes**

Abandon all changes.

▸**Load Optimized Defaults**

Use this menu to load the default values set by the motherboard manufacturer specifically for optimal performance of the motherboard.

▸**Save as User Defaults**

Save changes as the user's default profile.

▸**Restore User Defaults**

Restore the user's default profile.

▸**Launch EFI Shell from filesystem device**

This setting helps to launch the EFI Shell application from one of the available file system devices.

Appendix
GPIO WDT BKL Programming

This appendix provides WDT (Watch Dog Timer), GPIO (General Purpose Input/ Output) and LVDS Backlight programming guide.

CONTENT

Abstract

Abstract

In this document, code examples based on C programming language are provided for customer interest. **Inportb**, **Outportb**, **Inportl** and **Outportl** are basic functions used for access IO ports and defined as following.

Inportb: Read a single 8-bit I/O port.
Outportb: Write a single byte to an 8-bit port.
Inportl: Reads a single 32-bit I/O port.
Outportl: Write a single long to a 32-bit port.

General Purposed IO

1. General Purposed IO – GPIO/DIO

The associated access method (**EC_ReadByte**, **EC_WriteByte**) are provided in part 5. The GPIO port configuration offset in EC and addresses are listed in the following table:

Name	OFFSET	IO address	Name	OFFSET	IO address
N_GPI0	0xBD	Bit 4	**N_GPO0**	0xBD	Bit 0
N_GPI1	0xBD	Bit 5	**N_GPO1**	0xBD	Bit 1
N_GPI2	0xBD	Bit 6	**N_GPO2**	0xBD	Bit 2
N_GPI3	0xBD	Bit 7	**N_GPO3**	0xBD	Bit 3

1.1 Set output value of GPO

1. Read the value from the OFFSET in EC RAM of GPO.
2. Set the value of GPO address.
3. Write the value back to the OFFSET in EC RAM of GPO.

Example: Set **N_GPO0** output “high”

```
val = EC_ReadByte (0xBD);          // Read value from N_GPO0.
val = val | (1<<0);                // Set N_GPO0 address (bit 0) to 1 (output “high”).
EC_WriteByte (0xBD, val);          // Write back to N_GPO0.
```

Example: Set **N_GPO1** output “low”

```
val = EC_ReadByte (0xBD);          // Read value from N_GPO1.
val = val & (~(1<<1));             // Set N_GPO1 address (bit 1) to 0 (output “low”).
EC_WriteByte (0xBD, val);          // Write back to N_GPO1.
```

1.2 Read input value from GPI

1. Read the value from the OFFSET in EC of GPI.
2. Get the value of GPI address.

Example: Get **N_GPI2** input value.

```
val = EC_ReadByte (0xBD);          // Read value from N_GPI2.
val = val & (1<<6);                // Check N_GPI2 address (bit 6).
if (val)    printf (“Input of  N_GPI2  is High”);
else        printf (“Input of  N_GPI2  is Low”);
```

Watchdog Timer

2. Watchdog Timer – WDT

The watchdog timer unit is in second. Associated access method (**EC_ReadByte** and **EC_WriteByte**) are provided in part 5.

2.1 Set WDT Time

```
EC_WriteByte (0xC5, Time);          // Write WDT time, value 1 to 255.
```

2.2 Enable WDT

```
val = EC_ReadByte (0xC0);           // Read current WDT setting
val = val | 0x04;                   // Enable WDT by set WD_EN (bit 2) to 1.
EC_WriteByte (0xC0, val);           // Write back WDT setting.
```

2.3 Disable WDT

```
val = EC_ReadByte (0xC0);           // Read current WDT setting
val = val & 0xFB;                   // Enable WDT by set WD_EN (bit 2) to 0.
EC_WriteByte (0xC0, val);           // Write back WDT setting.
```

LVDS Backlight Brightness Control

3. LVDS Backlight Brightness Control

The LVDS controller support 17 level of backlight brightness value from 0 (30%) to 16 (100%) and it is accessible through SMBus. The associated access method (**SMBus_ReadByte**, **SMBus_WriteByte**) are provided in part 4.

3.1 Set the Level of LVDS Backlight

1. Write **0xED** into address **0x7F** on SMBus device **0x42**.
2. Write desired backlight level from 0x0 (30%) to 0x10 (100%) into address **0x6E** on SMBus device **0x42**.

Example: Set LVDS backlight level to 0x10 (100%)

```
SMBus_WriteByte (0x42, 0x7F, 0xED);
SMBus_WriteByte (0x42, 0x6E, 0x10);     // Set brightness to 100%
```

3.2 Read the Level of LVDS Backlight

1. Write **0xED** into address **0x7F** on SMBus device **0x42**.
2. Read current backlight level from address **0x6E** on SMBus device **0x42**.

Example: Get LVDS backlight level

```
SMBus_WriteByte (0x42, 0x7F, 0xED);
BKL_Value = SMBus_ReadByte (0x42, 0x6E);
```

SMBus Access

4. SMBus Access

The base address of SMBus must be known before access. The relevant bus and device information are as following.

```
#define IO_SC               0xCF8
#define IO_DA               0xCFC
#define PCIBASEADDRESS      0x80000000
#define PCI_BUS_NUM         0
#define PCI_DEV_NUM         31
#define PCI_FUN_NUM         4
```

4.1 Get SMBus Base Address

```
int SMBUS_BASE;
int DATA_ADDR = PCIBASEADDRESS + (PCI_BUS_NUM<<16) +
                                 (PCI_DEV_NUM<<11) +
                                 (PCI_FUN_NUM<<8);

Outportl (DATA_ADDR + 0x20, IO_SC);
SMBUS_BASE = Inportl (IO_DA) & 0xfffffff0;
```

4.2 SMBus_ReadByte (char DEVID, char OFFSET)

Read the value of **OFFSET** from SMBus device **DEVID**.

```
Outportb (LOWORD (SMBUS_BASE), 0xFE);
Outportb (LOWORD (SMBUS_BASE) + 0x04, DEVID + 1);   // out Base + 04, (DEVID + 1)
Outportb (LOWORD (SMBUS_BASE) + 0x03, OFFSET);      // out Base + 03, OFFSET
Outportb (LOWORD (SMBUS_BASE) + 0x02, 0x48);        // out Base + 02, 48H
mdelay (20);                                        // delay 20ms to let data ready
while ((Inportl (SMBUS_BASE) & 0x01) != 0);         // wait SMBus ready
SMB_DATA = Inportb (LOWORD (SMBUS_BASE) + 0x05);    // input Base + 05
```

4.3 SMBus_WriteByte (char DEVID, char OFFSET, char DATA)

Write **DATA** to **OFFSET** on SMBus device **DEVID**.

```
Outportb (LOWORD (SMBUS_BASE), 0xFE);
Outportb (LOWORD (SMBUS_BASE) + 0x04, DEVID);       // out Base + 04, (DEVID)
Outportb (LOWORD (SMBUS_BASE) + 0x03, OFFSET);      // out Base + 03, OFFSET

Outportb (LOWORD (SMBUS_BASE) + 0x05, DATA);        // out Base + 05, DATA
Outportb (LOWORD (SMBUS_BASE) + 0x02, 0x48);        // out Base + 02, 48H
mdelay (20);                                        // wait 20ms
```

Embedded Controller

5. Embedded Controller – EC Access

The relevant control information are as following.

```
#EC_CMD_PORT      0x66          // EC command port
#EC_DATA_PORT     0x62          // EC data port
#EC_DELAY         100
#EC_STAT_OBF      0x1           // bit 0: OBF
#EC_STAT_IBF      0x2           // bit 1: IBF
```

5.1 WaitPortStatus (char BITS, bool ONOFF)

```
int time=0, tick= EC_DELAY;
bool state;
for (time = 0; time < EC_DELAY*100; time += tick)    // *100 is the loop count to avoid infinite wait
{
    udelay (EC_DELAY);                               // Delay 100us to let data ready
    char data= Inportb (EC_CMD_PORT);
    state = ((data & BITS) !=0 );                    // Check EC status of desired bits
    if (state == ONOFF) {
        break;
    }
}
```

5.2 EC_ReadByte (char OFFSET)

Read the value from **OFFSET** of EC RAM.

```
WaitPortStatus (EC_STAT_IBF, false);          // Wait IBF = 0
Outportb (EC_CMD_PORT, 0x80);                 // 0x80: EC read command
WaitPortStatus (EC_STAT_IBF, false);          // Wait IBF = 0
Outportb (EC_DATA_PORT, OFFSET);              // Write OFFSET to EC_DATA_PORT
WaitPortStatus (EC_STAT_OBF, true);           // Wait OBF = 1
EC_DATA = Inportb (EC_DATA_PORT);             // Get value from EC_DATA_PORT
```

5.3 EC_WriteByte (char OFFSET, char DATA)

Write **DATA** to **OFFSET** of EC RAM.

```
WaitPortStatus (EC_STAT_IBF, false);          // Wait IBF = 0
Outportb (EC_CMD_PORT, 0x81);                 // 0x81: EC write command
WaitPortStatus (EC_STAT_IBF, false);          // Wait IBF = 0
Outportb (EC_DATA_PORT, OFFSET);              // Write OFFSET to EC_DATA_PORT
WaitPortStatus (EC_STAT_IBF, false);          // Wait IBF = 0
Outportb (EC_DATA_PORT, DATA);                // Write DATA to EC_DATA_PORT
WaitPortStatus (EC_STAT_IBF, false);          // Wait IBF = 0
```