ET876 Series

COM Express Type 10 Module

With Intel® Atom™ x7/x5 SoC

User's Manual

Version 1.0
(June 2020)

Compliance

CE

This product has passed CE tests for environmental specifications and limits. This product is in accordance with the directives of the European Union (EU). In a domestic environment, this product may cause radio interference in which case users may be required to take adequate measures.

FC

This product has been tested and found to comply with the limits for a Class B device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with manufacturer's instructions, may cause harmful interference to radio communications.

WEEE

This product must not be disposed of as normal household waste, in accordance with the EU directive of for waste electrical and electronic equipment (WEEE - 2012/19/EU). Instead, it should be disposed of by returning it to a municipal recycling collection point. Check local regulations for disposal of electronic products.

Green IBASE

This product is compliant with the current RoHS restrictions and prohibits use of the following substances in concentrations exceeding 0.1% by weight (1000 ppm) except for cadmium, limited to 0.01% by weight (100 ppm).

- Lead (Pb)
- Mercury (Hg)
- Cadmium (Cd)
- Hexavalent chromium (Cr6+)
- Polybrominated biphenyls (PBB)
- Polybrominated diphenyl ether (PBDE)

Important Safety Information

Carefully read the precautions before using the board.

Environmental conditions:

- Use this product in environments with ambient temperatures between -20˚C and 60˚C.
- Do not leave this product in an environment where the storage temperature may be below 40° C or above 85° C. To prevent from damages, the product must be used in a controlled environment.

Care for your IBASE products:

- Before cleaning the PCB, unplug all cables and remove the battery.
- Clean the PCB with a circuit board cleaner, degreaser or use cotton swabs and alcohol.
- Vacuum the dust with a computer vacuum cleaner to prevent the fan from being clogged.

WARNING

Attention during use:

- Do not use this product near water.
- Do not spill water or any other liquids on this product.
- Do not place heavy objects on the top of this product.

Anti-static precautions

- Wear an anti-static wrist strap to avoid electrostatic discharge.
- Place the PCB on an anti-static kit or mat.
- Hold the edges of PCB when handling.
- Touch the edges of non-metallic components of the product instead of the surface of the PCB.
- Ground yourself by touching a grounded conductor or a grounded bit of metal frequently to discharge any static.

CAUTION

Danger of explosion if the internal lithium-ion battery is replaced by an incorrect type. Replace only with the same or equivalent type recommended by the manufacturer. Dispose of used batteries according to the manufacturer's instructions or recycle them at a local recycling facility or battery collection point.

Warranty Policy

- **IBASE standard products:**

  24-month (2-year) warranty from the date of shipment. If the date of shipment cannot be ascertained, the product serial numbers can be used to determine the approximate shipping date.

- **3rd-party parts:**

  12-month (1-year) warranty from delivery for the 3rd-party parts that are not manufactured by IBASE, such as CPU, CPU cooler, memory, storage devices, power adapter, panel and touchscreen.

* PRODUCTS, HOWEVER, THAT FAIL DUE TO MISUSE, ACCIDENT, IMPROPER INSTALLATION OR UNAUTHORIZED REPAIR SHALL BE TREATED AS OUT OF WARRANTY AND CUSTOMERS SHALL BE BILLED FOR REPAIR AND SHIPPING CHARGES.

Technical Support & Services

1. Visit the IBASE website at www.ibase.com.tw to find the latest information about the product.
2. If you need any further assistance from your distributor or sales representative, prepare the following information of your product and elaborate upon the problem.
   - Product model name
   - Product serial number
   - Detailed description of the problem
   - The error messages in text or in screenshots if there is any
   - The arrangement of the peripherals
   - Software in use (such as OS and application software, including the version numbers)
3. If repair service is required, you can download the RMA form at http://www.ibase.com.tw/english/Supports/RMAService/. Fill out the form and contact your distributor or sales representative.

iBASE

Table of Contents

This page is intentionally left blank.

Chapter 1
General Information

The information provided in this chapter includes:

- Features
- Packing List
- Optional Accessories
- Specifications
- Block Diagram
- Product View
- Board Dimensions

1.1 Introduction

ET876 is a COM Express Type 10 module with Intel® Atom™ x7/x5 (QC / DC) processor. It comes with type 10 pinouts and complies with the PICMG COM.0 Rev.3.0 specifications for ultra-low power consumption. This product features LPDDR4 memory slots, and provides DDI display and LVDS or eDP interface connection, and high-speed I/O such as USB 3.0, SATA III and PCIe.

Photo of ET876

1.2 Features

- COM Express module type 10 with onboard Intel® Atom™ x7 or x5 (QC / DC)
- Onboard DDR3L Max. 4 GB, with-ECC
- Intel® I210IT PCIe Gigabit LAN
- LVDS or eDP, 2 x USB 3.0, 8 x USB 2.0 via the carrier board (IP417)
- 4 x PCIe (x1) lanes
- Compliant with TPM 2.0 and eMMC 5.0 (Optional)
- Configurable watchdog timer
- Wide-range operating temperature

1.3 Packing List

Your product package should include the items listed below. If any of the items below is missing, contact the distributor or dealer from whom you purchased the product.

- ET876 COM Express Module
- DVD Disk (including drivers and flash memory utility)
- This User's Manual

1.4 Optional Accessories

IBASE provides optional accessories as follows. Please contact us or your dealer if you need any.

- Heat spreader (HSET876-X-1 for ET876-X7/ X5Q/ X5)

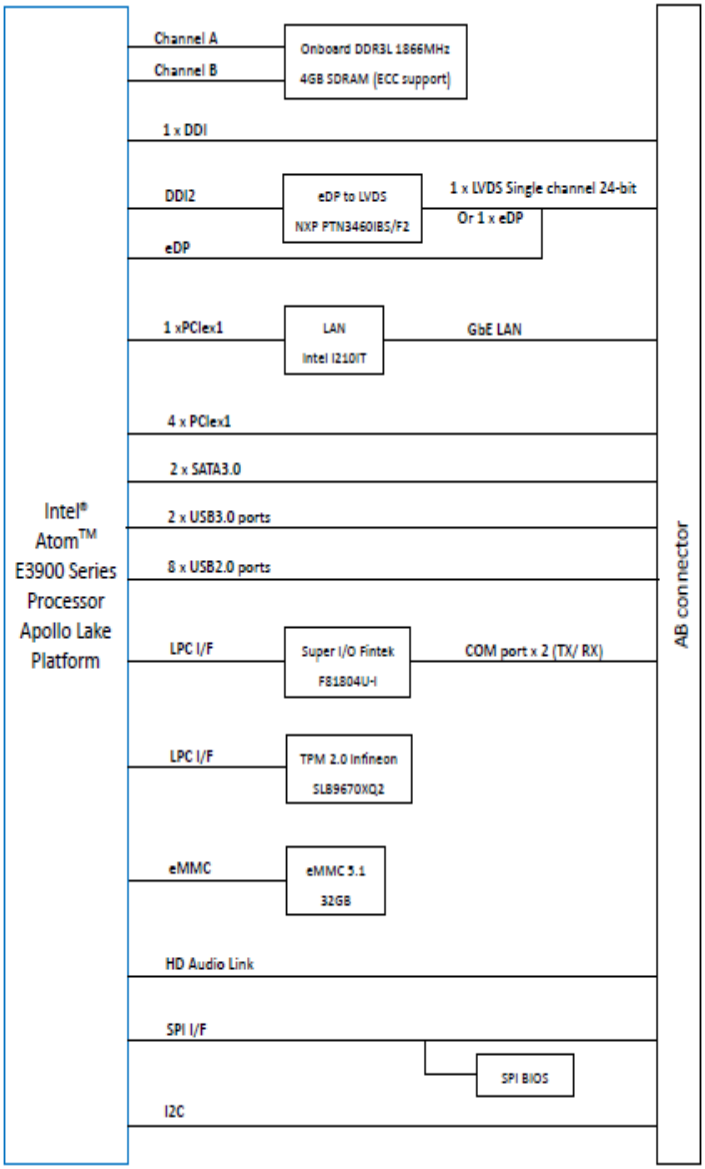
1.5 Specifications

Product Name	ET876
Operating System	• Windows 10 (64-bit) • Linux (Ubuntu)
CPU	• Intel® Atom™ QC x7 E3950 at 2 GHz, 2MB cache w/ ECC • Intel® Atom™ QC x5 E3940 at 1.8 GHz, 2MB cache w/ECC • Intel® Atom™ DC x5 E3930 at 1.8 GHz, 2MB cache w/ECC
Chipset	Integrated
Memory	Onboard DDR3L 1600 MHz, dual channel, expandable up to 4 GB, with ECC
Graphics	Intel® SoC integrated Gen9-LP graphics
Display	• 1 x DDI • 1 x eDP (4096 x 2160 at 60 Hz) or 1 x LVDS (1920 x 1200 at 60 Hz)

Audio	Intel® Atom™ SoC built-in HD Audio
Network	Intel® I210IT PCIe GbE LAN
Super I/O	Fintek F81804U-I
Max. Power Requirement	+12V, +5VSB
TPM	2.0
eMMC	5.0, up to 32 GB (Optional)
I²C	Supported
Watchdog Timer	Yes (256 segments, 0, 1, 2…255 sec / min)
BIOS	AMI BIOS
H/W Monitor	Yes
Dimensions	84 x 55 mm (3.35” x 2.17”)
RoHS	Yes
Certification	CE, FCC Class B
I/O Ports (via carrier board)	
Display	1 x DDI for LVDS or eDP (Optional)
LAN	1 x GbE LAN
USB	• 2 x USB 3.0 • 8 x USB 2.0
Serial	2 x UART (TX and RX only)
SATA	2 x SATA III via carrier board
Expansion Slots	4 x PCIe (x1) lanes
Environment	
Temperature	• Operating: **With Intel® Atom™ x7/x5:** -40 ~ 85°C (-40 ~ 185°F) • Storage: -40 ~ 90 °C (-40 ~ 194°F)
Relative Humidity	90 %, non-condensing at 60°C

All specifications are subject to change without prior notice.

1.6 Block Diagram



1.7 Product View

Top View

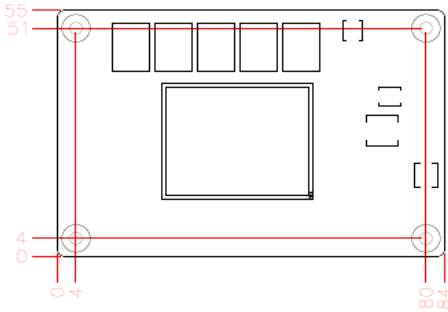
Bottom View

Photos of ET876

* The photos above are for reference only. Some minor components may differ.

1.8 Dimensions

Unit: mm

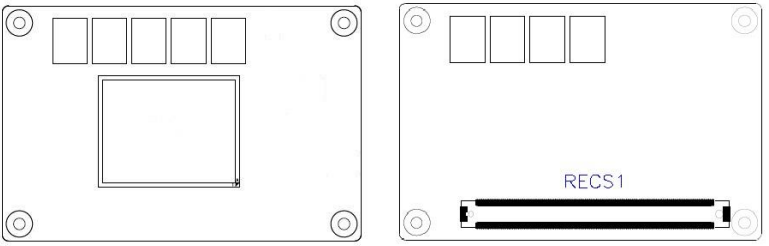


Chapter 2
Hardware Configuration

This section provides information on jumper settings and connectors on the ET876 in order to set up a workable system. On top of that, you will also need to install crucial pieces such as the CPU and the memory before using the product. The topics covered are:

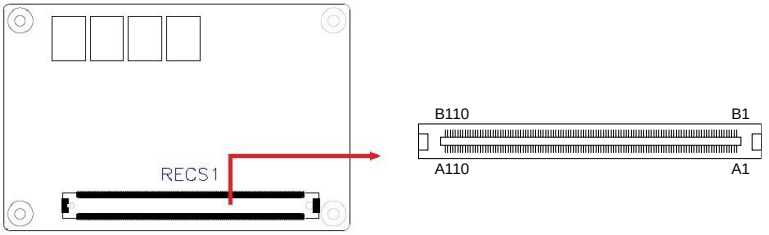
- Connector location
- Information of connector

2.1 Connector Location



Board diagram of ET876

2.1.1 COMe Module Type 10 Connector (RECS1)



Row A		Row B		Row A		Row B	
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A1	GND (FIXED)	B1	GND (FIXED)	A56	RSVD	B56	RSVD
A2	GBE0_MDI3-	B2	GBE0_ACT#	A57	GND	B57	GPO2
A3	GBE0_MDI3+	B3	LPC_FRAME#	A58	PCIE_TX3+	B58	PCIE_RX3+
A4	GBE0_LINK100#	B4	LPC_AD0	A59	PCIE_TX3-	B59	PCIE_RX3-
A5	GBE0_LINK1000#	B5	LPC_AD1	A60	GND (FIXED)	B60	GND (FIXED)
A6	GBE0_MDI2-	B6	LPC_AD2	A61	PCIE_TX2+	B61	PCIE_RX2+
A7	GBE0_MDI2+	B7	LPC_AD3	A62	PCIE_TX2-	B62	PCIE_RX2-
A8	GBE0_LINK#	B8	LPC_DRQ0#	A63	GPI1	B63	GPO3
A9	GBE0_MDI1-	B9	LPC_DRQ1#	A64	PCIE_TX1+	B64	PCIE_RX1+
A10	GBE0_MDI1+	B10	LPC_CLK	A65	PCIE_TX1-	B65	PCIE_RX1-
A11	GND (FIXED)	B11	GND (FIXED)	A66	GND	B66	WAKE0#
A12	GBE0_MDI0-	B12	PWRBTN#	A67	GPI2	B67	WAKE1#
A13	GBE0_MDI0+	B13	SMB_CK	A68	PCIE_TX0+	B68	PCIE_RX0+
A14	GBE0_CTREF	B14	SMB_DAT	A69	PCIE_TX0-	B69	PCIE_RX0-
A15	SUS_S3#	B15	SMB_ALERT#	A70	GND (FIXED)	B70	GND (FIXED)
A16	SATA0_TX+	B16	SATA1_TX+	A71	LVDS_A0+	B71	DD 0_PAIR0+
A17	SATA0_TX-	B17	SATA1_TX-	A72	LVDS_A0-	B72	DD 0_PAIR0-

Row A		Row B		Row A		Row B	
Pin	Signal	Pin	Signal	Pin	Signal	Pin	Signal
A18	SUS_S4#	B18	SUS_STAT#	A73	LVDS_A1+	B73	DD 0_PAIR1+
A19	SATA0_RX+	B19	SATA1_RX+	A74	LVDS_A1-	B74	DD 0_PAIR1-
A20	SATA0_RX-	B20	SATA1_RX-	A75	LVDS_A2+	B75	DD 0_PAIR2+
A21	GND (FIXED)	B21	GND (FIXED)	A76	LVDS_A2-	B76	DD 0_PAIR2-
A22	USB_SSRX0-	B22	USB_SSTX0-	A77	LVDS_VDD_EN	B77	DD 0_PAIR4+
A23	USB_SSRX0+	B23	USB_SSTX0+	A78	LVDS_A3+	B78	DD 0_PAIR4-
A24	SUS_S5#	B24	PWR_OK	A79	LVDS_A3-	B79	LVDS_BKLT_EN
A25	USB_SSRX1	B25	USB_SSTX1	A80	GND (FIXED)	B80	GND (FIXED)
A26	USB_SSRX1	B26	USB_SSTX1	A81	LVDS_A_CK+	B81	DD 0_PAIR3+
A27	BATLOW#	B27	WDT	A82	LVDS_A_CK-	B82	DD 0_PAIR3-
A28	(S)ATA_ACT#	B28	HDA_SDIN2	A83	LVDS_I2C_CK	B83	LVDS_BKLT_CTRL
A29	HDA_SYNC	B29	HDA_SDIN1	A84	LVDS_I2C_DAT	B84	VCC_5V_SBY
A30	HDA_RST#	B30	HDA_SDIN0	A85	GPI3	B85	VCC_5V_SBY
A31	GND (FIXED)	B31	GND (FIXED)	A86	RSVD	B86	VCC_5V_SBY
A32	HDA_BITCLK	B32	SPKR	A87	eDP_HPD	B87	VCC_5V_SBY
A33	HDA_SDOUT	B33	I2C_CK	A88	PCIE_CLK_REF+	B88	BIOS_DIS1#
A34	BIOS_DIS0#	B34	I2C_DAT	A89	PCIE_CLK_REF-	B89	0DI0_HPD
A35	THRMTRIP#	B35	THRM#	A90	GND (FIXED)	B90	GND (FIXED)
A36	USB6-	B36	USB7-	A91	SPI_POWER	B91	DD 0_PAIR5+
A37	USB6+	B37	USB7+	A92	SPI_MISO	B92	DD 0_PAIR5-
A38	USB_6_7_OC#	B38	USB_4_5_OC#	A93	GPO0	B93	DD 0_PAIR6+
A39	USB4-	B39	USB5-	A94	SPI_CLK	B94	DD 0_PAIR6-
A40	USB4+	B40	USB5+	A95	SPI_MOSI	B95	DD 0_DDC_AUX_SEL
A41	GND (FIXED)	B41	GND (FIXED)	A96	TPM_PP	B96	USB7_HOST_PRSNT
A42	USB2-	B42	USB3-	A97	TYPE10#	B97	SPI_CS#
A43	USB2+	B43	USB3+	A98	SER0_TX	B98	DD 0_CTRLCLK_AUX+
A44	USB_2_3_OC#	B44	USB_0_1_OC#	A99	SER0_RX	B99	DD 0_CTRLDATA_AUX-
A45	USB0-	B45	USB1-	A100	GND (FIXED)	B100	GND (FIXED)
A46	USB0+	B46	USB1+	A101	SER1_TX	B101	FAN_PWMOUT
A47	VCC_RTC	B47	ESPI_EN#	A102	SER1_RX	B102	FAN_TACHIN
A48	RSVD	B48	USB0_HOST_PRSNT	A103	LID#	B103	SLEEP#
A49	GBE0_SDP	B49	SYS_RESET#	A104	VCC_12V	B104	VCC_12V
A50	LPC_SERIRQ	B50	CB_RESET#	A105	VCC_12V	B105	VCC_12V
A51	GND (FIXED)	B51	GND (FIXED)	A106	VCC_12V	B106	VCC_12V
A52	RSVD	B52	RSVD	A107	VCC_12V	B107	VCC_12V
A53	RSVD	B53	RSVD	A108	VCC_12V	B108	VCC_12V
A54	GPI0	B54	GPO1	A109	VCC_12V	B109	VCC_12V
A55	RSVD	B55	RSVD	A110	GND (FIXED)	B110	GND (FIXED)

This page is intentionally left blank.

Chapter 3
Drivers Installation

This chapter introduces installation of the following drivers:

- Intel® Chipset Software Installation Utility
- Graphics Driver
- HD Audio Driver
- Intel® Trusted Execution Engine Drivers
- Intel® Serial I/O Drivers
- LAN Driver

3.1 Introduction

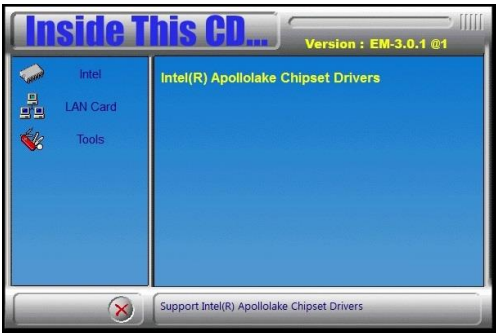
This section describes the installation procedures for software and drivers. The software and drivers are included with the motherboard. If you find anything missing, please contact the distributor where you made the purchase. The contents of this section include the following:

Note: After installing your Windows operating system, you must install the Intel® Chipset Software Installation Utility first before proceeding with the drivers installation.

3.2 Intel® Chipset Software Installation Utility

The Intel® Chipset drivers should be installed first before the software drivers to install INF files for Plug & Play function for Intel chipset components. Follow the instructions below to complete the installation.

1. Insert the disk enclosed in the package with the board. Click **Intel** on the left pane and then **Intel(R) Apollolake Chipset Drivers** on the right pane.

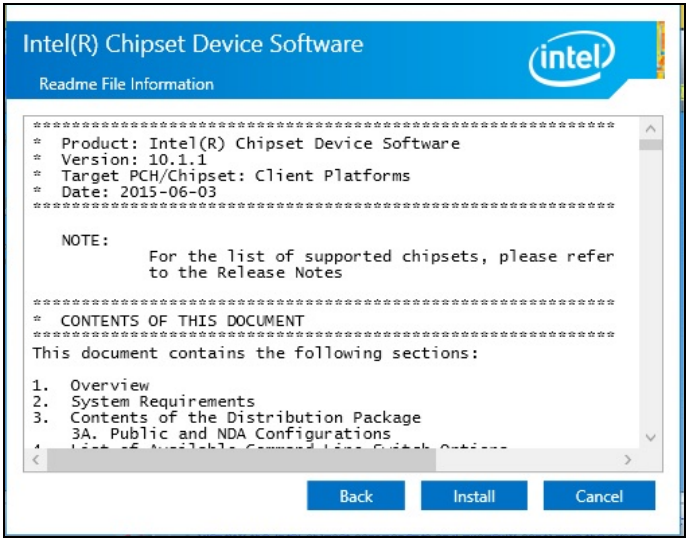


2. Click **Intel(R) Chipset Software Installation Utility**.

3. When the *Welcome* screen to the Intel® Chipset Device Software appears, click **Next** to continue.

4. Click **Yes** to accept the software license agreement and proceed with the installation process.

5. On the *Readme File Information* screen, click **Install** for installation.

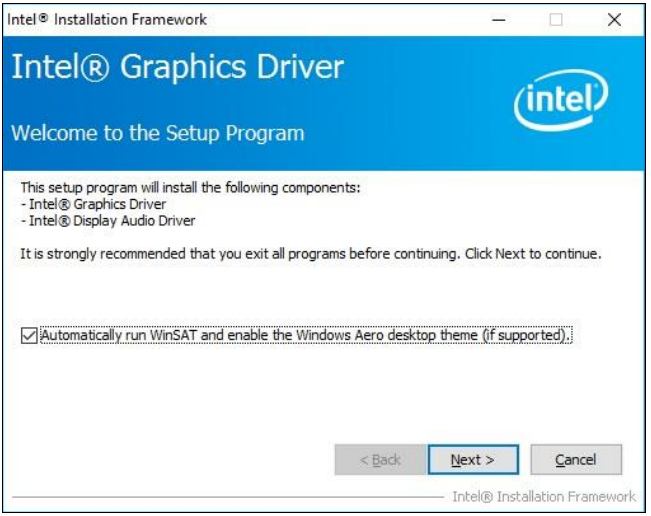


6. When the driver is completely installed, restart the computer for changes to take effect.

3.3 Graphics Driver Installation

1. Click **Intel(R) Apollolake Graphics Driver**.

2. When the *Welcome* screen appears, click **Next** to continue.

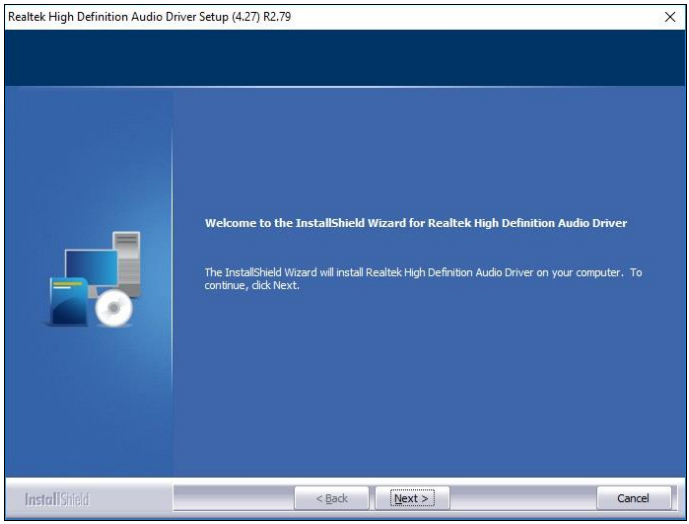


3. Click **Yes** to accept the license agreement and click **Next** until the installation starts.
4. Read the *Readme File Information* and then click **Next** until the installation starts.
5. Choose a destination folder for installation.
6. When the driver is completely installed, click **Finish** and restart the computer for changes to take effect.

3.4 HD Audio Driver Installation

1. Click **Realtek High Definition Audio Driver**.

2. On the *Welcome* screen of the InstallShield Wizard, click **Next**.

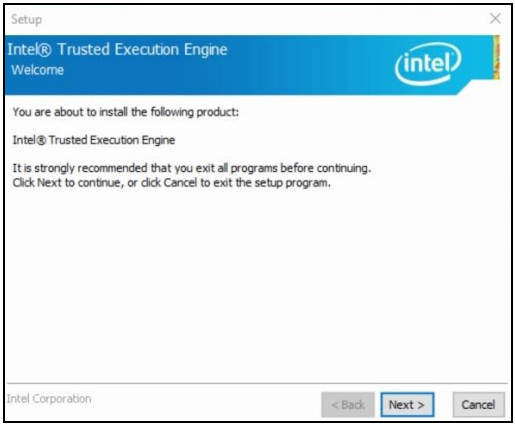


3. Click **Next** until the installation starts.
4. When the driver is completely installed, restart the computer for changes to take effect.

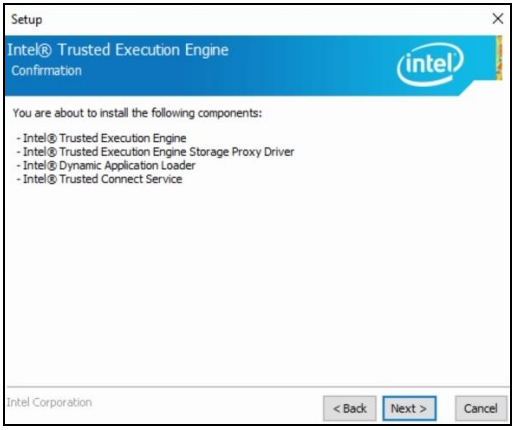
3.5 Intel® Trusted Execution Engine Drivers

1. Click **Intel(R) TXE Drivers**.

2. When the *Welcome* screen appears, click **Next**.



3. Accept the license agreement and click **Next** until the installation starts.

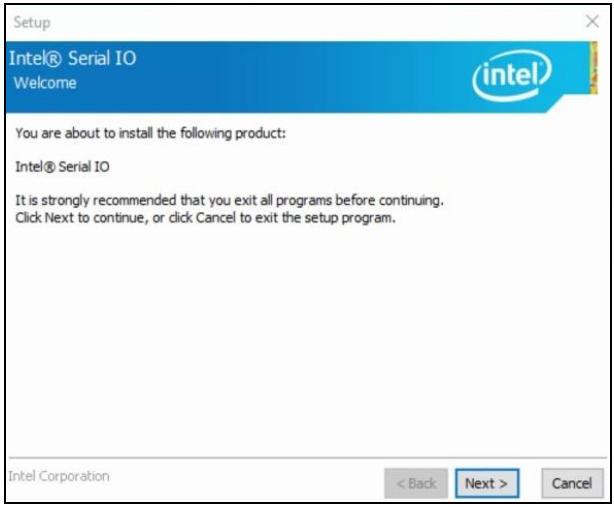


4. As the driver has been sccessfully installed, restart the computer for changes to take effect.

3.6 Intel® Serial IO Drivers

1. Click **Intel(R) Serial IO Drivers**.

2. When the *Welcome* screen to the InstallShield Wizard appears, click **Next**.

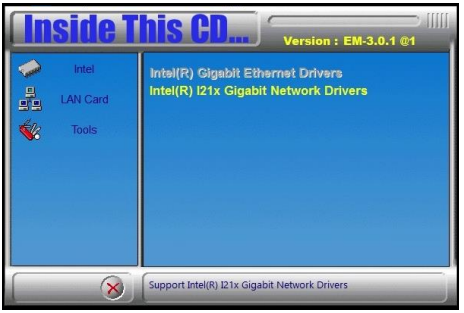


3. Accept the license agreement and click **Next**.
4. After reading the *Readme File Information*, click **Next** for installation.
5. As the driver has been sccessfully installed, restart the computer for changes to take effect.

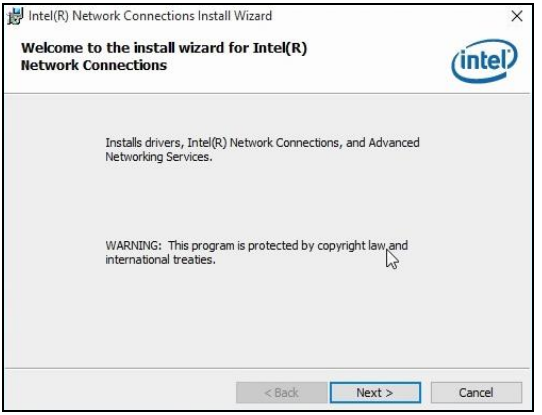
3.7 LAN Driver Installation

1. Click **LAN Card** on the left pane and then **Intel LAN Controller Drivers** on the right pane.

1. Click **Intel(R) I21x Gigabit Network Drivers.**.

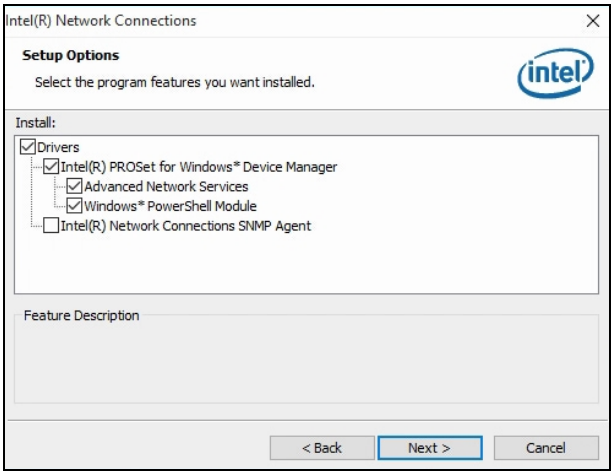


2. When the *Welcome* screen appears, click **Next**.



3. Accept the license agreement and click **Next**.

4. On the *Setup Options* screen, tick the checkbox to select the desired driver(s) for installation. Then click **Next** to continue.



5. The wizard is ready for installation. Click **Install**.

6. As the installation is complete, restart the computer for changes to take effect.

This page is intentionally left blank.

Chapter 4
BIOS Setup

This chapter describes the different settings available in the AMI BIOS that comes with the board. The topics covered in this chapter are as follows:

- Main Settings
- Advanced Settings
- Chipset Settings
- Security Settings
- Boot Settings
- Save & Exit

4.1 Introduction

The BIOS (Basic Input/Output System) installed in the ROM of your computer system supports Intel® processors. The BIOS provides critical low-level support for standard devices such as disk drives, serial ports and parallel ports. It also provides password protection as well as special support for detailed fine-tuning of the chipset controlling the entire system.

4.2 BIOS Setup

The BIOS provides a Setup utility program for specifying the system configurations and settings. The BIOS ROM of the system stores the Setup utility. When you turn on the computer, the BIOS is immediately activated. Press the <Del> key immediately allows you to enter the Setup utility. If you are a little bit late pressing the <Del> key, POST (Power On Self Test) will continue with its test routines, thus preventing you from invoking the Setup.

If you still need to enter Setup, restart the system by pressing the "Reset" button or simultaneously pressing the <Ctrl>, <Alt> and <Delete> keys. You can also restart by turning the system Off and back On again.

The following message will appear on the screen:

```
Press  <DEL>  to  Enter  Setup
```

In general, press the arrow keys to highlight items, <Enter> to select, the <PgUp> and <PgDn> keys to change entries, <F1> for help, and <Esc> to quit.

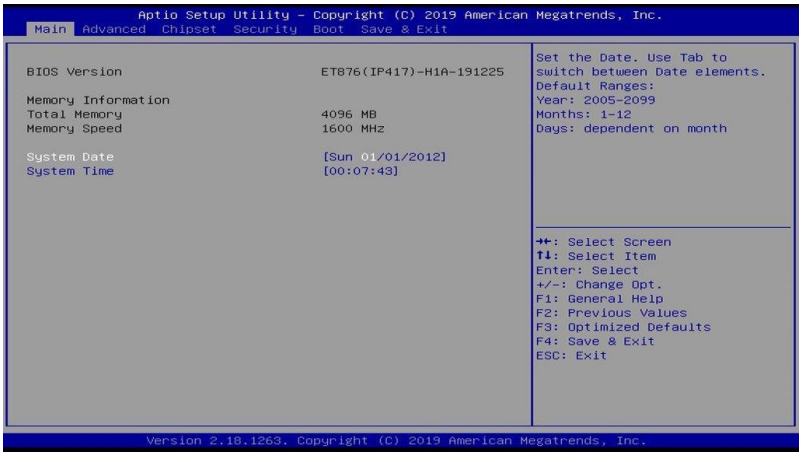
When you enter the BIOS Setup utility, the *Main Menu* screen will appear on the screen. The Main Menu allows you to select from various setup functions and exit choices.

Warning: It is strongly recommended that you avoid making any changes to the chipset defaults.

These defaults have been carefully chosen by both AMI and your system manufacturer to provide the absolute maximum performance and reliability. Changing the defaults could make the system unstable and crash in some cases.

Note: The content of BIOS Setup is on the basis of the model ET876-X7LV8G.

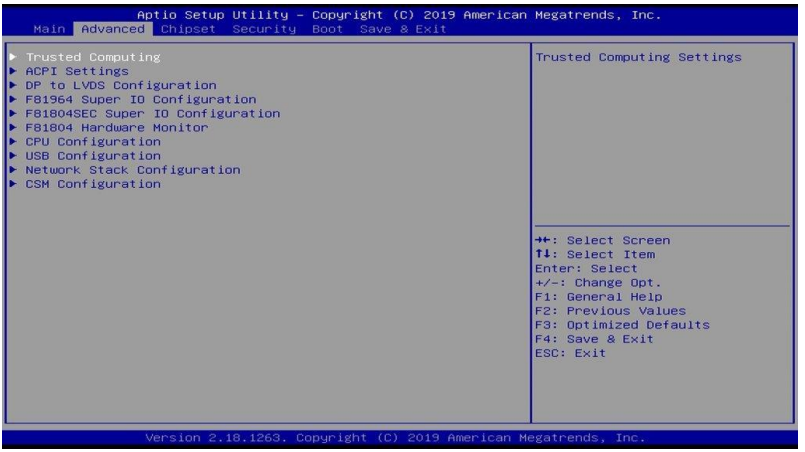
4.3 Main Settings



BIOS Setting	Description
System Date	Sets the date. Use the <Tab> key to switch between the data elements.
System Time	Set the time. Use the <Tab> key to switch between the data elements.

4.4 Advanced Settings

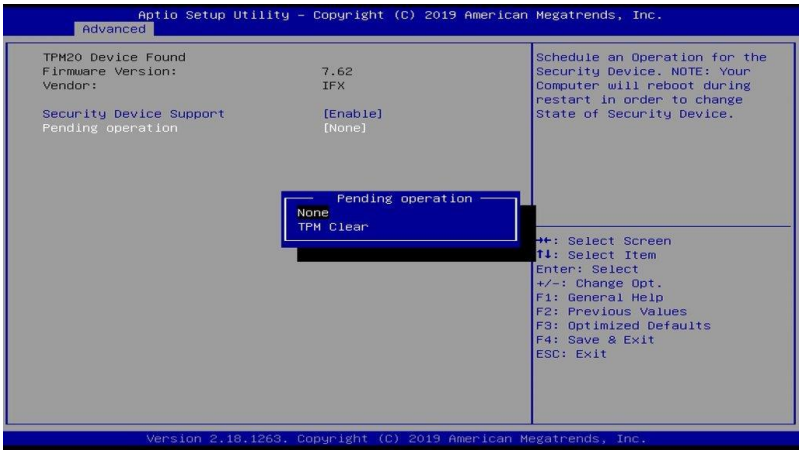
This section allows you to configure, improve your system and allows you to set up some system features according to your preference.



BIOS Setting	Description
Trusted Computing	Trusted computing settings.
ACPI Settings	Displays system ACPI parameters.
DP to LVDS Configuration [1]	Configures eDP to LVDS (eDP/DP).
F81964 Super IO Configuration	Displays super IO chip parameters.
F81804SEC Super IO Configuration	Displays super IO chip parameters.
F81804 Hardware Monitor	Shows super IO monitor hardware status.
CPU Configuration	Displays CPU configuration parameters.
USB Configuration	Displays USB configuration parameters.
Network Stack Configuration	Netowrk Stack settings.
CSM Configuration	Enables / Disables option ROM execution settings, etc.

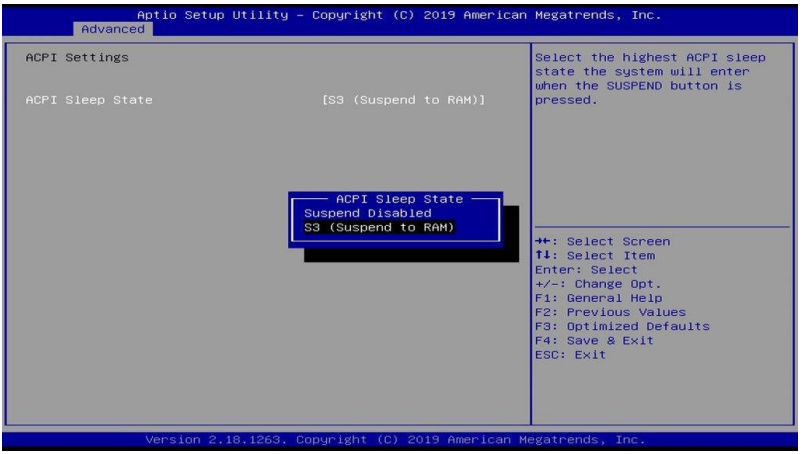
[1]: DP to LVDS Configuration is available for ET876-X7LV8G and ET876-420LVM8G.

4.4.1 Trusted Computing



BIOS Setting	Description
Security Device Support	Enables / Disables BIOS support for security device. OS will not show security device. TCG EFI protocol and INTIA interface will not be available.
Pending operation	Schedule an operation for the security device. Note: Your computer will reboot during restart in order to change state of security device. Options: None, TPM Clear

4.4.2 ACPI Settings



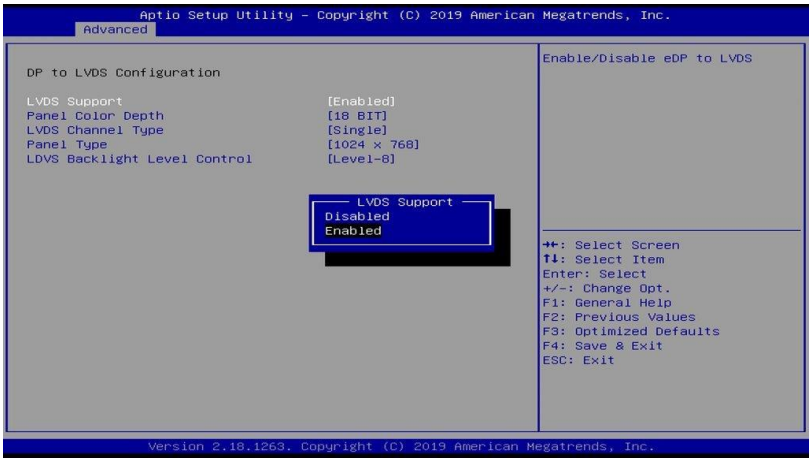
Setting	Description
ACPI Sleep State	Selects an ACPI sleep state (Suspend Disabled or S3) where the system will enter when the Suspend button is pressed.

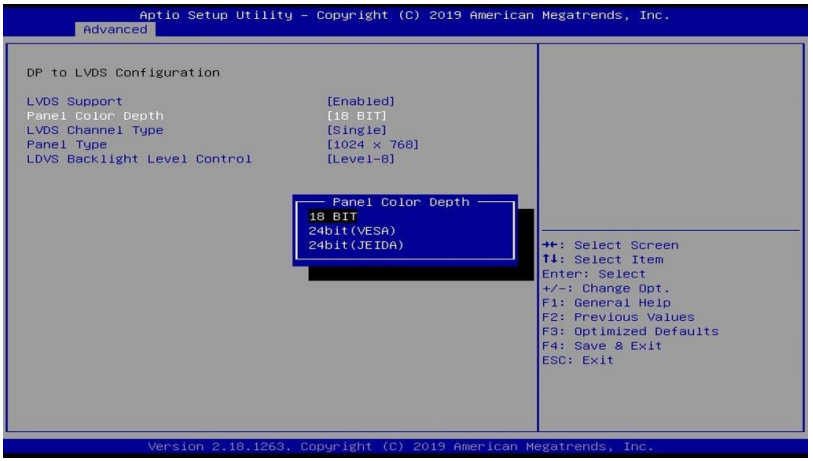
4.4.3 DP to LVDS Configuration

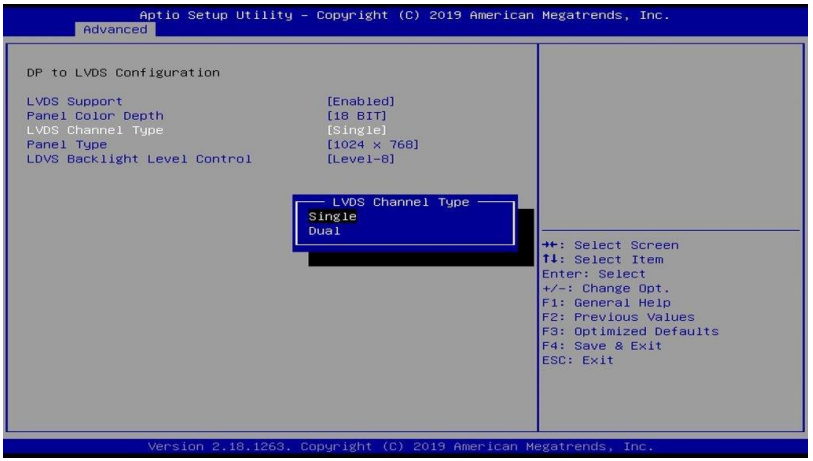
Note: DP to LVDS Configuration is only available for ET876-X7LV8G & ET876-420LVM8G.

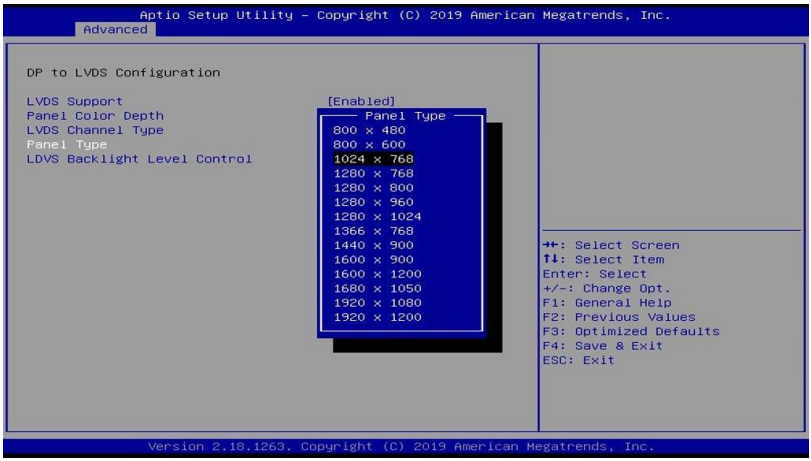
BIOS Setting	Description
LVDS Support	Enables / Disables eDP to LVDS.

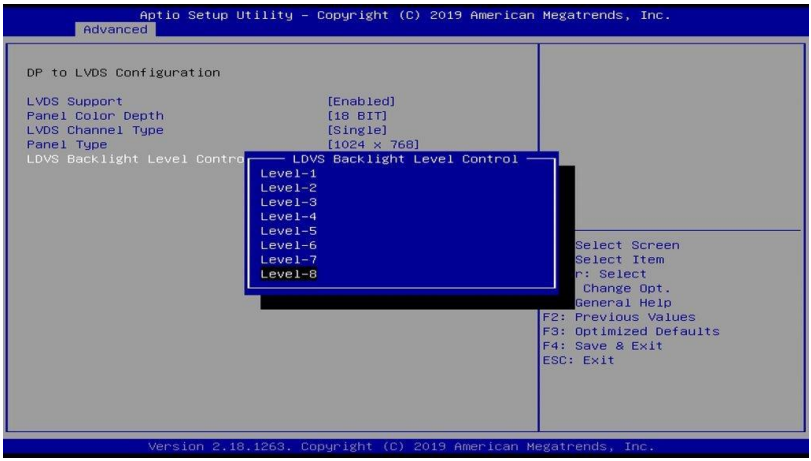
Below are the settings when LVDS Support is enabled.



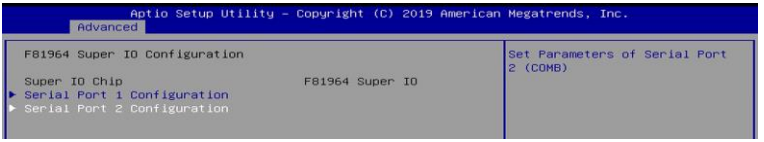

Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Advanced
DP to LVDS Configuration
LVDS Support [Enabled]
Panel Color Depth [18 BIT]
LVDS Channel Type [Single]
Panel Type [1024 x 768]
LDVS Backlight Level Control [Level-8]
Panel Color Depth
18 BIT
24bit(VESA)
24bit(JEIDA)
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.18.1263. Copyright (C) 2019 American Megatrends, Inc.


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Advanced
DP to LVDS Configuration
LVDS Support [Enabled]
Panel Color Depth [18 BIT]
LVDS Channel Type [Single]
Panel Type [1024 x 768]
LDVS Backlight Level Control [Level-8]
LVDS Channel Type
Single
Dual
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.18.1263. Copyright (C) 2019 American Megatrends, Inc.


Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Advanced
DP to LVDS Configuration
LVDS Support [Enabled]
Panel Color Depth
LVDS Channel Type
Panel Type
LDVS Backlight Level Control
Panel Type
800 × 480
800 × 600
1024 × 768
1280 × 768
1280 × 800
1280 × 960
1280 × 1024
1366 × 768
1440 × 900
1600 × 900
1600 × 1200
1680 × 1050
1920 × 1080
1920 × 1200
→←: Select Screen
↑↓: Select Item
Enter: Select
+/-: Change Opt.
F1: General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.18.1263. Copyright (C) 2019 American Megatrends, Inc.

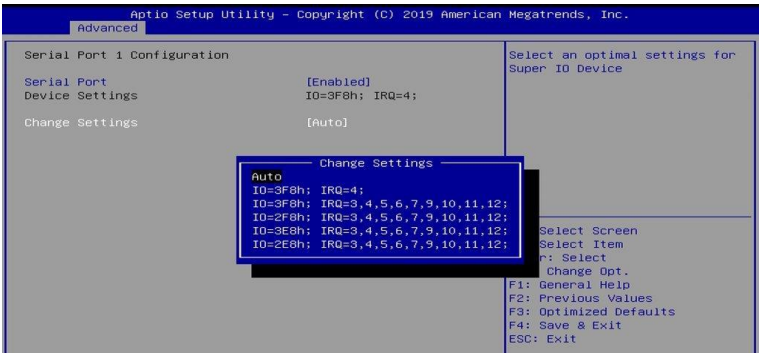

Aptio Setup Utility – Copyright (C) 2019 American Megatrends, Inc.
Advanced
DP to LVDS Configuration
LVDS Support [Enabled]
Panel Color Depth [18 BIT]
LVDS Channel Type [Single]
Panel Type [1024 × 768]
LDVS Backlight Level Contro
LDVS Backlight Level Control
Level-1
Level-2
Level-3
Level-4
Level-5
Level-6
Level-7
Level-8
Select Screen
Select Item
r: Select
Change Opt.
General Help
F2: Previous Values
F3: Optimized Defaults
F4: Save & Exit
ESC: Exit
Version 2.18.1263. Copyright (C) 2019 American Megatrends, Inc.

4.4.4 F81964 Super IO Configuration

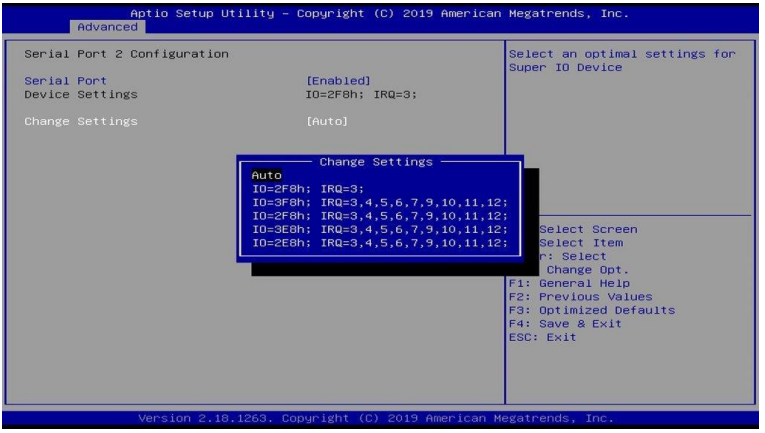


BIOS Setting	Description
Serial Port 1 Configuration	Set parameters of Serial Port 1 (COMA).
Serial Port 2 Configuration	Set parameters of Serial Port 1 (COMB).

4.4.4.1. Serial Port 1 Configuration



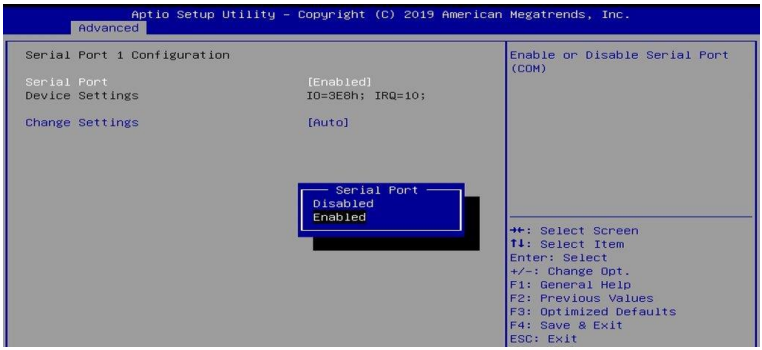
4.4.4.2. Serial Port 2 Configuration

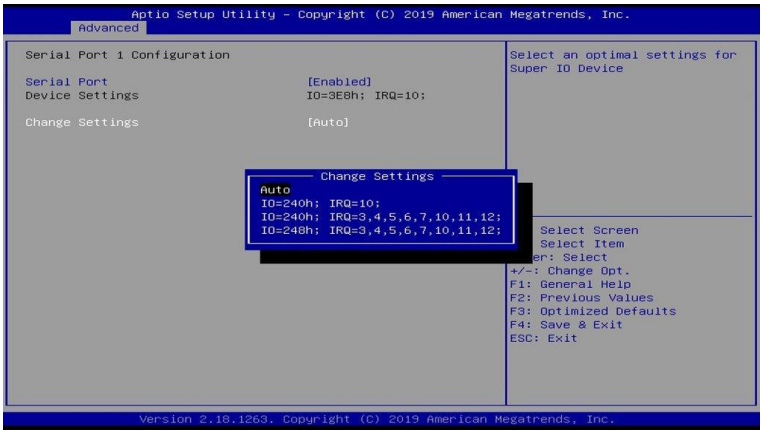


4.4.5 F81804SEC Super IO Configuration

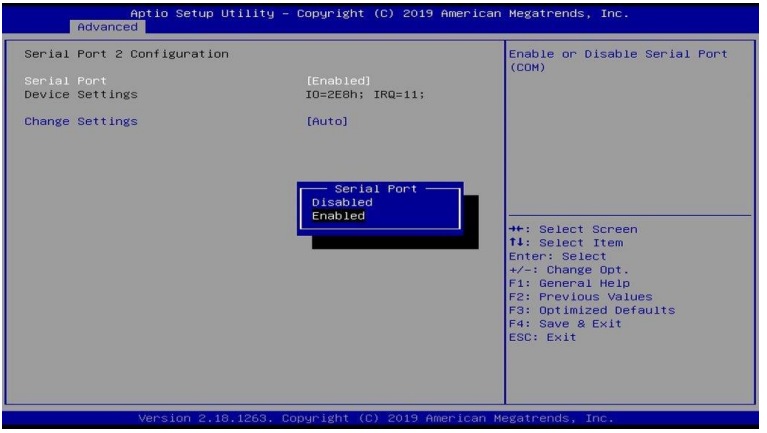
BIOS Setting	Description
Serial Port 1 Configuration	Set parameters of Serial Port 1 (COMA).
Serial Port 2 Configuration	Set parameters of Serial Port 2 (COMB).

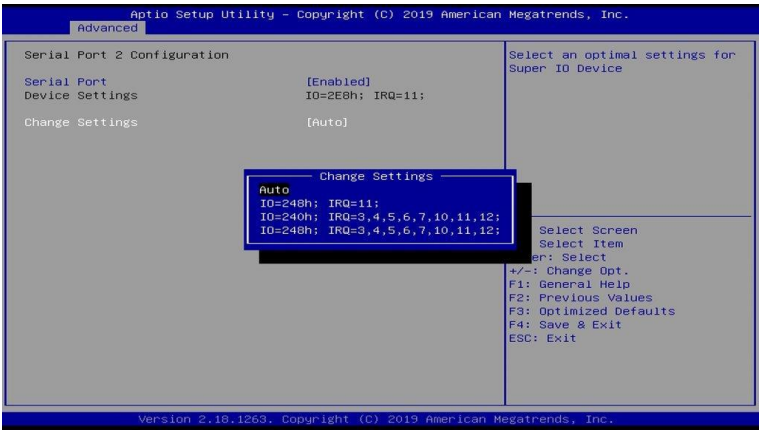
4.4.5.1. Serial Port 1 Configuration



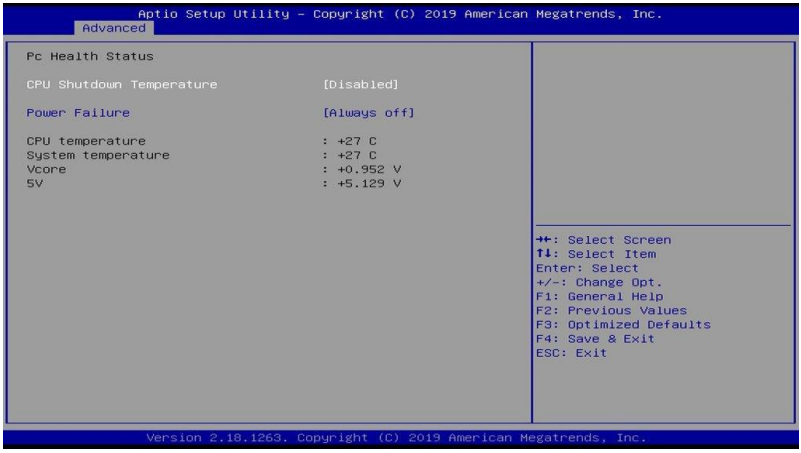


4.4.5.2. Serial Port 2 Configuration



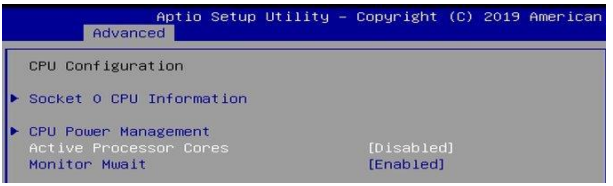


4.4.6 F81804 Hardware Monitor



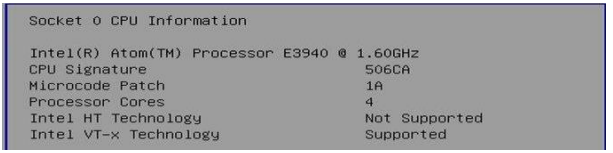
BIOS Setting	Description
CPU Shutdown Temperature	Sets a threshold of temperature to shut down if CPU goes overheated. Options: Disabled, 70°C, 75°C, 80°C, 85°C, 90°C, 95°C
Power Failure	Options: Always on, Always off
Temperatures / Voltages	These fields are the parameters of the hardware monitoring function feature of the motherboard. The values are read-only values as monitored by the system and show the PC health status.

4.4.7 CPU Configuration



BIOS Setting	Description
Socket 0 CPU Information	Displays the socket specific CPU information.
CPU Power Management	Shows the CPU power management options.
Active Processor Cores	Enables / Disables the number of cores to enable in each processor package.
Monitor Mwait	Enables / Disables Monitor Mwait.

4.4.8.1. Socket 0 CPU Information

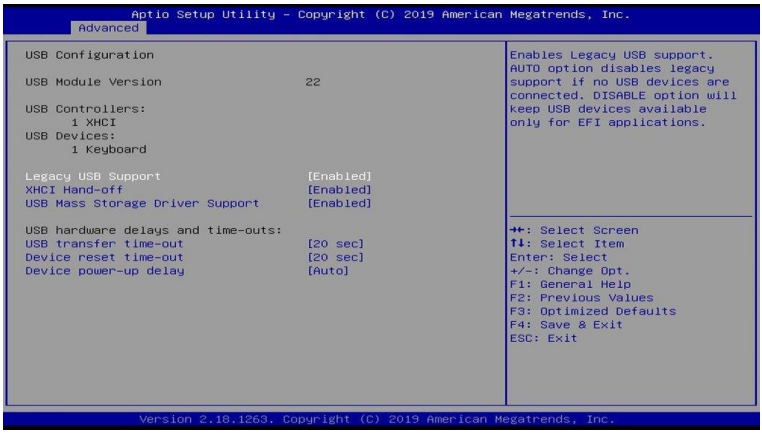


4.4.8.2. CPU Power Management

4.4.8.3. Active Processor Core

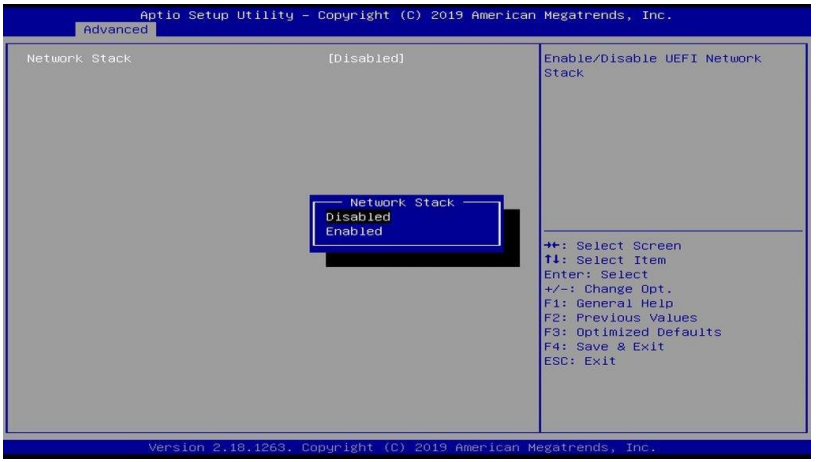
4.4.8.4. Monitor Mwait

4.4.8 USB Configuration



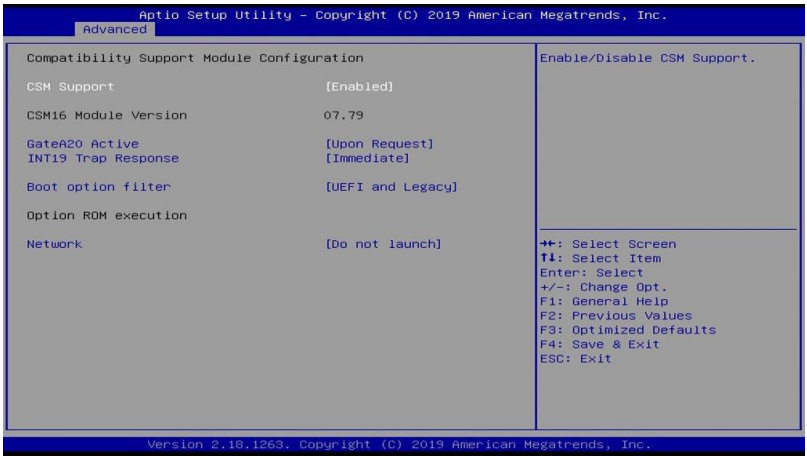
BIOS Setting	Description
Legacy USB Support	• **Enabled** enables Legacy USB support. • **Auto** disables legacy support if there is no USB device connected. • **Disabled** keeps USB devices available only for EFI applications.
XHCI Hand-off	This is a workaround for OSes without XHCI hand-off support. The XHCI ownership change should be claimed by XHCI driver.
USB Mass Storage Driver Support	Enables / Disables the support for USB mass storage driver.
USB Transfer time-out	The time-out value (1 / 5 10 / 20 secs) for Control, Bulk, and Interrupt transfers.
Device reset time-out	Gives seconds (10 / 20 / 30 / 40 secs) to delay execution of Start Unit command to USB mass storage device.
Device power-up delay	Maximum time the device will take before it properly reports itself to the Host Controller. “Auto” uses default value: for a root port it is 100 ms, for a hub port, the delay is taken from hub descriptor.

4.4.9 Network Stack Configuration



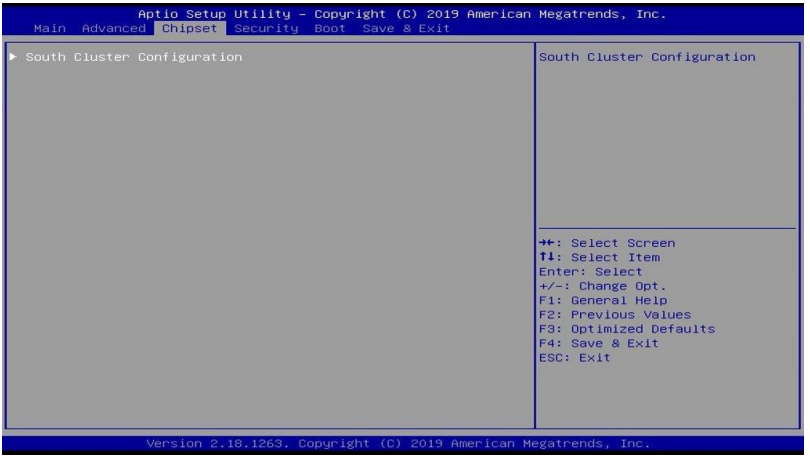
BIOS Setting	Description
Network Stack	Enables / Disables UEFI network stack.

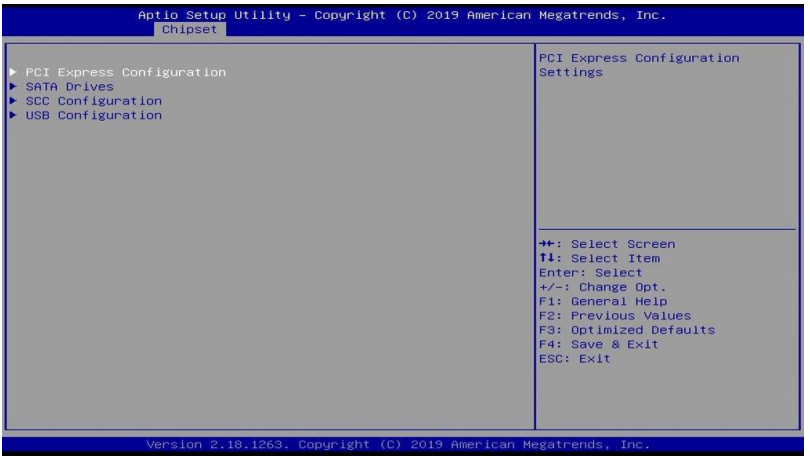
4.4.10 CSM Configuration



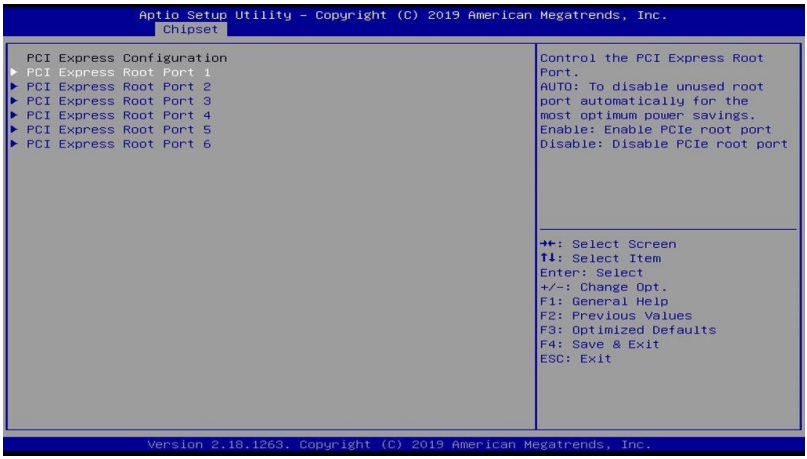
BIOS Setting	Description
CSM Support	Enables / Disables CSM support.
GateA20 Active	• **Upon Request** disables GA20 when using BIOS services. • **Always cannot** disable GA20, but is useful when any RT code is executed above 1 MB.
INT19 Trap Response	Selects the way that BIOS reacts on INT19 trapping by Option ROM. • Immediate executes the trap right away • Postponed executes the trap during legacy boot.
Boot option filter	Controls the priority of Legacy and UEFI.
Network	Controls the execution of UEFI and Legacy PXE OpROM.

4.5 Chipset Settings





4.5.1 PCI Express Configuration

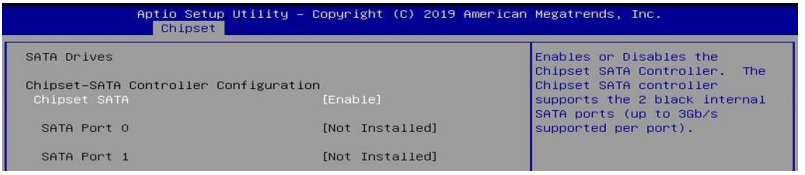


BIOS Setting	Description
PCI Express Root Ports 1 ~ 6	Control the PCI Express Root Port. Enables / Disables PCIe root port. Auto is to disable unused root port automatically for the most optimum power savings.

4.5.1.1. PCIe Root Ports 1~6

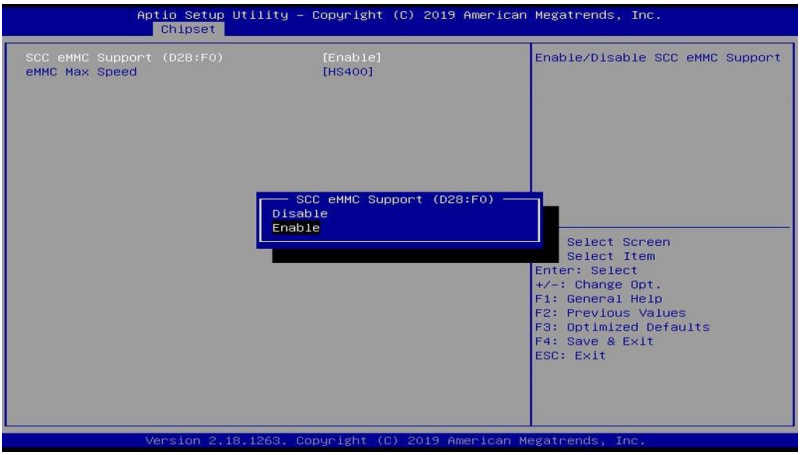
BIOS Setting	Description
ASPM	PCI Express Active State Power Management Settings.
L1 Substates	PCI Express L1 Substates Settings.
PME SCI	Enables / Disables PCI Express PME SCI.
PCIe Speed	Configures the PCIe speed as Auto, Gen1, or Gen2.

4.5.2 SATA Drives



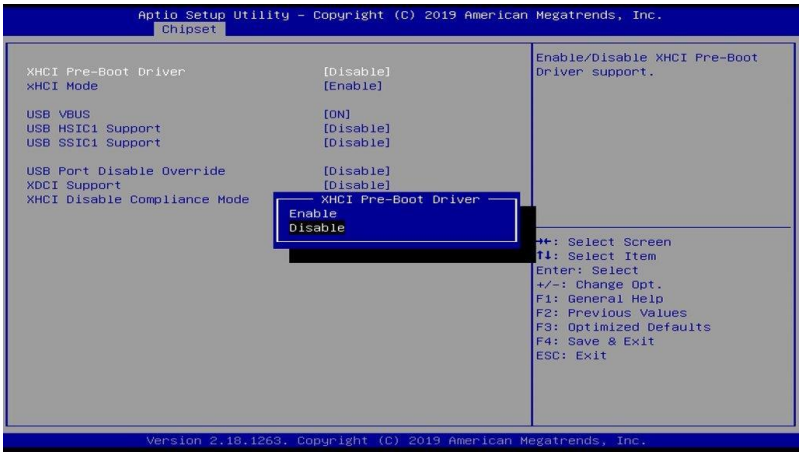
BIOS Setting	Description
Chipset SATA	Enables / Disables the chipset SATA controller. The chipsest SATA Controller supports the 2 black internal SATA ports (up to 3Gb/s supported per port).

4.5.3 SCC Configuration



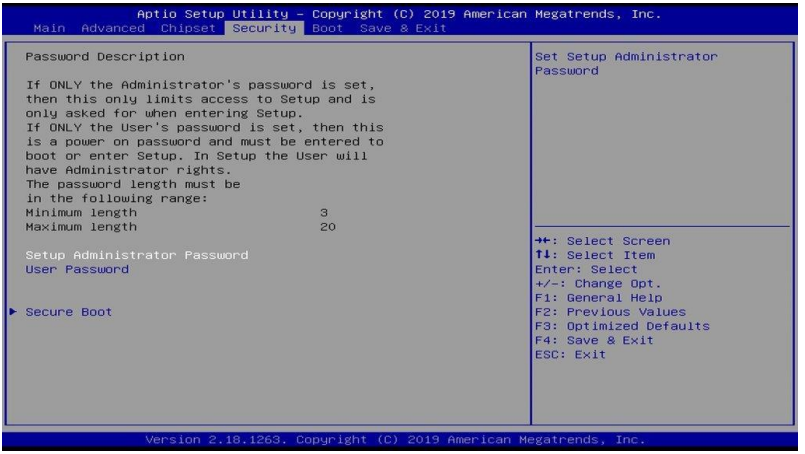
BIOS Setting	Description
SCC eMMC Support	Enables / Disables SCC eMMC support.
eMMC Max Speed	Select the eMMC max. speed. Options: HS400, HS200, DDR50

4.5.4 USB Configuration



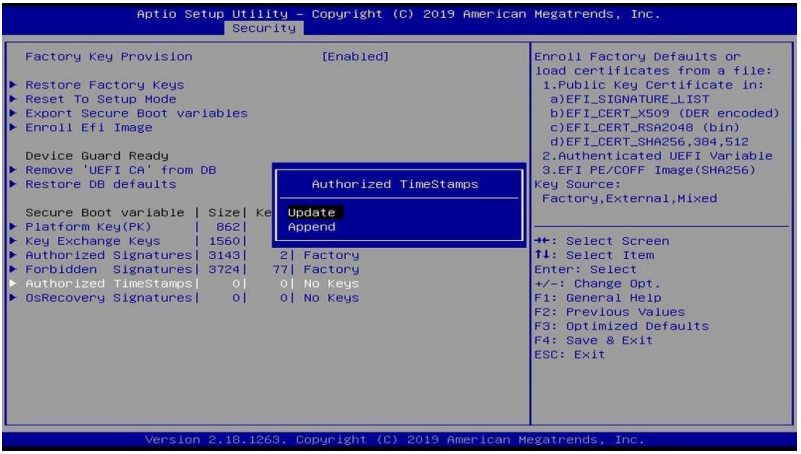
BIOS Setting	Description
XHCI Pre-Boot Driver	Enables / Disables XHCI Pre-Boot driver support.
XDCI Mode	Once disabled, XHCI controller would be function disabled, none of the USB devices are detectable and usable during boot and in OS. Do not disable it unless for debug purpose.
USB VBUS	VBUS should be set as ON in Host mode, and should be set as OFF in OTG device mode.
USB HSIC1 Support	Enables / Disables USB HSIC1.
USB SSIC1 Support	Enables / Disables USB SSIC1.
USB Port 0 Disable Override	Selectively enables / disables the corresponding USB port from reporting a device connection to the controller.
XDCI Support	Enables / Disables XDCI. Options: Disable, PCI Mode
XHCI Disable Compliance Mode	Options to disable XHCI Link Compliance Mode. Default is FALSE to not disable Compliance Mode. Set True to disable Compliance Mode. Options: False, True

4.6 Security Settings



BIOS Setting	Description
Administrator Password	Sets an administrator password for the setup utility.
User Password	Sets a user password.
Secure Boot	Customizable secure boot settings.

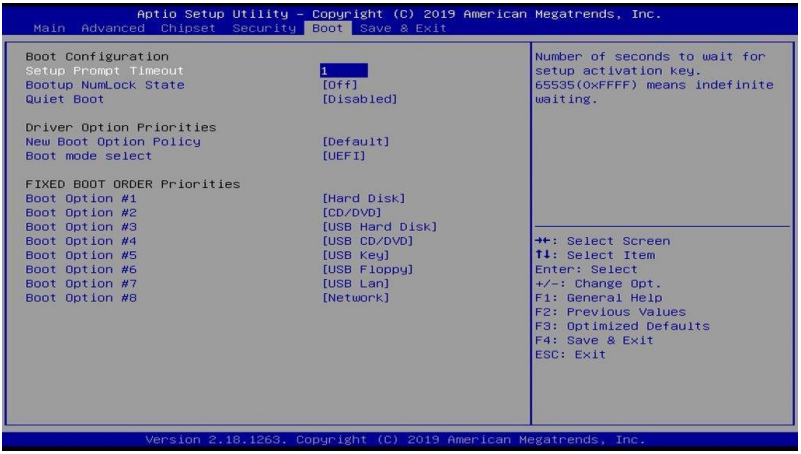
4.6.1 Secure Boot



BIOS Setting	Description
Secure Boot	Secure Boot activated when Secure Boot is enrolled, System mode is User/Deployed and CSM is disabled.
Secure Boot Customization	Secure Boot mode – Custom & Standard, Set UEFI Secure Boot mode to STANDARD mode or CUSTOM mode, this change is effect after save. And after reset, the mode will return to STANDARD mode.
Restore Factory	Force System to User Mode. Configure NVRAM to

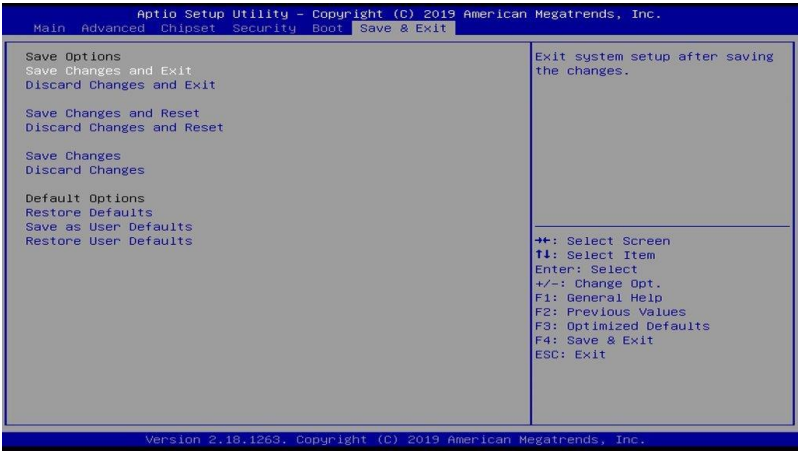
Keys	contain OEM-defined factory default Security Boot keys.
Reset To Setup Mode	Delete NVRAM content of all UEFI Secure Boot key databases.
Key Management	Enables expert users to modify Secure Boot Policy variables without full authentication.
Factory Key Provision	Provision factory default keys on next re-boot only when System in Setup Mode
Export Secure Boot variables	Copy NVRAM content of Secure Boot variables to files in a root folder on a file system device
Enroll Efi Image	Allow the image to run in Secure Boot mode. Enroll SHA256 Hash certificate of a PE image into Authorized Signature Database (db)
Remove 'UEFI CA' from DB	Device Guard ready system must not list 'Microsoft UEFI CA' Certificate in Authorized Signature database (db)
Remove DB defaults	Restore DB variable to factory defaults
Platform Key (PK) Key Exchange Key Authorized Signature Forbidden Signature Authorized TimeStamps OsRecovery Signatures	Enroll Factory Defaults or load certificates from a file: 1.Public Key Certificate in: a)EFI_SIGNATURE_LIST b)EFI_CERT_X509 (DER encoded) c)EFI_CERT_RSA2048 (bin) d)EFI_CERT_SHA256,384,512 2.Authenticated UEFI Variable 3.EFI PE/COFF Image(SHA256) Key Source: Factory,External,Mixed

4.7 Boot Settings



BIOS Setting	Description
Setup Prompt Timeout	Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
Bootup NumLock State	Selects the keyboard NumLock state.
Quiet Boot	Enables / Disables Quiet Boot option.
New Boot Option Policy	Controls the placement of newly detected UEFI boot options.
Boot mode select	Selects a Boot mode, Legacy / UEFI.
Boot Option Priorities	Sets the system boot order priorities for hard disk, CD/DVD, USB, Network.

4.8 Save & Exit Settings



BIOS Setting	Description
Save Changes and Exit	Exits system setup after saving the changes.
Discard Changes and Exit	Exits system setup without saving any changes.
Save Changes and Reset	Resets the system after saving the changes.
Discard Changes and Reset	Resets system setup without saving any changes.
Save Changes	Saves changes done so far to any of the setup options.
Discard Changes	Discards changes done so far to any of the setup options.
Restore Defaults	Restores / Loads defaults values for all the setup options.
Save as User Defaults	Saves the changes done so far as User Defaults.
Restore User Defaults	Restores the user defaults to all the setup options.

Appendix

This section provides the mapping addresses of peripheral devices and the sample code of watchdog timer configuration.

A. I/O Port Address Map

Each peripheral device in the system is assigned a set of I/O port addresses which also becomes the identity of the device. The following table lists the I/O port addresses used.

Address	Device Description
0x00000A00-0x00000A0F	Motherboard resources
0x00000A10-0x00000A1F	Motherboard resources
0x00000A20-0x00000A2F	Motherboard resources
0x0000002E-0x0000002F	Motherboard resources
0x0000004E-0x0000004F	Motherboard resources
0x00000061-0x00000061	Motherboard resources
0x00000063-0x00000063	Motherboard resources
0x00000065-0x00000065	Motherboard resources
0x00000067-0x00000067	Motherboard resources
0x00000070-0x00000070	Motherboard resources
0x00000070-0x00000070	System CMOS/real time clock
0x00000080-0x0000008F	Motherboard resources
0x00000092-0x00000092	Motherboard resources
0x000000B2-0x000000B3	Motherboard resources
0x00000680-0x0000069F	Motherboard resources
0x00000400-0x0000047F	Motherboard resources
0x00000500-0x000005FE	Motherboard resources
0x00000600-0x0000061F	Motherboard resources
0x0000164E-0x0000164F	Motherboard resources
0x0000F040-0x0000F05F	Intel(R) Celeron(R)/Pentium(R) Processor SMBUS - 5AD4
0x0000D000-0x0000DFFF	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5AD6
0x000003F8-0x000003FF	Communications Port (COM1)

Address	Device Description
0x000002F8-0x000002FF	Communications Port (COM2)
0x000003E8-0x000003EF	Communications Port (COM3)
0x000002E8-0x000002EF	Communications Port (COM4)
0x00000060-0x00000060	Standard PS/2 Keyboard
0x00000064-0x00000064	Standard PS/2 Keyboard
0x00000000-0x0000006F	PCI Express Root Complex
0x00000078-0x00000CF7	PCI Express Root Complex
0x00000D00-0x0000FFFF	PCI Express Root Complex
0x00000020-0x00000021	Programmable interrupt controller
0x00000024-0x00000025	Programmable interrupt controller
0x00000028-0x00000029	Programmable interrupt controller
0x0000002C-0x0000002D	Programmable interrupt controller
0x00000030-0x00000031	Programmable interrupt controller
0x00000034-0x00000035	Programmable interrupt controller
0x00000038-0x00000039	Programmable interrupt controller
0x0000003C-0x0000003D	Programmable interrupt controller
0x000000A0-0x000000A1	Programmable interrupt controller
0x000000A4-0x000000A5	Programmable interrupt controller
0x000000A8-0x000000A9	Programmable interrupt controller
0x000000AC-0x000000AD	Programmable interrupt controller
0x000000B0-0x000000B1	Programmable interrupt controller
0x000000B4-0x000000B5	Programmable interrupt controller
0x000000B8-0x000000B9	Programmable interrupt controller
0x000000BC-0x000000BD	Programmable interrupt controller
0x000004D0-0x000004D1	Programmable interrupt controller
0x0000F000-0x0000F03F	Intel(R) HD Graphics
0x0000E000-0x0000EFFF	Intel(R) Celeron(R)/Pentium(R) Processor PCI Express Root Port - 5ADB

Address	Device Description
0x0000F090-0x0000F097	Standard SATA AHCI Controller
0x0000F080-0x0000F083	Standard SATA AHCI Controller
0x0000F060-0x0000F07F	Standard SATA AHCI Controller
0x00000040-0x00000043	System timer
0x00000050-0x00000053	System timer

B. Interrupt Request Lines (IRQ)

Peripheral devices use interrupt request lines to notify CPU for the service required. The following table shows the IRQ used by the devices on board.

Level	Function
IRQ 25	High Definition Audio Controller
IRQ 39	Intel SD Host Controller
IRQ 8	High precision event timer
IRQ 27	Intel(R) Serial IO I2C Host Controller - 5AAC
IRQ 4	Communications Port (COM1)
IRQ 3	Communications Port (COM2)
IRQ 10	Communications Port (COM3)
IRQ 11	Communications Port (COM4)
IRQ 4294967281	Intel(R) USB 3.0 eXtensible Host Controller - 1.0 (Microsoft)
IRQ 1	Standard PS/2 Keyboard
IRQ 12	PS/2 Compatible Mouse
IRQ 4294967293	Intel(R) I210 Gigabit Network Connection
IRQ 4294967292	Intel(R) I210 Gigabit Network Connection
IRQ 4294967291	Intel(R) I210 Gigabit Network Connection
IRQ 4294967290	Intel(R) I210 Gigabit Network Connection
IRQ 4294967289	Intel(R) I210 Gigabit Network Connection
IRQ 4294967288	Intel(R) I210 Gigabit Network Connection
IRQ 42	Intel SD Host Controller
IRQ 54 ~ IRQ 204	Microsoft ACPI-Compliant System
IRQ 256 ~ IRQ 511	Microsoft ACPI-Compliant System
IRQ 4294967287	Intel(R) I210 Gigabit Network Connection #2
IRQ 4294967286	Intel(R) I210 Gigabit Network Connection #2
IRQ 4294967285	Intel(R) I210 Gigabit Network Connection #2
IRQ 4294967284	Intel(R) I210 Gigabit Network Connection #2
IRQ 4294967283	Intel(R) I210 Gigabit Network Connection #2
IRQ 4294967282	Intel(R) I210 Gigabit Network Connection #2
IRQ 4294967280	Intel(R) Trusted Execution Engine Interface

Level	Function
IRQ 4294967279	Intel(R) HD Graphics
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3452
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3452
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3452
IRQ 14	Intel(R) Serial IO GPIO Host Controller - INT3452
IRQ 4294967294	Standard SATA AHCI Controller
IRQ 0	System timer

C. Watchdog Timer Configuration

The Watchdog Timer (WDT) is used to generate a variety of output signals after a user programmable count. The WDT is suitable for use in the prevention of system lock-up, such as when software becomes trapped in a deadlock. Under these sorts of circumstances, the timer will count to zero and the selected outputs will be driven.

Under normal circumstance, you will need to restart the WDT at regular intervals before the timer counts to zero.

Sample Code:

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include <dos.h>
#include <conio.h>
#include <stdio.h>
#include <stdlib.h>
#include "F81804.H"
//---------------------------------------------------------------------------
int main (int argc, char *argv[]);
void EnableWDT(int);
void DisableWDT(void);
//---------------------------------------------------------------------------
int main (int argc, char *argv[])
{
        unsigned char bBuf;
        unsigned char bTime;
        char **endptr;

        char SIO;

        printf("Fintek 81804 watch dog program\n");
        SIO = Init_F81804();
        if (SIO == 0)
        {
                printf("Can not detect Fintek 81804, program abort.\n");
                return(1);
        }//if (SIO == 0)

        if (argc != 2)
        {
                printf("Parameter incorrect!!\n");
                return (1);
        }
```

```
        bTime = strtol (argv[1], endptr, 10);
        printf("System will reset after %d seconds\n", bTime);

        if (bTime)
        {       EnableWDT(bTime); }
        else
        {       DisableWDT(); }
        return 0;
}
//-----------------------------------------------------------------------
void EnableWDT(int interval)
{
        unsigned char bBuf;

        bBuf = Get_F81804_Reg(0x2B);
        bBuf &= (~0x20);
        Set_F81804_Reg(0x2B,   bBuf);          //Enable WDTO

        Set_F81804_LD(0x07);                   //switch to logic device 7
        Set_F81804_Reg(0x30,   0x01);          //enable timer

        bBuf = Get_F81804_Reg(0xF5);
        bBuf &= (~0x0F);
        bBuf |= 0x52;
        Set_F81804_Reg(0xF5,   bBuf);          //count mode is second

        Set_F81804_Reg(0xF6,   interval);      //set timer

        bBuf = Get_F81804_Reg(0xFA);
        bBuf |= 0x01;
        Set_F81804_Reg(0xFA,   bBuf);          //enable WDTO output

        bBuf = Get_F81804_Reg(0xF5);
        bBuf |= 0x20;
        Set_F81804_Reg(0xF5,   bBuf);          //start counting
}
//-----------------------------------------------------------------------
void DisableWDT(void)
{
        unsigned char bBuf;

        Set_F81804_LD(0x07);                   //switch to logic device 7

        bBuf = Get_F81804_Reg(0xFA);
        bBuf &= ~0x01;
        Set_F81804_Reg(0xFA,   bBuf);          //disable WDTO output

        bBuf = Get_F81804_Reg(0xF5);
        bBuf &= ~0x20;
        bBuf |= 0x40;
        Set_F81804_Reg(0xF5,   bBuf);          //disable WDT
}
//-----------------------------------------------------------------------


//-----------------------------------------------------------------------
//
```

```
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#include "F81804.H"
#include <dos.h>
//---------------------------------------------------------------------------
unsigned int F81804_BASE;
void Unlock_F81804 (void);
void Lock_F81804 (void);
//---------------------------------------------------------------------------
unsigned int Init_F81804(void)
{
        unsigned int result;
        unsigned char ucDid;

        F81804_BASE = 0x4E;
        result = F81804_BASE;

        ucDid = Get_F81804_Reg(0x20);
        if (ucDid == 0x07)                      //Fintek 81804
        {       goto Init_Finish;               }

        F81804_BASE = 0x2E;
        result = F81804_BASE;

        ucDid = Get_F81804_Reg(0x20);
        if (ucDid == 0x07)                      //Fintek 81804
        {       goto Init_Finish;               }

        F81804_BASE = 0x00;
        result = F81804_BASE;

Init_Finish:
        return (result);
}
//---------------------------------------------------------------------------
void Unlock_F81804 (void)
{
        outportb(F81804_INDEX_PORT, F81804_UNLOCK);
        outportb(F81804_INDEX_PORT, F81804_UNLOCK);
}
//---------------------------------------------------------------------------
void Lock_F81804 (void)
{
        outportb(F81804_INDEX_PORT, F81804_LOCK);
}
//---------------------------------------------------------------------------
void Set_F81804_LD( unsigned char LD)
{
        Unlock_F81804();
        outportb(F81804_INDEX_PORT, F81804_REG_LD);
        outportb(F81804_DATA_PORT, LD);
        Lock_F81804();
}
```

```
//---------------------------------------------------------------------------
void Set_F81804_Reg( unsigned char REG, unsigned char DATA)
{
                Unlock_F81804();
                outportb(F81804_INDEX_PORT, REG);
                outportb(F81804_DATA_PORT, DATA);
                Lock_F81804();
}
//---------------------------------------------------------------------------
unsigned char Get_F81804_Reg(unsigned char REG)
{
                unsigned char Result;
                Unlock_F81804();
                outportb(F81804_INDEX_PORT, REG);
                Result = inportb(F81804_DATA_PORT);
                Lock_F81804();
                return Result;
}
//---------------------------------------------------------------------------
```

```
//---------------------------------------------------------------------------
//
// THIS CODE AND INFORMATION IS PROVIDED "AS IS" WITHOUT WARRANTY OF ANY
// KIND, EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED TO THE
// IMPLIED WARRANTIES OF MERCHANTABILITY AND/OR FITNESS FOR A PARTICULAR
// PURPOSE.
//
//---------------------------------------------------------------------------
#ifndef   F81804_H
#define   F81804_H                      1
//---------------------------------------------------------------------------
#define         F81804_INDEX_PORT       (F81804_BASE)
#define         F81804_DATA_PORT        (F81804_BASE+1)
//---------------------------------------------------------------------------
#define         F81804_REG_LD           0x07
//---------------------------------------------------------------------------
#define         F81804_UNLOCK           0x87
#define         F81804_LOCK             0xAA
//---------------------------------------------------------------------------
unsigned int Init_F81804(void);
void Set_F81804_LD( unsigned char);
void Set_F81804_Reg( unsigned char,
unsigned char); unsigned char
Get_F81804_Reg( unsigned char);
//---------------------------------------------------------------------------
#endif  //   F81804_H
```