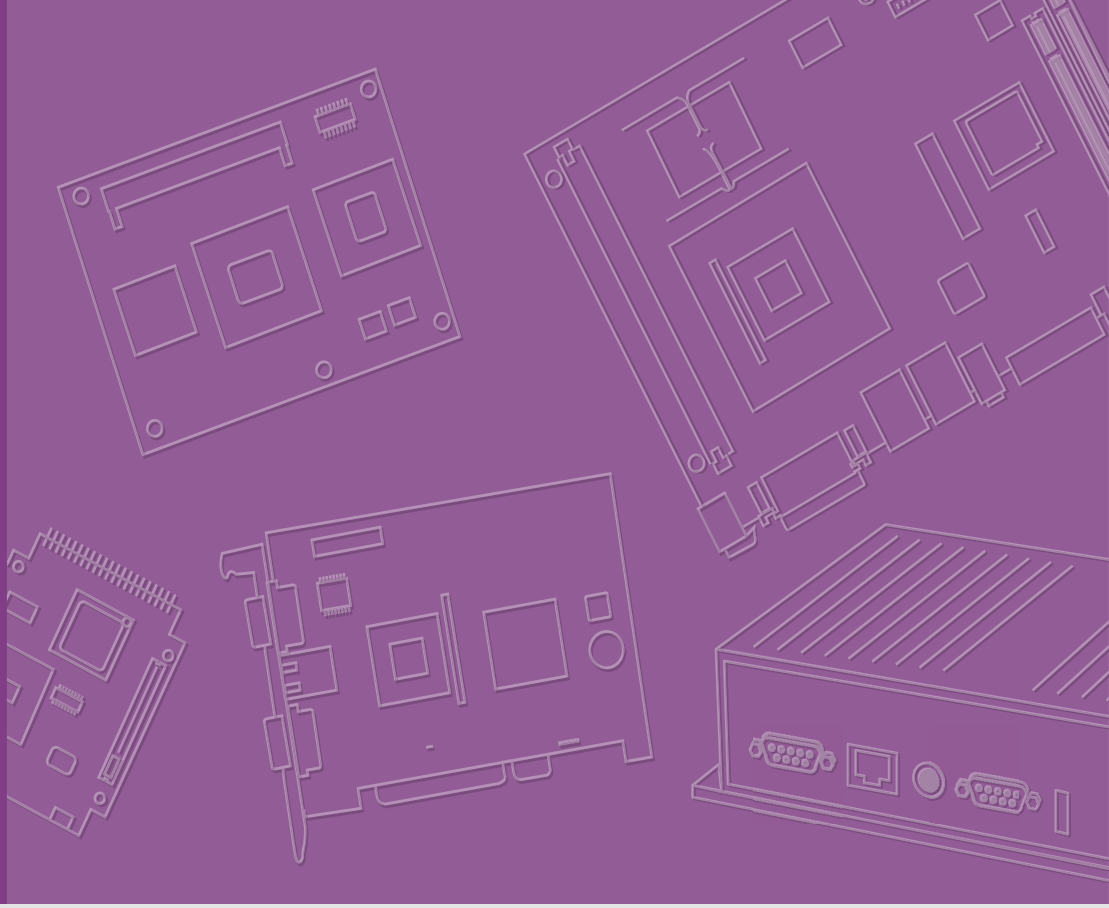


User Manual

# AIMB-585

## Intel® Xeon® E3/Core™ i7/i5/i3 (LGA1151) Micro-ATX with VGA/ DVI/eDP/DP/HDMI, 6 x COM, 2 x LAN, DDR4, PCIe x16, PCIe x8 and SATA III

ADVANTECH

*Enabling an Intelligent Planet*

# Copyright



# Acknowledgements

IBM and PC are trademarks of International Business Machines Corporation.

Intel® Xeon® and Core™ are trademarks of Intel Corporation.

All other product names or trademarks are properties of their respective owners.

# Product Warranty (2 Years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product is defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Part No. 2006058502 Edition 3

Printed in China May 2024

# Declaration of Conformity

### FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

# Technical Support and Assistance

1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

# Initial Inspection

Before you begin installing your motherboard, please make sure that the following materials have been shipped:

- 1 x AIMB-585 Intel® Xeon™ E3 & Core™ i7/i5/i3 Micro-ATX Motherboard
- 2 x SATA HDD cable
- 2 x SATA power cable
- 1 x I/O port bracket
- 1 x Startup Manual
- 1 x Warranty Card

If any of these items are missing or damaged, contact your distributor or sales representative immediately. We have carefully inspected the AIMB-585 mechanically and electrically before shipment. It should be free of marks and scratches and in perfect working order upon receipt. As you unpack the AIMB-585, check it for signs of shipping damage. (For example, damaged box, scratches, dents, etc.) If it is damaged or it fails to meet the specifications, notify our service department or your local sales representative immediately. Also notify the carrier. Retain the shipping carton and packing material for inspection by the carrier. After inspection, we will make arrangements to repair or replace the unit.

# Contents

# Chapter 1

## General Information

## 1.1 Introduction

AIMB-585 is designed with the Intel® Q70/C236/H110 chipset for industrial applications that require both performance computing and enhanced power management capabilities. The motherboard supports Intel® Xeon® E3 and Core™ i7/i5/i3 processors with up to 8MB L3 cache and DDR4 2400 MHz, up to 16GB per slot, totaling up to 64GB.

## 1.2 Features

- **Rich I/O connectivity:** 2 x GbE LAN via PCIe x1 bus, 1 x PCIe x16 slot (Gen 3), 1 x PCIe x8 slot (Gen 3), 1 x PCIe x4 slot (Gen 3), 1 x PCIe x1 slot (Gen 3), 2 x USB 2.0 ports, and 12 x USB 3.0 ports.
- **Standard Micro-ATX form factor with industrial features:** The AIMB-585 is a full-featured Micro-ATX motherboard with balanced expandability and performance.
- **Wide selection of storage devices:** SATA III HDD, customers benefit from the flexibility of using the most suitable storage device for larger capacity.
- **Optimized integrated graphics solution:** With the Intel® Flexible Display Interface, it supports versatile display options and a 32-bit 3D graphics engine.

## 1.3 Specifications

### 1.3.1 System

- **CPU:** 6th Gen Intel® Xeon® E3 or Core™ i7/i5/i3 processor
- **BIOS:** AMI EFI 128 Mbit SPI BIOS
- **System chipset:** Intel® C236/Q170/H110
- **SATA hard disk drive interface:** 4 x on-board SATA connectors with data transmission rate up to 600 MB

### 1.3.2 Memory

- **RAM:** Up to 64GB in 4 slots, 288-pin DIMM sockets. Supports dual-channel DDR4 2400MHz SDRAM.
  - AIMB-585QG2 & AIMB-585L supports non-ECC unbuffered DIMMs and does not support any memory configuration that mixes non-ECC with ECC unbuffered DIMMs.
  - AIMB-585WG2 supports ECC buffered DIMMs.

***Note!*** *A 32-bit OS may not fully detect 4GB of RAM when 4GB is installed.*

### 1.3.3 Input/Output

- **PCIe slot:** 1 x PCIe x16 expansion slot, 1 x PCIe x8 expansion slot, 1 x PCIe x4 expansion slot, 1 x PCIe x1 expansion slot
- **Serial port:** 6 x serial ports, one is RS-232/422/485 with hardware auto-flow control and five are RS-232. One of the DB-9 connectors located on the rear panel is RS-232.

- **Keyboard and PS/2 mouse connector:** 2 x 6-pin mini-DIN connectors are located on the mounting bracket for easy connection to a PS/2 keyboard and mouse.
- **USB ports:** Supports up to 2 x USB 2.0 ports with transmission rates up to 480 Mbps and 12 x USB 3.0 ports with transmission rates up to 5 Gbps.

***Note!*** *Under Windows 7 OS, all of USB 2.0/3.0 ports are not workable until the XHCI driver is installed. It is suggested to install the XHCI driver for the PS/2 keyboard & mouse first.*

- **GPIO:** AIMB-585 supports 16-bit GPIO from super I/O for general purpose control applications.

### 1.3.4 Graphics

- **Controller:** Intel® HD Graphics
- **Display memory:** 1GB maximum shared memory with 2GB and above system memory installed
- **DVI:** Supports DVI up to 1920 x 1200 @ 60Hz refresh rate.
- **VGA:** Supports VGA up to 1920 x 1200 @ 60Hz refresh rate.
- **HDMI:** Supports HDMI 1.4 3840 x 2160 @ 30Hz refresh rate.
- **DisplayPort:** Supports max resolution 4096 x 2304 @60Hz refresh rate.
- **eDP:** Supports max resolution 3840 x 2160 @ 60Hz refresh rate.
- **Triple Displays:** HDMI + eDP/VGA+ DP, HDMI+eDP/VGA+ DVI, HDMI+DP+DVI
- **Dual Displays:** HDMI+eDP/VGA, HDMI+DVI, eDP/VGA+ DVI, HDMI + DP, DP+ DVI, eDP/VGA+DP

### 1.3.5 Ethernet LAN

- Supports dual 10/100/1000 Mbps Ethernet port(s) via PCI Express x1 bus which provides 500 MB/s data transmission rate
- **Controller:** LAN1: Intel® I219LM; LAN2: Intel® I210AT

### 1.3.6 Industrial Features

- **Watchdog timer:** It can generate a system reset. The watchdog timer is programmable, with each unit equal to one second or one minute (255 levels).

### 1.3.7 Mechanical and Environmental Specifications

- **Operating temperature:** 0 ~ 60°C (32 ~ 140°F, Depending on CPU)
- **Storage temperature:** -40 ~ 85°C (-40 ~ 185°F)
- **Humidity:** 5 ~ 95% non-condensing
- **Power supply voltage:** +3.3 V, +5 V, +12 V, -12 V, 5 Vsb
- **Power consumption:**

  LAG1151 Core i7-6700 3.4 GHz, 8MB L3 Cache, 4pcs 8GB DDR4 2400MHz memory

| +5 V | 3.3 V | 12 V | 5 Vsb | -12 V |
|---|---|---|---|---|
| 1.31 A | 0.35 A | 4.52 A | 0.06 A | 0 A |

  Measure the maximum current value with the system under maximum load (CPU: top speed, RAM & graphics: full loading).

- **Board size:** 244 mm x 244 mm (9.6" x 9.6")
- **Board weight:** 0.365 kg

## 1.4 Jumpers and Connectors

Connectors on the AIMB-585 motherboard link it to devices such as hard disk drives and a keyboard. In addition, the board has a number of jumpers used to configure your system for your application.

The tables below list the function of each of the board jumpers and connectors. Later sections in this chapter give instructions on setting jumpers. Chapter 2 gives instructions for connecting external devices to your motherboard.

**Table 1.1: Jumpers**

| Label | Function |
|---|---|
| JFP1 | Power Switch / Reset / External Speaker / SATA HDD LED / SMBus connector |
| JFP2 | Power LED / Keyboard Lock |
| JSETCOM2 | Serial port: RS232/RS422/RS485 jumper settings |
| JCMOS1 | CMOS clear (default 1-2 pin) |
| JCASE1 | Case open connector |
| JEDP1 | eDP power jumper |
| JIR1+JOBS1 +JWDT1 | Jumper for CIR/Watchdog/OBS |
| JUSBPWR2 | USB power selection for LAN1_USB12/ LAN2_USB34/ USB561112 |
| JUSBPWR1 | USB power selection for USB78/ USB910/ USB1516 |

**Table 1.2: Connectors**

| Label | Function |
|---|---|
| COM1 | Serial Port 1 (RS-232) |
| COM2 | Serial Port COM2, pin header 2 x 5, COM2 supports RS232/422/485 |
| COM3/4/5/6 | Serial port: COM 3/4/5/6, box header 2x20 |
| DP1+HDMI | DisplayPort Connector (top) and HDMI connector (bottom) |
| DVI1 | DVI connector |
| LAN1_USB12 | LAN1 & USB12 connector |
| LAN2_USB34 | LAN2 & USB34 connector |
| LANLED1 | Front Panel LAN Indicator connector |
| USB5/6/11/12 | USB port 5-6, 11-12 |
| USB 7/8/9/10 | USB 7/8/9/10 (internal 2 x 10-pin header on board) |
| USB 15/16 | USB 15/16 from Renesas (internal 2 x 10 pin header on board) (Optional) |
| SATA1-4 | Serial III ATA connector |
| CPUFAN1 | CPU FAN connector (4-pin) |
| SYS-FAN1/2/3/4 | System FAN Power Connector (4-pin) (Fan3/Fan4 Optional) |
| eDP1 | eDP connector (2 x 10-pin header) |
| KBMS1 | On board external keyboard and Mouse connector |
| AUDIO1 | Line-Out, Mic-In connector |

| | |
|---|---|
| FPAUDIO1 | Front Panel audio connector (FP_AU-DIO) |
| PSON1 | AT(1-2) / ATX(2-3) (Default 2-3) |
| SPI_CN1 | SPI flash programming connector |
| GPIO1 | GPIO pin header (SMD pitch=2.0 mm) |
| SMBUS1 | SMBUS expansion pin header 1 x 4 p |
| ATX12V1 | ATX 4-pin 12V Auxiliary power connector |
| EATXPWR1 | ATX 24-pin power connector |
| INV1 | ePD inverter |
| VOLT1 | Voltage Display connector |
| SPDIF1 | Digital Audio connector 4 x 1 header pitch = 2.54 mm |
| LPC1 | Low pin count interface (2 x 7-pin header) |

## 1.5 Board layout: Jumper and Connector Locations

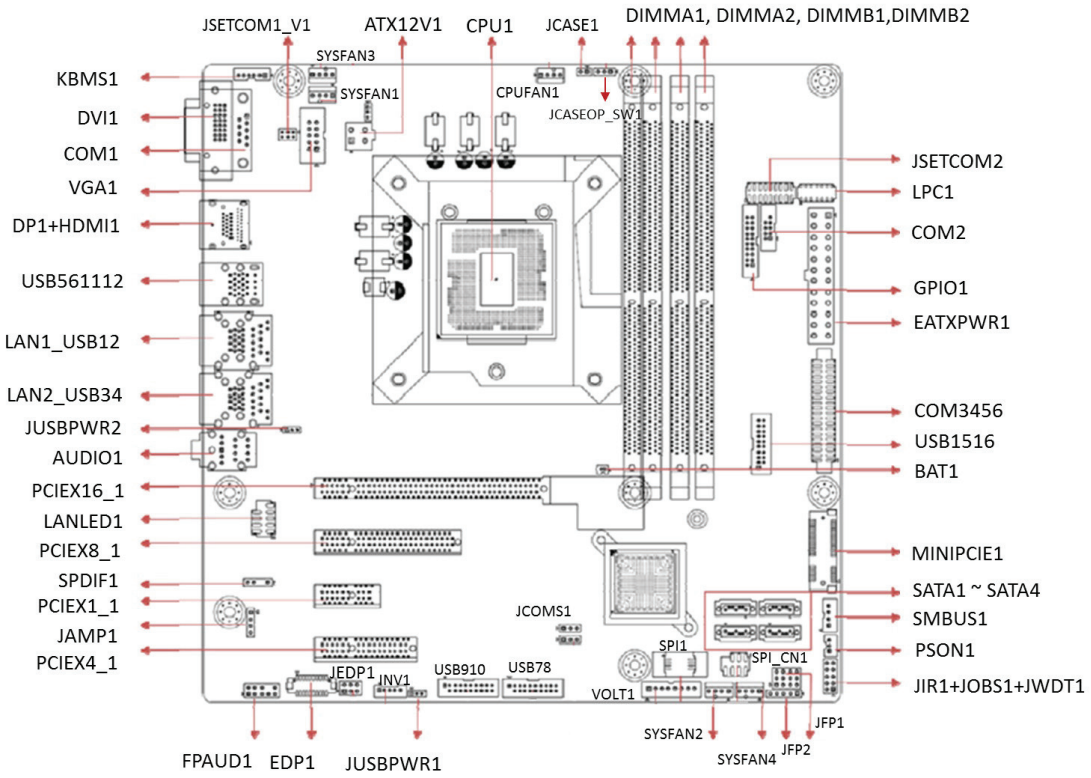



**Figure 1.1 Jumper and Connector Locations**

**Figure 1.2 I/O Connectors**

## 1.6 AIMB-585 Board Diagram

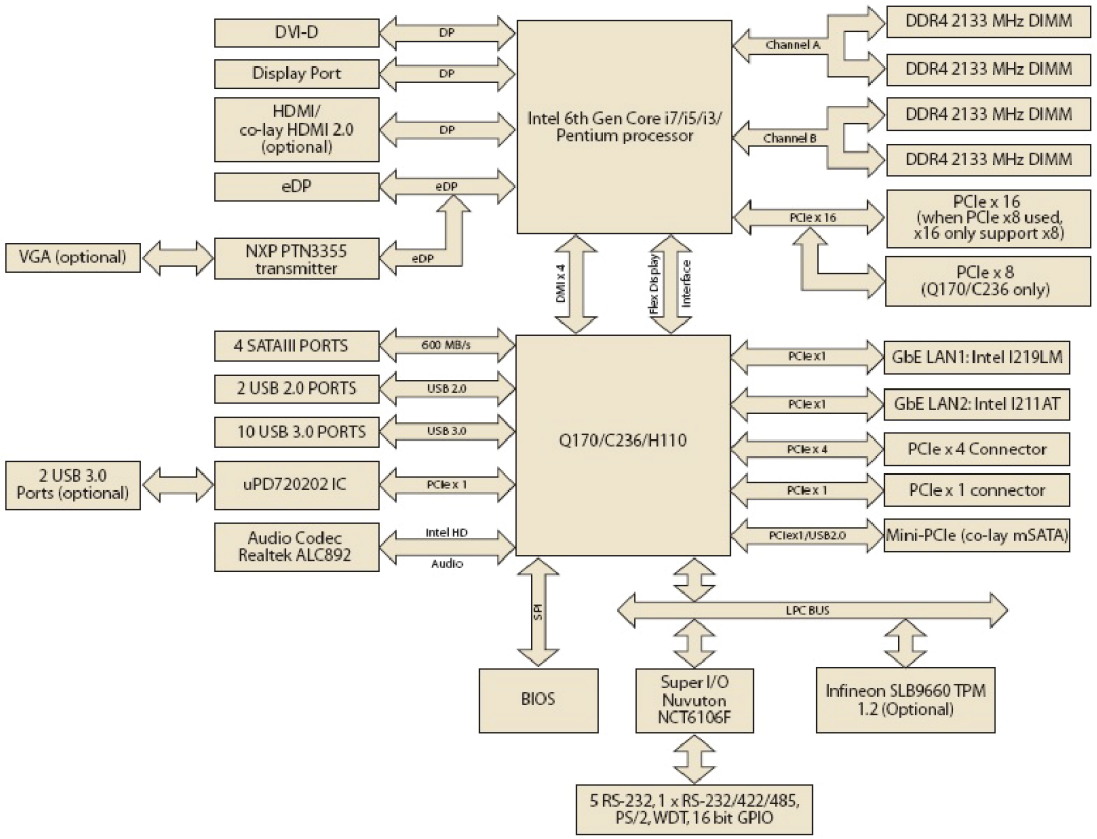



**Figure 1.3 AIMB-585 Block Diagram**

## 1.7 Safety Precautions

***Warning!*** *Always completely disconnect the power cord from the chassis whenever you work with the hardware. Do not make connections while the power is on. Sensitive electronic components can be damaged by sudden power surges. Only experienced electronics personnel should open the PC chassis.*

***Caution!*** *Always ground yourself to remove any static charge before touching the motherboard. Modern electronic devices are very sensitive to electrostatic discharges. As a safety precaution, use a grounding wrist strap at all times. Place all electronic components on a static-dissipative surface or in a static-shielded bag when they are not in the chassis.*

***Caution!*** *The computer is provided with a battery-powered real-time clock circuit. There is a danger of explosion if the battery is incorrectly replaced. Replace only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*

***Caution!*** *There is a danger of a new battery exploding if it is incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.*

## 1.8 Jumper Settings

This section provides instructions on how to configure your motherboard by setting the jumpers. It also includes the motherboard's default settings and your options for each jumper.

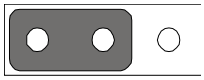
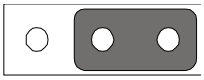
### 1.8.1 How to Set Jumpers

You can configure your motherboard to match the needs of your application by setting the jumpers. A jumper is a metal bridge that closes an electrical circuit. It consists of two metal pins and a small metal clip (often protected by a plastic cover) that slides over the pins to connect them. To “close” (or turn ON) a jumper, you connect the pins with the clip. To “open” (or turn OFF) a jumper, you remove the clip. Sometimes a jumper consists of a set of three pins, labeled 1, 2, and 3. In this case you connect either pins 1 and 2, or 2 and 3. A pair of needle-nose pliers may be useful when setting jumpers.

### 1.8.2 CMOS Clear (CMOS1)

The AIMB-585 motherboard contains a jumper that can erase CMOS data and reset the system BIOS information. Normally, this jumper should be set with pins 1-2 closed. If you want to reset the CMOS data, set CMOS1 to 2-3 closed for just a few seconds, and then move the jumper back to 1-2 closed. This procedure will reset the CMOS to its default setting.

**Table 1.3: CMOS1**

| Function | Jumper Setting | |
|---|---|---|
| *Keep CMOS data |  | 1-2 closed |
| Clear CMOS data |  | 2-3 closed |

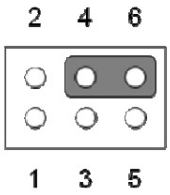
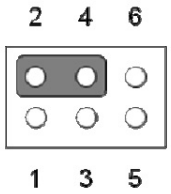
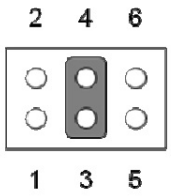
* Default

### 1.8.3 JEDP1: eDP Power 3.3 V/ 5 V/ 12 V Selector

**Table 1.4: JeDP1: eDP Power 3.3 V/5 V/ 12 V Selector**

| Closed Pins | Result |
|---|---|
| *JEDP1, 4-6 | Jumper for +3.3 V |
| EDP1, 2-4 | Jumper for +V5 |
| JEDP1, 3-4 | Jumper for +12 V |

*Default

| | |
|---|---|
| Jumper position for +3.3V (Default) |  |
| Jumper position for +5V |  |
| Jumper position for +12V |  |

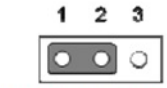
### 1.8.4 JUSBPWR1-2 (USB Power Selection Connector)

JUSBPWR1: selection for USB78, USB910, USB1516

JUSBPWR2: selection for LAN1_USB12, LAN2_USB34, USB561112

**Table 1.5: JUSBPWR1-2 (USB Power Selection Connector)**

| Pin | Pin Name |
|---|---|
| 1 | +V5_Vsb |
| 2 | +V5_USB |
| 3 | +V5 |



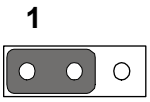

Default: 1-2 Pin (+5 VSB)

### 1.8.5 PSON1: ATX, AT Mode Selector

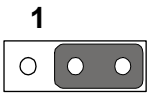
**Table 1.6: PSON1: ATX, AT Mode Selector**

| Closed Pins | Result |
|---|---|
| 1-2 | AT Mode |
| 2-3* | ATX Mode |

*Default




AT Mode
1-2 closed

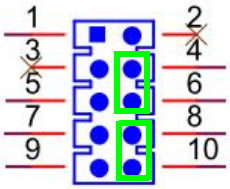



ATX Mode
2-3 closed

### 1.8.6 JIR1+JOB1+JWD1: Watchdog Timer Output, OBS Alarm Option, and CIR interface

**Table 1.7: JIR1+JOB1+JWD1: Watchdog Timer Output and OBS Alarm Connector**

| Pin | Pin Name |
|---|---|
| 1 | +V5 |
| 2 | NC |
| 3 | NC |
| 4 | Watch dog reset# output |
| 5 | IRRX |
| 6 | System reset input# |
| 7 | GND |
| 8 | SIO Warning Beep output |
| 9 | IRTX |
| 10 | SP1 Buzzer Beep input |



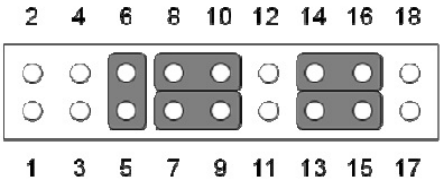

***Note!*** *Note: Watchdog time-out reset# (4-6 short) / SIO Warning Beep enable (8-10 short.)*

## 1.8.7 JSETCOM2: COM2 RS232, RS422, RS485 Selection

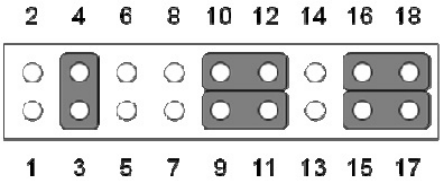
**Table 1.8: COM2 RS232, RS422, RS485 Selection**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | UART_SIN [2] | 2 | RXD_RS485 |
| 3 | UART_SIN [2] | 4 | RXD_RS422 |
| 5 | UART_SIN [2] | 6 | RXD_RS232 |
| 7 | DCDB | 8 | SOUT [2] |
| 9 | COM2_DCD# | 10 | COM2_SOUT |
| 11 | COM2_TXD485- | 12 | COM2_RXD485+ |
| 13 | SIN [B] | 14 | DTR [B] |
| 15 | COM2_SIN | 16 | COM2_DTR# |
| 17 | COM2_TXD485+ | 18 | COM2_RXD485- |

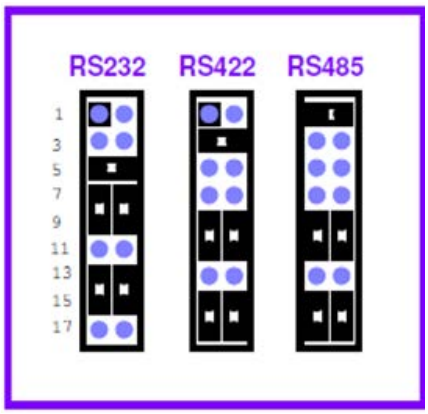
RS-232 Mode (Default)
(5-6) (7-9) (8-10) (13-15) (14-16)




RS-422 Mode
(3-4) (9-11) (10-12) (15-17) (16-18)




RS-485 Mode
(1-2) (9-11) (10-12) (15-17) (16-18)



### 1.8.8 JCASE1: Case Open Sensor

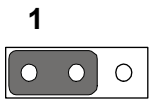
The AIMB-585 motherboard contains a jumper that provides a chassis open sensor. The buzzer on the motherboard beeps when the case is opened.

### 1.8.9 JCASEOP_SW1: Case Open Selection Pin Header

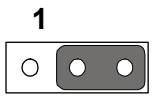
**Table 1.9: JCASEOP_SW1: Case Open Selection Pin Header**

| Closed Pins | Result |
|---|---|
| 1-2 | Normal Mode |
| 2-3* | Normal Open (Default) |

*Default

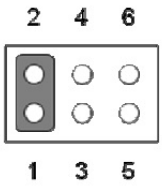
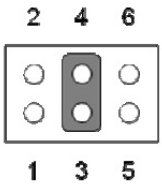
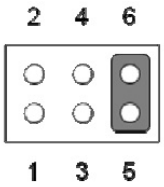



Normal Close
1-2 closed




Normal Open (Default)
2-3 closed

### 1.8.10 JSETCOM1_V1: COM1_RI# Pin RI# / 5V / 12V

| | |
|---|---|
| Jumper position for RI# (Default) |   |
| Jumper position for +5V |   |
| Jumper position for +12V |   |

## 1.9 System Memory

AIMB-585 has four 288-pin memory sockets for 2400MHz memory modules with maximum capacity of 64GB (Maximum 16GB for each DIMM). AIMB-585QG2/L supports only non-ECC DDR4 memory modules and does not support registered DIMMs (RDIMMs). AIMB-585WG2 can support ECC DDR4 memory modules.

## 1.10 Memory Installation Procedures

To install DIMMs, first make sure the two handles of the DIMM socket are in the “open” position, i.e., the handles lean outward. Slowly slide the DIMM module along the plastic guides on both ends of the socket. Then firmly but gently (avoid pushing down too hard) press the DIMM module well down into the socket, until you hear a click when the two handles have automatically locked the memory module into the

correct position of the DIMM socket. To remove the memory module, just push both handles outward, and the memory module will be ejected by the mechanism.

## 1.11 Cache Memory

The AIMB-585 supports a CPU with one of the following built-in full speed L3 caches:

8MB for Intel® Xeon® E3 1275v5
6MB for Intel® Xeon® E3 1225v5
8MB for Intel® Xeon® E3 1268Lv5
8MB for Intel® Core™ i7 6700
8MB for Intel® Core™ i7 6700TE
6MB for Intel® Core™ i5 6500
6MB for Intel® Core™ i5 6500TE
4MB for Intel® Core™ i3 6100
4MB for Intel® Core™ i3 6100TE
3MB for Intel® Pentium® G4400/G4400TE
2MB for Intel® Celeron® G3900/G3900TE

The built-in second-level cache in the processor yields much higher performance than conventional external cache memories.

## 1.12 Processor Installation

The AIMB-585 is designed for the LGA1151 sock to accommodate Intel® Xeon® and Intel® Core™ i7/i5/i3 Pentium®/Celeron® processors.

# Chapter 2

## Connecting Peripherals

## 2.1 Introduction

You can access most of the connectors from the top of the board as it is being installed in the chassis. If you have a number of cards installed or have a packed chassis, you may need to partially remove the card to make all the connections.

## 2.2 USB Ports (LAN1_USB12/LAN2_USB34/ USB561112/USB78/USB910/USB1516)

The AIMB-585 provides up to 14 USB ports. The USB interface complies with USB Specification Rev 2.0 supporting transmission rates up to 480 Mbps and Rev 3.0 supporting transmission rates up to 5 Gbps, and is fuse protected. The USB interface can be disabled in the system BIOS setup.

The AIMB-585 is equipped with two high-performance 1000 Mbps Ethernet LAN adapters, both of which are supported by all major network operating systems. The RJ-45 jacks on the rear panel provide convenient LAN connection.

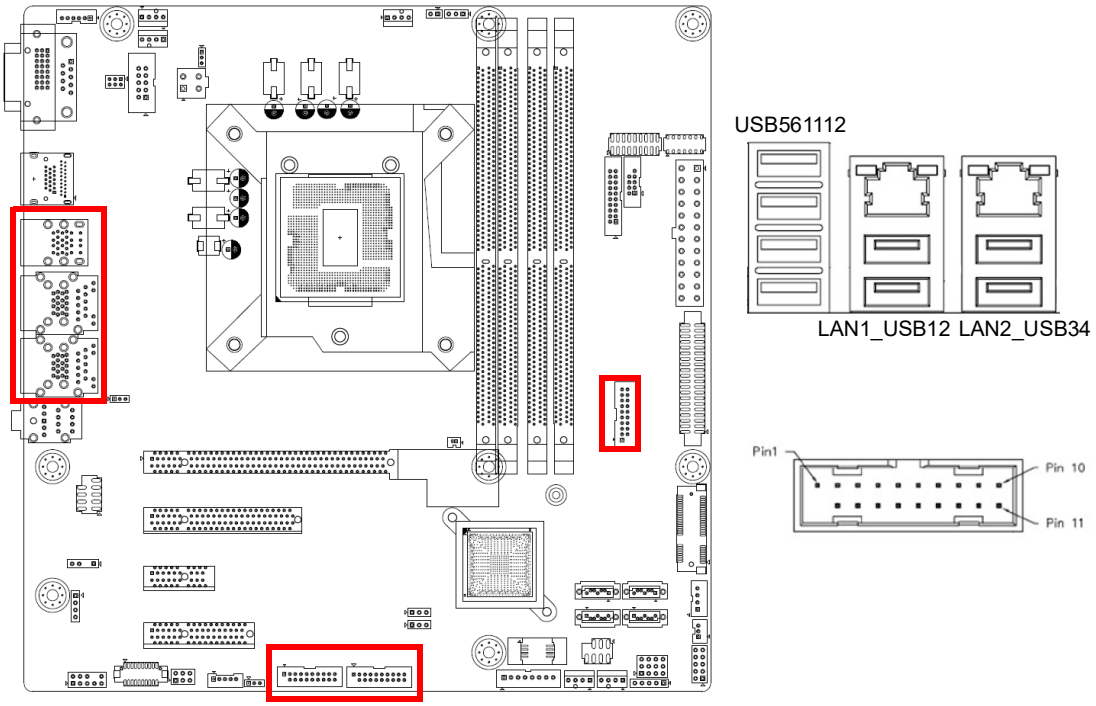
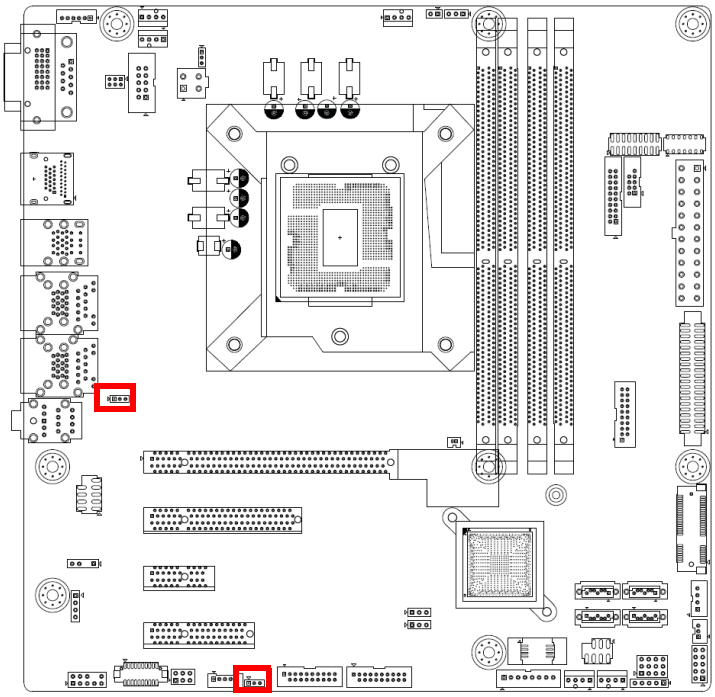


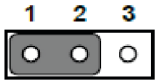

**Table 2.1: LAN LED Indicator**

| LAN Mode | LAN Indicator | |
|---|---|---|
| **LAN1 indicator** | LED1 (Right) | Off for mal-link; Link (On) / Active (Flash) |
| | LED2 (Left) | 100 Mbps (On) / 10 Mbps (Off); Color: Orange |
| | LED2 (Left) | 1000 Mbps (On); Color: Green |
| **LAN2 indicator** | LED1 (Right) | Off for mal-link; Link (On) / Active (Flash) |
| | LED2 (Left) | 100 Mbps (On) / 10 Mbps (Off); Color: Orange |
| | LED2 (Left) | 1000 Mbps (On); Color: Green |

## 2.3 USB Power Switch (JUSBPWR1/JUSBPWR2)

AIMB-585 allows users to set USB power between +5 VSB and +5 V. When the jumper is set as +5 V (default pin3 2-3); the board doesn't support wake from S3 via keyboard or mouse. If you need to set it to +5 Vsb, you need to modify the jumper (pins 1-2). There is another way to control USB power by GPIO. This requires the BOM option by HW design. Each GPIO can control all rear USB ports or all USB ports on the board pin header.

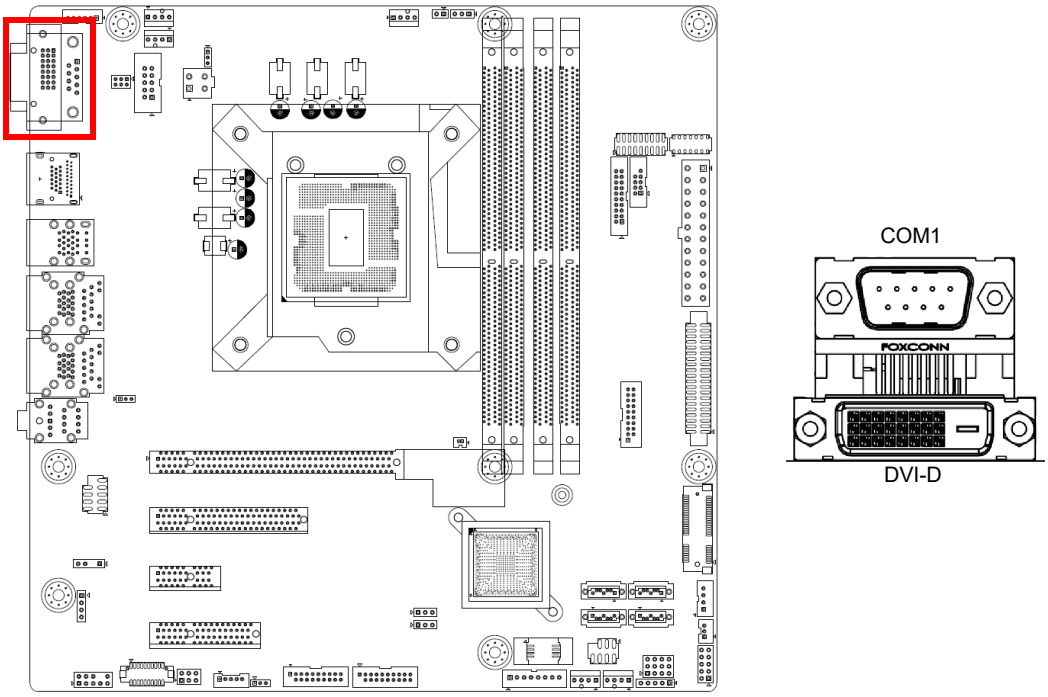





| Pins | Result |
|---|---|
| 1-2* | Set USB VBUS as +5VSB |
| 2-3 | Set USB VBUS as +5V |

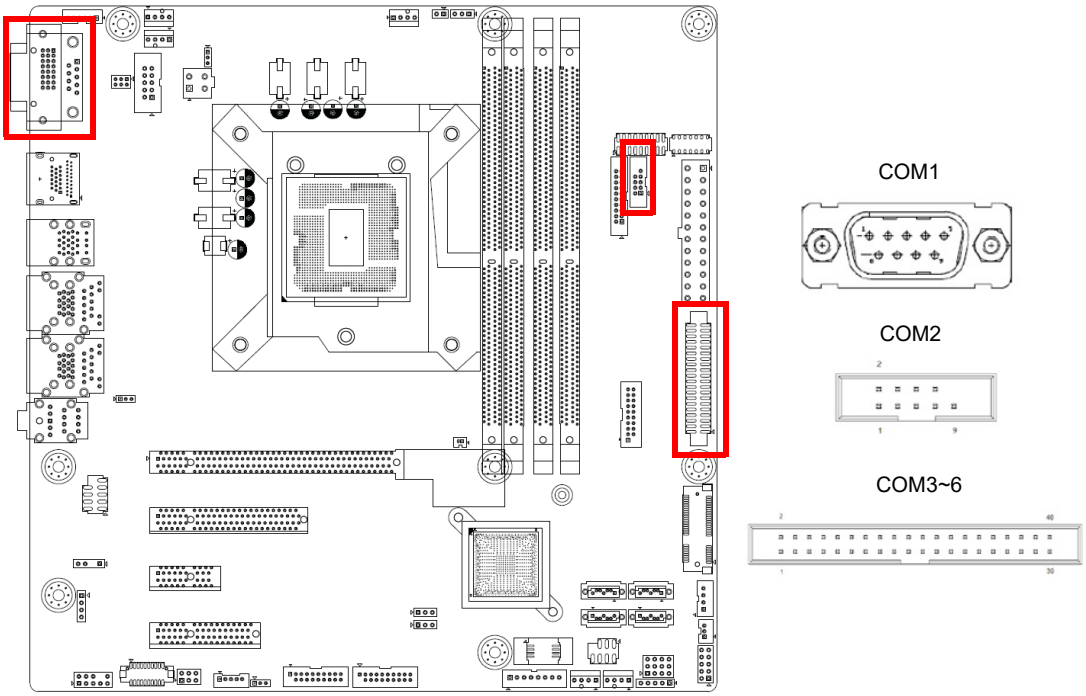
***Note!*** *When USB power is switched to +5V, it can't be connected with power KVM.*

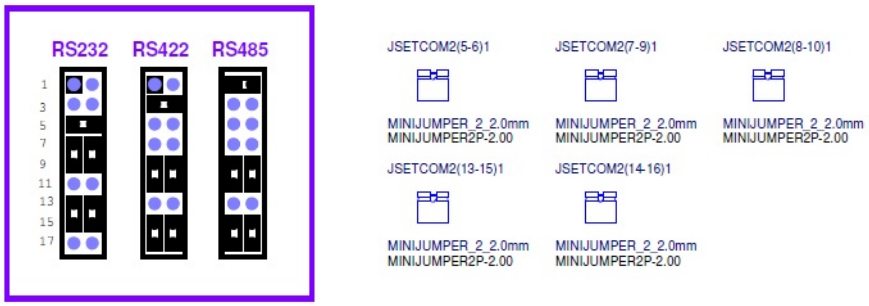
## 2.4 COM1/DVI-D Connector (COM1+DVI 1) Connector




AIMB-585 includes COM1 and DVI interfaces that can drive conventional COM1 and DVI displays. COM1 is a standard 9-pin connector that supports RS-232. Pin assignments for COM1 and DVI connectors are detailed in Appendix B.

## 2.5 Serial Ports (COM1~COM6)




COM2 RS232/422/485 Jumper setting

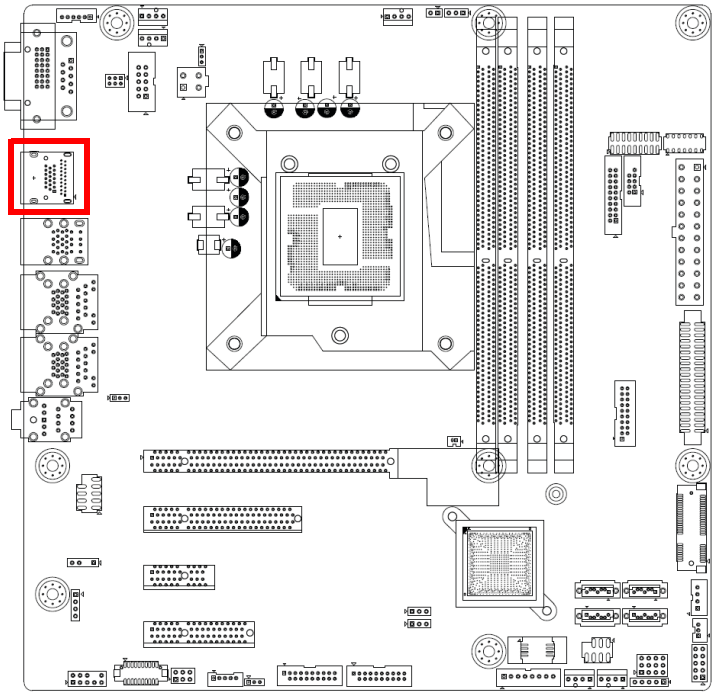
AIMB-585 supports six serial ports. COM1, COM2, COM4-6 supports RS-232. COM2 supports RS-232/422/485 (with 5V/12V power). JSETCOM2 is used to select RS-232/422/485 mode for COM2.

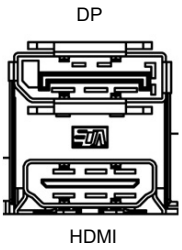
These ports can connect to serial devices, such as a mouse or a printer, or to a communications network.

The IRQ and address ranges for both ports are fixed. However, if you want to disable the port or change these parameters later, you can do this in the system BIOS setup.

Different devices implement the RS-232 standards in different ways. If you have problems with a serial device, be sure to check the pin assignments for the connector.

## 2.6 DisplayPort (DP1)





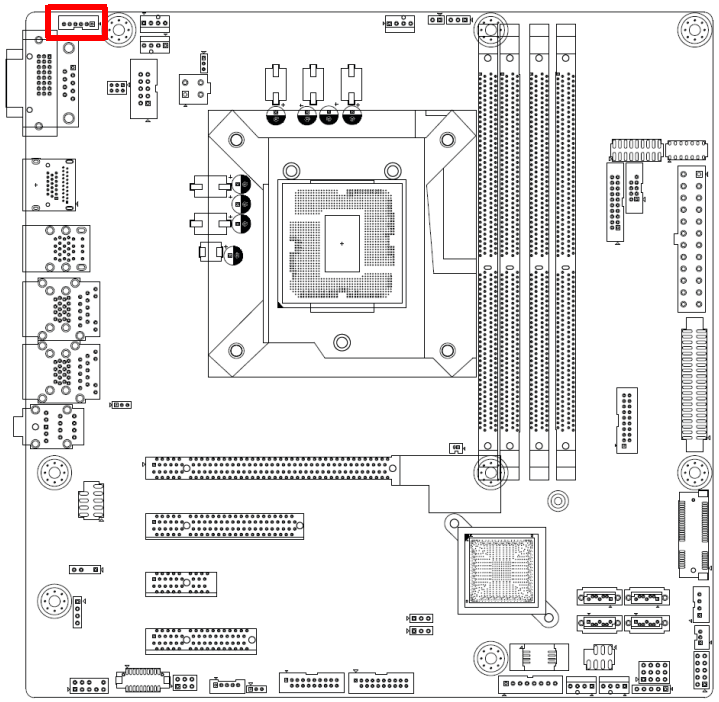

AIMB-585 has one external DP/HDMI connector to support the DisplayPort panel and HDMI monitor.

DP max resolution supported is 4096 x 2304 @ 60 Hz.

HDMI default supports HDMI 1.2.

HDMI 2.0 (4096 x 2160 @ 60 Hz) is supported through the BOM option.

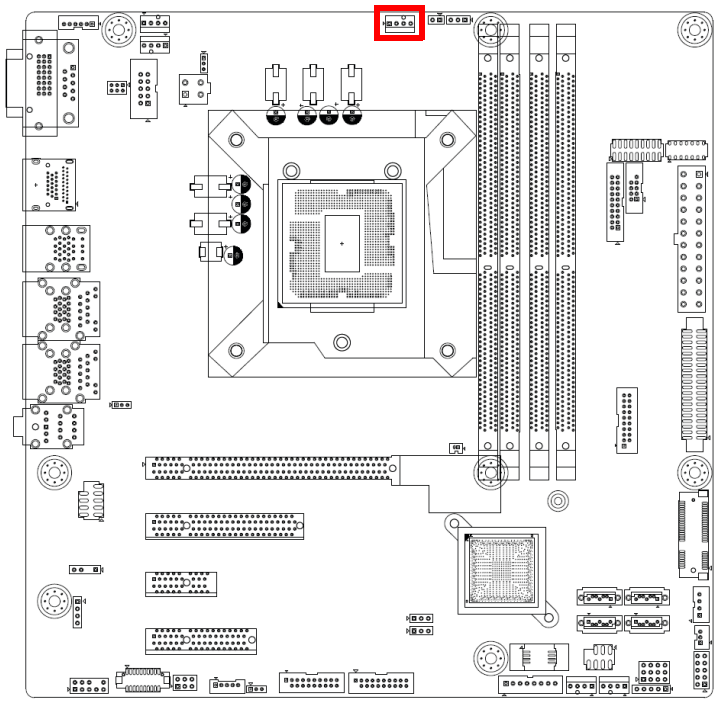
## 2.7 PS/2 Keyboard and Mouse Connector

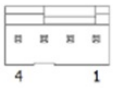



| Pin | Signal |
|---|---|
| 1 | KB_CLK# |
| 2 | KB_DAT# |
| 3 | MS_CLK# |
| 4 | GND |
| 5 | VCC (+5VSB) |
| 6 | MS_DAT# |

6-pin mini-DIN connectors (KBMS1) for supporting the PS/2 keyboard and PS/2 mouse by cable (P/N 1703060191).

## 2.8 CPU Fan Connector (CPU_FAN1)

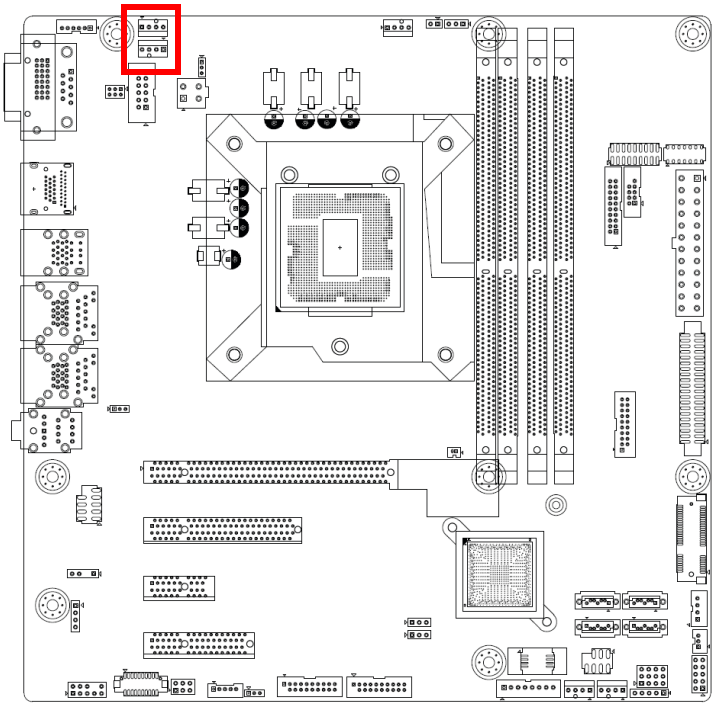





| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | CPU FAN VCC |
| 3 | CPU FAN SPEED |
| 4 | CPU FAN PWM |

If a fan is used, this connector supports cooling fans of 500 mA (6 W) or less.

## 2.9 System FAN Connector (SYSFAN1/2/3/4)

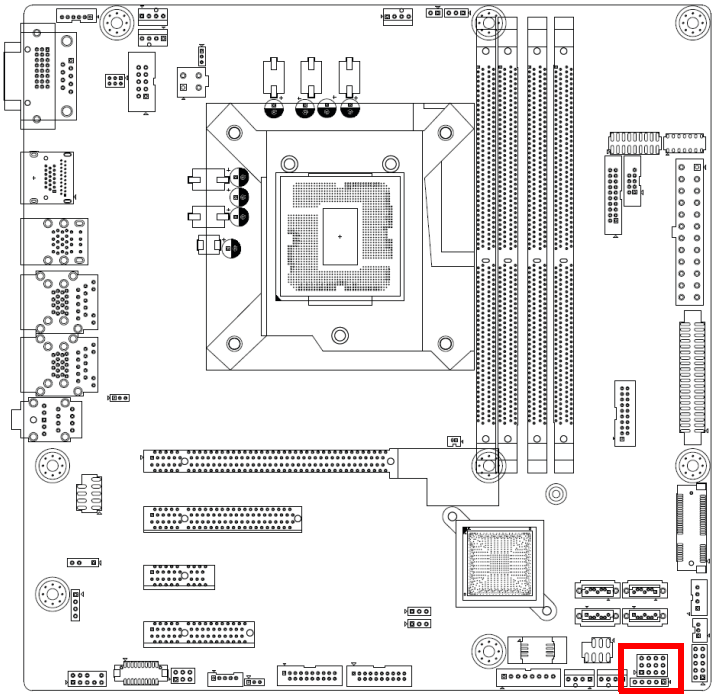


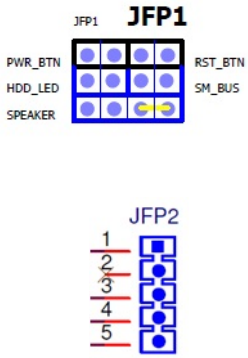

| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | SYSTEM FAN VCC |
| 3 | SYSTEM FAN SPEED |
| 4 | SYSTEM FAN PWM |

If a fan is used, this connector supports cooling fans of 500 mA (6 W) or less. Default only with System Fan 1 & System Fan 2. System Fan 3 and System Fan 4 are BOM optional. Please note that System Fan 3 and System Fan 4 can't have the rotational speed monitored in the BIOS. System Fan 3 will be controlled by System Fan 1 and System Fan 4 will be controlled by System Fan 2.

## 2.10 Front Panel Connectors (JFP1/JFP2)

There are several headers for monitoring and controlling AIMB-585.






### 2.10.1 ATX Soft Power Switch (JFP1/PWR_SW)

If your computer case is equipped with an ATX power supply, you should connect the power on/off button on your computer case to (JFP1/ PWR_SW) for convenient power on and off.

### 2.10.2 Reset (JFP1/RESET)

Many computer cases offer the convenience of a reset button. Connect the wire for the reset button.

### 2.10.3 HDD LED (JFP1/HDDLED)

You can connect an LED to the connector (JFP1/HDDLED) to indicate when the HDD is active.

### 2.10.4 External Speaker (JFP1/SPEAKER)

JFP2/SPEAKER is a 4-pin connector for an external speaker. If there is no external speaker, the AIMB-585 provides an onboard buzzer as an alternative. To enable the buzzer, set pins 7 & 10 as closed.

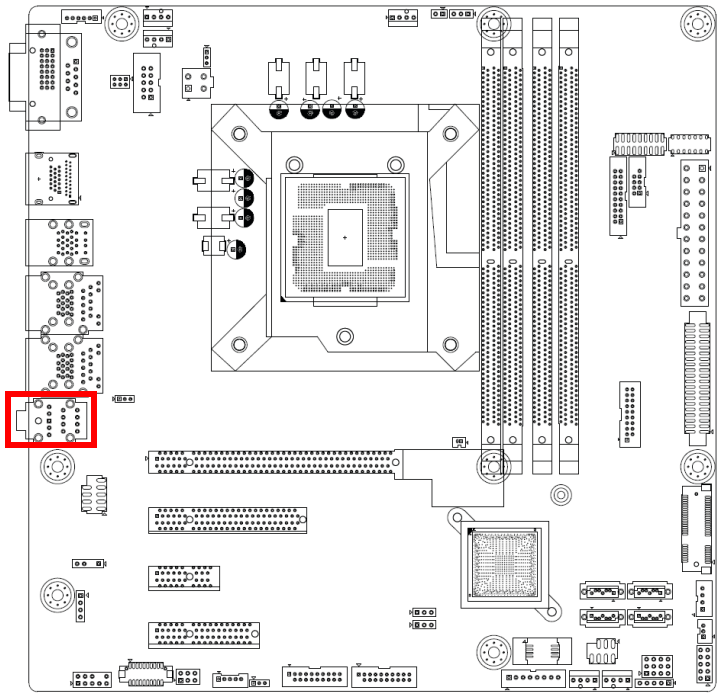
### 2.10.5 Power LED and Keyboard Lock Connector (JFP2/PWR_LED & KEY LOCK)

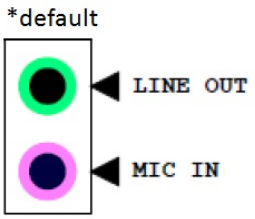
(JFP2/PWR_LED & KEY LOCK) is a 5-pin connector for the power on LED and key lock function. Refer to Appendix B for detailed information on the pin assignments. The power LED cable should be connected to pins 1-3. The key lock button cable should be connected to pins 4-5. There are 3 modes for the power supply connection. The first is “ATX power mode”; the system turns on/off via a momentary power button. The second is “AT Power Mode”; the system turns on/off via the power supply switch. The third is “AT Power Mode”, which makes use of the front panel power switch. The power LED status is indicated in the following table:

**Table 2.2: ATX Power Supply LED Status (Not supported for AT power)**

| Power Mode | LED (ATX Power Mode) (On/Off via the Button) | LED (AT power Mode) (On/Off by Switching the Power Supply On/Off) | LED (AT power Mode) (On/Off via the Front Panel Switch) |
|---|---|---|---|
| PSON1 (on the back plane) jumper setting | pins 2-3 closed | pins 1-2 closed | Connect pins 1 & 2 to the panel switch via cable |
| System On | On | On | On |
| System Off | Off (Windows 7)<br>Slow Flashes (Windows 8) | Off | Off |
| S3 | Fast flashes | N/A | N/A |
| S4 | Slow flashes | N/A | N/A |

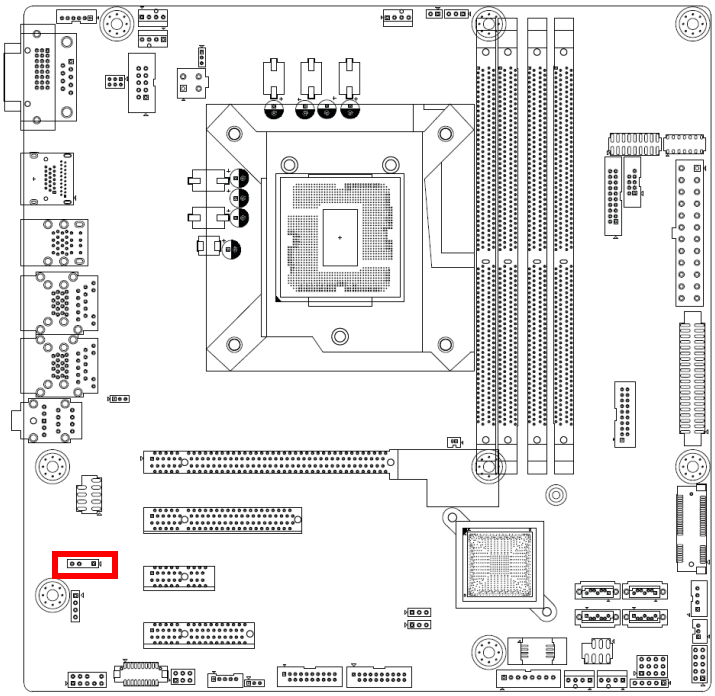
## 2.11 Line-Out, Mic-In Connector (AUDIO1)





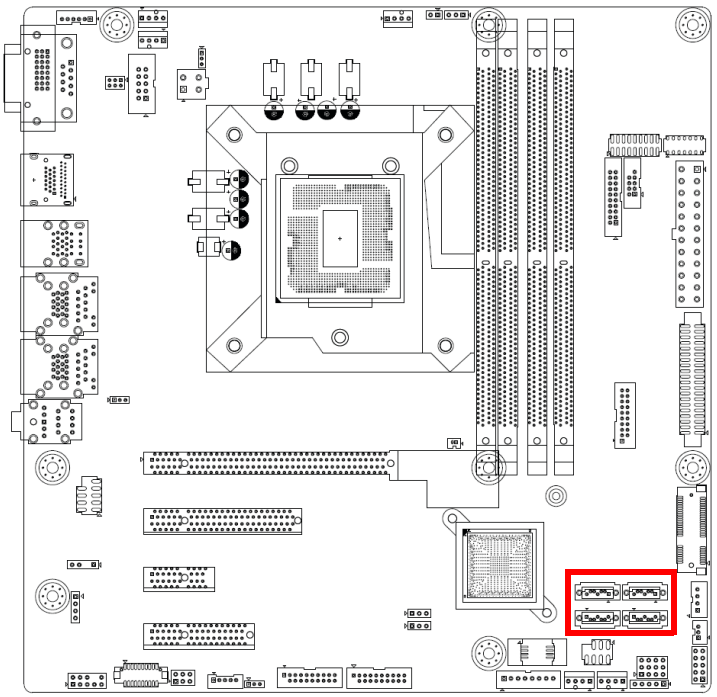
## 2.12 Digital Audio Connector (SPDIF_OUT1)

This connector is for the S/PDIF audio module to allow digital sound output. Connect one end of the S/PDIF audio cable to this connector and the other end to the S/PDIF module.



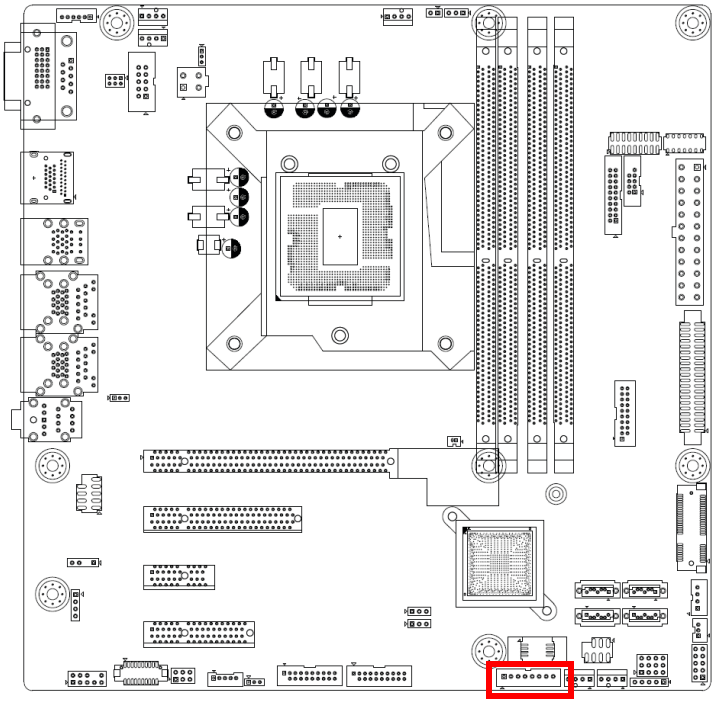
***Note!*** *The S/PDIF module is purchased separately.*

## 2.13 Serial ATA Interface (SATA1 ~ SATA4)



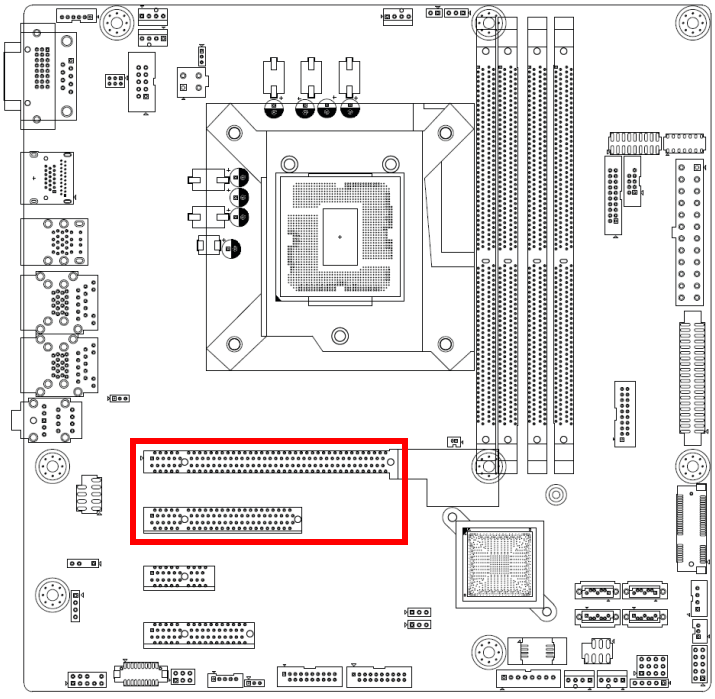
AIMB-585 features a high-performance Serial ATA III interface (up to 600 MB/s) which eases hard drive cabling with thin, space-saving cables.

## 2.14 8-Pin Alarm Board Connector (VOLT1)



VOLT1 connects to the alarm board on the chassis. These alarm boards give warnings if a power supply or fan fails, or if the chassis overheats.

## 2.15 PCI Express x16 / PCI Express x8 Slot

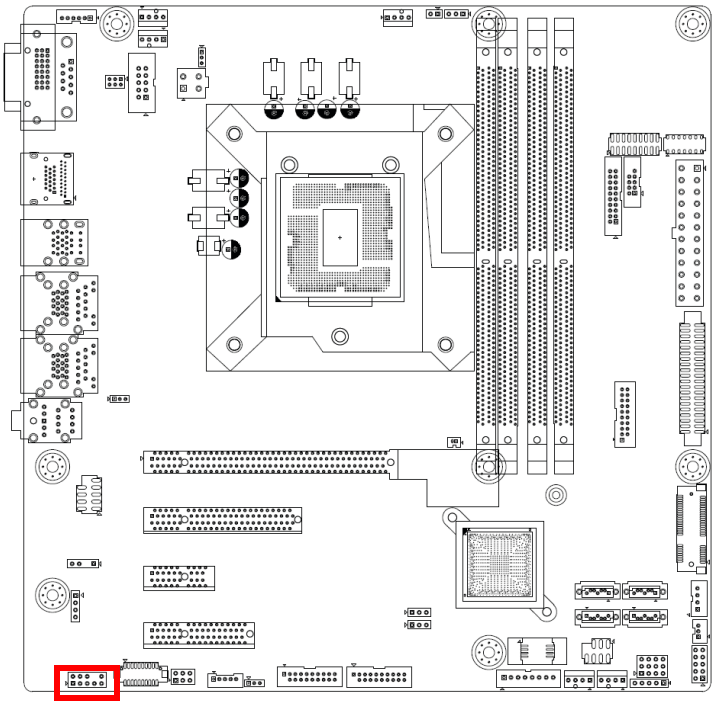


AIMB-585 provides a PCIe x16 slot and PCIe x8 slot for users to install add-on cards when their applications require higher graphics performance than the CPU embedded graphics controller can provide.

***Note!*** *When the PCIe x8 slot is used, the PCIe x16 slot only supports x8 bandwidth automatically.*

## 2.16 Front Panel Audio Connector (FPAUD1)

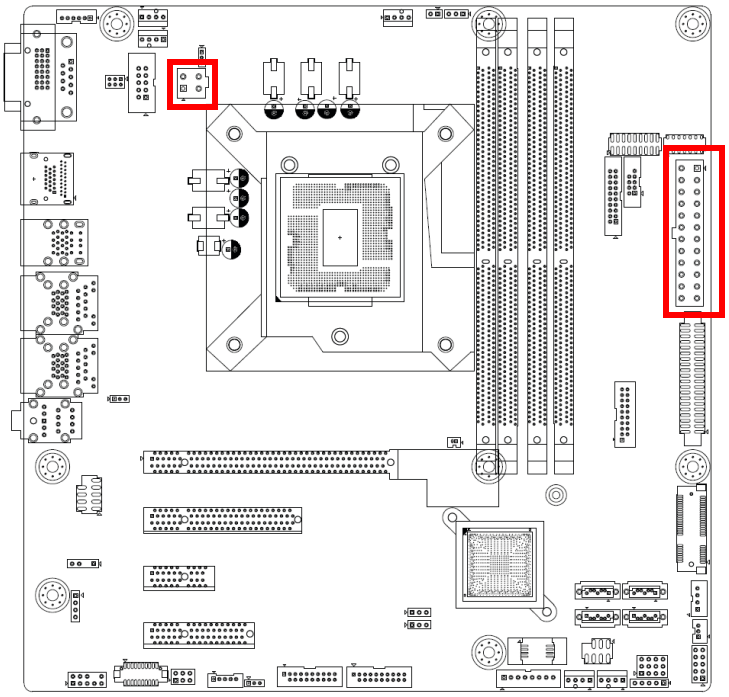
This connector is for a chassis-mounted front panel audio I/O module that supports either HD Audio or the legacy AC'97 (optional) audio standard. Connect this connector with the front panel audio I/O module cable.



***Note!*** *For motherboards with the optional HD Audio feature, we recommend that you connect a high-definition front panel audio module to this connector to take advantage of the motherboard's high definition audio capability.*

## 2.17 ATX Power Connector (EATXPWR1, ATX12V1)

This connector is for an ATX Micro-Fit power supply. The plugs from the power supply are designed to fit these connectors in only one direction. Determine the proper orientation and push down firmly until the connectors mate completely.

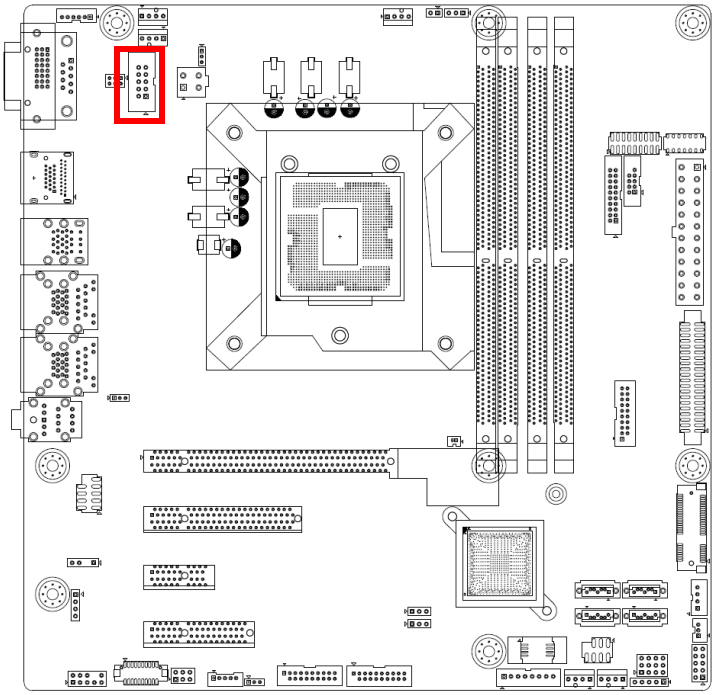


***Note!***

1. Please connect the ATX12V1 connector with the PSU ATX 12V 4-pin connector.
2. For a fully configured system, we recommend that you use a power supply unit (PSU) that complies with ATX 12 V Specification 2.0 (or later version) and provides a minimum power of 180 W.

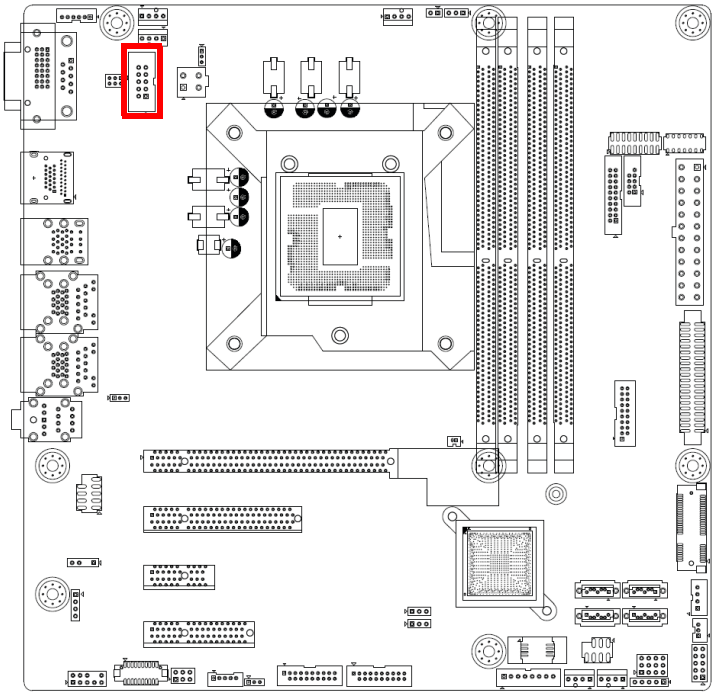
## 2.18 VGA (VGA1)

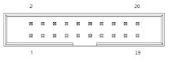
AIMB-585 has one 2 x 5-pin header on the board for VGA (VGA1), but this function is BOM optional.



| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | RED | 6 | DDC DAT |
| 2 | DDC CLK | 7 | VSYNC |
| 3 | GREEN | 8 | GND |
| 4 | Advantech define | 9 | HSYNC |
| 5 | BLUE | 10 | VCC (+5V) |

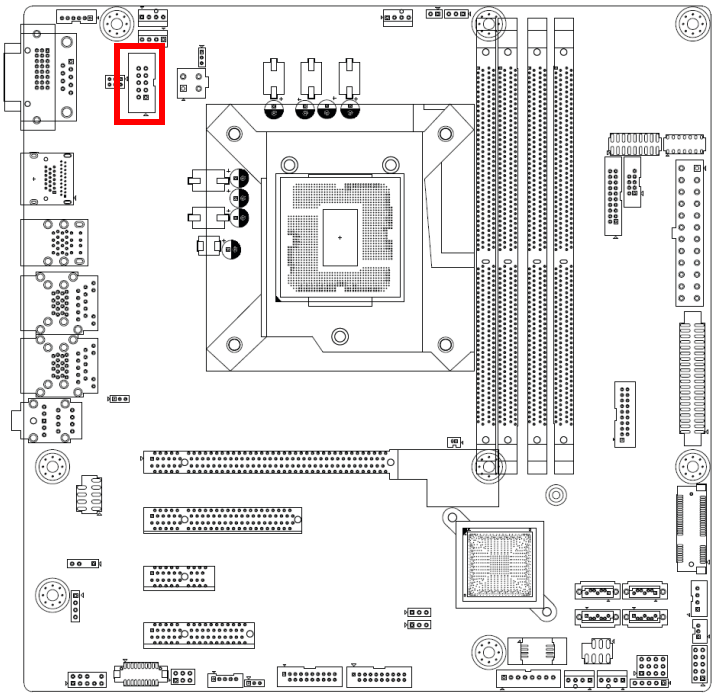
## 2.19 General Purpose I/O Connector (GPIO1)



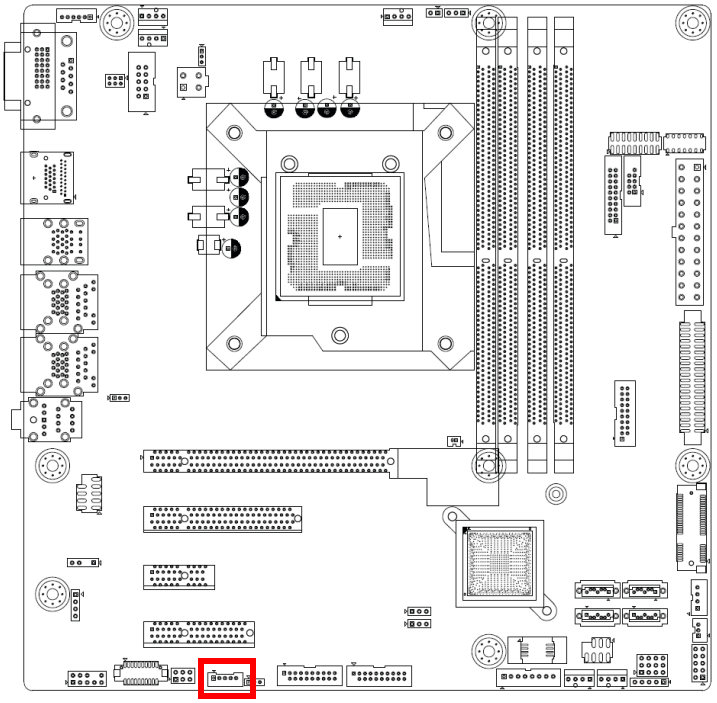


| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GPIO0 | 2 | GPIO8 |
| 3 | GPIO1 | 4 | GPIO9 |
| 5 | GPIO2 | 6 | GPIO10 |
| 7 | GPIO3 | 8 | GPIO11 |
| 9 | GPIO4 | 10 | GPIO12 |
| 11 | GPIO5 | 12 | GPIO13 |
| 13 | GPIO6 | 14 | GPIO14 |
| 15 | GPIO7 | 16 | GPIO15 |
| 17 | +5VSB | 18 | GND |
| 19 | +5VSB | 20 | GND |

## 2.20 eDP Connector (eDP1)



## 2.21 EDP Backlight Inverter (INV1)




| Pin | Signal |
|---|---|
| 1 | +12V |
| 2 | GND |
| 3 | BKL EN |
| 4 | BKL CTRL |
| 5 | +5V |

# Chapter 3

## BIOS Operation

## 3.1 Introduction

With the AMI BIOS Setup program, you can modify BIOS settings to control the special features of your computer. The Setup program uses a number of menus for making changes. This chapter describes the basic navigation of the AIMB-585 setup screens.

## 3.2 BIOS Setup

The AIMB-585 Series system has AMI BIOS built in, with a setup utility that allows users to configure required settings or to activate certain system features.

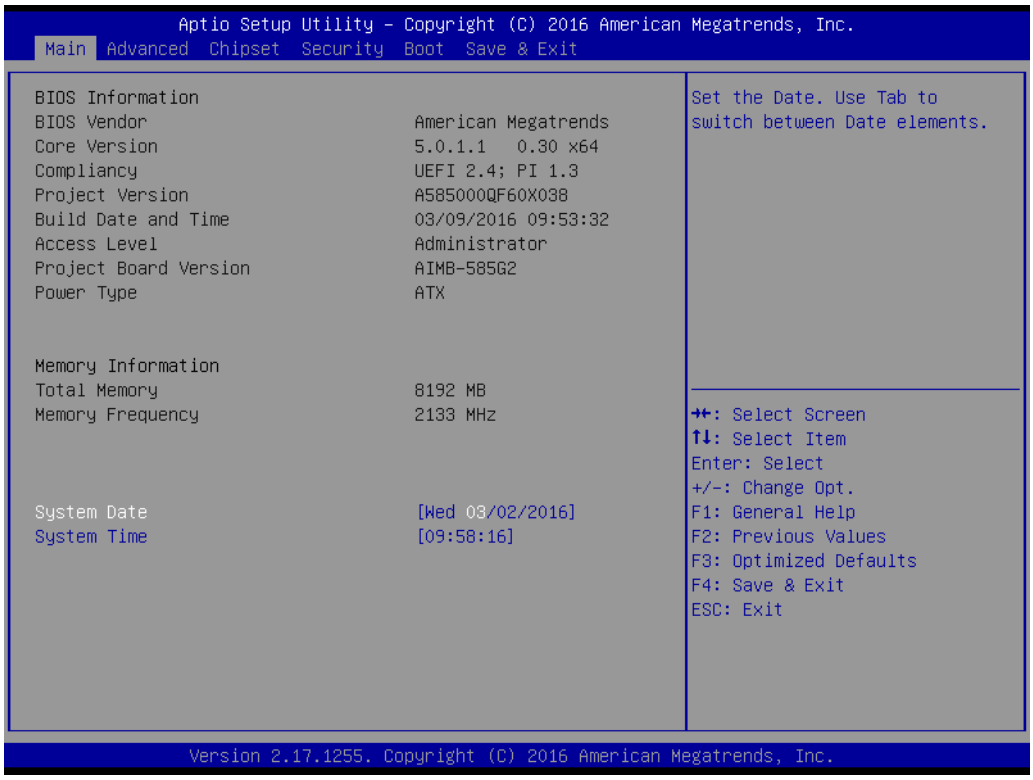
The setup utility saves the configuration in the flash memory of the motherboard. When the power is turned off, the battery on the board supplies the necessary power to preserve the flash memory.

When the power is turned on, press the <Del> or <Esc> button during the BIOS POST (Power-On Self Test) to access the CMOS SETUP screen.

| **Control Keys** | |
|---|---|
| < ← >< → > | Select Screen |
| < ↑ >< ↓ > | Select Item |
| <Enter> | Select |
| <+/-> | Change Opt |
| <F1> | General help |
| <F2> | Previous Values |
| <F3> | Optimized Defaults |
| <F4> | Save & Exit |
| <Esc> | Exit |

### 3.2.1 Main Menu

Press <Del> or <Esc> to enter the AMI BIOS CMOS Setup Utility. The Main Menu will appear on the screen. Use the arrow keys to select among the items and press <Enter> to accept or enter the sub-menu.




The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

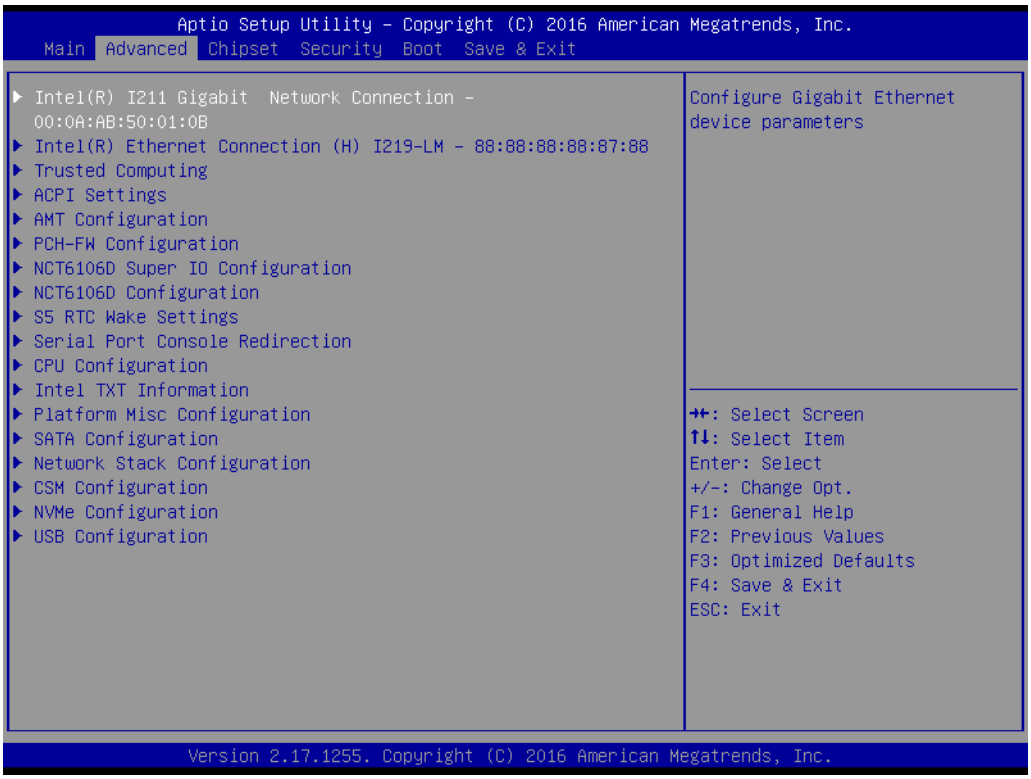
Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

- **System Time / System Date**

  Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

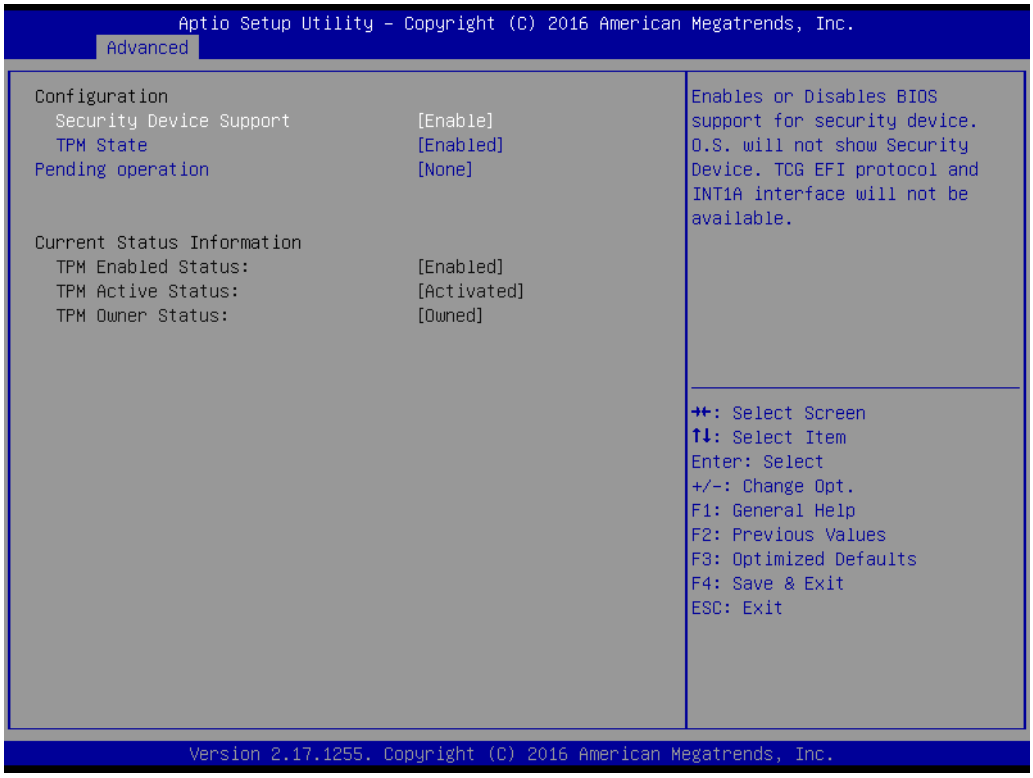
### 3.2.2 Advanced BIOS Features

Select the Advanced tab from the AIMB-585 setup screen to enter the Advanced BIOS Setup screen. You can select any of the items in the left frame of the screen, such as CPU Configuration, to go to the sub-menu for that item. You can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screen is shown below. The sub-menus are described on the following pages.



### 3.2.2.1 Trusted Computing

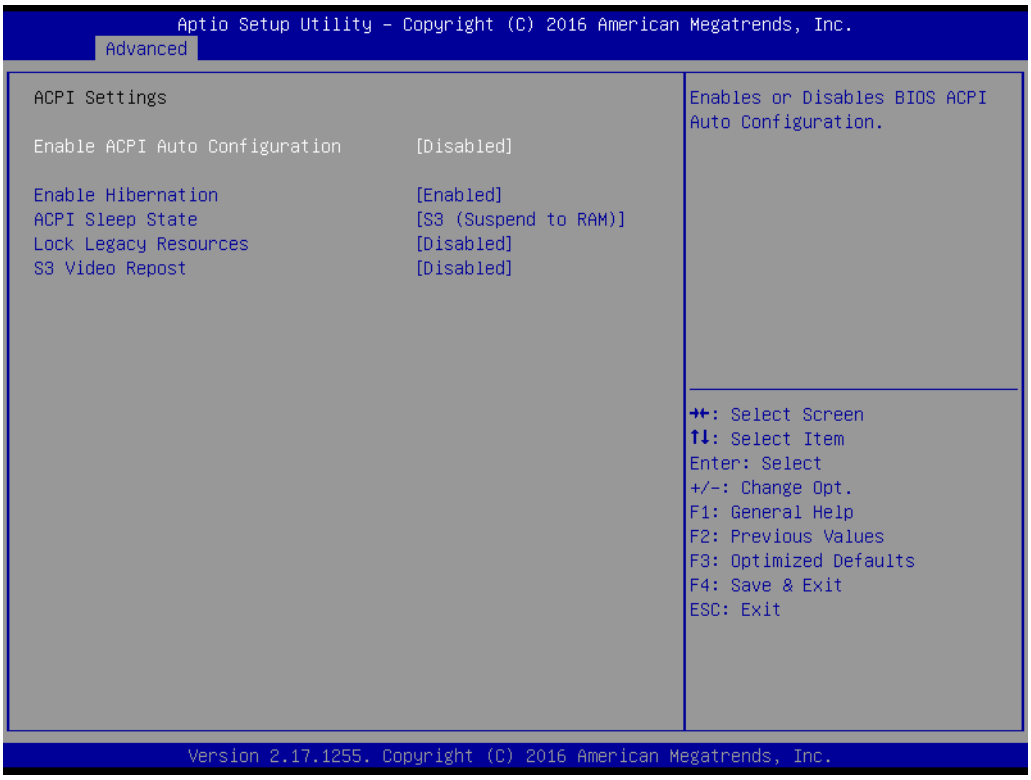
You can enable/disable TPM (TPM 1.2/2.0) setup in BIOS. TPM (Trusted Platform Module) is a secure key generator and key cache management component that enables protected storage of encryption keys and authentication credentials for enhanced security capabilities.




- **Security Device Support [ Disable ]**

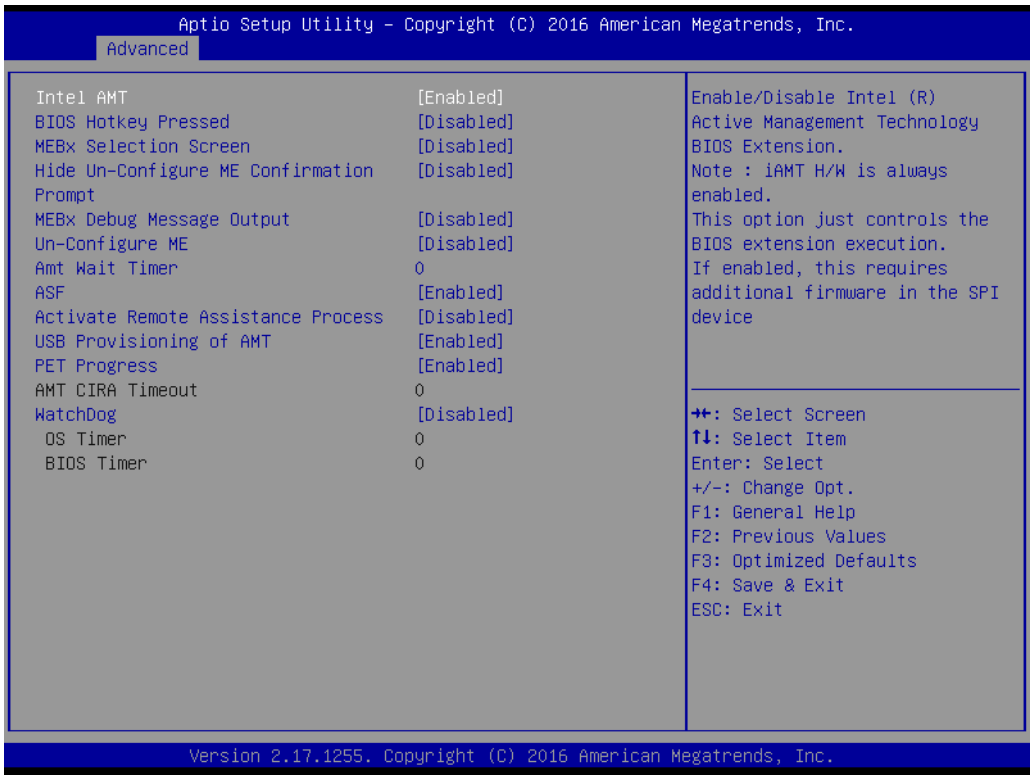
***Note!*** *TCG EFI Protocol and INT1A interface won't be available.*

### 3.2.2.2 ACPI Settings




- **Enable ACPI Auto Configuration [ Disabled]**
  Enable/Disable BIOS ACPI auto configuration.
- **Enable Hibernation [ Enabled ]**
  Enable/Disable System ability to Hibernate (OS/S4 Sleep State). This option may be not effective with some OS.
- **ACPI Sleep State [ Auto ]**
  Select the ACPI sleep state the system will enter when the SUSPEND button is pressed.
- **Lock Legacy Resources [ Disabled ]**
  Enable/Disable Lock Legacy Resources.
- **S3 Video Repost [ Disabled ]**
  Enable/Disable S3 Video Repost.

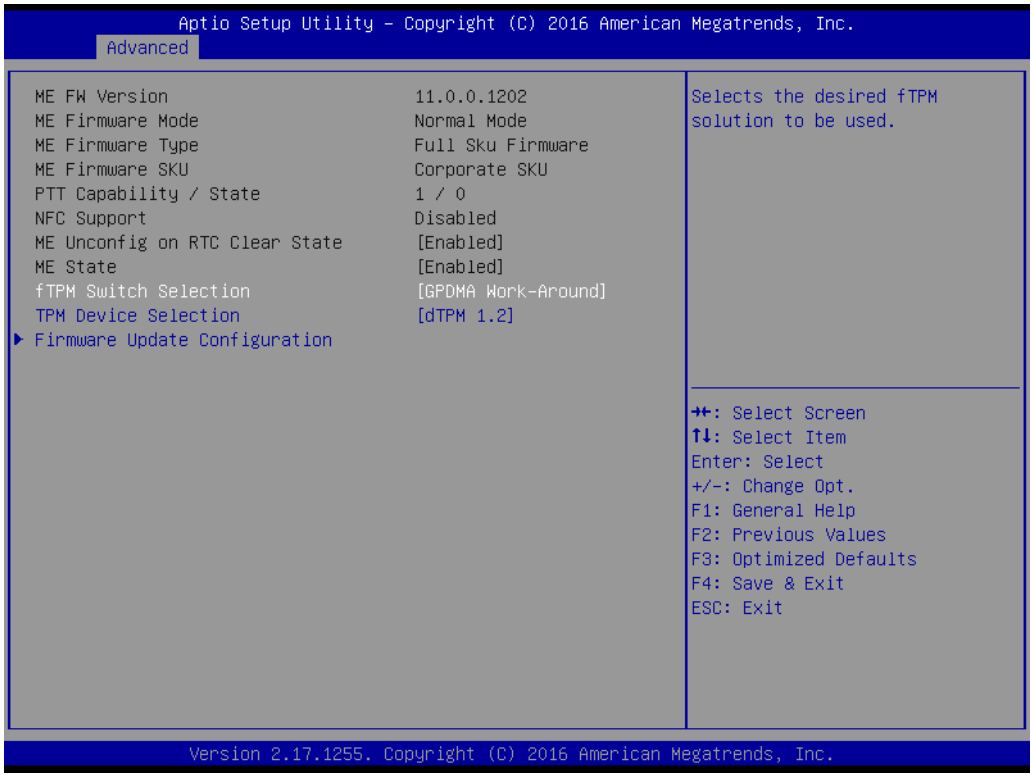
### 3.2.2.3 AMT Configuration



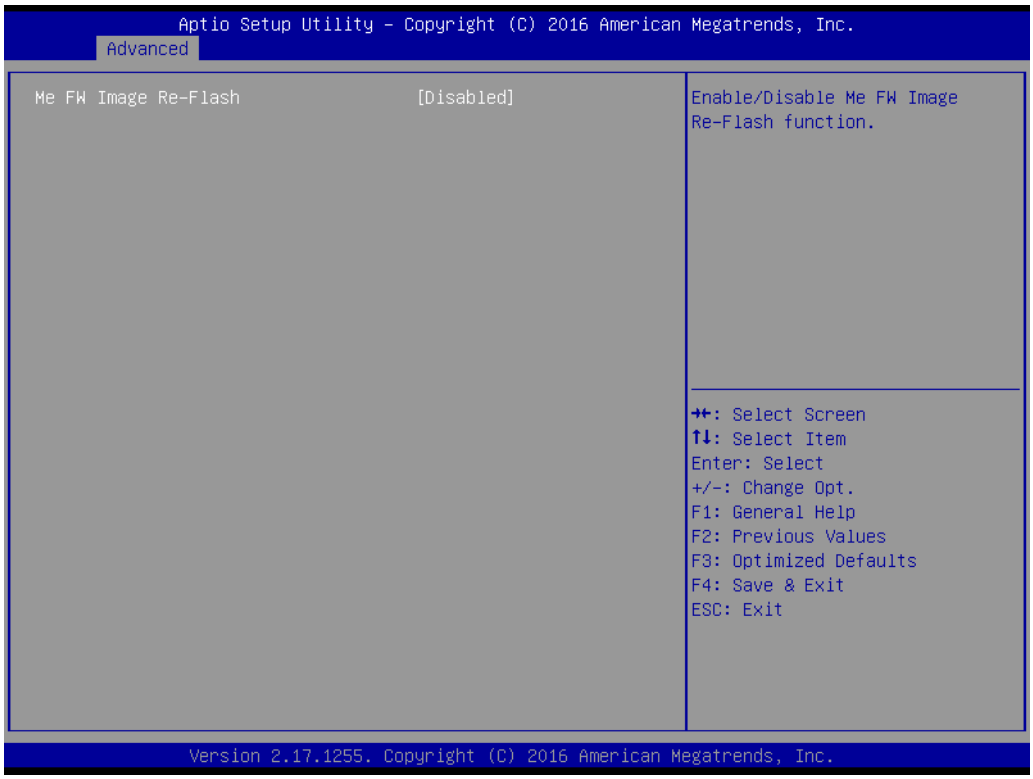

- **Intel AMT [ Enabled ]**
  This item allows users to enable or disable Intel AMT BIOS extension.
- **BIOS Hotkey Pressed [ Disabled ]**
  Enable/Disable BIOS hotkey press.
- **MEBx Select Screen [ Disabled ]**
  Enable/Disable MEBx selection screen.
- **Hide Un-Configure ME Confirmation [ Disabled ]**
  Hide Un-Configure ME without password Confirmation Prompt.
- **MEBx Debug Message Output [ Disabled ]**
  Enable MEBx debug message output.
- **Un-Configure ME [ Disabled ]**
  Sets this item to [Disabled] to unconfigure AMT/ME without using a password or set it as [Enabled] to use a password.
- **Amt Wait timer [0]**
  Set timer to wait before sending ASF_GET_BOOT_OPTIONS.
- **Disable ME [ Disabled ]**
  Set ME to Soft Temporary Disabled.
- **ASF [ Enabled ]**
  Enable/Disable Alert Specification Format.
- **Active Remote Assistance Process [ Disabled ]**
  Trigger CIRA boot.
- **USB Configure [ Enable ]**
  Enable/Disable USB Configure function.
- **PET Progress [ Enable ]**
  User can Enable/Disable PET Events progress to receive PET events or not.

- **AMT CIRA Timeout [ 0 ]**
  OEM defined timeout for MPS connection to be established.
- **Watchdog [ Disabled ]**
  When set to [Enabled], the Watchdog timer will monitor the time taken for each task performed by software or hardware.
  - **OS Timer [ 0 ]**
    Set OS watchdog timer.
  - **BIOS Timer [ 0]**
    Set BIOS watchdog timer.

### 3.2.2.4 PCH FM Configuration

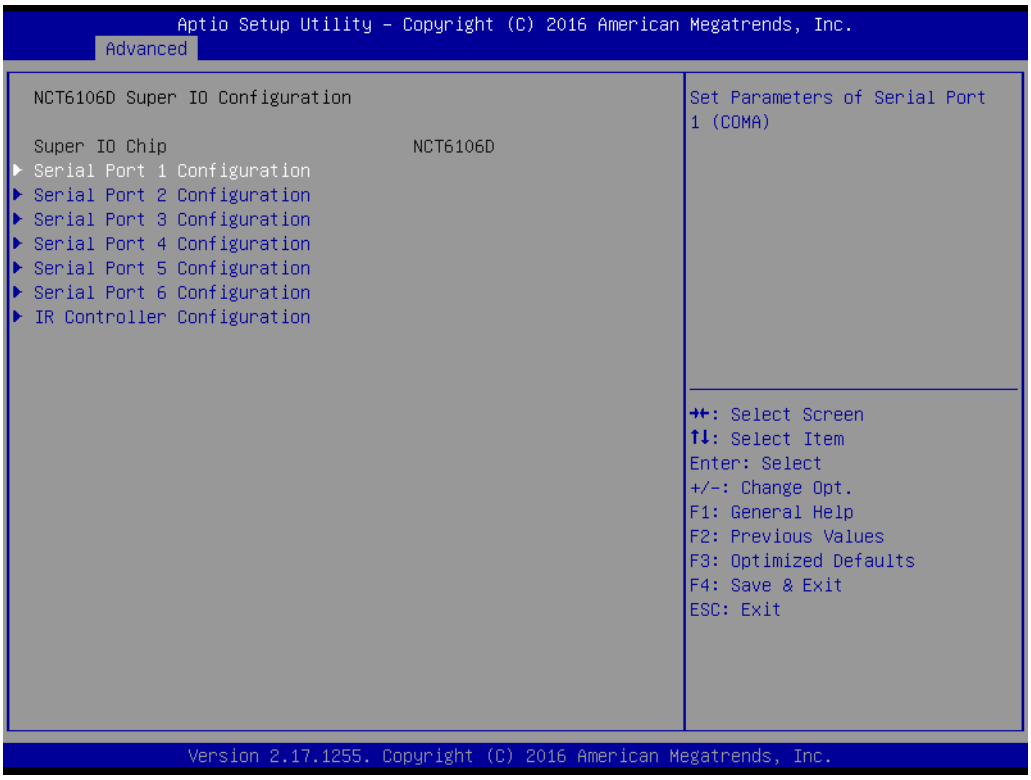



- **MEDS BIOS Status Code [ Disable ]**
- **Firmware update Configuration**



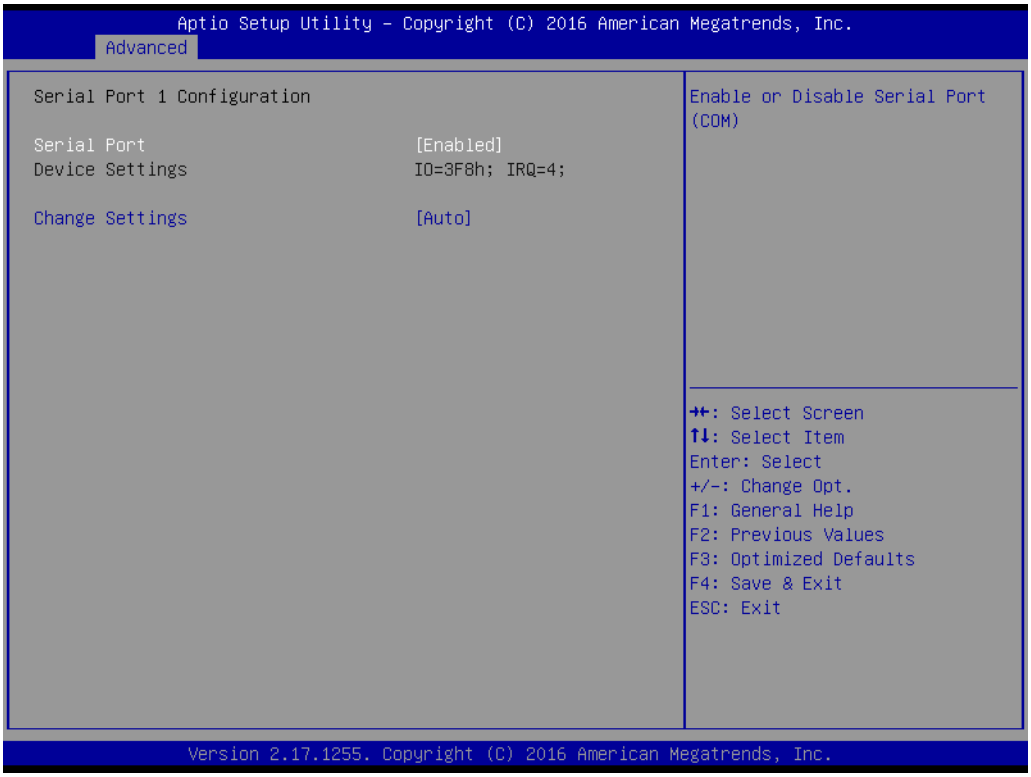

  - **ME FW Image Re-Flash [ Disabled ]**

### 3.2.2.5 NCT6106D Super IO Configuration



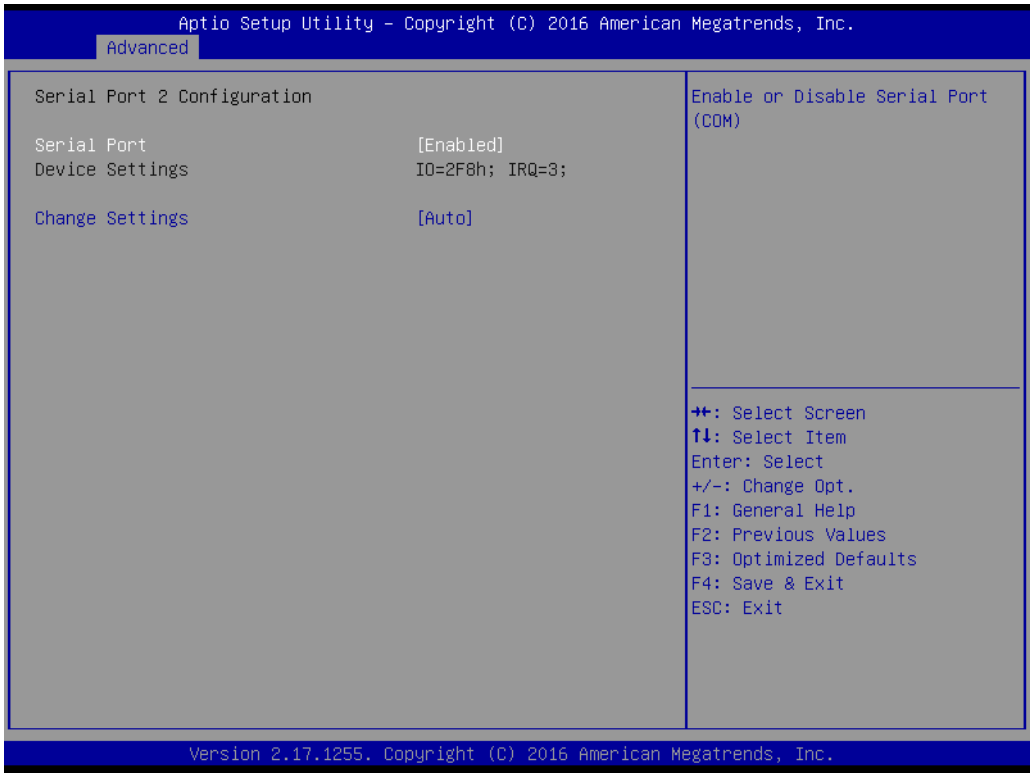

- **Super IO Chip [ NCT6106D ]**

- **Serial Port 1 Configuration**



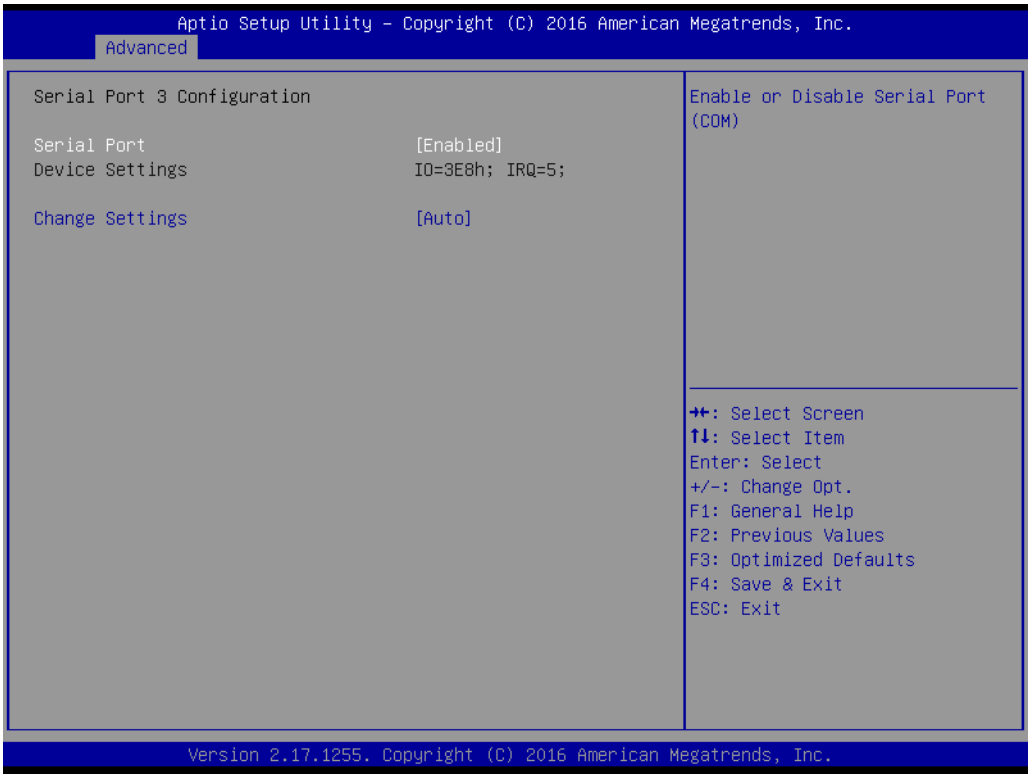
- **Serial Port [ Enabled ]**
- **Device Settings: IO=3F8h; IRQ =4**
- **Change Settings [ Auto ]**
  To select an optimal setting for serial port 1.

## Serial Port 2 Configuration



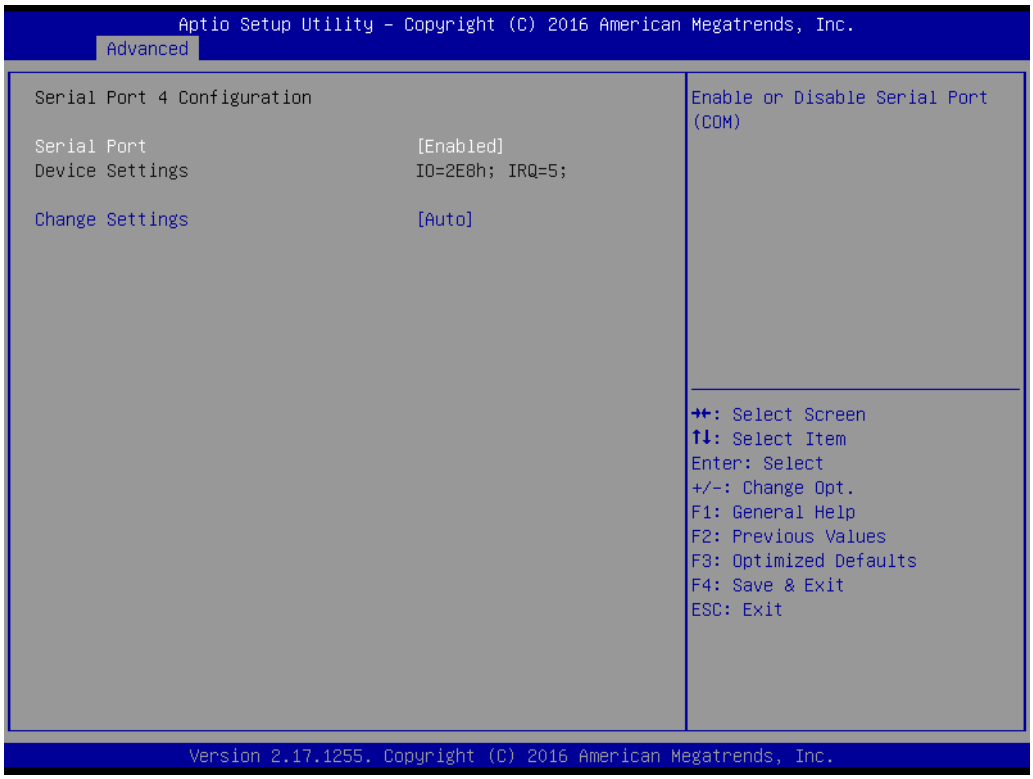

- **Serial Port [ Enabled ]**
- **Device Settings: IO=2F8h; IRQ =3**
- **Change Setting [ Auto ]**
  To select an optimal setting for serial port 2.

## Serial Port 3 Configuration



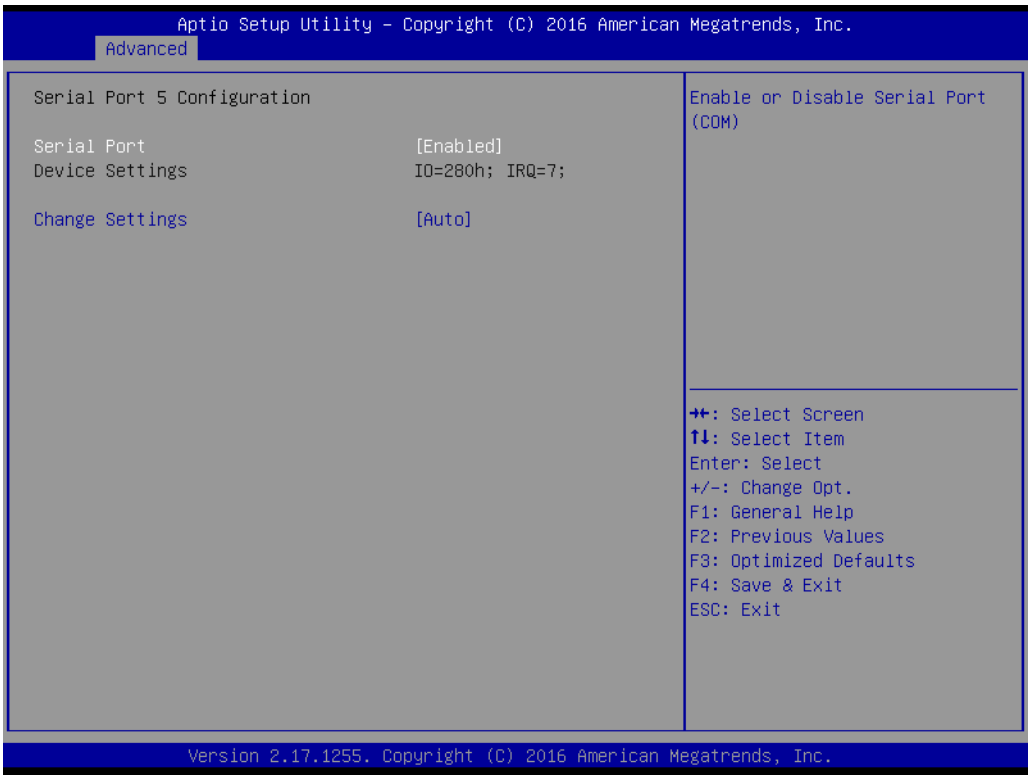

- **Serial Port [ Enabled ]**
  Enable/Disable Serial Port 3.
- **Device Settings: IO=3E8h; IRQ =5**
- **Change Settings [ Auto ]**
  Select an optimal setting for serial port 3.

## Serial Port 4 Configuration



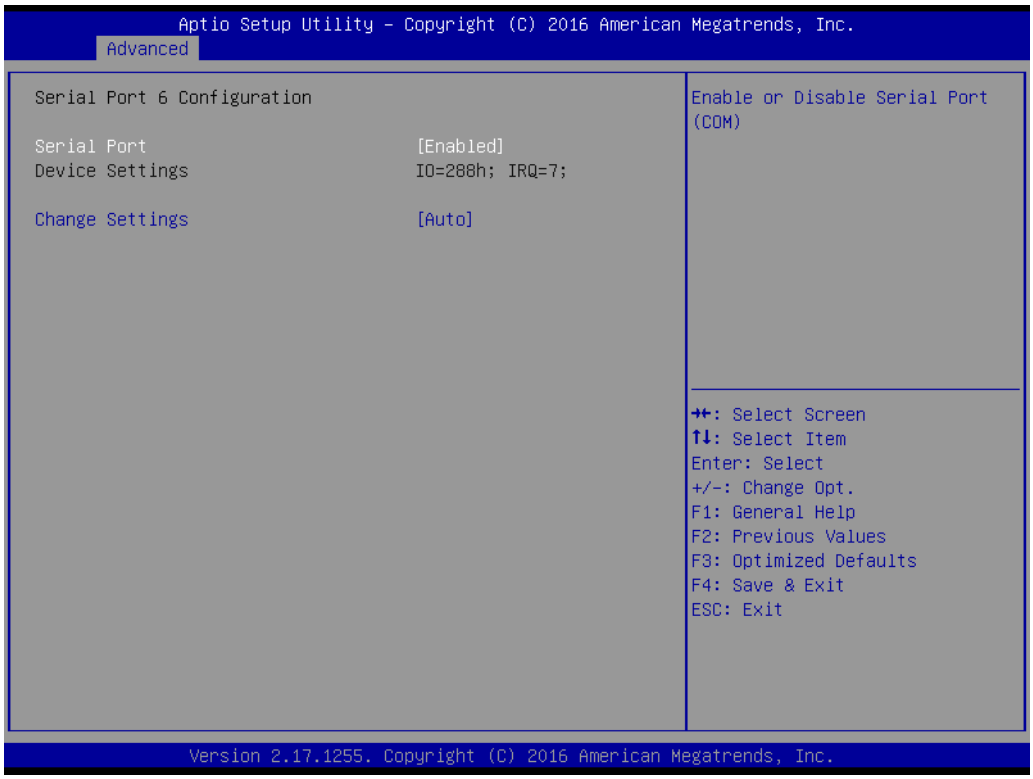

- **Serial Port [Enabled]**
  Enable/Disable serial port 4.
- **Device Settings: IO=2E8h; IRQ =5**
- **Change Settings [ Auto ]**
  Select an optimal setting for serial port 4.

## Serial Port 5 Configuration




- **Serial Port [Enabled]**
  Enable/Disable serial port 5.
- **Device Settings: IO=280h; IRQ =7**
- **Change Settings [ Auto ]**
  Select an optimal setting for serial port 5.

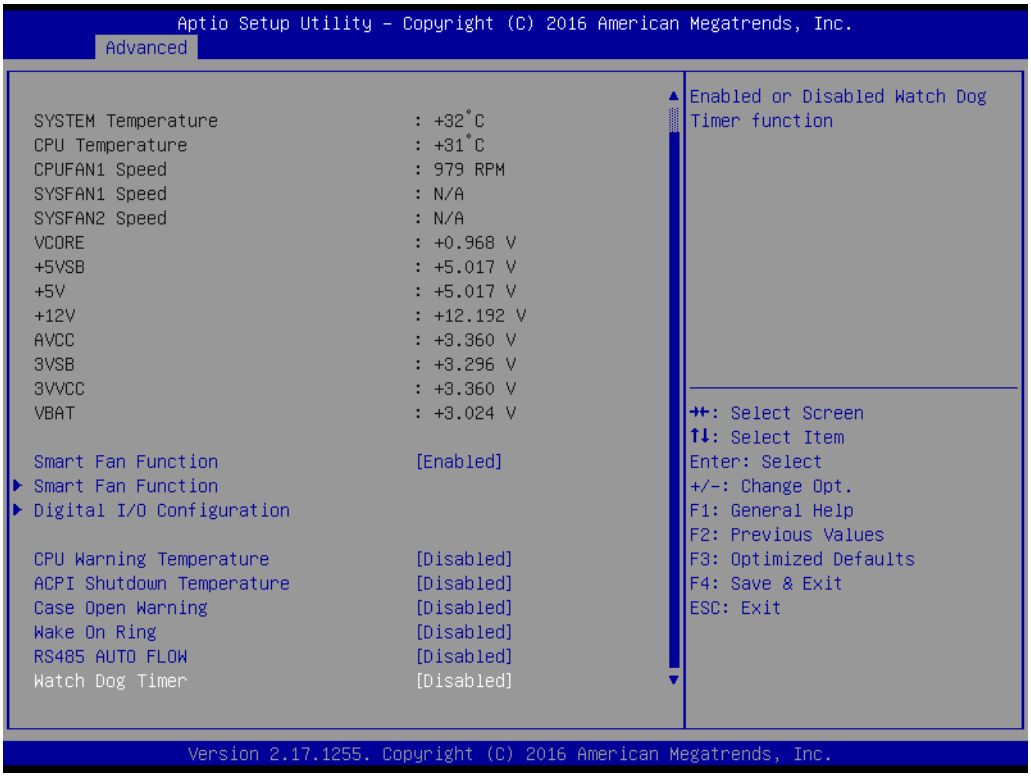
## Serial Port 6 Configuration




- **Serial Port [ Enabled ]**
  Enable/Disable serial port 6.
- **Device Settings: IO=288h; IRQ =7**
- **Change Setting [ Auto ]**
  Select an optimal setting for serial port 6.

### 3.2.2.6 NCT6106D Configuration

- **PC Health Status**



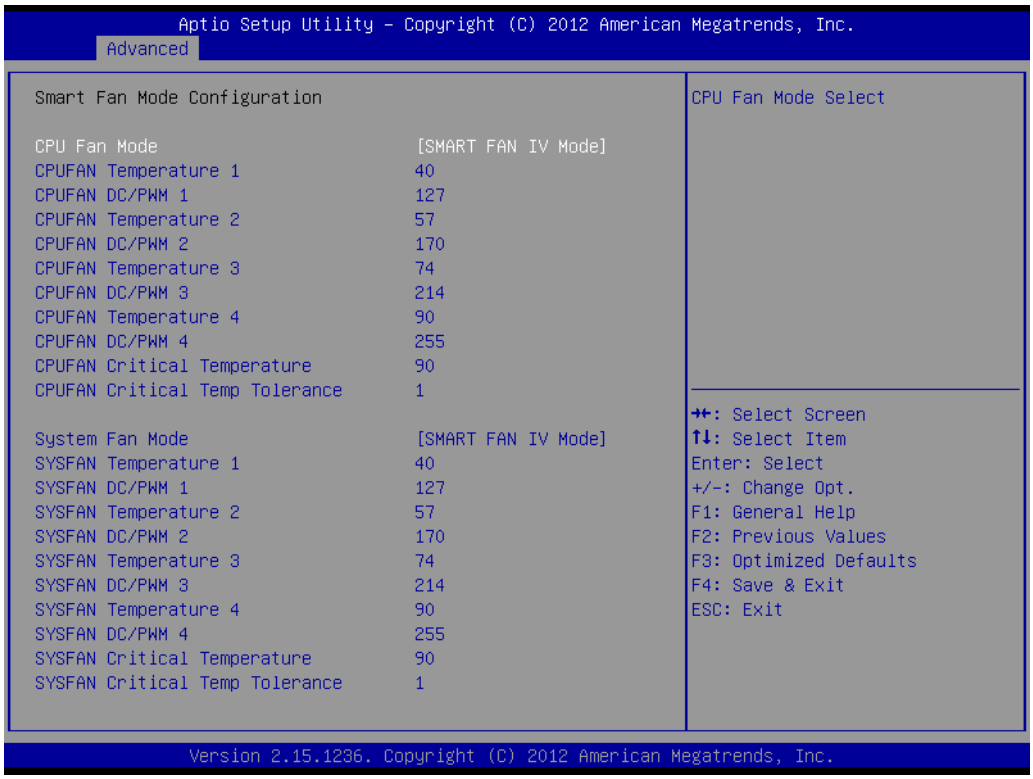

– **CPU Warning Temperature [ Disabled ]**

Use this to set the CPU warning temperature threshold. When the system reaches the warning temperature, the speaker will beep.

– **ACPI Shutdown Temperature [ Disabled ]**

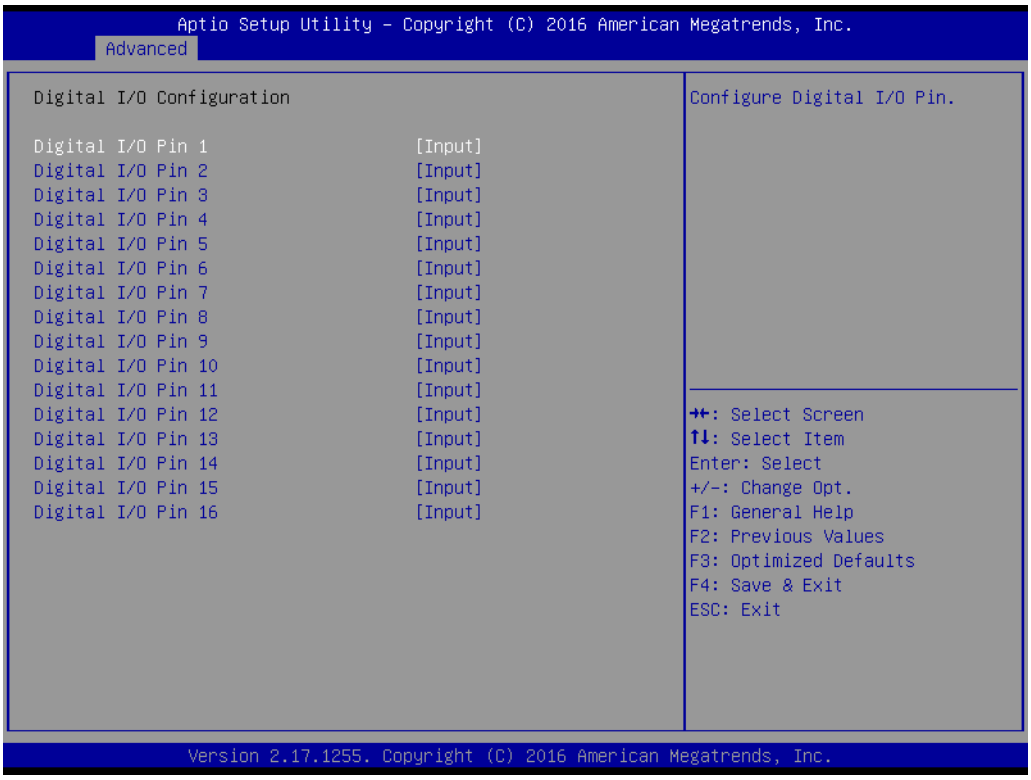
Use this to set the ACPI shutdown temperature threshold. When the system reaches the shutdown temperature, it will be automatically shut down by ACPI OS to protect the system from overheating damage.

## Smart Fan Mode Configuration




- **CPU FAN Mode [ SMART FAN IV Mode ]**
  The item shows you CPU temperature and fan speed (PWM) information.
- **SYSFAN Mode [ SMART FAN IV Mode ]**
  The item shows you system temperature and fan speed (PWM) information.

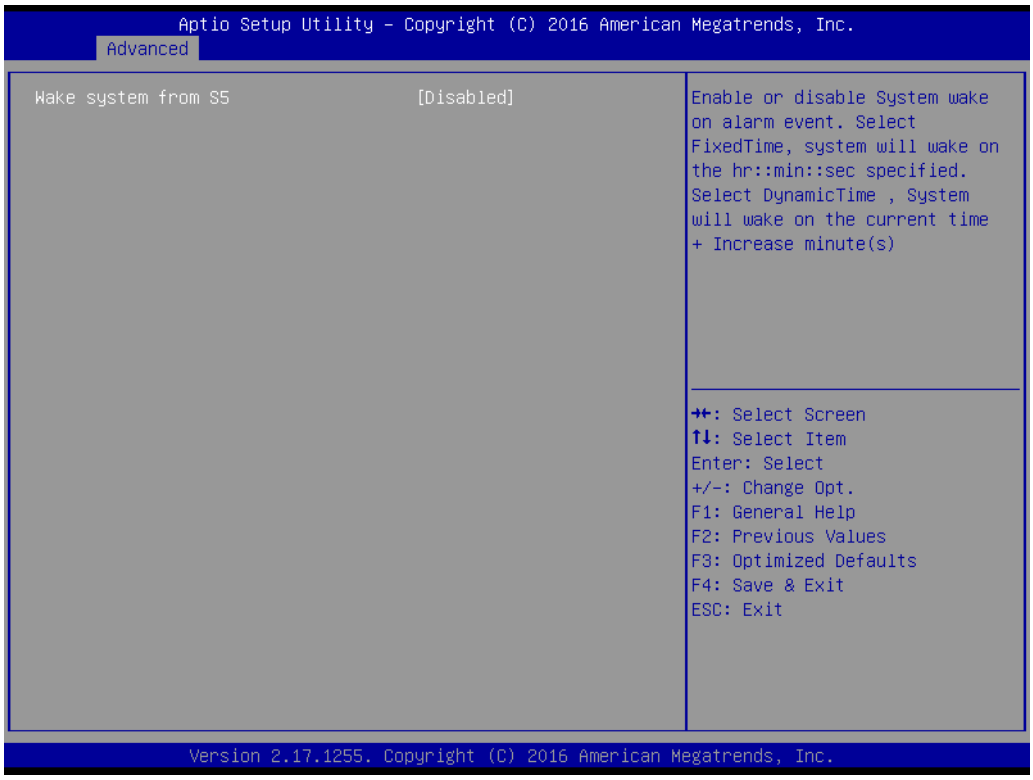
## Digital I/O Configuration




– **Digital I/O Pin 1 - 16 [ Input ]**

### 3.2.2.7 S5RTC Wake Settings

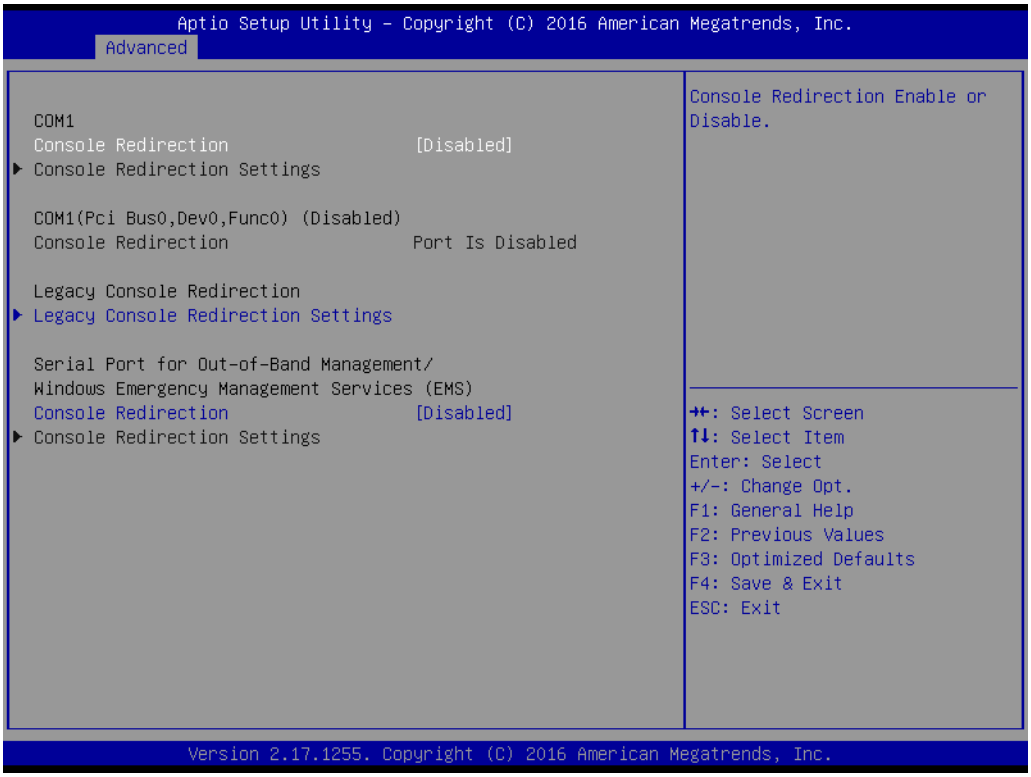
This item allows you to enable or disable system wake on alarm event.




- **Wake system with Fixed Time [ Disabled ]**

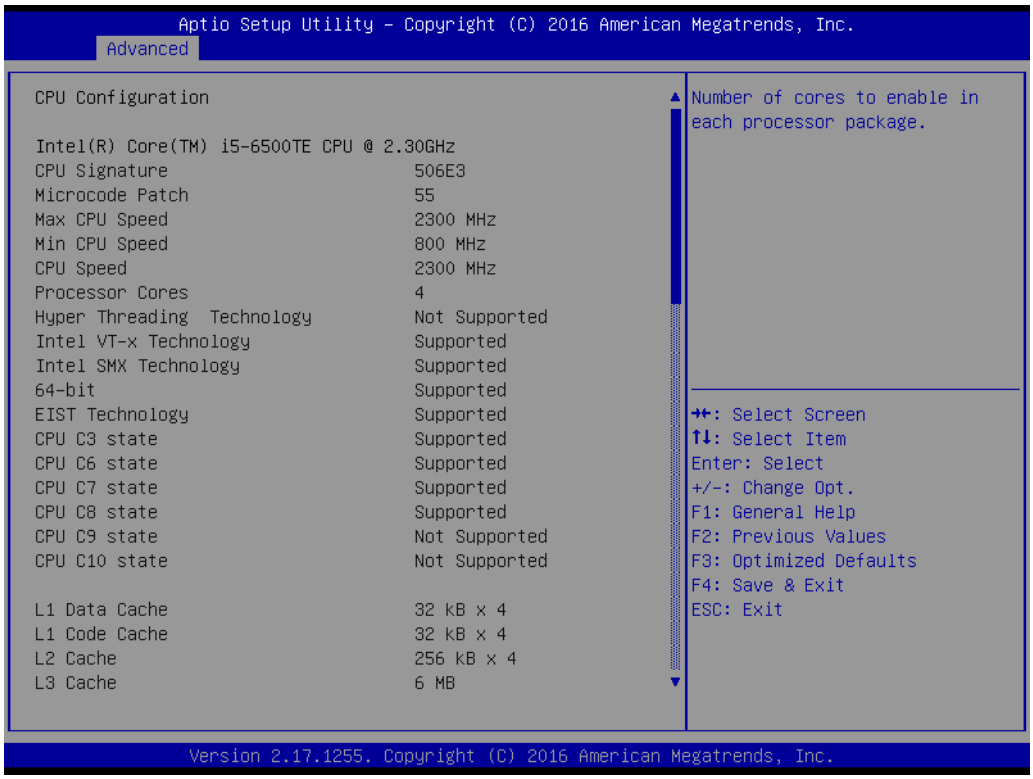
***Note!*** *When enabled, the system will wake up at the specified time.*

### 3.2.2.8 Serial Port Console Redirection




- **Console Redirection [ Enabled ]**
  Enable/Disable the console redirection feature.

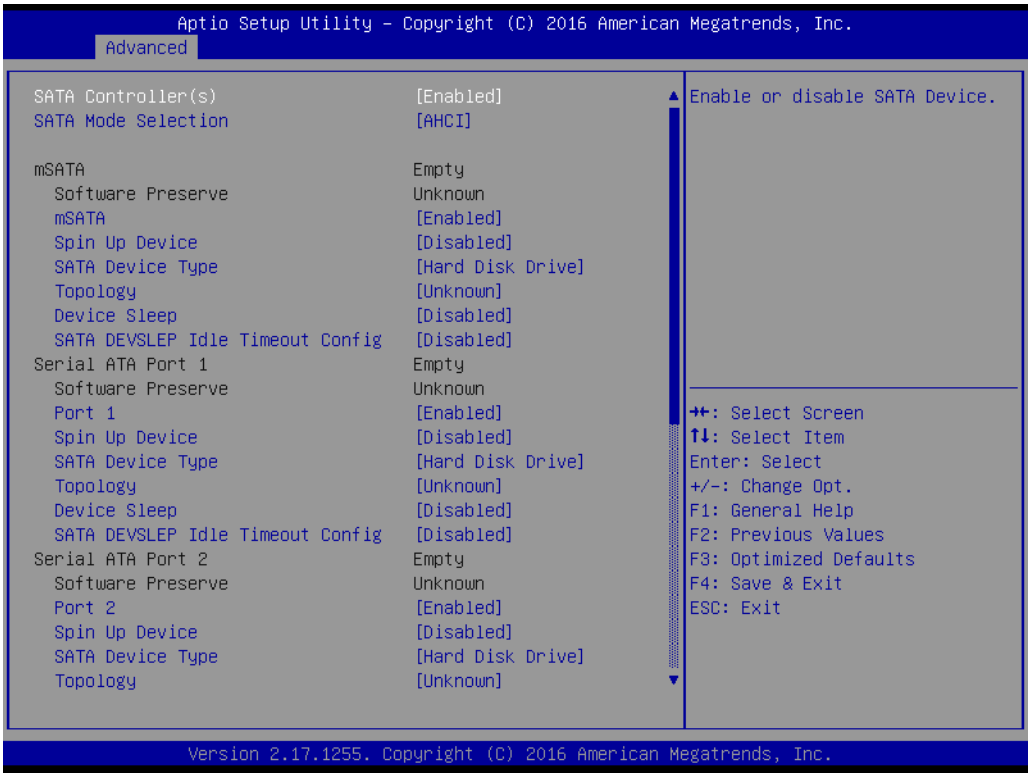
### 3.2.2.9 CPU Configuration




- **CPU Configuration**

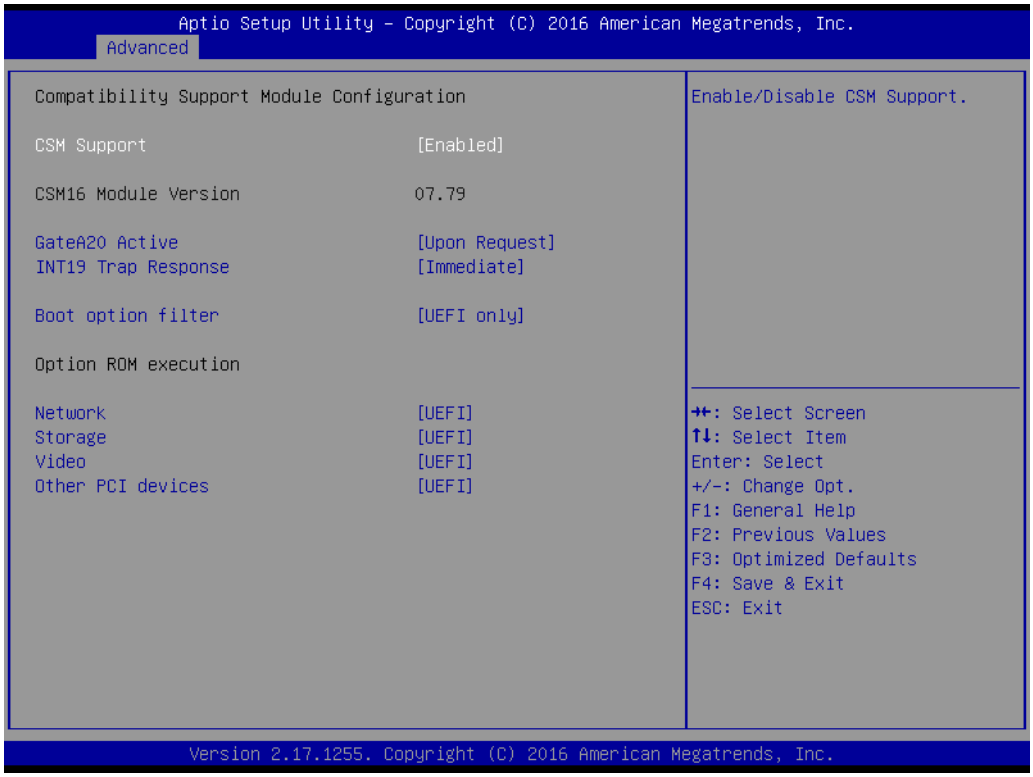
  The item shows you CPU specifications and features. The content may be different with different CPUs.

### 3.2.2.10 SATA Configuration




- **SATA Controllers [ Enabled ]**
  Enable/Disable SATA Function.
- **SATA Mode [ AHCI ]**
  This can be configured as IDE, AHCI, or RAID mode.

### 3.2.2.11 CSM Configuration




- **Boot option filter [UEFI only]**
- **Network [UEFI]**
- **Storage [UEFI]**
- **Video [UEFI]**
- **Other PCI device [UEFI]**

***Note!*** *If your HDD or other boot device is installed as Legacy mode, it may cause a blue screen situation. There are 2 ways to solve this:*

*1. Re-install your OS as UEFI Mode.*

*2. Change all of settings above as "Legacy".*

** Boot option filter-> Legacy Only*

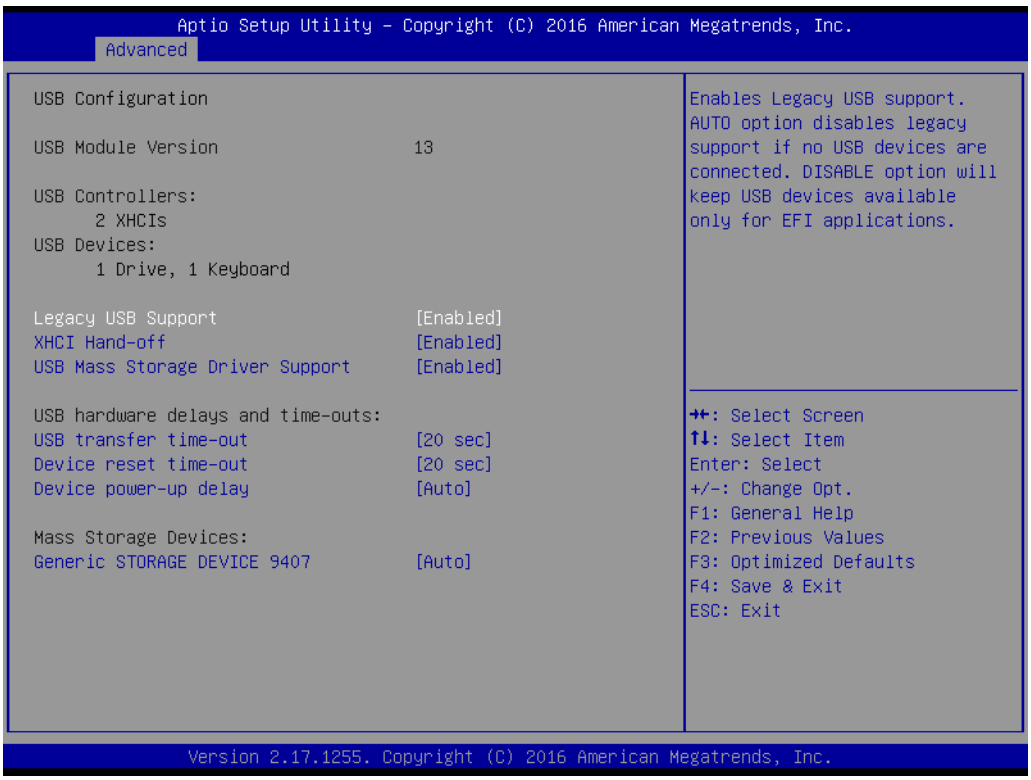
** Network -> Legacy*

** Storage -> Legacy*

** Video -> Legacy*

** Other PCI devices -> Legacy*

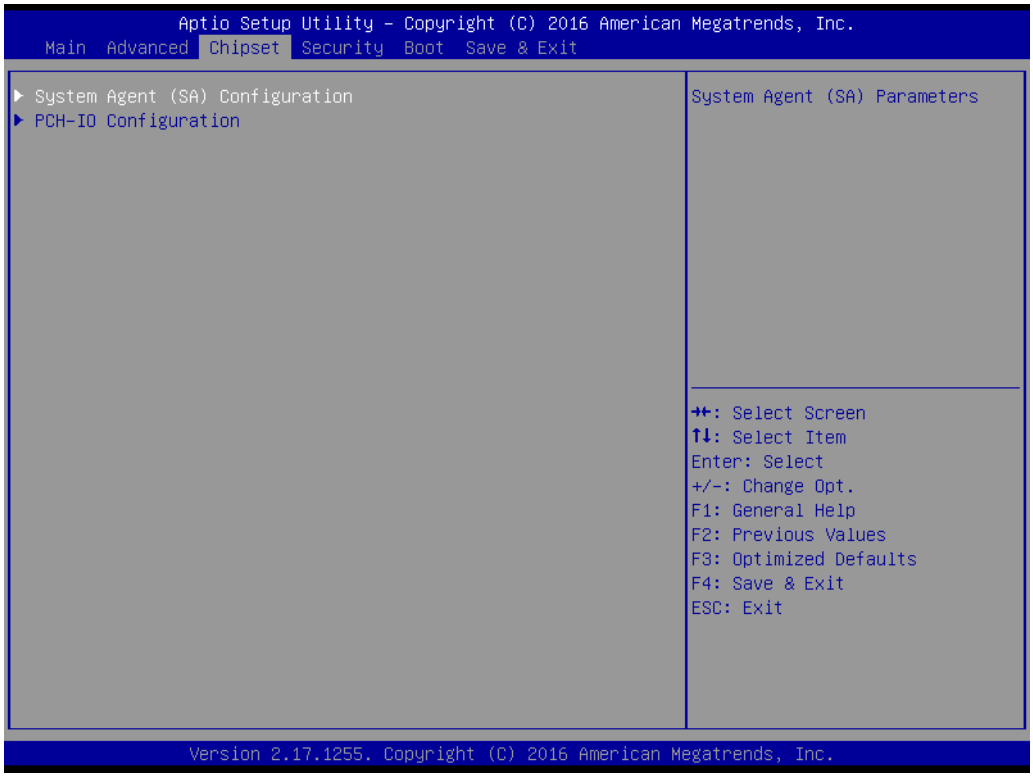
### 3.2.2.12 USB Configuration



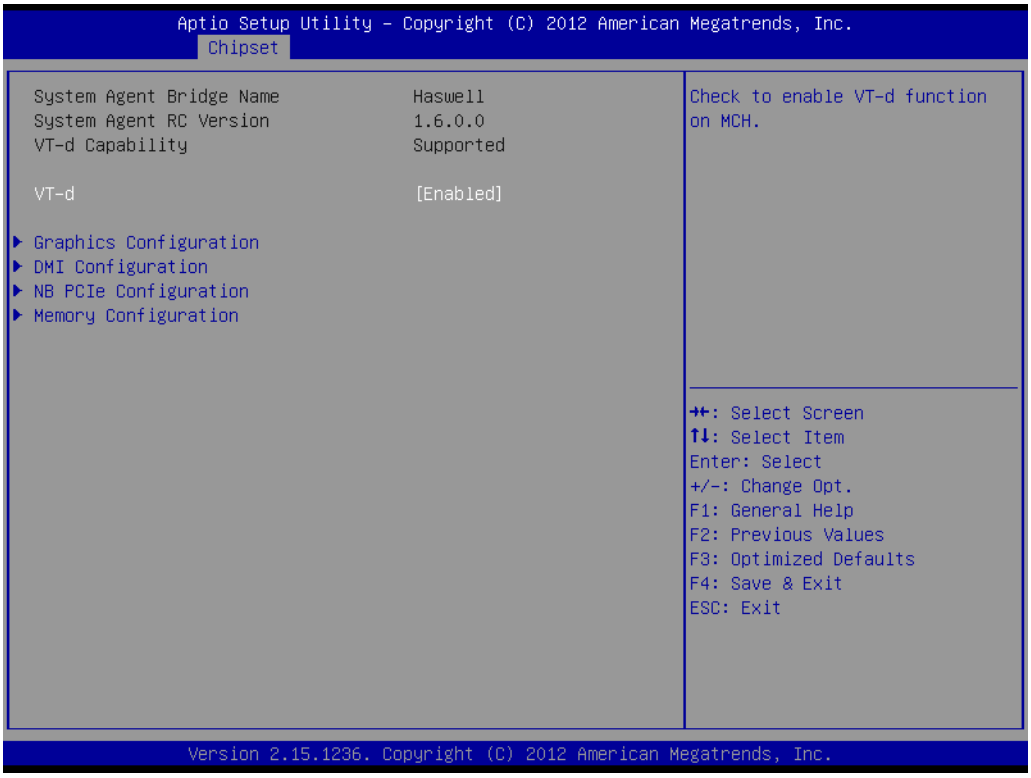

- **Legacy USB Support [ Enabled ]**
  Enable/Disable for legacy USB. Auto option disables legacy support if no USB devices are connected.
- **XHCI Hand-off [ Enabled ]**
- **USB Mass Storage Driver Support [ Enabled ]**
- **USB hardware delays and time-outs**
  USB Device transfer, reset time-out, and delay settings.
- **Mass Storage Devices [ Auto ]**
  Shows USB mass storage device information.

## 3.3 Chipset Configuration Setting

Select the chipset tab from the BIOS setup screen to enter the Chipset Setup screen. Users can select any item in the left frame of the screen, such as PCI express Configuration, to go to the sub-menu for that item. Users can display a Chipset Setup option by highlighting it using the <Arrow> keys. All Chipset Setup options are described in this section. The Chipset Setup screens are shown below. The sub-menus are described on the following pages.

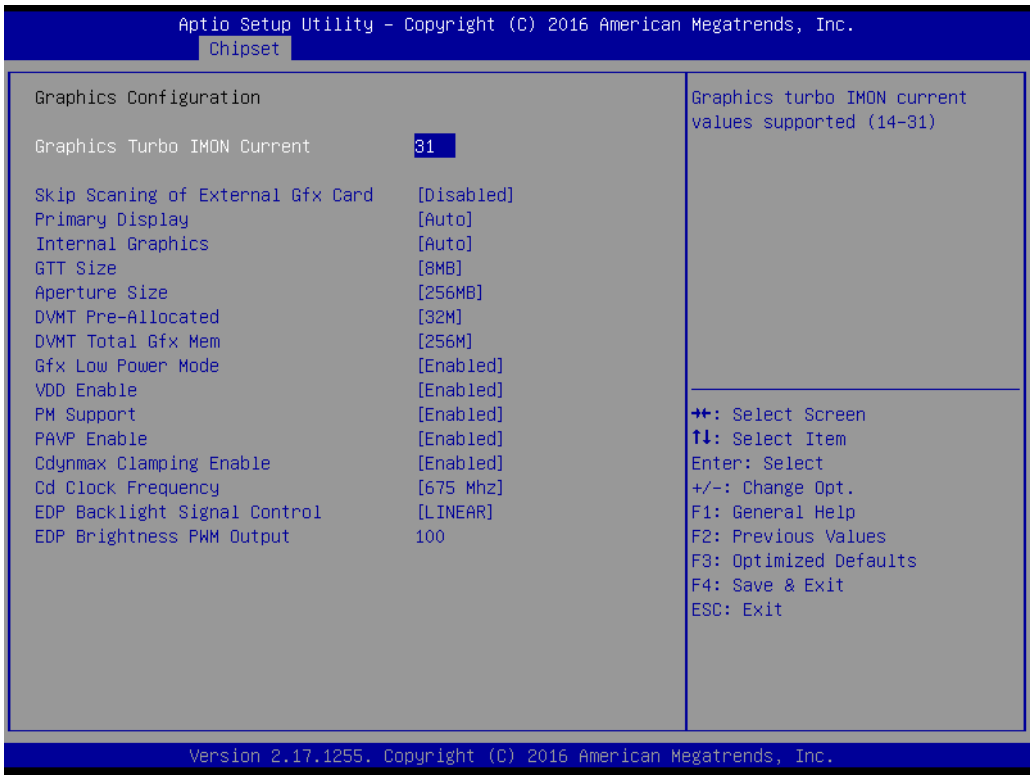


### 3.3.1 System Agent (SA) Configuration




- **VT-d [ Enabled ]**
  Enable/Disable VT-d function on MCH.

### 3.3.1.1 Graphics Configuration




- **Graphics Turbo IMON Current [ 14-31 ]**
- **Skip Scanning of External Gfx Card [disabled]**
- **Primary Display [ Auto ]**
  Select which of IGFX/PEG/PCI Graphics device should be the Primary Display.
- **Internal Graphics [ Auto ]**
  Keep IGD enabled based on the setup options.
- **GTT size [8MB]**
- **Aperture Size [ 256MB ]**
- **DVMT Pre-Allocated [ 32M ]**
  Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
- **DVMT Total Gfx Mem [ 256M ]**
  Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
- **Gfx Low Power Mode [ Enabled ]**

***Note!*** *When BIOS is set as "Auto", only a single display works under DOS.*

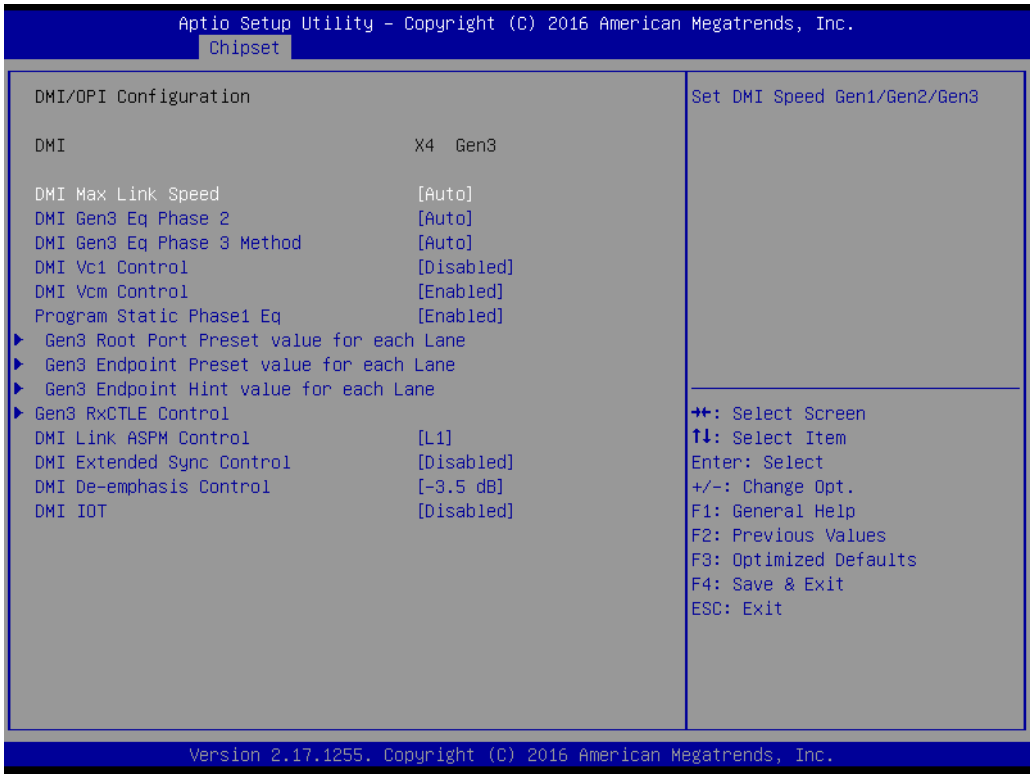
***Note!*** *The triple display function can only work under Windows 7 and 8, the 2nd and 3rd displays can not work under DOS.*

The table below shows 2-3 display combinations and all of the combinations that are verified and tested.

**Table 3.1: Display Combination List Table**

| Display Combination List | BIOS | DOS | WES 8 |
|---|---|---|---|
| Single Display | | | |
| VGA | PASS | PASS | PASS |
| DVI | PASS | PASS | PASS |
| DP | PASS | PASS | PASS |
| EDP | PASS | PASS | PASS |
| HDMI | PASS | PASS | PASS |
| Dual Display | | | |
| CRT+DVI | NA | NA | PASS |
| CRT+HDMI | NA | NA | PASS |
| CRT+DP | NA | NA | PASS |
| CRT+EDP | NA | NA | PASS |
| DVI+HDMI | NA | NA | PASS |
| DVI+DP | NA | NA | PASS |
| DVI+EDP | NA | NA | PASS |
| HDMI+DP | NA | NA | PASS |
| HDMI+EDP | NA | NA | PASS |
| DP+EDP | NA | NA | PASS |
| Triple Display | | | |
| DP+HDMI+DVI | NA | NA | PASS |
| CRT+HDMI+DVI | NA | NA | PASS |
| CRT+DP+HDMI | NA | NA | PASS |
| DP+EDP+DVI | NA | NA | PASS |
| CRT+EDP+DVI | NA | NA | PASS |
| CRT+DP+EDP | NA | NA | PASS |
| CRT+DP+DVI | NA | NA | PASS |

### 3.3.1.2 DMI Configuration



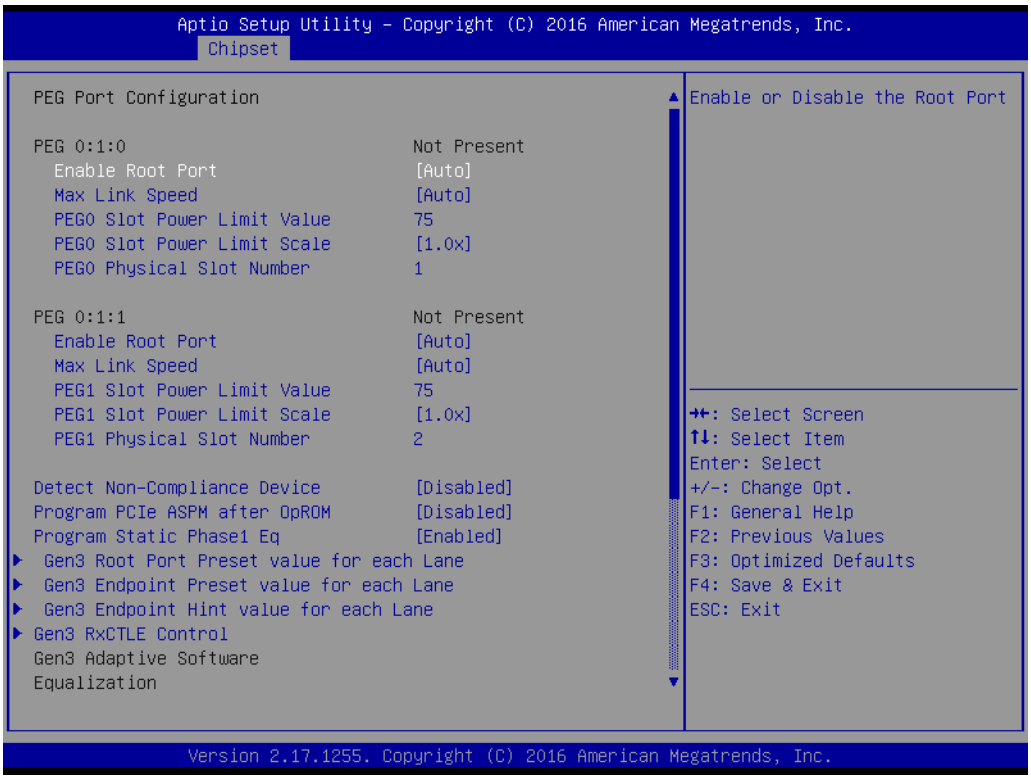

- **DMI Vc1 Control [ Disabled ]**
- **DMI Vcm Control [ Enabled ]**
- **DMI Link ASPM Control [ L1 ]**

  Enable/Disable control of Active State Power Management on the SA side of the DMI Link.
- **DMI Extended Synch Control [ Disabled ]**

  Enable DMI Extended Synchronization.
- **DMI De-emphasis Control [ -3.5 dB ]**

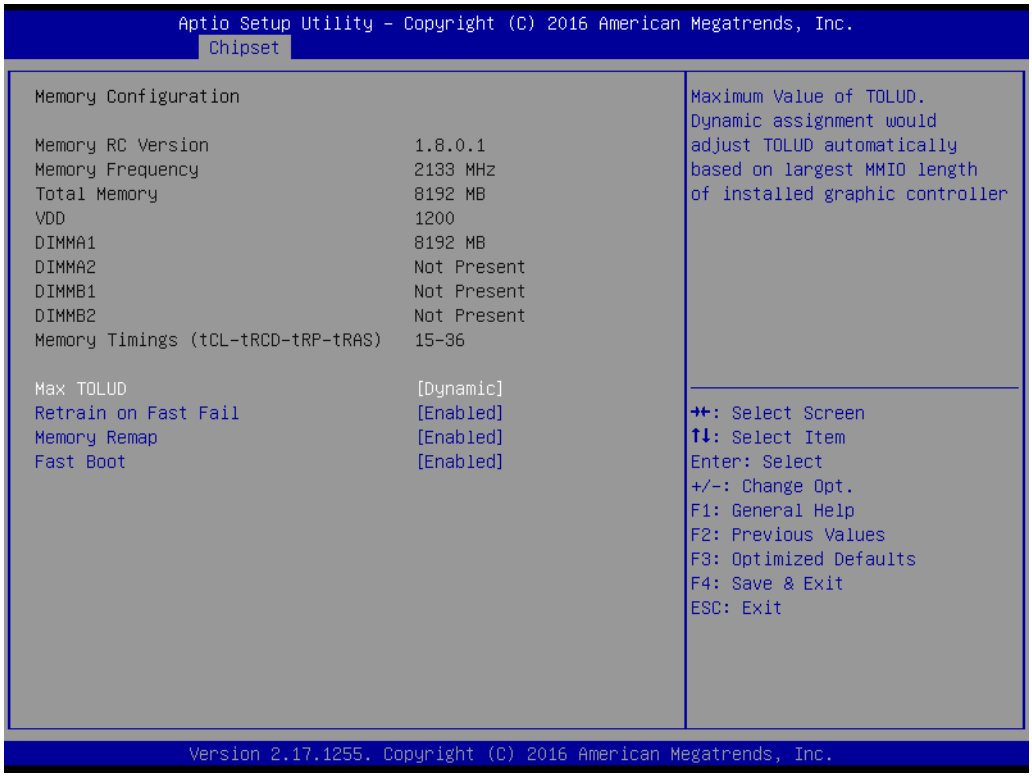
  Configure the De-emphasis control on DMI
- **DMI IOT [ Disabled ]**

### 3.3.1.3 PEG Port Configuration




- **Enable Root Port [ Auto ]**
- **Max Link Speed [Auto]**
- **Detect Non-Compliance Device [ Disabled ]**
  Detect Non-Compliance PCI Express Device in PEG
- **Program PCIe ASPM after OpROM [ Disabled ]**
  Enabled: PCIe ASPM will be programmed after OpROM.
  Disabled: PCIe ASPM will be programmed before OpROM.
- **Program Static Phase1 Eq [Enabled]**
- **PEG Gen3 Root Port Preset Value for each Lane**
  Root Port Preset Value Per lane for Gen3 Equalization.
- **PEG Gen3 Endpoint Preset Value each Lane**
  Endpoint Preset Value Per lane for Gen3 Equalization.
- **PEG Gen3 Endpoint Hint Value each Lane**
  Endpoint Hint Value Per lane for Gen3 Equalization.

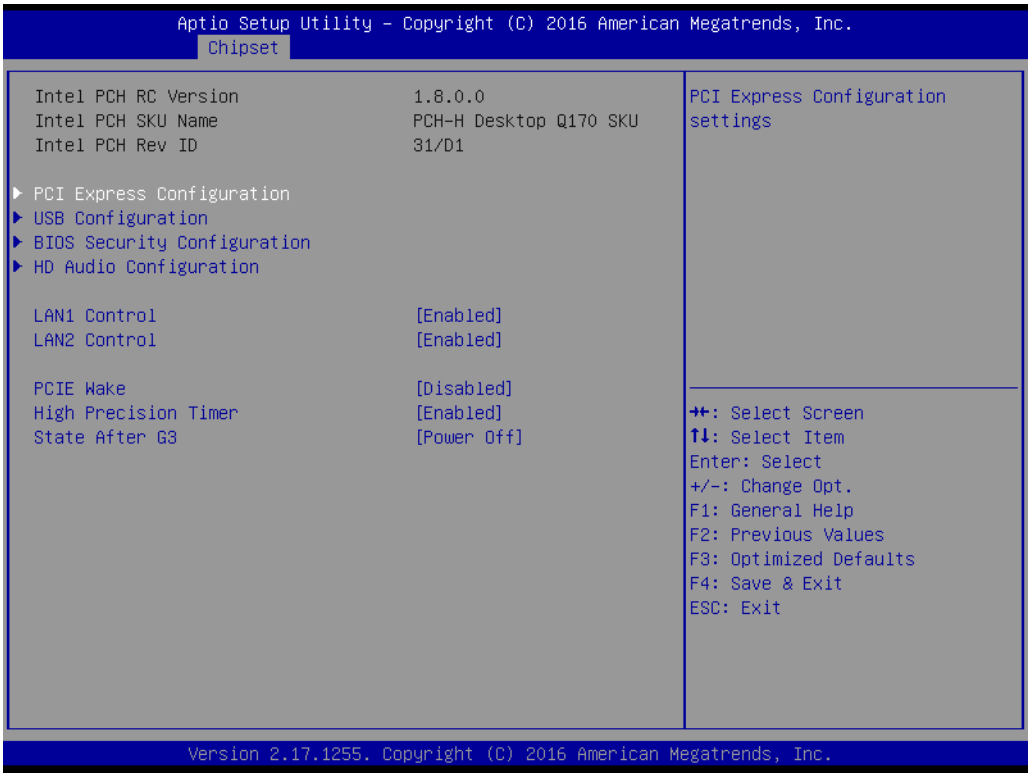
### 3.3.1.4 Memory Configuration




The item shows you memory specification included RC version, frequency, size, and voltage information etc.

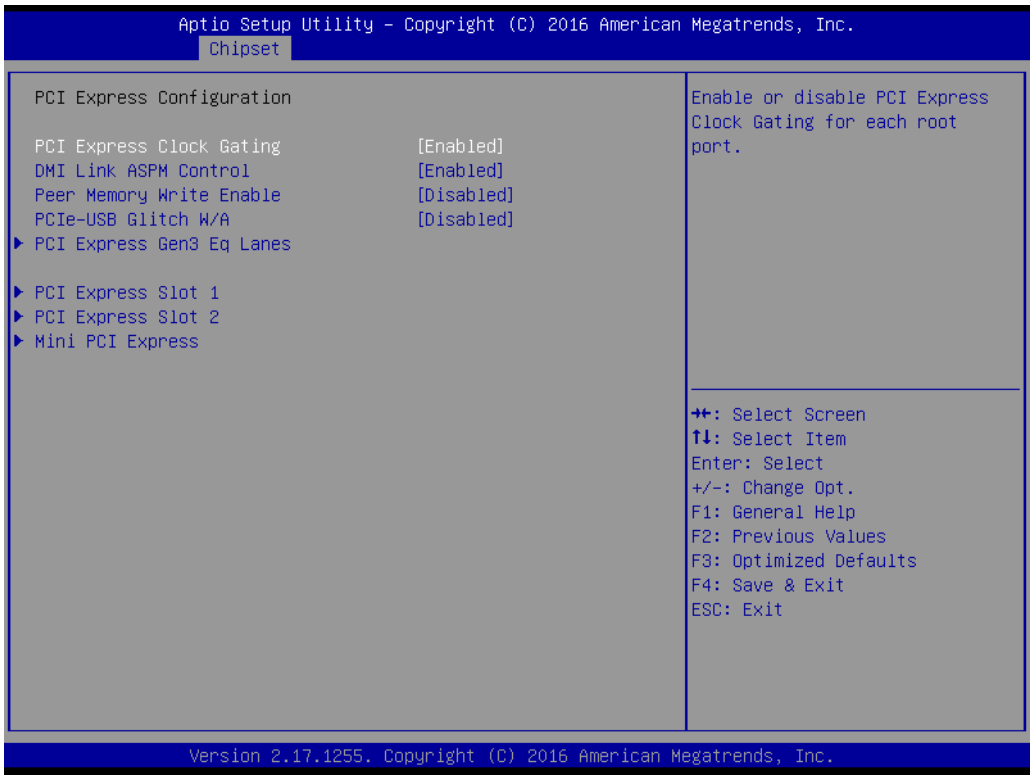
- **Max TOLUD [ Dynamic ]**
  Maximum Value of TOLUD. Dynamic assignment would adjust TOLUD automatically based on largest MMIO length of installed graphics controller.
- **Retrain on Fast Fall [Enabled]**
  Enable/Disable Retrain on Fast Fall.
- **Memory Remap [Enabled]**
  Enable/Disable Memory remap.
- **Fast Boot [Enabled]**
  Enable/Disable Fast Boot support.

## 3.3.2 PCH-IO Configuration




- **PCI Express Configuration**
  Details of PCI Express items. (See 3.3.2.1)
- **USB Configuration**
  Details of USB items. (See 3.3.2.2)
- **BIOS Security Configuration**
  Details of BIOS security items. (See 3.3.2.3)
- **LAN 1controller [ Enabled ]**
  Enable/Disable the LAN 1 controller.
- **LAN 2 controller [ Enabled ]**
- **PCIE Wake [ Disabled ]**
  Enable/Disable PCIE to wake the system from S5.
- **High Precision Timer**
  Enable/Disable High Precision Timer.
- **State After G3 [ Power Off ]**
  This item allows users to select off, on, and last state.

### 3.3.2.1 PCI Express Configuration

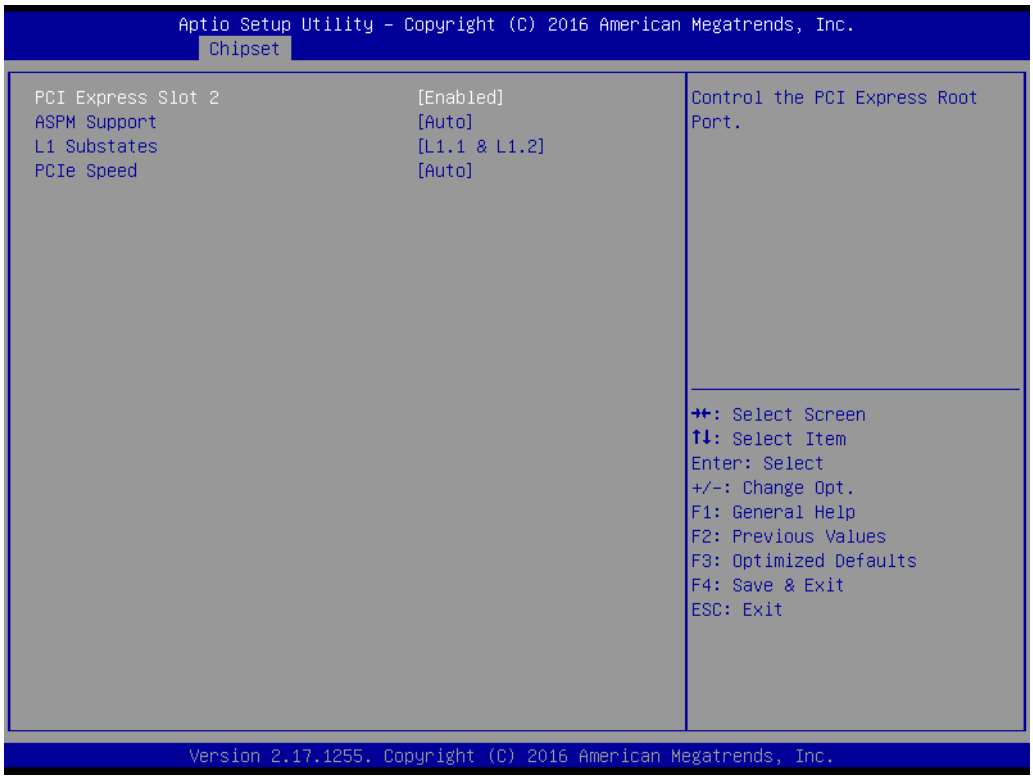



- **PCI Express Clock Gating [ Enabled ]**
  Enable/Disable PCI Express clock gating for each port.
- **DMI Link ASPM Control [ Enabled ]**
  The control of Active State Power Management on both the NB side and SB side of the DMI Link.
- **Peer Memory Write Enable [Disabled]**
- **PCIe-USB Glitch W/A [ Disabled ]**
  PCIe-USB W/A for bad USB device(s) connected behind PCIE/PEG Port.

## PCI Express Root Port 1


- **PCI Express Root Port 1 [ Enabled ]**
  Control the PCI Express Root Port.
- **ASPM Support [ Auto ]**
  Set the ASPM Level: Force L0s - Force all links to L0s State : AUTO - BIOS auto configure : DISABLE - Disables ASPM
- **L1 Substates  PCI Express L1 Substates settings.**
- **PCIe Speed [ Auto ]**
  Select PCI Express port speed.

## PCI Express Root Port 2

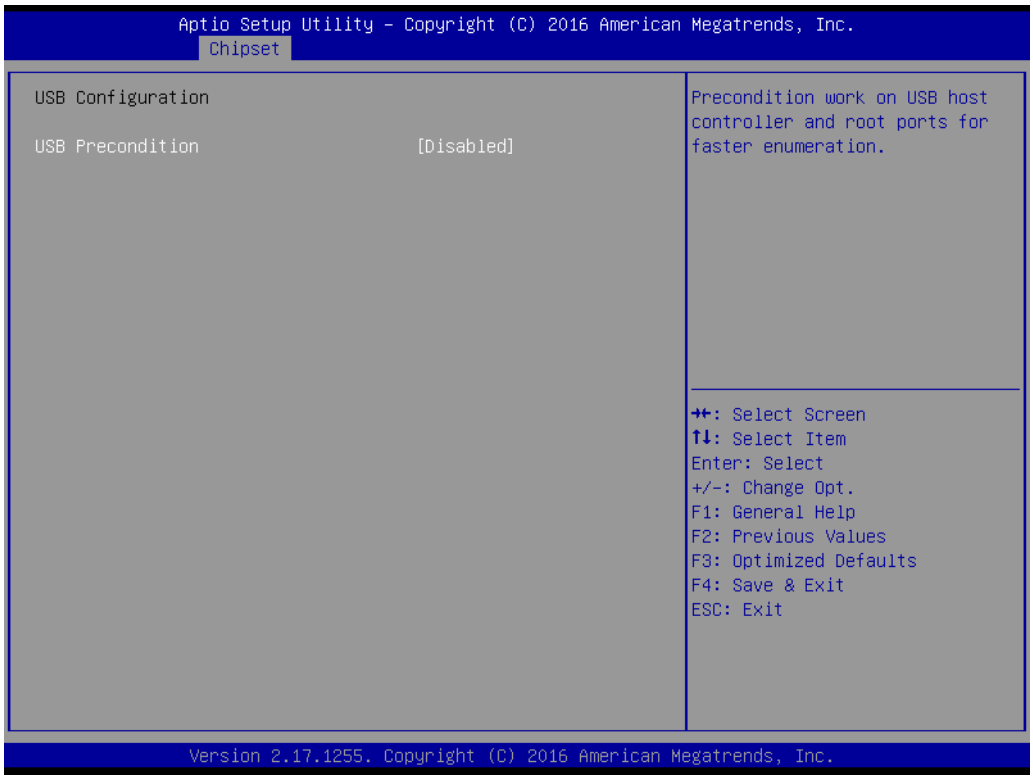



- **PCI Express Root Port 2 [ Enabled ]**
  Control the PCI Express Root Port.
- **ASPM Support [ Auto ]**
  Set the ASPM Level: Force L0s - Force all links to L0s State: AUTO - BIOS auto configure: DISABLE - Disables ASPM
- **L1 Substates PCI Express L1 Substates settings.**
- **PCIe Speed [ Auto ]**
  Select PCI Express port speed.

## Mini PCI Express

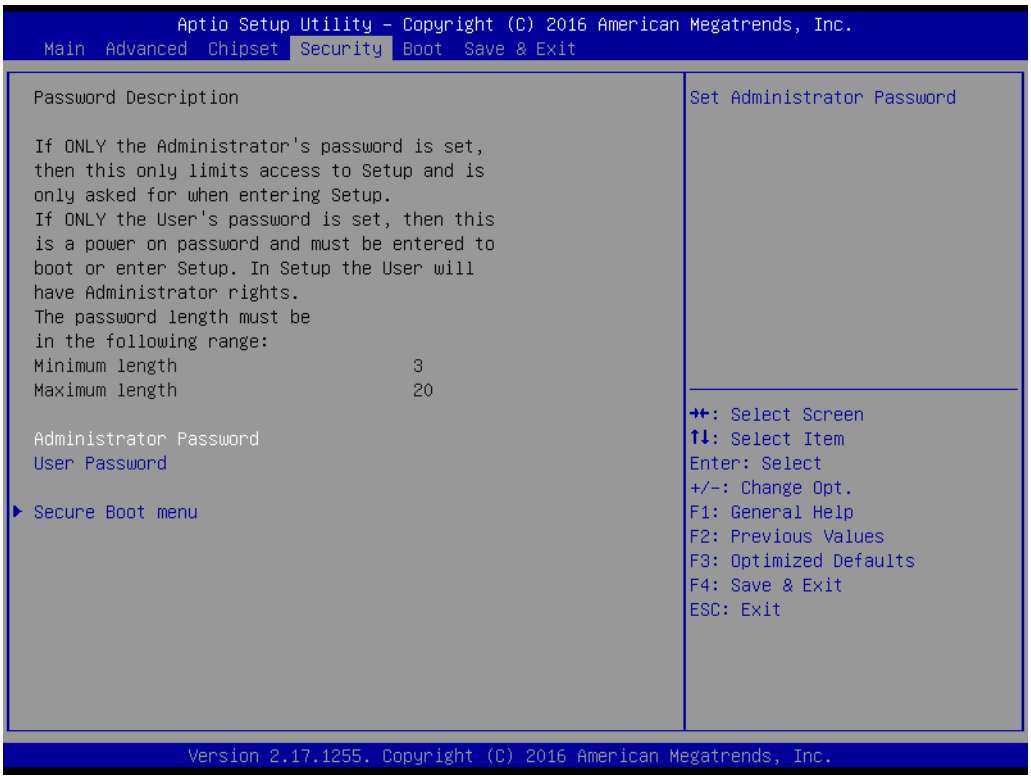

- **Mini PCI Express [ Enabled ]**
  Control the Mini PCI Express Root Port.
- **ASPM Support [ Auto ]**
  Set the ASPM Level: Force L0s - Force all links to the L0s State: AUTO - BIOS
  auto configure: DISABLE - Disables ASPM
- **L1 Substates PCI Express L1 Substates settings.**
- **PCIe Speed [ Auto ]**
  Select Mini PCI Express port speed.

### 3.3.2.2 USB Configuration




- **USB Precondition [ Disabled ]**
  Enable/Disable precondition work on the USB host controller for faster enumeration.

## 3.4 Security Settings



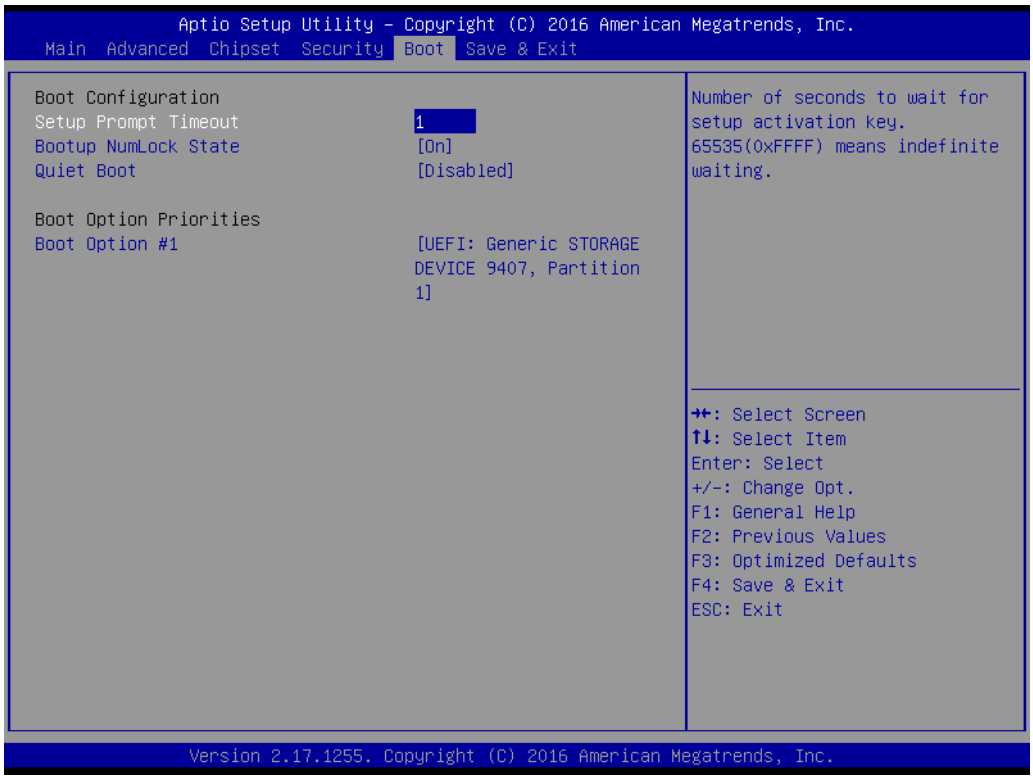

- **Administrator Password**

  Select this option and press <ENTER> to access the sub-menu, and then type in the password. Set the Administrator password.

- **User Password**

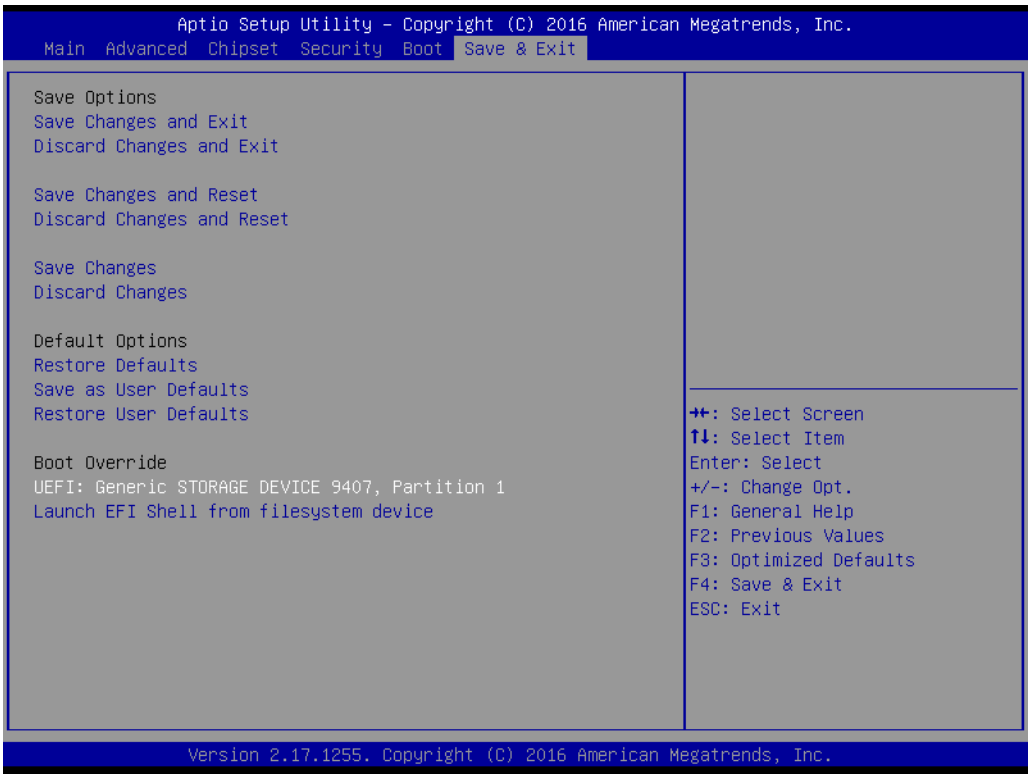
  Select this option and press <ENTER> to access the sub-menu, and then type in the password. Set the User Password.

## 3.5 Boot Setting




- **Setup Prompt Timeout**
  User the <+> and <-> keys to adjust the number of seconds to wait for the setup activation key.
- **Bootup NumLock State [ On ]**
  On or Off power on state for the NumLock.
- **Quiet Boot [ Disabled ]**
  If this option is set to disabled, the BIOS displays normal POST messages. If enabled, an OEM logo is shown instead of POST messages.
- **Boot Option #1/#2**
  Choose boot priority for boot devices.

## 3.6 Save & Exit Configuration




- **Save Changes and Exit**

  When you have completed system configuration, select this option to save changes, exit the BIOS setup menu, and reboot the computer for all system configuration parameters.

  1. Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel]
  2. Select Ok or cancel.

- **Discard Changes and Exit**

  Select this option to quit Setup without making any permanent changes to the system configuration.

  1. Select Exit Discarding Changes from the Exit menu and press <Enter>. The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]
  2. Select Ok to discard changes and exit.
     Select Discard Changes from the Exit menu and press <Enter>.

- **Save Changes and Reset**

  When users have completed system configuration, select this option to save changes, exit the BIOS setup menu, and reboot the computer for all system configuration parameters.

  1. Select Exit Saving Changes from the Exit menu and press <Enter>. The following message appears: Save Configuration Changes and Exit Now? [Ok] [Cancel]
  2. Select Ok or cancel.

- **Discard Changes and Reset**

  Select this option to quit Setup without making any permanent changes to the system configuration.

1. Select Reset Discarding Changes from the Exit menu and press <Enter>.
   The following message appears: Discard Changes and Exit Setup Now? [Ok] [Cancel]
2. Select Ok to discard changes and reset.
   Select Discard Changes from the Exit menu and press <Enter>.

- **Restore Defaults**

  The BIOS automatically configures all setup items to optimal settings when users select this option. Defaults are designed for maximum system performance, but may not work best for all computer applications. In particular, do not use the defaults if the user's computer is experiencing system configuration problems. Select Restore Defaults from the Exit menu and press <Enter>.

- **Save as User Default**

  Save the all current settings as a user default.

- **Restore User Default**

  Restore all settings to user default values.

# Chapter 4

## Software Introduction & Service

## 4.1 Introduction

Advantech Embedded Software Services is dedicated to enriching the quality of life through the fusion of Advantech platforms and Microsoft Windows embedded technology. Our mission involves empowering the embedded computing community by seamlessly integrating Windows Embedded software products into Advantech platforms. By doing so, we relieve customers from the complexities of managing multiple vendors, including hardware suppliers, system integrators, and embedded OS distributors. Ultimately, our objective is to make Windows Embedded Software solutions effortlessly and broadly accessible to the embedded computing community.

## 4.2 Value-Added Software Services

Software API: An interface that defines the ways by which an application program may request services from libraries and/or operating systems. It provides not only the underlying drivers required but also a rich set of user-friendly, intelligent, and integrated interfaces, which speeds development, enhances security, and offers add-on value for Advantech platforms. It plays the role of catalyst between developer and solution, and makes Advantech embedded platforms easier and simpler to adopt and operate with customer applications.

### 4.2.1 Software API

#### 4.2.1.1 Control

**GPIO**

General Purpose Input/Output is a flexible parallel interface that allows a variety of custom connections. It allows users to monitor the level of signal input or set the output status to switch on/off the device. Our API also provides Programmable GPIO, which allows developers to dynamically set the GPIO input or output status.

**SMBus**

SMBus is the System Management Bus defined by Intel Corporation in 1995. It is used in personal computers and servers for low-speed system management communications. The SMBus API allows a developer to interface a embedded system environment and transfer serial messages using the SMBus protocols, allowing multiple simultaneous device control.

#### 4.2.1.2 Display

**Brightness Control**

The Brightness Control API allows a developer to access embedded devices and easily control brightness.

**Backlight**

The Backlight API allows a developer to control the backlight (screen) on/off in embedded devices.

#### 4.2.1.3 Monitor

**Watchdog**

A watchdog timer (WDT) is a device that performs a specific operation after a certain period of time if something goes wrong and the system does not recover on its own. A watchdog timer can be programmed to perform a warm boot (restarting the system) after a certain number of seconds.

**Hardware Monitor**

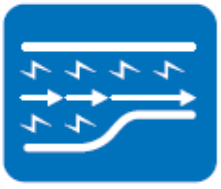
The Hardware Monitor (HWM) API is a system health supervision API that inspects certain condition indexes, such as fan speed, temperature, and voltage.

#### 4.2.1.4 Power Saving

**CPU Speed**


This monitor makes use of Intel® SpeedStep® technology to save power consumption. The system will automatically adjust the CPU speed depending on the system loading.

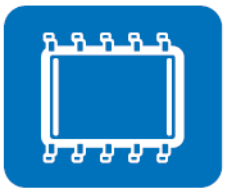
**System Throttling**



This refers to a series of methods for reducing power consumption in computers by lowering the clock frequency. This API allows the user to adjust the clock from 87.5% to 12.5%.

### 4.2.2 Software Utility

**BIOS Flash**



The BIOS Flash utility allows customers to update the flash ROM BIOS version, or use it to back up the current BIOS by copying it from the flash chip to a file on the customers' disk. The BIOS Flash utility also provides a command line version and an API for fast implementation into customized applications.

**Monitoring**

Monitoring is a utility for customers to monitor system health items such as voltage, CPU and system temperature, and fan speed. These items are important to a device. If critical errors occur and are not solved immediately, permanent damage may be caused.

# Chapter 5

## Chipset Software Installation Utility

## 5.1 Before You Begin

To facilitate the installation of the enhanced display drivers and utility software, read the instructions in this chapter carefully. The drivers for AIMB-585 are located on the Advantech website (http://support.advantech.com). Updates are provided via Service Packs from Microsoft*.

Before you begin, it is important to note that most display drivers need to have the relevant software application already installed in the system prior to installing the enhanced display drivers. In addition, many of the installation procedures assume that you are familiar with both the relevant software applications and operating system commands. Review the relevant operating system commands and the pertinent sections of your application software user manual before performing the installation.

## 5.2 Introduction

The Intel® Chipset Software Installation (CSI) utility installs the Windows INF files that outline to the operating system how the chipset components will be configured. This is needed for the proper functioning of the following features:

- Core PCI PnP services
- IDE Ultra ATA 100/66/33 and Serial ATA interface support
- Identification of Intel® chipset components in the Device Manager

***Note!*** *This utility is used for the following versions of Windows, and it has to be installed **before** installing all the other drivers:*

- *Windows 7 (32-bit)*
- *Windows 7 (64-bit)*
- *Windows 8 (64-bit)*
- *Windows 10 (64-bit)*

## 5.3 Windows 8 Driver Setup

1. Enter the Advantech website, then search for the product AIMB-585. There is a "Chipset" driver inside.

**Win8.1(64bit) driver for AIMB-585**

**Solution :** Win8.1(64bit) driver for AIMB-585

| Download File | Released Date | Download Site | |
|---|---|---|---|
| AIMB-585_USB3.0_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_COM_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_RAID_AHCI_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_ME_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_LAN_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_Graphic_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_Chipset_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_Audio_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |

# Chapter 6

## VGA Setup

## 6.1 Introduction

The Intel® Xeon®, Core™ i7/i5/i3, Pentium®, and Celeron® CPUs come equipped with an integrated graphics controller. To activate this feature, it's essential to install the VGA driver. The optimized integrated graphics solution offers flexible Intel Graphics, supporting versatile display options and a 32-bit 3D graphics engine. Experience dual independent displays and enhanced widescreen flat panel modes, including extended, twin, and clone dual display modes. Additionally, benefit from optimized 3D support for an immersive and realistic visual experience.

## 6.2 Windows 8 VGA Driver Installation

***Note!*** *Before installing this driver, make sure the CSI utility has been installed in your system. See Chapter 5 for information on installing the CSI utility.*

When visiting the Advantech website, search for the AIMB-585 product. You will find the 'Graphics' driver available for download.

**Win8.1(64bit) driver for AIMB-585**

Solution : Win8.1(64bit) driver for AIMB-585

| Download File | Released Date | Download Site | |
|---|---|---|---|
| AIMB-585_USB3.0_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_COM_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_RAID_AHCI_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_ME_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_LAN_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_Graphic_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_Chipset_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_Audio_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |

# Chapter 7

## LAN Configuration

## 7.1 Introduction

The AIMB-585 features dual Gigabit Ethernet LANs, utilizing dedicated PCI Express x1 lanes (Intel® I219LM for LAN1 and I211AT for LAN2). These LANs provide a combined bandwidth of up to 500 MB/sec, eliminating network dataflow bottlenecks and delivering Gigabit Ethernet speeds at 1000 Mbps.

## 7.2 Features

- Integrated 10/100/1000 Mbps transceiver
- 10/100/1000 Mbps triple-speed MAC
- High-speed RISC core with 24KB cache
- On-chip voltage regulation
- Wake-on-LAN (WOL) support
- PCI Express x1 host interface

## 7.3 Installation

***Note!*** *Before installing the LAN drivers, make sure the CSI utility has been installed on your system. See Chapter 5 for information on installing the CSI utility.*

The AIMB-585's Intel® 219LM (LAN1) and 211AT (LAN2) Gigabit integrated controllers support all major network operating systems. However, the installation procedure varies from system to system. Please find and use the section that provides the driver setup procedure for the operating system you are using.

## 7.4 Windows® 8 Driver Setup (Intel® I219LM / Intel® I211AT)

Enter the Advantech website, then search for product AIMB-585.
There is a "LAN" driver inside.

**Win8.1(64bit) driver for AIMB-585**

Solution : Win8.1(64bit) driver for AIMB-585

| Download File | Released Date | Download Site | |
|---|---|---|---|
| AIMB-585_USB3.0_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_COM_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_RAID_AHCI_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_ME_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_LAN_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_Graphic_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_Chipset_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |
| AIMB-585_Audio_Win8.1(64bit).zip | 2016-03-31 | Primary | Secondary |

# Appendix A

## Programming the Watchdog Timer

# A.1 Programming the Watchdog Timer

The AIMB-585 watchdog timer can be used to monitor system software operation and take corrective action if the software fails to function within the programmed period. This section describes the operation of the watchdog timer and how to program it.

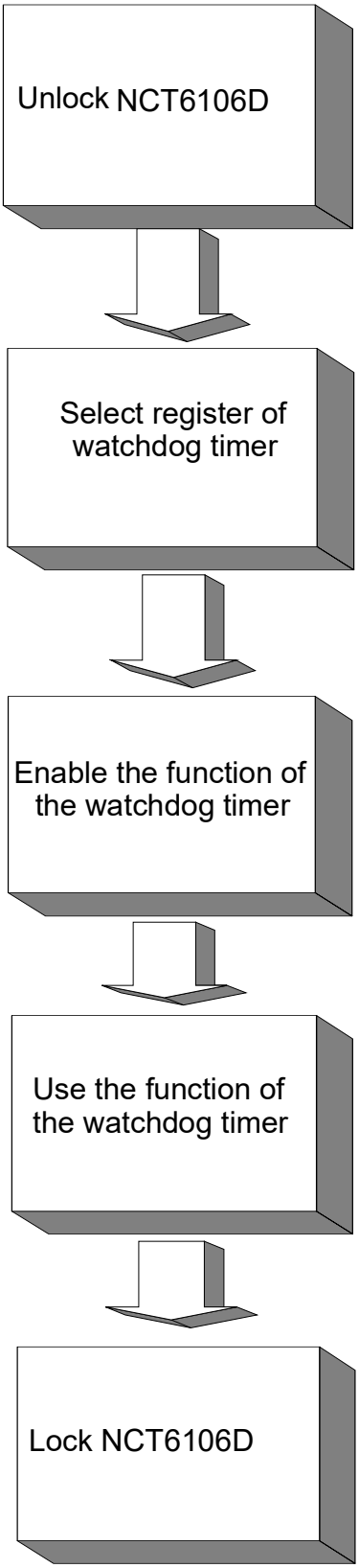
## A.1.1 Watchdog Timer Overview

The watchdog timer is built into the super I/O controller Nuvoton NCT610D. It provides the following user-programmable functions:

- It can be enabled and disabled by a user program.
- The timer can be set from 1 to 255 seconds or 1 to 255 minutes.
- It generates an interrupt or reset signal if the software fails to reset the timer before time-out.

## A.1.2 Programming the Watchdog Timer

The I/O port address of the watchdog timer is 2E (hex) and 2F (hex). 2E (hex) is the address port. 2F (hex) is the data port. You must first assign the address of the register by writing an address value into address port 2E (hex). Then, write/read data to/from the assigned register through data port 2F (hex).


Unlock NCT6106D
Select register of watchdog timer
Enable the function of the watchdog timer
Use the function of the watchdog timer
Lock NCT6106D

| Table A.1: Watchdog Timer Registers | | |
|---|---|---|
| **Address of Register (2E)** | **Attribute** | |
| Read/Write | Value (2F) & description | |
| 87 (hex) | ----- | Write this address to I/O address port 2E (hex) twice to unlock the NCT6106D. |
| 07 (hex) | write | Write 08 (hex) to select the register of the watchdog timer. |
| 30 (hex) | write | Write 01 (hex) to enable the function of the watchdog timer. Disabled is set as the default. |
| F5 (hex) | write | Set seconds or minutes as units for the timer.<br>Write 0 to bit 3: set second as the counting unit. [default]<br>Write 1 to bit 3: set minutes as the counting unit. |
| F6 (hex) | write | 0: stop timer [default]<br>01~FF (hex): The amount of the count, in seconds or minutes, depending on the value set in register F5 (hex). This number decides how long the watchdog timer waits for a strobe before generating an interrupt or reset signal. Writing a new value to this register can reset the timer to count with the new value. |
| F7 (hex) | read/write | Bit 7:Write 1 to enable the mouse to reset the timer, 0 to disable[default]. Bit 6: Write 1 to enable the keyboard to reset the timer, 0 to disable.[default]<br>Bit 5: Write 1 to generate a timeout signal immediately and automatically return to 0. [default=0]<br>Bit 4: Read status of watchdog timer, 1 means timer is “timeout”. |
| AA (hex) | ----- | Write this address to I/O port 2E (hex) to lock the watchdog timer 2. |

### A.1.3 Example Program

1. Enable the watchdog timer and set 10 sec. as the timeout interval

```
;------------------------------------------------------
Mov dx,2eh ; Unlock NCT6106D
Mov al,87h
Out dx,al
Out dx,al
;------------------------------------------------------
Mov al,07h ; Select registers of the watchdog timer
Out dx,al
Inc dx
Mov al,08h
Out dx,al
;------------------------------------------------------
Dec dx ; Enable the function of the watchdog timer
Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al
;------------------------------------------------------
Dec dx ; Set second as the counting unit
Mov al,0f5h
Out dx,al
Inc dx
In al,dx
And al,not 08h
Out dx,al
;------------------------------------------------------
Dec dx ; Set timeout interval as 10 seconds and start counting
Mov al,0f6h
Out dx,al
Inc dx
Mov al,10
Out dx,al
;------------------------------------------------------
Dec dx ; Lock NCT6106D
Mov al,0aah
Out dx,al
```

2. Enable the watchdog timer and set 5 minutes as the timeout interval

```
;------------------------------------------------------
Mov dx,2eh ; Unlock NCT6106D
Mov al,87h
Out dx,al
```

```
Out dx,al
;--------------------------------------------------------
Mov al,07h ; Select registers of the watchdog timer
Out dx,al
Inc dx
Mov al,08h
Out dx,al
;--------------------------------------------------------
Dec dx ; Enable the function of the watchdog timer
Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al
;--------------------------------------------------------
Dec dx ; Set minutes as the counting unit
Mov al,0f5h
Out dx,al
Inc dx
In al,dx
Or al,08h
Out dx,al
;--------------------------------------------------------
Dec dx ; Set timeout interval as 5 minutes and start counting
Mov al,0f6h
Out dx,al
Inc dx
Mov al,5
Out dx,al
;--------------------------------------------------------
Dec dx ; Lock NCT6106D
Mov al,0aah
Out dx,al
```

3. Enable the watchdog timer to be reset by mouse

```
;--------------------------------------------------------
Mov dx,2eh ; Unlock NCT6106D
Mov al,87h
Out dx,al
Out dx,al
;--------------------------------------------------------
Mov al,07h ; Select registers of the watchdog timer
Out dx,al
Inc dx
Mov al,08h
Out dx,al
```

```
;------------------------------------------------------------
Dec dx ; Enable the function of the watchdog timer
Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al
;------------------------------------------------------------
Dec dx ; Enable the watchdog timer to be reset by mouse
Mov al,0f7h
Out dx,al
Inc dx
In al,dx
Or al,80h
Out dx,al
;------------------------------------------------------------
Dec dx ; Lock NCT6106D
Mov al,0aah
Out dx,al
```

4. Enable the watchdog timer to be reset by keyboard

```
;------------------------------------------------------------
Mov dx,2eh ; Unlock NCT6106D
Mov al,87h
Out dx,al
Out dx,al
;------------------------------------------------------------
Mov al,07h ; Select registers of the watchdog timer
Out dx,al
Inc dx
Mov al,08h
Out dx,al
;------------------------------------------------------------
Dec dx ; Enable the function of the watchdog timer
Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al
;------------------------------------------------------------
Dec dx ; Enable the watchdog timer to be strobe reset by keyboard
Mov al,0f7h
Out dx,al
Inc dx
In al,dx
Or al,40h
```

```
Out dx,al
;--------------------------------------------------------
Dec dx ; Lock NCT6106D
Mov al,0aah
Out dx,al
```

5. Generate a time-out signal without the timer counting

```
;--------------------------------------------------------
Mov dx,2eh ; Unlock NCT6106D
Mov al,87h
Out dx,al
Out dx,al
;--------------------------------------------------------
Mov al,07h ; Select registers of the watchdog timer
Out dx,al
Inc dx
Mov al,08h
Out dx,al
;--------------------------------------------------------
Dec dx ; Enable the function of the watchdog timer
Mov al,30h
Out dx,al
Inc dx
Mov al,01h
Out dx,al
;--------------------------------------------------------
Dec dx ; Generate a time-out signal
Mov al,0f7h
Out dx,al ;Write 1 to bit 5 of F7 register
Inc dx
In al,dx
Or al,20h
Out dx,al
;--------------------------------------------------------
Dec dx ; Lock NCT6106D
Mov al,0aah
Out dx,al
```

# Appendix B

## Pin Assignments

# B.1 Keyboard & Mouse Connector (KBMS1)

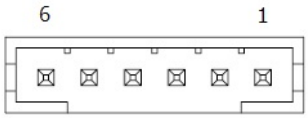



**Table B.1: Keyboard & Mouse Connector (KBMS1)**

| Pin | Signal |
|---|---|
| 1 | KB_CLK# |
| 2 | KB_DAT# |
| 3 | MS_CLK# |
| 4 | GND |
| 5 | VCC (+5VSB) |
| 6 | MS_DAT# |

# B.2 Digital Visual Interface Connector (DVI1)

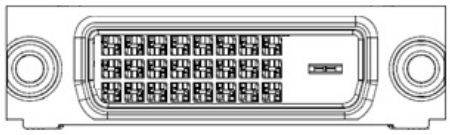


**Table B.2: Digital Visual Interface Connector (DVI1)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | TMDS D2- | 13 | GND |
| 2 | TMDS D2+ | 14 | VCC (+5V) |
| 3 | GND | 15 | GND |
| 4 | GND | 16 | Hot plug detect |
| 5 | GND | 17 | TMDS D0- |
| 6 | DDC CLK | 18 | TMDS D0+ |
| 7 | DDC DAT | 19 | GND |
| 8 | NC | 20 | GND |
| 9 | TMDS D1- | 21 | GND |
| 10 | TMDS D1+ | 22 | GND |
| 11 | GND | 23 | TMDS CLK+ |
| 12 | GND | 24 | TMDS CLK- |

## B.3 COM1 Connector (COM1)

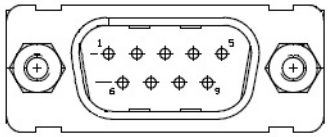


**Table B.3: COM1 Connector (COM1)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | DCD# [1] | 6 | DSR# [1] |
| 2 | RXD [1] | 7 | RTS# [1] |
| 3 | TXD [1] | 8 | CTS# [1] |
| 4 | DTR# [1] | 9 | RI# [1] |
| 5 | GND | | |

## B.4 Video Graphics Array Connector (VGA1)

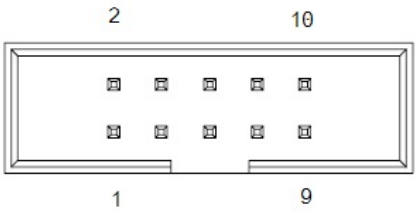



**Table B.4: Video Graphics Array Connector (VGA1)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | RED | 6 | DDC DAT |
| 2 | DDC CLK | 7 | VSYNC |
| 3 | GREEN | 8 | GND |
| 4 | Advantech defined | 9 | HSYNC |
| 5 | BLUE | 10 | VCC (+5V) |

## B.5 DisplayPort1 (Up) + HDMI1 (Down) Stack Connector (DP1+HDMI1)

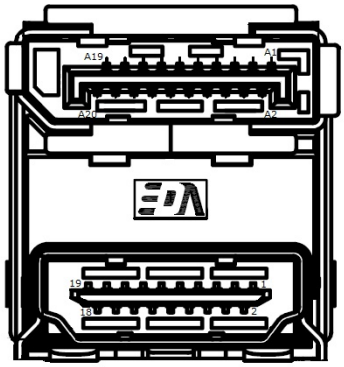


**Table B.5: DisplayPort1 (Up) + HDMI1 (Down) Stack Connector (DP1+HDMI1)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| A1 | ML0+ | A11 | GND |
| A2 | GND | A12 | ML3- |
| A3 | ML0- | A13 | CONFIG1 |
| A4 | ML1+ | A14 | GND |
| A5 | GND | A15 | AUX+ |
| A6 | ML1- | A16 | GND |
| A7 | ML2+ | A17 | AUX- |
| A8 | GND | A18 | Hot plug detect |
| A9 | ML2- | A19 | GND |
| A10 | ML3+ | A20 | DP_PWR (+3.3V) |

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | TMDS D2+ | 11 | GND |
| 2 | GND | 12 | TMDS CLK- |
| 3 | TMDS D2- | 13 | NC |
| 4 | TMDS D1+ | 14 | NC |
| 5 | GND | 15 | SCL |
| 6 | TMDS D1- | 16 | SDA |
| 7 | TMDS D0+ | 17 | GND |
| 8 | GND | 18 | VCC (+5V) |
| 9 | TMDS D0- | 19 | Hot plug detect |
| 10 | TMDS CLK+ | | |

## B.6 Universal Serial Bus Port 5 / 6 / 11 / 12 (USB561112)

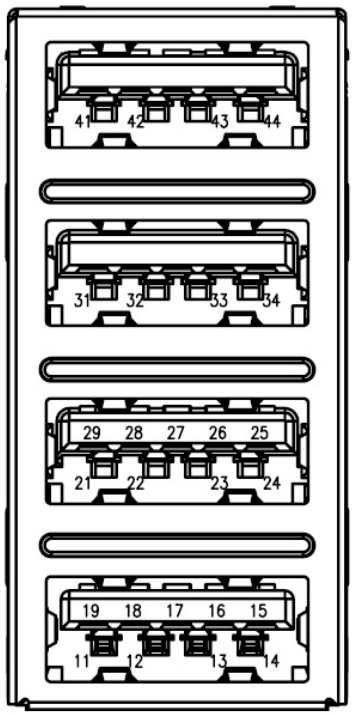
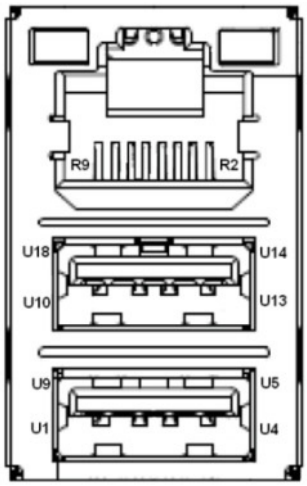



**Table B.6: Universal Serial Bus Port 5/6/11/12 (USB561112)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 11 | VBUS (*) | 21 | VBUS (*) |
| 12 | D-_6 | 22 | D-_5 |
| 13 | D+_6 | 23 | D+_5 |
| 14 | GND | 24 | GND |
| 15 | RX-_6 | 25 | RX-_5 |
| 16 | RX+_6 | 26 | RX+_5 |
| 17 | GND | 27 | GND |
| 18 | TX-_6 | 28 | TX-_5 |
| 19 | TX+_6 | 29 | TX+_5 |
| (*) Depends on JUSBPWR2 Jumper Setting | | | |
| **Pin** | **Signal** | **Pin** | **Signal** |
| 31 | VBUS (*) | 41 | VBUS (*) |
| 32 | D-_12 | 42 | D-_11 |
| 33 | D+_12 | 43 | D+_11 |
| 34 | GND | 44 | GND |
| (*) Depends on JUSBPWR2 Jumper Setting | | | |

# B.7 RJ45 + USB 3.0 Stack Connector (LAN1_USB12)




| Table B.7: RJ-45 + USB 3.0 Stack Conn. (LAN1_USB12) | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| U1 | VBUS (*) | U10 | VBUS (*) |
| U2 | D-_1 | U11 | D-_2 |
| U3 | D+_1 | U12 | D+_2 |
| U4 | GND | U13 | GND |
| U5 | RX-_1 | U14 | RX-_2 |
| U6 | RX+_1 | U15 | RX+_2 |
| U7 | GND | U16 | GND |
| U8 | TX-_1 | U17 | TX-_2 |
| U9 | TX+_1 | U18 | TX+_2 |
| (*) Depends on JUSBPWR2 Jumper Setting | | | |
| **Pin** | **Signal** | **Pin** | **Signal** |
| R2 | MDI_0+ | R6 | MDI_2+ |
| R3 | MDI_0- | R7 | MDI_2- |
| R4 | MDI_1+ | R8 | MDI_3+ |
| R5 | MDI_1- | R9 | MDI_3- |

## B.8 RJ-45 + USB 3.0 Stack Connector (LAN2_USB34)

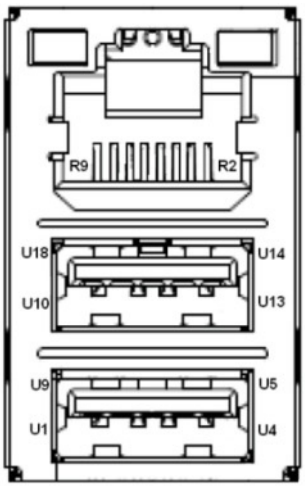
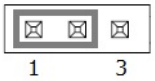



**Table B.8: RJ-45 + USB 3.0 Stack Connector (LAN2_USB34)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| U1 | VBUS (*) | U10 | VBUS (*) |
| U2 | D-_3 | U11 | D-_4 |
| U3 | D+_3 | U12 | D+_4 |
| U4 | GND | U13 | GND |
| U5 | RX-_3 | U14 | RX-_4 |
| U6 | RX+_3 | U15 | RX+_4 |
| U7 | GND | U16 | GND |
| U8 | TX-_3 | U17 | TX-_4 |
| U9 | TX+_3 | U18 | TX+_4 |
| (*) Depends on JUSBPWR2 Jumper Setting | | | |
| **Pin** | **Signal** | **Pin** | **Signal** |
| R2 | MDI_0+ | R6 | MDI_2+ |
| R3 | MDI_0- | R7 | MDI_2- |
| R4 | MDI_1+ | R8 | MDI_3+ |
| R5 | MDI_1- | R9 | MDI_3- |

## B.9 USB Power Selection Header #2 (JUSBPWR2)




| Table B.9: USB Power Selection Header #2 (JUSBPWR2) | |
|---|---|
| **Pin** | **Signal** |
| 1 | +3.3VSB |
| 2 | Advantech defined |
| 3 | +3.3 |

## B.10 LAN LED (LANLED1)


| Table B.10: LAN LED (LANLED1) | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| 1 | LAN1 ACTIVE | 2 | LAN2 ACTIVE |
| 3 | LAN1 LED PWR | 4 | LAN2 LED PWR |
| 5 | LAN1 LINK1000 | 6 | LAN2 LINK1000 |
| 7 | LAN1 LINK100 | 8 | LAN2 LINK100 |
| 9 | +3.3VSB | | |

## B.11 HD Audio Interface (SPDIF1)


| Table B.11: HD Audio Interface (SPDIF1) | |
|---|---|
| **Pin** | **Signal** |
| 1 | +5V |
| 2 | KEY |
| 3 | SPDIF OUT |
| 4 | GND |

## B.12 Audio Amplifier Output Pin Header (JAMP1)


**Table B.12: Audio Amplifier Output Pin Header (JAMP1)**

| Pin | Signal |
|---|---|
| 1 | AUDIO GND |
| 2 | AMP_OUT-L |
| 3 | AUDIO GND |
| 4 | AMP_OUT-R |

## B.13 Front Panel Audio Pin Header (FPAUD1)

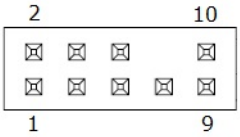
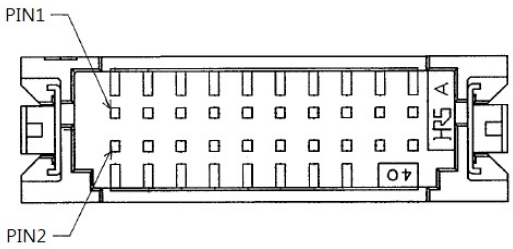



**Table B.13: Front Panel Audio Pin Header (FPAUD1)**

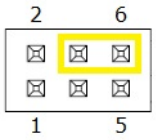
| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | MIC IN-L | 2 | GND |
| 3 | MIC IN-R | 4 | FPAUD_DETECT# |
| 5 | LINE OUT-R | 6 | SENSE R1 |
| 7 | SENSE | 8 | KEY |
| 9 | LINE OUT-L | 10 | SENSE R2 |

# B.14 Embedded DisplayPort (EDP1)



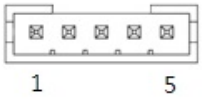

| Table B.14: Embedded DisplayPort (EDP1) | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| 1 | GND | 2 | GND |
| 3 | ML0- | 4 | NC |
| 5 | ML0+ | 6 | NC |
| 7 | GND | 8 | NC |
| 9 | ML1- | 10 | GND |
| 11 | ML1+ | 12 | AUX- |
| 13 | GND | 14 | AUX+ |
| 15 | NC | 16 | GND |
| 17 | NC | 18 | Hot plug detect |
| 19 | EDP Power (*) | 20 | EDP Power (*) |
| (*) Depends on JEDP1 Jumper Setting | | | |

# B.15 Voltage Selector for EDP1 Connector (JEDP1)




| Table B.15: Voltage Selector for EDP1 Connector (JEDP1) | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| 1 | NC | 2 | +5V |
| 3 | +12V | 4 | EDP1 VDD |
| 5 | NC | 6 | +3.3V |

## B.16 EDP Backlight Inverter Power Connector (INV1)




| Table B.16: EDP Backlight inverter power connector (INV1) | |
|---|---|
| **Pin** | **Signal** |
| 1 | +12V |
| 2 | GND |
| 3 | BKL EN |
| 4 | BKL CTRL |
| 5 | +5V |

## B.17 USB Power Selection Header #1 (JUSBPWR1)


| Table B.17: USB Power Selection Header #1 (JUSBPWR1) | |
|---|---|
| **Pin** | **Signal** |
| 1 | +3.3VSB |
| 2 | Advantech defined |
| 3 | +3.3 |

## B.18 Dual Port USB 3.0 Header (USB910)

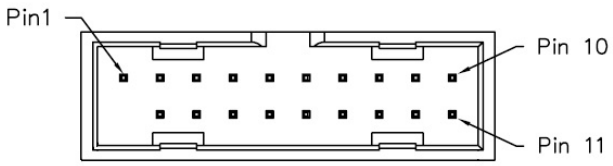



**Table B.18: Dual Port USB 3.0 Header (USB910)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | VBUS (*) | 11 | D+_10 |
| 2 | RX-_9 | 12 | D-_10 |
| 3 | RX+_9 | 13 | GND |
| 4 | GND | 14 | TX+_10 |
| 5 | TX-_9 | 15 | TX-_10 |
| 6 | TX+_9 | 16 | GND |
| 7 | GND | 17 | RX+_10 |
| 8 | D-_9 | 18 | RX-_10 |
| 9 | D+_9 | 19 | VBUS (*) |
| 10 | NC | | |

(*) Depends on JUSBPWR1 Jumper Setting

## B.19 Dual Port USB 3.0 Header (USB78)

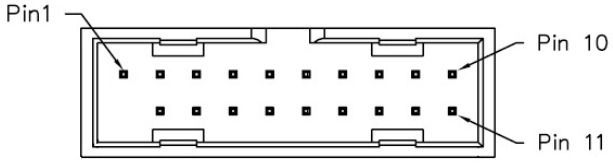



**Table B.19: Dual Port USB 3.0 Header (USB78)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | VBUS (*) | 11 | D+_8 |
| 2 | RX-_7 | 12 | D-_8 |
| 3 | RX+_7 | 13 | GND |
| 4 | GND | 14 | TX+_8 |
| 5 | TX-_7 | 15 | TX-_8 |
| 6 | TX+_7 | 16 | GND |
| 7 | GND | 17 | RX+_8 |
| 8 | D-_7 | 18 | RX-_8 |
| 9 | D+_7 | 19 | VBUS (*) |
| 10 | NC | | |

(*) Depends on JUSBPWR1 Jumper Setting

## B.20 COMS Mode Selection (JCOMS1)


**Table B.20: COMS Mode Selection (JCOMS1)**

| Pin | Signal |
|---|---|
| 1 | VBAT |
| 2 | RTC RESET# |
| 3 | GND |

## B.21 Alarm Board / CMM Power Connector (VOLT1)

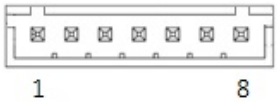


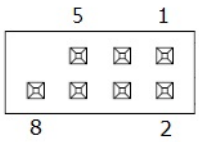

**Table B.21: Alarm Board / CMM Power Connector (VOLT1)**

| Pin | Signal |
|---|---|
| 1 | +5VSB |
| 2 | GND |
| 3 | GND |
| 4 | -5V |
| 5 | +5V |
| 6 | +3.3V |
| 7 | -12V |
| 8 | +12V |

## B.22 System Fan #2 Connector (SYSFAN2)


| Table B.22: System Fan #2 Connector (SYSFAN2) | |
|---|---|
| **Pin** | **Signal** |
| 1 | GND |
| 2 | SYSTEM FAN VCC |
| 3 | SYSTEM FAN SPEED |
| 4 | SYSTEM FAN PWM |

## B.23 SPI Pin Header (SPI_CN1)




| Table B.23: SPI Pin Header (SPI_CN1) | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| 1 | +3.3VSB | 2 | GND |
| 3 | CS# | 4 | SCLK |
| 5 | MISO | 6 | MOSI |
| | | 8 | NC |

## B.24 System Fan #4 Connector (SYSFAN4)


| Table B.24: System Fan #4 Connector (SYSFAN4) | |
|---|---|
| **Pin** | **Signal** |
| 1 | GND |
| 2 | SYSTEM FAN VCC |
| 3 | SYSTEM FAN SPEED |
| 4 | SYSTEM FAN PWM |

## B.25 Power LED and Keyboard Lock Pin Header (JFP2)


**Table B.25: Power LED / Keyboard Lock Pin Header (JFP2)**

| Pin | Signal |
|---|---|
| 1 | LED Power |
| 2 | NC |
| 3 | GND |
| 4 | Keyboard Lock |
| 5 | GND |

## B.26 Power Switch / HDD LED / SMBus / Speaker Pin Header (JFP1)

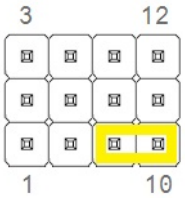



**Table B.26: Power Switch / HDD LED / SMBus / Speaker Pin Header (JFP1)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V | 2 | HDD LED+ |
| 3 | Power Button+ | 4 | SPK_P2 |
| 5 | HDD LED- | 6 | Power Button- |
| 7 | SPK_P3 | 8 | SMB_DATA |
| 9 | System Reset+ | 10 | SPK_P4 |
| 11 | SMB_CLK | 12 | System Reset- |

## B.27 CIR Interface, Watchdog Timer Output and OBS Beep (JIR1+JOBS1+JWDT1)

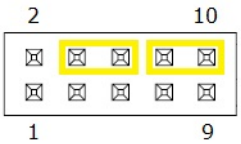



**Table B.27: CIR Interface, Watchdog Timer Output, and OBS Beep (JIR1+JOBS1+JWDT1)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +5V | 2 | NC |
| 3 | NC | 4 | Watch Dog Reset# output |
| 5 | IRRX | 6 | System Reset input# |
| 7 | GND | 8 | SIO Warning Beep output |
| 9 | IRTX | 10 | SP1 Buzzer Beep input |

## B.28 AT/ATX Mode Selection (PSON1)


**Table B.28: AT/ATX Mode Selection (PSON1)**

| Pin | Signal |
|---|---|
| 1 | AT |
| 2 | +3.3V |
| 3 | ATX |

## B.29 SMBus Connector from PCH (SMBUS1)


**Table B.29: SMBus Connector from PCH (SMBUS1)**

| Pin | Signal |
|---|---|
| 1 | +5VSB |
| 2 | SMB CLK |
| 3 | SMB DAT |
| 4 | GND |

# B.30 Serial ATA Interface Connector (SATA1 / SATA2 / SATA3 / SATA4)

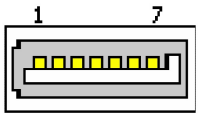



**Table B.30: Serial ATA Interface Connector (SATA1 / SATA2 / SATA3 / SATA4)**

| Pin | Signal |
|---|---|
| 1 | GND |
| 2 | TX+ |
| 3 | TX- |
| 4 | GND |
| 5 | RX- |
| 6 | RX+ |
| 7 | GND |

# B.31 Mini PCIe, mSATA Connector (MINIPCIE1)

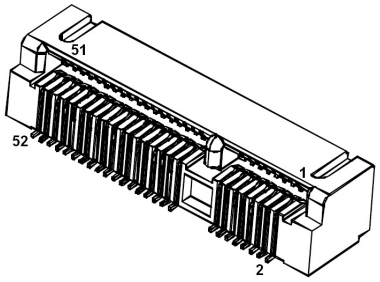



**Table B.31: Mini PCIe, mSATA Connector (MINIPCIE1)**

**MINIPCIE:**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | WAKE# | 2 | +3.3Vaux |
| 3 | Reserved | 4 | GND |
| 5 | Reserved | 6 | +1.5V |
| 7 | CLKREQ# | 8 | Reserved |
| 9 | GND | 10 | Reserved |
| 11 | REFCLK- | 12 | Reserved |
| 13 | REFCLK+ | 14 | Reserved |
| 15 | GND | 16 | Reserved |
| 17 | Reserved | 18 | GND |
| 19 | Reserved | 20 | DISABLE# |
| 21 | DETECT# | 22 | RESET# |
| 23 | PCIE_RX+ | 24 | +3.3Vaux |
| 25 | PCIE_RX- | 26 | GND |
| 27 | GND | 28 | +1.5V |
| 29 | GND | 30 | SMB_CLK |
| 31 | PCIE_TX- | 32 | SMB_DATA |
| 33 | PCIE_TX+ | 34 | GND |
| 35 | GND | 36 | USB_D- |
| 37 | GND | 38 | USB_D+ |
| 39 | +3.3Vaux | 40 | GND |
| 41 | +3.3Vaux | 42 | Reserved |
| 43 | V1.2_DETECT# | 44 | LED_WLAN# |
| 45 | Reserved | 46 | Reserved |
| 47 | Reserved | 48 | +1.5V |
| 49 | Reserved | 50 | GND |
| 51 | MSATA_DETECT# | 52 | +3.3Vaux |

**Table B.31: Mini PCIe, mSATA Connector (MINIPCIE1)**

**mSATA:**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | Reserved | 2 | +3.3V |
| 3 | Reserved | 4 | GND |
| 5 | Reserved | 6 | +1.5V |
| 7 | Reserved | 8 | Reserved |
| 9 | GND | 10 | Reserved |
| 11 | Reserved | 12 | Reserved |
| 13 | Reserved | 14 | Reserved |
| 15 | GND | 16 | Reserved |
| 17 | Reserved | 18 | GND |
| 19 | Reserved | 20 | Reserved |
| 21 | DETECT# | 22 | Reserved |
| 23 | RX+ | 24 | +3.3V |
| 25 | RX- | 26 | GND |
| 27 | GND | 28 | +1.5V |
| 29 | GND | 30 | SMB_CLK |
| 31 | TX- | 32 | SMB_DATA |
| 33 | TX+ | 34 | GND |
| 35 | GND | 36 | Reserved |
| 37 | GND | 38 | Reserved |
| 39 | +3.3V | 40 | GND |
| 41 | +3.3V | 42 | Reserved |
| 43 | Reserved | 44 | Reserved |
| 45 | Reserved | 46 | Reserved |
| 47 | Reserved | 48 | +1.5V |
| 49 | Reserved | 50 | GND |
| 51 | MSATA_DETECT# | 52 | +3.3V |

## B.32 CMOS Battery Connector (BAT1)


**Table B.32: CMOS Battery Connector (BAT1)**

| Pin | Signal |
|---|---|
| 1 | VBAT |
| 2 | GND |

## B.33 Dual Port USB 3.0 Header (USB1516)

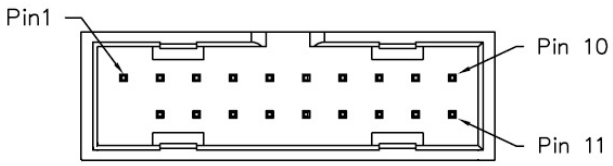



**Table B.33: Dual Port USB 3.0 Header (USB1516)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | VBUS (*) | 11 | D+_15 |
| 2 | RX-_16 | 12 | D-_15 |
| 3 | RX+_16 | 13 | GND |
| 4 | GND | 14 | TX+_15 |
| 5 | TX-_16 | 15 | TX-_15 |
| 6 | TX+_16 | 16 | GND |
| 7 | GND | 17 | RX+_15 |
| 8 | D-_16 | 18 | RX-_15 |
| 9 | D+_16 | 19 | VBUS (*) |
| 10 | NC | | |

(*) Depends on JUSBPWR1 Jumper Setting

# B.34 COM3 ~ COM6 Box Header (COM3456)

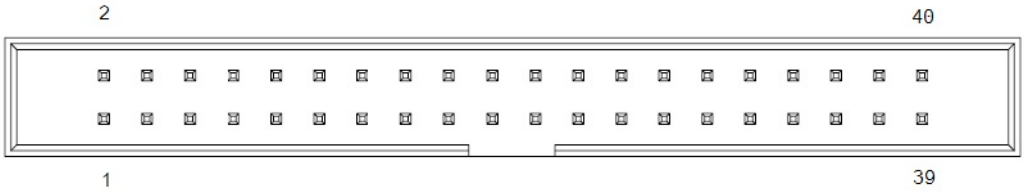



**Table B.34: COM3 ~ COM6 Box Header (COM3456)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | DCD# [3] | 2 | DSR# [3] |
| 3 | RXD [3] | 4 | RST# [3] |
| 5 | TXD [3] | 6 | CTS# [3] |
| 7 | DTR# [3] | 8 | RI# [3] |
| 9 | GND | 10 | GND |
| 11 | DCD# [4] | 12 | DSR# [4] |
| 13 | RXD [4] | 14 | RST# [4] |
| 15 | TXD [4] | 16 | CTS# [4] |
| 17 | DTR# [4] | 18 | RI# [4] |
| 19 | GND | 20 | GND |
| 21 | DCD# [5] | 22 | DSR# [5] |
| 23 | RXD [5] | 24 | RST# [5] |
| 25 | TXD [5] | 26 | CTS# [5] |
| 27 | DTR# [5] | 28 | RI# [5] |
| 29 | GND | 30 | GND |
| 31 | DCD# [6] | 32 | DSR# [6] |
| 33 | RXD [6] | 34 | RST# [6] |
| 35 | TXD [6] | 36 | CTS# [6] |
| 37 | DTR# [6] | 38 | RI# [6] |
| 39 | GND | 40 | GND |

## B.35 ATX 24-Pin Power Connector (EATXPWR1)

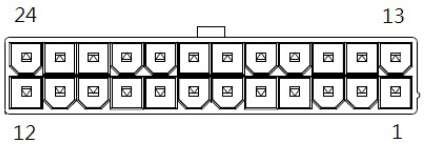



**Table B.35: ATX 24-Pin Power Connector (EATXPWR1)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | +3.3V | 13 | +3.3V |
| 2 | +3.3V | 14 | -12V |
| 3 | GND | 15 | GND |
| 4 | +5V | 16 | PSON# |
| 5 | GND | 17 | GND |
| 6 | +5V | 18 | GND |
| 7 | GND | 19 | GND |
| 8 | PWROK | 20 | -5V |
| 9 | +5VSB | 21 | +5V |
| 10 | +12V | 22 | +5V |
| 11 | +12V | 23 | +5V |
| 12 | +3.3V | 24 | GND |

## B.36 16-Bit General Purpose I/O Pin Header (GPIO1)

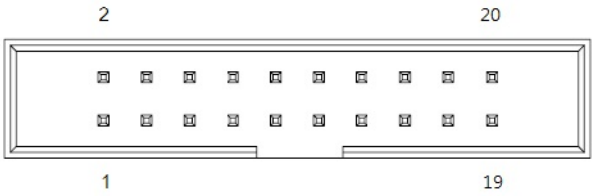
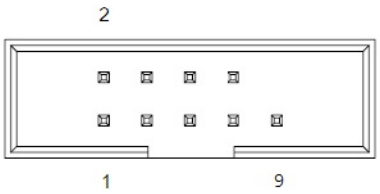



**Table B.36: 16-Bit General Purpose I/O Pin Header (GPIO1)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | GPIO0 | 2 | GPIO8 |
| 3 | GPIO1 | 4 | GPIO9 |
| 5 | GPIO2 | 6 | GPIO10 |
| 7 | GPIO3 | 8 | GPIO11 |
| 9 | GPIO4 | 10 | GPIO12 |
| 11 | GPIO5 | 12 | GPIO13 |
| 13 | GPIO6 | 14 | GPIO14 |
| 15 | GPIO7 | 16 | GPIO15 |

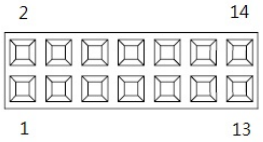
| Table B.36: 16-Bit General Purpose I/O Pin Header (GPIO1) | | | |
|---|---|---|---|
| 17 | +5VSB | 18 | GND |
| 19 | +5VSB | 20 | GND |

## B.37 COM2 Box Header (COM2)




| Table B.37: COM2 Box Header (COM2) | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| 1 | DCD# [2] | 2 | DSR# [2] |
| 3 | RXD [2] | 4 | RST# [2] |
| 5 | TXD [2] | 6 | CTS# [2] |
| 7 | DTR# [2] | 8 | RI# [2] |
| 9 | GND | | |

## B.38 Low Pin Count Interface Connector (LPC1)




| Table B.38: Low Pin Count Interface Connector (LPC1) | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| 1 | CLK (24MHz) | 2 | AD1 |
| 3 | RESET# | 4 | AD0 |
| 5 | FRAME# | 6 | +3.3V |
| 7 | AD3 | 8 | GND |
| 9 | AD2 | 10 | SMB CLK |
| 11 | SERIRQ | 12 | SMB DAT |
| 13 | +5VSB | 14 | +5V |

## B.39 COM2 RS232,RS422,RS485 Selection Pin Header (JSETCOM2)

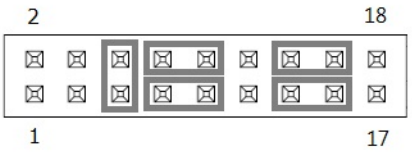



**Table B.39: COM2 RS232,RS422,RS485 Selection Pin Header (JSETCOM2)**

| Pin | Signal | Pin | Signal |
|---|---|---|---|
| 1 | UART_SIN [2] | 2 | RXD_RS485 |
| 3 | UART_SIN [2] | 4 | RXD_RS422 |
| 5 | UART_SIN [2] | 6 | RXD_RS232 |
| 7 | DCDB | 8 | SOUT [2] |
| 9 | COM2_DCD# | 10 | COM2_SOUT |
| 11 | COM2_TXD485- | 12 | COM2_RXD485+ |
| 13 | SIN [B] | 14 | DTR [B] |
| 15 | COM2_SIN | 16 | COM2_DTR# |
| 17 | COM2_TXD485+ | 18 | COM2_RXD485- |

## B.40 Case Open Selection Pin Header (JCASEOP_SW1)

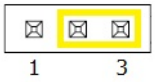
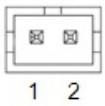



**Table B.40: Case Open Pin Header (JCASEOP_SW1)**

| Pin | Signal |
|---|---|
| 1 | Normal Open |
| 2 | Advantech defined |
| 3 | Normal Close |

## B.41 Case Open Connector (JCASE1)

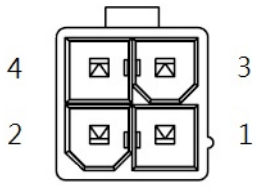



| Table B.41: Case Open Connector (JCASE1) | |
|---|---|
| **Pin** | **Signal** |
| 1 | Case Open |
| 2 | GND |

## B.42 CPU FAN Connector (CPUFAN1)


| Table B.42: CPU FAN Connector (CPUFAN1) | |
|---|---|
| **Pin** | **Signal** |
| 1 | GND |
| 2 | CPU FAN VCC |
| 3 | CPU FAN SPEED |
| 4 | CPU FAN PWM |

## B.43 ATX 4-Pin Main Power Connector (ATX12V1)




| Table B.43: ATX 4-Pin Main Power Connector (ATX12V1) | |
|---|---|
| **Pin** | **Signal** |
| 1 | GND |
| 2 | GND |
| 3 | +12V |
| 4 | +12V |

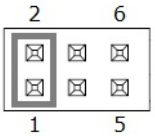
## B.44 System Fan #1 Connector (SYSFAN1)


| Table B.44: System Fan #1 Connector (SYSFAN1) | |
|---|---|
| **Pin** | **Signal** |
| 1 | GND |
| 2 | SYSTEM FAN VCC |
| 3 | SYSTEM FAN SPEED |
| 4 | SYSTEM FAN PWM |

## B.45 System Fan #3 Connector (SYSFAN3)


| Table B.45: System Fan #3 Connector (SYSFAN3) | |
|---|---|
| **Pin** | **Signal** |
| 1 | GND |
| 2 | SYSTEM FAN VCC |
| 3 | SYSTEM FAN SPEED |
| 4 | SYSTEM FAN PWM |

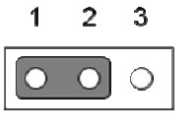
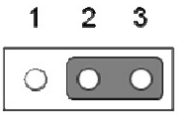
## B.46 COM1 RI# Selection Pin Header (JSETCOM1_V1)




| Table B.46: COM1 RI# Pin Header (JSETCOM1_V1) | | | |
|---|---|---|---|
| **Pin** | **Signal** | **Pin** | **Signal** |
| 1 | RI# [1] | 2 | Advantech defined |
| 3 | Advantech defined | 4 | +5V |
| 5 | +12V | 6 | Advantech defined |

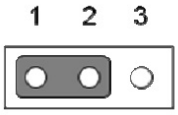
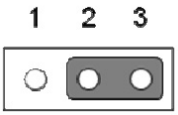
## B.47 USB VBUS Selection for LAN1_USB12, LAN2_USB34, USB561112 (JUSBPWR2)

**Table B.47: USB VBUS Selection for LAN1_USB12, LAN2_USB34, USB561112 (JUSBPWR2)**

| Function | Jumper Setting |
|---|---|
| Set USB VBUS as +5VSB (Default) |  |
| Set USB VBUS as +5V |  |

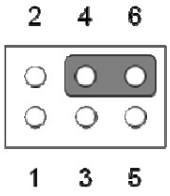
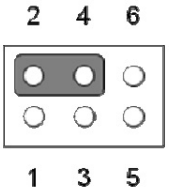
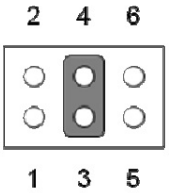
## B.48 USB VBUS Selection for USB78, USB910, USB1516 (JUSBPWR1)

**Table B.48: USB VBUS Selection for USB78, USB910, USB1516 (JUSBPWR1)**

| Function | Jumper Setting |
|---|---|
| Set USB VBUS as +5VSB (Default) |  |
| Set USB VBUS as +5V |  |

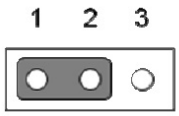
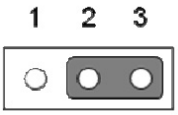
## B.49 Voltage Selection for EDP1 Connector (JEDP1)

**Table B.49: Voltage Selection for EDP1 Connector (JEDP1)**

| Function | Jumper Setting |
|---|---|
| Jumper position for +3.3V (Default) |  |
| Jumper position for +5V |  |
| Jumper position for +12V |  |

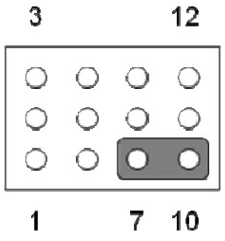
## B.50 CMOS Clear (JCOMS1)

**Table B.50: CMOS Clear (JCOMS1)**

| Function | Jumper Setting |
|---|---|
| Keep CMOS Data (Default) |  |
| Clear CMOS Data |  |

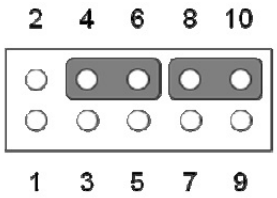
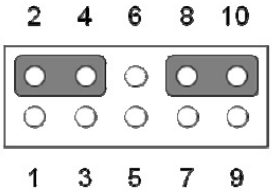
## B.51 PWRBTN# / RESET# / HDD LED / Serial Bus from HW Monitor IC / Internal Buzzer / External Speaker Header (JFP1)

**Table B.51: PWRBTN#/ RESET#/HDD LED / Serial Bus from HW Monitor IC / Internal Buzzer / External Speaker Header (JFP1)**

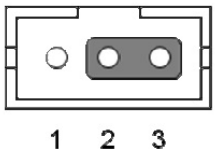
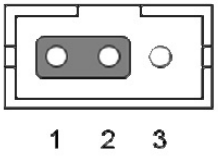
| Function | Jumper Setting |
|---|---|
| Internal Buzzer (Default) |  |

## B.52 CIR Interface, Watchdog Timer Output and OBS Beep (JIR1+JOBS1+JWDT1)

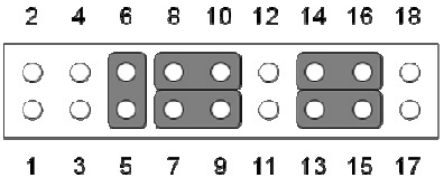
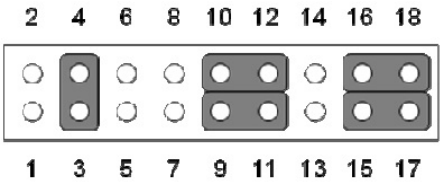
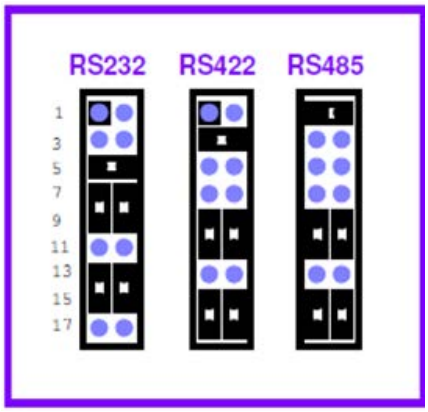
**Table B.52: CIR Interface, Watchdog Timer Output and OBS Beep (JIR1+JOBS1+JWDT1)**

| Function | Jumper Setting |
|---|---|
| Watchdog Timer Output (4-6) (Default)<br>OBS BEEP(8-10) (Default) |  |
| Watchdog Timer Disable (2-4)<br>OBS BEEP(8-10) (Default) |  |

## B.53 AT / ATX Mode Selection (PSON1)

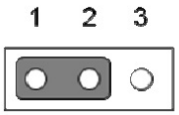
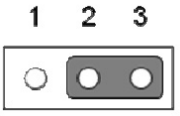
| Table B.53: AT / ATX Mode Selection (PSON1) | |
|---|---|
| **Function** | **Jumper Setting** |
| ATX Mode (Default) |  |
| AT Mode |  |

## B.54 COM2 RS232/RS422/RS485 Selection Pin Header (JSETCOM2)

| Table B.54: COM2 RS232/RS422/RS485 Selection Pin Header (JSETCOM2) | |
|---|---|
| **Function** | **Jumper Setting** |
| RS-232 Mode (Default)<br>(5-6) (7-9) (8-10) (13-15) (14-16) |  |
| RS-422 Mode<br>(3-4) (9-11) (10-12) (15-17) (16-18) |  |
| RS-485 Mode<br>(1-2) (9-11) (10-12) (15-17) (16-18) |  |

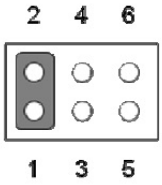
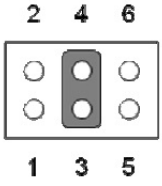
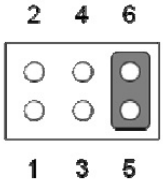
## B.55 Case Open Selection Pin Header (JCASEOP_SW1)

**Table B.55: Case Open Pin Header (JCASEOP_SW1)**

| Function | Jumper Setting |
|---|---|
| Normal Close |  |
| Normal Open (Default) |  |

## B.56 COM1_RI# Pin RI# / 5V / 12V Selection (JSETCOM1_V1)

**Table B.56: COM1_RI# Pin RI# / 5V / 12V Selection (JSETCOM1_V1)**

| Function | Jumper Setting |
|---|---|
| Jumper position for RI# (Default) |  |
| Jumper position for +5V |  |
| Jumper position for +12V |  |

ADVANTECH

*Enabling an Intelligent Planet*

## www.advantech.com

**Please verify specifications before quoting. This guide is intended for reference purposes only.**