

# Approval Sheet

<b>Customer</b>	
<b>Product Number</b>	<b>M3CT-4GWS4LPC-R</b>
<b>Module speed</b>	<b>PC3-12800</b>
<b>Pin</b>	<b>240pin</b>
<b>Cl-tRCD-tRP</b>	<b>11-11-11</b>
<b>Operating Temp</b>	<b>0°C~85°C</b>
<b>Date</b>	<b>16<sup>th</sup> September 2024</b>

**The Total Solution For  
Industrial Flash Storage**

Rev 1.0

## 1. Features

### Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			CL	tRCD	tRP
		CL=7	CL=9	CL=11			
<b>PC3-12800</b>	<b>P</b>	1066	1333	1600	11	11	11

- JEDEC Standard 240-pin Dual In-Line Memory Module
- Intend for PC3-12800 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.35 Volt (-0.067/+0.1V) or 1.5 Volt ( $\pm 0.075V$ )
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- Gold Plating Thickness 30 $\mu$ "
- Temperature Sensor with SPD EEPROM
- 8 bit pre-fetch
- Two different termination values (Rtt\_Nom & Rtt\_WR)
- Auto & self refresh 7.8 $\mu$ s ( $T_C \leq +85^{\circ}C$ )
- 16/10/1 Addressing (row/column/rank)-4GB
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 6,7,8,9,10,11
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- ECC Function
- RoHS Compliant (*Section 11*)

## 2. Ordering Information

DDR3L VLP ECC UDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
M3CT-4GWS4LPC-R	4GB	PC3-12800	512Mx72	9	1	Y

### 3. Pin Configurations (Front side/Back side) X72 UDIMM

Front								Back							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DM3	182	VDD	212	DM5
3	DQ0	33	/DQS3	63	NC,CK1	93	/DQS5	123	DQ5	153	NC	183	VDD	213	NC
4	DQ1	34	DQS3	64	NC,/CK1	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0	155	DQ30	185	/CK0	215	DQ46
6	/DQS0	36	DQ26	66	VDD	96	DQ42	126	NC	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	/EVENT	217	VSS
8	VSS	38	VSS	68	NC	98	VSS	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	NC	191	VDD	221	DM6
12	DQ8	42	NC	72	VDD	102	/DQS6	132	DQ13	162	NC	192	/RAS	222	NC
13	DQ9	43	NC	73	/WE	103	DQS6	133	VSS	163	VSS	193	/S0	223	VSS
14	VSS	44	VSS	74	/CAS	104	VSS	134	DM1	164	CB6	194	VDD	224	DQ54
15	/DQS1	45	CB2	75	VDD	105	DQS0	135	NC	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	/S1, NC	106	DQS1	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1, NC	107	VSS	137	DQ14	167	NC	197	VDD	227	DQ60
18	DQ10	48	NC	78	VDD	108	DQS6	138	DQ15	168	/RESET	198	NC	228	DQ61
19	DQ11	49	NC	79	NC	109	DQS7	139	VSS	169	CKE1, NC	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DM7
21	DQ16	51	VDD	81	DQ32	111	/DQS7	141	DQ21	171	A15	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	NC	83	VSS	113	VSS	143	DM2	173	VDD	203	DM4	233	DQ62
24	/DQS2	54	VDD	84	/DQS4	114	DQS8	144	NC	174	A12	204	NC	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQS9	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

1. Pin76, 77, 169: /S1, ODT1, CKE1: Used for dual-rank UDIMMs; NC on single-rank UDIMMs  
2. Pin63, 64: CK1, /CK1 Used for dual-rank UDIMMs; not used on single-rank DIMMs

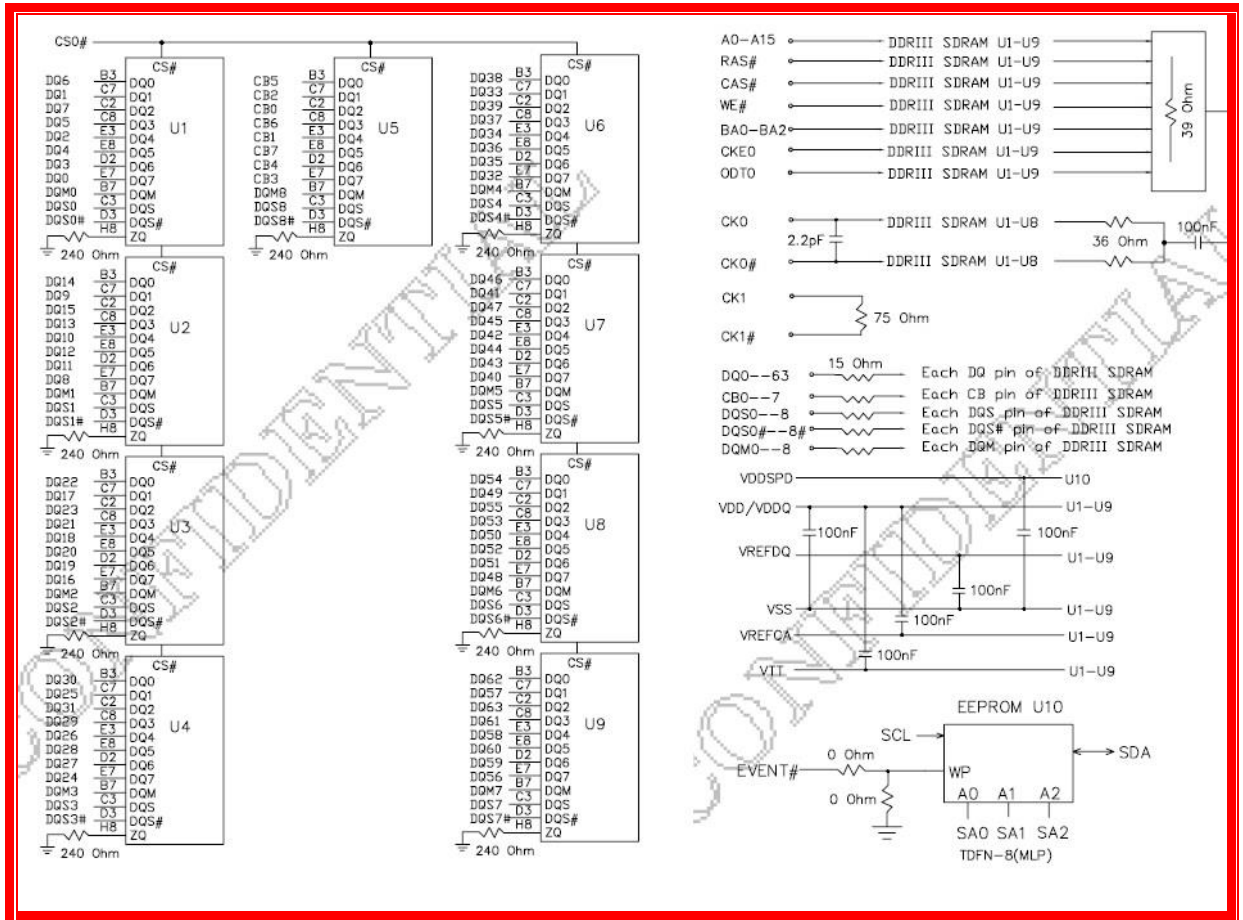
## 4. Architecture

### Pin Definition

Pin Name	Description	Pin Name	Description
A0–A15	SDRAM address bus	SCL	I <sup>2</sup> C serial bus clock for EEPROM
BA0–BA2	SDRAM bank select	SDA	I <sup>2</sup> C serial bus data line for EEPROM
/RAS	SDRAM row address strobe	SA0–SA2	I <sup>2</sup> C slave address select for EEPROM
/CAS	SDRAM column address strobe	V <sub>DD</sub> *	SDRAM core power supply
/WE	SDRAM write enable	V <sub>DDQ</sub> *	SDRAM I/O Driver power supply
/S0–/S1	DIMM Rank Select Lines	V <sub>REFDQ</sub>	SDRAM I/O reference supply
CKE0–CKE1	SDRAM clock enable lines	V <sub>REFCA</sub>	SDRAM command/address reference supply
ODT0–ODT1	On-die termination control lines	V <sub>SS</sub>	Power supply return (ground)
DQ0–DQ63	DIMM memory data bus	V <sub>DDSPD</sub>	Serial EEPROM positive power supply
CB0–CB7	DIMM ECC check bits (for x72 module)	NC	Spare pins (no connect)
DQS0–DQS8	SDRAM data strobes (positive line of differential pair)	TEST	Used by memory bus analysis tools (unused on memory DIMMs)
/DQS0–/DQS8	SDRAM data strobes (negative line of differential pair)	/RESET	Set DRAMs to Known State
DM0–DM8	SDRAM data masks/high data strobes (x8-based x72 DIMMs)	/EVENT	Reserved for optional temperature-sensing hardware
CK0–CK1	SDRAM clocks (positive line of differential pair)	V <sub>TT</sub>	SDRAM I/O termination supply
/CK0–/CK1	SDRAM clocks (negative line of differential pair)	RSVD	Reserved for future use

\*The V<sub>DD</sub> and V<sub>DDQ</sub> pins are tied common to a single power-plane on these designs.

5. Function Block Diagram:  
- (4GB, 1 Rank, 512Mx8 DDR3L SDRAMs)



## 6. SDRAM Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note	
T <sub>OPER</sub>	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.	85 to 95	°C	1,3
T <sub>STG</sub>	Storage Temperature	-55 to 100	°C	4,5	
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pins relative to V <sub>ss</sub>	-0.4 to +1.975	V	4	
V <sub>DD</sub>	Voltage on VDD supply relative to V <sub>ss</sub>	-0.4 to +1.975	V	4,6	
V <sub>DDQ</sub>	Voltage on VDDQ supply relative to V <sub>ss</sub>	-0.4 to +1.975	V	4,6	

**Note:**

1. Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center / top side of the DRAM. For measurement conditions, please refer to the JEDEC document JESD51-2.
2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.
3. Some applications require operation of the Extended Temperature Range between 85°C and 95°C case temperature. Full specifications are guaranteed in this range, but the following additional conditions apply:
  - a) Refresh commands must be doubled in frequency, therefore reducing the refresh interval tREFI to 3.9us.
  - b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 = 0b and MR2 A7 = 1b), in this case IDD6 current can be increased around 10~20% than normal Temperature range.
4. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
6. VDD and VDDQ must be within 300 mV of each other at all times; and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

## 7. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
<b>Recommended DC Operating Conditions</b>						
<b>Recommended DC Operating Conditions - DDR3L (1.35V) operation</b>						
<b>V<sub>DD</sub></b>	Supply Voltage	1.283	1.35	1.45	V	1,2
<b>V<sub>DDSPD</sub></b>	Supply Voltage	3	3.3	3.6	V	
<b>V<sub>DDQ</sub></b>	Supply Voltage	1.283	1.35	1.45	V	1,2
<b>Recommended DC Operating Conditions - DDR3 (1.5V) operation</b>						
<b>V<sub>DD</sub></b>	Supply Voltage	1.425	1.5	1.575	V	1,2
<b>V<sub>DDSPD</sub></b>	Supply Voltage	3	3.3	3.6	V	
<b>V<sub>DDQ</sub></b>	Supply Voltage	1.425	1.5	1.575	V	1,2
<b>Note:</b>						
1. Under all conditions V <sub>DDQ</sub> must be less than or equal to V <sub>DD</sub> .						
2. V <sub>DDQ</sub> tracks with V <sub>DD</sub> . AC parameters are measured with V <sub>DD</sub> and V <sub>DDQ</sub> tied together.						



## 8. Operating, Standby, and Refresh Currents

- 4GB ECC UDIMM (1 Rank, 512Mx8 DDR3L SDRAMs)

Symbol	Parameter/Condition		PC3-12800	Unit
I DD0	One bank; Active – Precharge		351	Ma
I DD1	One bank; Active – Read – Precharge		540	Ma
I DD2N	Precharge Standby Current		216	Ma
IDD2NT	Precharge Standby ODT Current		270	Ma
I DD2P	Precharge Power Down Current	Fast Mode	117	Ma
	Precharge Power Down Current	Slow Mode	117	Ma
I DD2Q	Precharge Quiet Standby Current		216	Ma
I DD3N	Active Standby Current		297	Ma
I DD3P	Active Power-Down Current		189	Ma
I DD4R	Operating Current Burst Read		855	Ma
I DD4W	Operating Current Burst Write		765	Ma
I DD5B	Burst Refresh Current		1665	Ma
I DD6	Self-Refresh Current: Normal Temperature Range		135	Ma
I DD7	Operating Bank Interleave Read Current		1260	Ma
I DD8	RESET Low Current		108	Ma

## 9. Timing Parameters

Symbol	Parameter	PC3-12800		Unit
		Min.	Max.	
<b>Clock Timing</b>				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.25	<1.5	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-70	70	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-60	60	Ps
JIT (CC)	Cycle to Cycle Period Jitter	140		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	120		Ps
TERR (2per)	Cumulative error across 2 cycle	-103	103	Ps
TERR (3per)	Cumulative error across 3 cycle	-122	122	Ps
TERR (4per)	Cumulative error across 4 cycle	-136	136	Ps
TERR (5per)	Cumulative error across 5 cycle	-147	147	Ps
TERR (6per)	Cumulative error across 6 cycle	-155	155	Ps
TERR (7per)	Cumulative error across 7 cycle	-163	163	Ps
TERR (8per)	Cumulative error across 3 cycle	-169	169	Ps
TERR (9per)	Cumulative error across 4 cycle	-175	175	Ps
TERR (10per)	Cumulative error across 5 cycle	-180	180	Ps
TERR (11per)	Cumulative error across 6 cycle	-184	184	Ps
TERR (12per)	Cumulative error across 7 cycle	-188	188	Ps

TERR (nper)	Cumulative error across 13~50 cycle	$tERR(nper)_{min} = (1 + 0.68 \ln(n)) * tJIT(per)_{min}$ $tERR(nper)_{max} = (1 + 0.68 \ln(n)) * tJIT(per)_{max}$		Ps
Data Timing				
Symbol	Parameter	Min.	Max.	Unit
tDQSQ	DQS, DQS# to DQ skew, per group, per access	-	100	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-450	225	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	225	Ps
tDS(base) AC135	Data setup time to DQS, DQS# Base specification	25	-	Ps
tDH(base) DC90	Data setup time to DQS, DQS# Base specification	55	-	Ps
Data Strobe Timing				
Symbol	Parameter	Min.	Max.	Unit
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQCK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps
tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.27	0.27	tCK(avg)

tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.18	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.18	-	tCK(avg)
<b>Command and Address Timing</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK
tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	35	9 *tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	40	-	ns
tIS(base) AC160	Command and Address setup time to CK, CK# Base specification	60	-	Ps

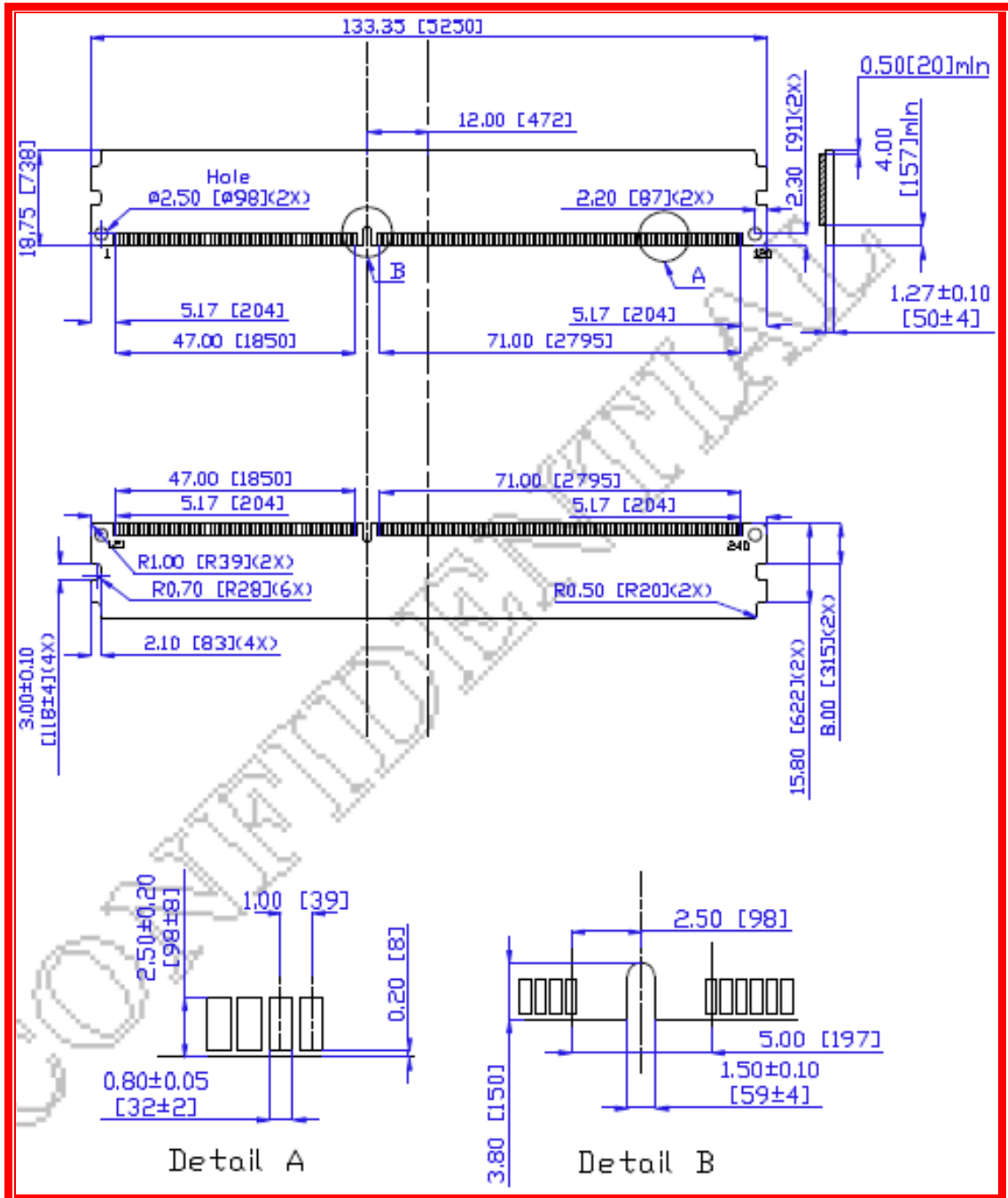
tIS(base) AC135		185	-	Ps
tIH(base) DC90	Command and Address hold time from CK, CK# Base specification	130	-	Ps
<b>Calibration Timing</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tZQinit	Power-up and RESET calibration time	512	-	nCK
tZQoper	Normal operation Full calibration time	256	-	nCK
tZQCS	Normal operation Short calibration time	80	-	nCK
<b>Reset Timing</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK, 270nS)	-	
<b>Self Refresh Timings</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tXS	Exit Self Refresh to commands not requiring a locked DLL	max(5nCK, 270nS)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE(min)+ 1tCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK, 10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK, 10ns)	-	
<b>Power Down Timings</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nC K, 6ns)	-	

tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK, 5ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCKE(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
<b>ODT Timings</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK

tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns
tAON	RTT-turn-on	-225	225	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)
<b>Write Leveling Timing</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	165	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	165	-	ps
tWLO	Write leveling output delay	0	7.5	ns
tWLOE	Write leveling output error	0	2	ns

**10. PACKAGE DIMENSION**

- (4GB, 1 Rank, 512Mx8 DDR3L base ECC VLP UDIMM)



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.



## 11. RoHS Declaration



宜鼎國際股份有限公司  
Innodisk Corporation

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Tel:(02)7703-3000 Internet: <https://www.innodisk.com/>

## RoHS 自我宣告書 (RoHS Declaration of Conformity)

**Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products**

- 一、宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及 (EU) 2015/863 關於 RoHS 之規範要求。  
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.
- 二、本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。  
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.
- 三、本公司聲明我們的產品符合 RoHS 指令的附件中 7(a)、7(c)-1、6(c) 允許豁免。  
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.
- ※ 7(a) Lead in high melting temperature type solders (i.e. lead-based alloys containing 85% by weight or more lead).
  - ※ 7(c)-1 Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.
  - ※ 6(c) Copper alloy containing up to 4% lead by weight. (This exemption applies to products that use antennas)

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯 (DEHP)	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯 (BBP)	< 1000 ppm
鄰苯二甲酸二丁酯 (DBP)	< 1000 ppm
鄰苯二甲酸二異丁酯 (DIBP)	< 1000 ppm

innodisk

宜鼎國際股份有限公司  
Innodisk Corporation

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立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司



Company Representative 公司代表人： 蘭川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2023 / 06 / 14



## 12. REACH Declaration

	<p>宜鼎國際股份有限公司 Innodisk Corporation REACH Declaration</p> <p>Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: <a href="https://www.innodisk.com/">https://www.innodisk.com/</a></p>
<p>Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006). We hereby confirm that the product(s),</p> <p><b>Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.</b></p>	
<p>■ The standard products of <b>not listed in the <u>Appendix2</u></b> meet the requirements of REACH SVHC regulations(SVHCs &lt; 0.1% in Article), as described in the candidate list table currently including 240 substances (release date: 23-JAN-2024) and shown on the ECHA website. <a href="https://echa.europa.eu/candidate-list-table">https://echa.europa.eu/candidate-list-table</a></p>	
<p>■ The standard products listed in the <u>Appendix2</u> contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table.</p> <p>Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs &gt; 0.1% in Article).</p>	
<p>■ Comply with REACH Annex XVII.</p>	
<p><b>Guarantor</b></p>	
<p>Company name 公司名稱 : <u>Innodisk Corporation 宜鼎國際股份有限公司</u></p>	
<p>Company Representative 公司代表人 :  <u>Yichuan Chen 陳怡全</u></p>	
<p>Company Representative Title 公司代表人職稱 : <u>Quality Assurance Div. SR. Manager 品保處經理</u></p>	
<p>Date 日期 : <u>2024 / 02 / 19</u></p>	
<p>1</p>	

## Revision Log

Rev	Date	Modification
0.1	16 <sup>th</sup> September 2024	Preliminary Edition
1.0	16 <sup>th</sup> September 2024	Official Released