



**User Manual**

# **ARK-2251**

## **Fanless Embedded Box Computer**

**ADVANTECH**

*Enabling an Intelligent Planet*

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## **Attention!**

Please note:

This package contains a hard-copy user manual in Chinese for China CCC certification purposes. There is an English user manual included as a PDF file on the CD. Please disregard the Chinese hard copy user manual if the product is not to be sold and/or installed in China.

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## Product Warranty (2 years)

Advantech warrants to you, the original purchaser, that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products which have been repaired or altered by persons other than repair personnel authorized by Advantech, or which have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most of our customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced at no charge during the warranty period. For out-of-warranty repairs, you will be billed according to the cost of replacement materials, service time and freight. Please consult your dealer for more details.

If you think you have a defective product, follow these steps:

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages you get when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain an return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a fully-completed Repair and Replacement Order Card and a photocopy proof of purchase date (such as your sales receipt) in a shippable container. A product returned without proof of the purchase date is not eligible for warranty service.
5. Write the RMA number visibly on the outside of the package and ship it prepaid to your dealer.

## Declaration of Conformity

### FCC Class B

Note: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation.

This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.



## Technical Support and Assistance

1. Visit the Advantech website at [www.advantech.com/support](http://www.advantech.com/support) to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before you call:
  - Product name and serial number
  - Description of your peripheral attachments
  - Description of your software (operating system, version, application software, etc.)
  - A complete description of the problem
  - The exact wording of any error messages

## Warnings, Cautions, and Notes

**Warning!** Warnings indicate conditions, which if not observed, can cause personal injury!



*Les avertissements indiquent des conditions qui, si elles ne sont pas respectées, peuvent entraîner des blessures!*

**Caution!** Cautions are included to help prevent hardware damage and data losses.



*Des précautions sont incluses pour vous aider à éviter d'endommager le matériel ou de perdre les données.*

**Note!** Notes provide optional additional information.



*Les remarques fournissent des informations supplémentaires facultatives.*

## Packing List

Before installation, please ensure the following items have been shipped:

- 1 x ARK-2251 Unit
- 1 x User Manual (Simplified Chinese)
- 1 x Wrench for top cover
- 1 x Mounting kit
- 1 x Bracket & thermal pad for M.2 M Key SSD (NVMe)
- 1 x WISE-DeviceOn
- 1 x McAfee Application Control Lite/Acronis Backup 11.7 for Windows PC
- 1 x 3-pin plug-in block for power in
- 1 x 4-pin terminal block for switch
- 1 x 6-pin terminal block for Canbus

## Ordering Information

Model Number	Description
ARK-2251-S2A1	Intel® Core™ i3-1315UE 1.2G+3GbE+6USB+6COM
ARK-2251-S2A1U	Intel® Core™ i3-1315UE 1.2G+3GbE+6USB+6COM
ARK-2251-S3A1	Intel® Core™ i5-1335UE 1.3G+3GbE+6USB+6COM
ARK-2251-S3A1U	Intel® Core™ i5-1335UE 1.2G+3GbE+6USB+6COM

## Optional Accessories

Part Number	Description
96PSA-A120W24T2-4	AC to DC adapter, 24V/120W
96PSA-A150W24T2-4	AC to DC adapter, 24V/150W
1702002600	Power cable 3-pin 183 cm, USA type
1702002605	Power cable 3-pin 183 cm, EU type
1702031801	Power cable 3-pin 183 cm, UK type
1700000237	Power cable 3-pin 183 cm, PSE type
1700024369-01	1M HDMI cable
1700031560-01	1.8M HDMI cable

# Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all AC outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergent.
4. For pluggable equipment, the power outlet should be near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The power outlet sockets should have grounded connections.
8. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
9. All cautions and warnings on the equipment should be noted.
10. If the equipment is not used for a long time, disconnect the equipment from the power source to avoid damage from transient over-voltage.
11. Never pour liquid into an opening as this can cause fire or electrical shock.
12. Never open the equipment. For safety reasons, only qualified service personnel should open the equipment.
13. If one of the following occurs, have the equipment checked by service personnel:
  - The power cord or plug is damaged.
  - Liquid has penetrated into the equipment.
  - The equipment has been exposed to moisture.
  - The equipment is malfunctioning or does not operate according to the user manual.
  - The equipment has been dropped and damaged.
  - The equipment shows obvious signs of breakage.
14. Do not leave the equipment in an environment with a storage temperature of below -20 °C (-4 °F) or above 60 °C (140 °F) as this may cause damage. The equipment should be stored in a controlled environment.
15. Any unverified component may cause unexpected damage. To ensure correct installation, always use the components (e.g., screws) provided in the accessory box.
16. **CAUTION:** The equipment is equipped with a battery-powered real-time clock circuit. There is a risk of explosion if a battery is incorrectly replaced. Replace only with same or equivalent type as recommended by the manufacturer. Discard all used batteries according to the manufacturer's instructions.
17. Always disconnect the power cord from the chassis before manually handling the hardware. Do not implement connections or configuration changes while the device is powered on. Sudden power surges may damage sensitive electronic components.
18. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position should not exceed 70 dB (A).
19. **DISCLAIMER:** These instructions are provided according to IEC 704-1 specifications. Advantech disclaims all responsibility for the accuracy of any statements contained herein.
20. The product is intended to be supplied by an UL listed power Supply suitable for use at minimum Tma 60 °C which output is rated: 12-24Vdc, 7.5-3.75A min. If need further assistance, please contact Advantech for further information.

21. RESTRICTED ACCESS AREA: The equipment should only be installed in a Restricted Access Area.
22. The PoE is to be connected only to PoE networks without routing to the outside plant.

## Consignes de Sécurité

1. Veuillez lire attentivement ces instructions de sécurité.
2. Veuillez conserver ce manuel de l'utilisateur pour référence ultérieure.
3. Veuillez débrancher cet équipement de la prise secteur avant le nettoyage. Utilisez un chiffon humide. Ne pas utiliser de détergent liquide ou pulvérisé pour le nettoyage. Utilisez une feuille ou un chiffon humide pour le nettoyage.
4. Pour les équipements enfichables, la prise de courant doit être à proximité de l'équipement et doit être facilement accessible.
5. S'il vous plaît garder cet équipement de l'humidité.
6. Posez cet équipement sur une surface fiable lors de l'installation. Une chute ou une chute pourrait causer des blessures.
7. Au moyen d'un cordon d'alimentation connecté à une prise de courant avec mise à la terre.
8. Placez le cordon d'alimentation de sorte que personne ne puisse marcher dessus. Ne placez rien sur le cordon d'alimentation.
9. Tous les avertissements et mises en garde sur l'équipement doivent être notés.
10. Si l'appareil n'est pas utilisé pendant une longue période, débranchez-le du secteur pour ne pas être endommagé par une surtension transitoire.
11. Ne jamais verser de liquide dans les ouvertures de ventilation; Cela pourrait provoquer un incendie ou un choc électrique.
12. N'ouvrez jamais l'équipement. Pour des raisons de sécurité, seul le personnel de maintenance qualifié doit ouvrir l'équipement.
13. Si l'une des situations suivantes se présente, faites vérifier le matériel par le personnel de service:
  - Le cordon d'alimentation ou la fiche est endommagé.
  - Un liquide a pénétré dans l'appareil.
  - L'équipement a été exposé à l'humidité.
  - L'équipement ne fonctionne pas bien ou vous ne pouvez pas le faire fonctionner conformément au manuel d'utilisation.
  - Equipment L'équipement est tombé et a été endommagé.
  - Equipment L'équipement présente des signes évidents de rupture.
14. Ne laissez pas cet équipement dans un environnement où la température de stockage peut être inférieure à -40 °C (-40 °F) ou supérieure à 85 °C (185 °F). Cela pourrait endommager l'équipement. L'équipement doit être dans un environnement contrôlé.
15. Tout composant non vérifié peut causer des dommages inattendus. Pour garantir une installation correcte, veuillez toujours utiliser les composants (ex. Vis) fournis avec la boîte d'accessoires.
16. ATTENTION: L'ordinateur est équipé d'un circuit d'horloge temps réel alimenté par batterie. Il y a un risque d'explosion si la batterie est remplacée de manière incorrecte. Remplacez uniquement avec le même type ou un type équivalent recommandé par le fabricant. Jetez les piles usagées conformément aux instructions du fabricant.
17. Débranchez toujours complètement le cordon d'alimentation de votre châssis lorsque vous utilisez du matériel. Ne faites pas de connexion quand l'appareil

est sous tension. Les composants électroniques sensibles peuvent être endommagés par des surtensions soudaines.

18. Niveau de pression acoustique au poste de l'opérateur selon la norme CEI 704-1: 1982 n'est pas supérieur à 70 dB (A).
19. **AVERTISSEMENT:** Cet ensemble d'instructions est donné conformément à la norme CEI 704-1. Advantech décline toute responsabilité quant à l'exactitude des déclarations contenues dans ce.
20. Ce produit est destiné à être alimenté par un bloc d'alimentation homologué UL adapté à une utilisation à Tma 50 degrés C min. dont la sortie est conforme à PS2 (ou LPS), ES1 (ou SELV) et dont la sortie est nominale: 9-36Vdc, 16.65-4.16A, si besoin d'aide supplémentaire, veuillez contacter Advantech pour plus d'informations.
21. N'ouvrez jamais l'équipement. Pour des raisons de sécurité, l'équipement ne doit être ouvert que par du personnel de service qualifié (Par personne qualifiée).
22. Le PoE doit être connecté uniquement aux réseaux PoE sans routage vers l'installation extérieure.



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# Chapter 1

## General Introduction

This chapter details background information on the ARK-2251 series.

## 1.1 Introduction

ARK-2251 is a compact, fanless, embedded system that features an 13th Gen Intel® Core™ i processor and essential I/O for easy access and installation.

### Rugged Design with Compact Dimension

ARK-2251 is equipped with a dual channel memory slot that supports up to 64GB of DDR5 4800 MHz SO-DIMM. Designed for operation in harsh industrial environments, this ruggedized system supports a wide operating temperature range (-20 ~ 60°C/-4 ~ 140°F) and wide input power range (12 ~ 24 VDC). The system I/O includes 6 x USB 3.1 Gen1 (2 x are independent), 6 x RS232/422/485, 2 x 10/100/1000/2500 Mbps LAN ports, and 1 x 10/100/1000 Mbps LAN port, as well as 1 x Mic In and Line Out, 2 x HDMI. ARK-2251 also features 1 x full-sized mPCIe, 1 x mSATA (shared with mPCIe), 1 x M.2 2230 E key, 1 x M.2 2280 M key which support NVME.

### Built-In Intelligent Management Tools – Advantech iEdge

Advantech's iEdge platform, together with McAfee and Acronis, provides a valuable suite of programmable APIs - such as a multi-level watchdog, hardware monitor, system restore, and other user-friendly interfaces. With the inclusion of iEdge, ARK-2251 can be used for remotely managing, monitoring, configuring, and controlling numerous terminals to ensure easy maintenance and recovery.

## 1.2 Product Specifications

### 1.2.1 Processor System

- **CPU:**
  - Core i3-1315UE
  - Core i5-1335UE
- **Frequency:**
  - Core i3-1315UE: 1.2 GHz turbo boost up to 4.5 GHz
  - Core i5-1335UE: 1.3 GHz turbo boost up to 4.5 GHz
- **Core Number:**
  - Core i3-1315UE: 2P + 4E
  - Core i5-1335UE: 2P + 8E
- BIOS: AMI EFI 256 Mbit

### 1.2.2 Memory

- **Technology:** DDR5 4800 Mhz
- **Max capacity:** Up to 64 GB

### 1.2.3 Socket

- **Socket:** 2 x Dual Channel DDR5 4800 MHz 262 pin SO-DIMM (no support ECC)

### 1.2.4 Graphics

- **Chipset:** Intel® Iris® Xe graphics
- **HDMI 2.0b:** Up to 4096 x 2160 @ 60Hz
- **Dual Display:** 2 x HDMI

### 1.2.5 Ethernet

- **LAN1:** 10/100/1000 Mbps Intel i219 GbE, supports Wake On LAN
- **LAN2:** 10/100/1000/2500 Mbps Intel i226 GbE, supports Wake On LAN
- **LAN3:** 10/100/1000/2500 Mbps Intel i226 GbE, supports Wake On LAN
- **POE Load (optional):** LAN2 & LAN3: 15.4W per port

### 1.2.6 Audio

- **Interface:** Realtek ALC888S, High Definition Audio, Mic-in, Line-out

### 1.2.7 I/O Interface

- **Serial Ports:** 6 x RS-232/422/485 with auto flow control
- **USB Ports:** 6 x USB 3.1 Gen1 (2 x are independent)
- **GPIO:** 8-bit programmable DIO
- **CANbus:** 2 x CANBus

### 1.2.8 Expansion

- **Mini PCIe:** 1 x full-sized mPCIe
- **M.2:** 1 x M2. 2230 E key and 1 x M.2 2280 M key

### 1.2.9 Storage

- **NVME:** 1x M.2 M Key supporting NVME
- **mSATA:** Shared with mPCIe

### 1.2.10 Other

- **WatchDog Timer:** 255 levels timer interval, setup by software
- **TPM:** TPM 2.0 (project supported by AMO-I029)

### 1.2.11 Software Support

- **Microsoft Windows:** Windows 10
- **Linux:** Ubuntu 22.04, others by project support

### 1.2.12 Power Requirements

- **Power Type:** ATX/AT
- **Power Input Voltage:** 12-24 V<sub>DC</sub>, 10A- 5A
- **Power Adapter:** AC to DC, 12-24 V<sub>DC</sub>, 10A- 5A, 120W (150W for adding PoE Module)

### 1.2.13 Power Consumption

- **Typical:** (OS idle mode) 19.05W for ARK-2251-S2A1, 19.30W for ARK-2251-S3A1, 19.47W for ARK-2251-S7A1
- **Max.:** (full loading) 38.21W for ARK-2251-S2A1, 41.23W for ARK-2251-S3A1, 42.13W for ARK-2251-S7A1

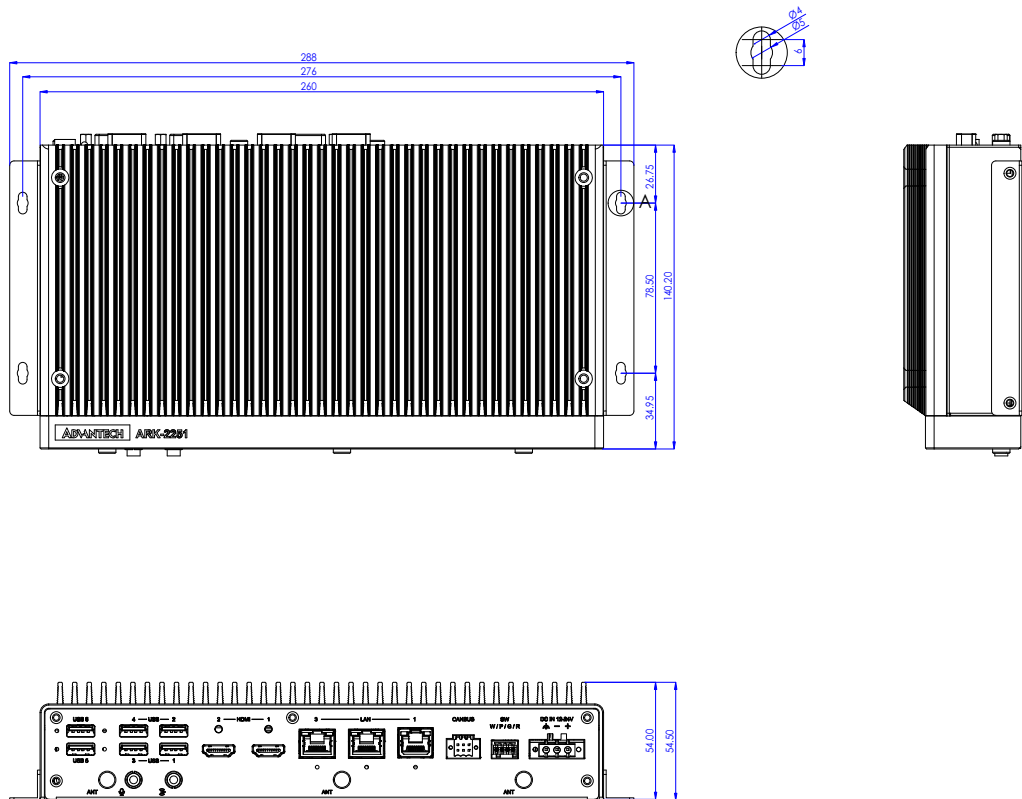
### 1.2.14 Mechanical

- **Construction:** Aluminum housing
- **Mounting:** Wall mounting
- **Dimensions (W x H x D):** 260 x 54 x 140.2 mm (10.24" x 2.13" x 5.52")
- **Weight:** 2.3KG

### 1.2.15 Environment

- **Operating Temperature:** With extended temp. peripherals: -20 ~ 60°C with 0.7m/s air flow (only up to 40°C when using with the adapter).
- **Storage Temperature:** -40~85°C (-40 ~ 185°F)
- **Relative Humidity:** 95% @ 40 °C (non-condensing)
- **Vibration during Operation:** 3 Grms, IEC60068-2-64, random, 5~500 Hz, and 1hr/axis (with Wall Mount)
- **Shock during Operation:** 30 G, IEC-60068-2-27, half sine, 11 ms duration (with Wall Mount)
- **EMC:** CE/FCC Class B, CCC, and BSMI
- **Safety:** UL, CB, CCC, and BSMI

## 1.3 Mechanical Drawing



## 1.4 Optional MOS Modules for iDoor Expansion

**Table 1.1: Optional MOS Modules for iDoor Expansion**

Part Number	Description
MOS-2230-Z1201E	CANBus module, 2-Ch, USB Interface
MOS-2220-X1101E	Parallel LPT module, 1-Ch, USB Interface
MOS-2110Z-1201E	USB module, 2-Ch, PCIe Interface
MOS-2120-Z1101E	Giga LAN Ethernet module, 1-Ch, PCIe Interface
MOS-1120Y-0202E	Isolated RS-232, 2-Ch, DB9, PCIe Interface
MOS-1121Y-0202E	Isolated RS-422/485, 2-Ch, DB9, PCIe Interface
MOS-1120Y-1402E	Non-Isolated RS-232, DB37, 4-Ch, PCIe Interface
MOS-1130Y-0201E	Isolated CANBus, 2-Ch, DB9, PCIe Interface
MOS-1110Y-0101E	Isolated 16 DI/8 DO, 1-Ch, DB37, PCIe Interface
MOS-2120-Z1201	Dual Intel I210 GbE LAN iDoor, 2-Ch, PCIe I/F
MOS-2220-Z1101E	High-speed Serial COM module, 1-Ch, USB Interface



# Chapter 2

## Hardware Installation

## 2.1 Introduction

This chapter details instructions for installing the ARK-2251 series. The following sections show the internal jumper settings and the external connector pin assignments.

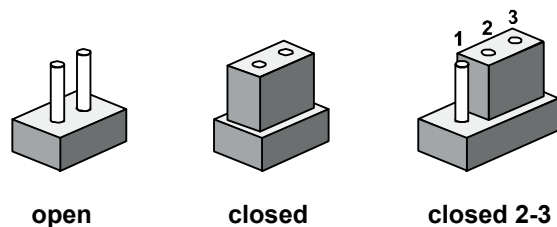
**Note!** Hardware installation must be performed by the skilled personnel



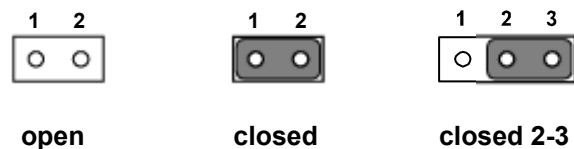
## 2.2 Jumpers

### 2.2.1 Jumper Description

Configure the ARK-2251 to meet specific application needs by adjusting jumpers. A jumper, functioning as a metal bridge, closes an electric circuit. It typically comprises two metal pins and a small metal clip, often protected by plastic. To close a jumper, connect the pins with the clip, and to open it, remove the clip. In cases where a jumper has three pins labeled 1, 2, and 3, connect either pins 1 and 2 or 2 and 3.



The jumper settings are schematically depicted in this manual as follows.



A pair of needle-nose pliers may be helpful when working with jumpers. If you have any doubts about the best hardware configuration for your application, contact your local distributor or sales representative before you make any changes. Generally, you simply need a standard cable to make most connections.

### 2.2.2 Jumper List

**Table 2.1: Jumper List**

Location	Function
CN22	AT/ATX Mode
JCMOS1	Clear CMOS
J1	Mini PCIe/M.2 E PCIe Switch
ERP1	Power Saving for ERP
CN20	Mini PCIe Power Selection
SW_422_3	RS-485/RS-422 Failsafe
SW_422_4	RS-485/RS-422 Failsafe
SW_422_5	RS-485/RS-422 Failsafe
SW_422_6	RS-485/RS-422 Failsafe



## 2.2.3 Jumper Locations

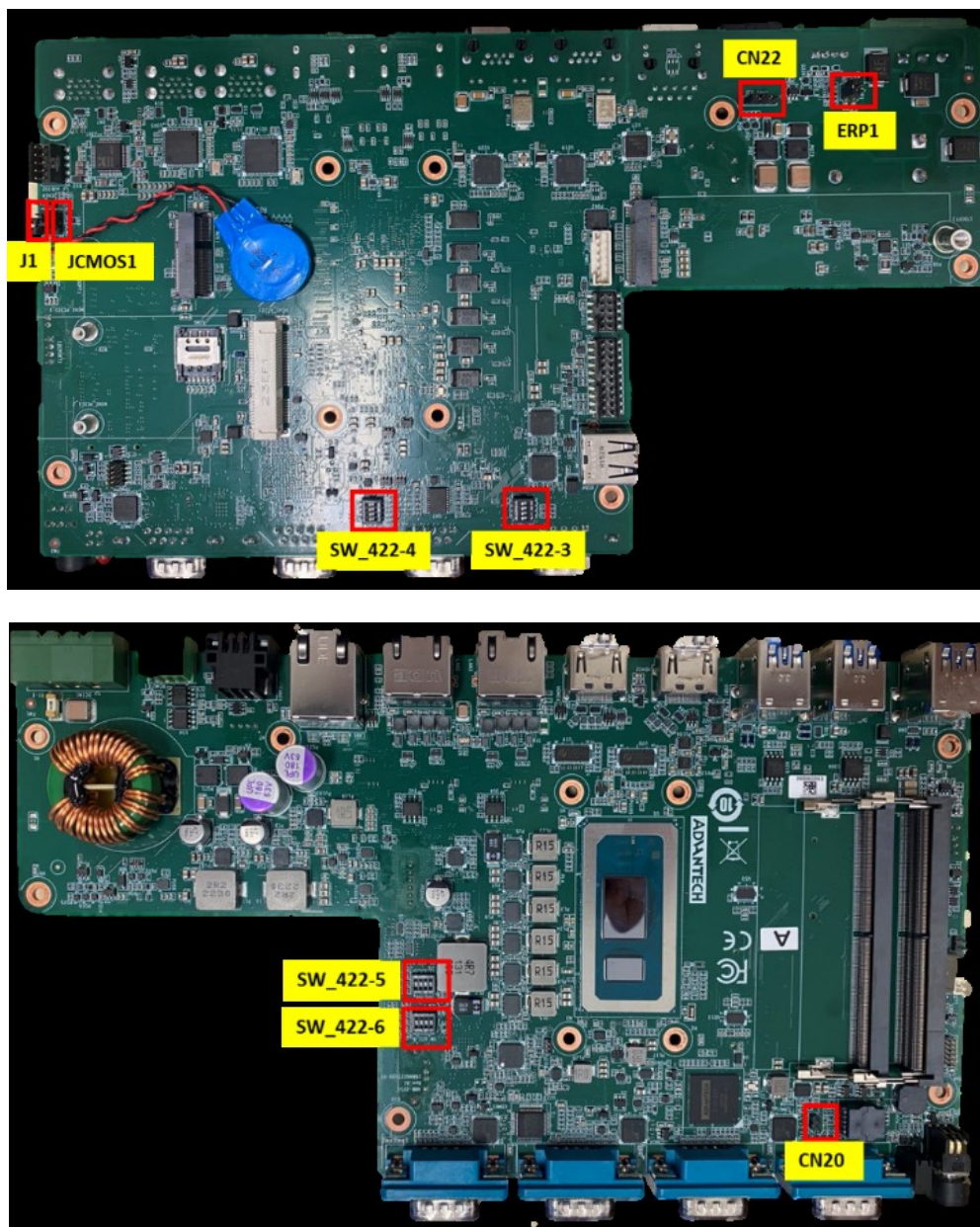
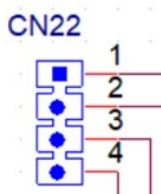


Figure 2.1 Jumper Layout

## 2.2.4 Jumper Settings

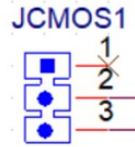
Table 2.2: CN22 Jumper Setting: AT/ATX Mode

Pin	Description
1-2	ATX Mode (default)
3-4	AT Mode



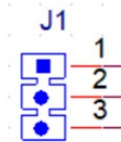
**Table 2.3: JCMOS1 Jumper Setting: Clear CMOS**

PIN	Description
1-2	Normal (default)
2-3	Clear CMOS



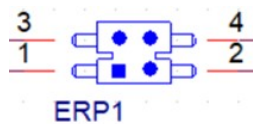
**Table 2.4: J1 Jumper Setting: Mini PCIe/M.2 E PCIe Switch**

PIN	Description
1-2	Mini PCIe
2-3	M.2 E (default)



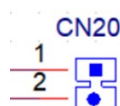
**Table 2.5: ERP1 Jumper Setting: Power Saving for ERP**

PIN	Description
1-2	ERP Disable (default)
3-4	ERP Enable



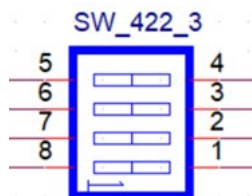
**Table 2.6: CN20 Jumper Setting: Mini PCIe Power Selection**

PIN	Description
1-2	Mini PCIe VCC=3.8V
3-4	Mini PCIe VCC=3.3V (default)

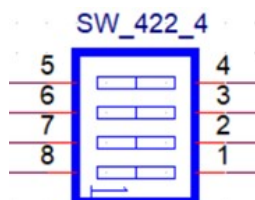


**Table 2.7: SW\_422\_3 Setting: RS-485/RS-422 Failsafe**

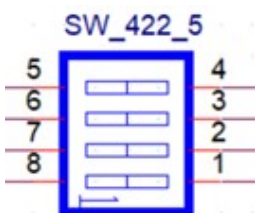
PIN	Description
1-8, 2-7, 3-6, 4-5	Enable COM3 failsafe
1-8, 2-7, 3-6, 4-5	Disable COM3 failsafe (default)

**Table 2.8: SW\_422\_4 Setting: RS-485/RS-422 Failsafe**

PIN	Description
1-8, 2-7, 3-6, 4-5	Enable COM4 failsafe
1-8, 2-7, 3-6, 4-5	Disable COM4 failsafe (default)

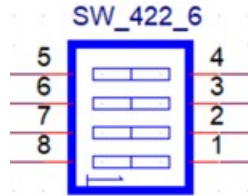
**Table 2.9: SW\_422\_5 Setting: RS-485/RS-422 Failsafe**

PIN	Description
1-8, 2-7, 3-6, 4-5	Enable COM5 failsafe
1-8, 2-7, 3-6, 4-5	Disable COM5 failsafe (default)

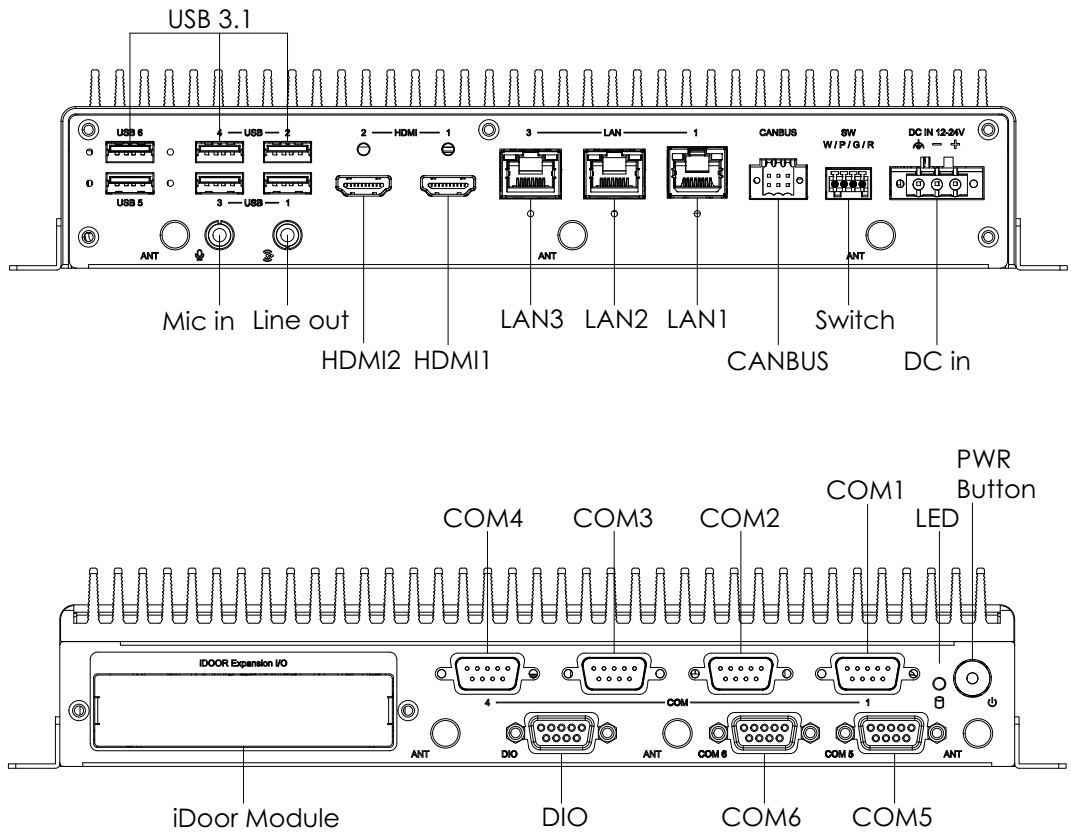


**Table 2.10: SW\_422\_6 Setting: RS-485/RS-422 Failsafe**

PIN	Description
1-8, 2-7, 3-6, 4-5	Enable COM6 failsafe
1-8, 2-7, 3-6, 4-5	Disable COM6 failsafe (default)



## 2.3 System IO



**Figure 2.2 ARK-2251 Front and Rear I/O Connector Diagram**

## 2.4 External I/O

### 2.4.1 Power On/Off Button

ARK-2251 features a power on/off button with an LED indicator on top that shows on status (ON: Green LED, OFF: Orange LED).



Figure 2.3 Power ON/OFF Button

### 2.4.2 Power Input Connector

The power input connector supports 12 ~ 24 V. The 3 pins are defined as +, -, and GND.

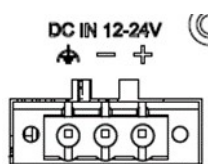


Figure 2.4 Power Input Connector

### 2.4.3 Ethernet Connector (LAN)

ARK-2251 is equipped with two Intel® i226-LM Ethernet controllers connected to LAN2 and LAN3 (Optional for PoE), as well as Intel® i219 Ethernet controllers connected to LAN1. The Ethernet ports provide standard RJ45 jack connectors with LED indicators on the sides to show Active/Link status (Green LED) and speed status (Yellow LED). LAN2 and LAN3 support PoE function by additional MIOe-PSE module(optional). The maximum voltage and rated current output for each PoE port is 50V/ 0.308A, 15.4W.

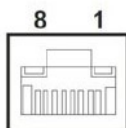


Figure 2.5 Ethernet Connector (LAN)

Table 2.11: Ethernet Connector (LAN) PIN Definition

Pin	10/100/1000/2500 Mbps Signal Name
1	BI_DA+(GHz)
2	BI_DA+(GHz)
3	BI_DB+(GHz)
4	BI_DC+(GHz)
5	BI_DC-(GHz)
6	BI_DB-(GHz)
7	BI_DD+(GHz)
8	BI_DD-(GHz)
H3	GND
H4	GND

\* LAN 2 and 3 are up to 2.5G, while LAN 1 is up to 1G.

## 2.4.4 USB 3.1 Connector

ARK-2251 supports 6 x USB 3.1 Gen 1 (2x are independent) interfaces, which support plug-and-play functionality and hot swapping for external devices. The USB interfaces comply with USB UHCI, Rev. 3.0.



Figure 2.6 USB 3.1 Connector

Table 2.12: USB 3.1 PIN Definition

Pin	Signal Name
1	+5V
2	D-_0
3	D+_0
4	GND
5	USB0_SSRX-
6	USB0_SSRX+
7	GND
8	USB0_SSTX-
9	USB0_SSTX+

## 2.4.5 Audio Connector

ARK-2251 supports stereo Line-Out and Mic- In audio ports. The audio chip is controlled by ALC888S and compliant with Azalea standards.



Figure 2.7 Audio Connector

## 2.4.6 COM Connector

ARK-2251 provides six 9-pin D-sub connectors, which support RS-232/422/485 serial communication interface ports. The default setting is RS-232, if you want to use RS-422/485, you can change the setting in BIOS.

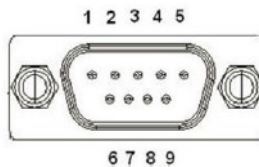


Figure 2.8 COM Connector

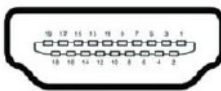
**Table 2.13: COM Connector PIN Definition**

Pin	RS-232	RS-422	RS-485
1	DCD	Tx-	DATA-
2	RxD	Tx+	DATA+
3	TxD	Rx+	NC
4	DTR	Rx-	NC
5	GND	GND	GND
6	DSR	NC	NC
7	RTS	NC	NC
8	CTS	NC	NC
9	RI	NC	NC

NC represents “No Connection”

## 2.4.7 HDMI Connector

ARK-2251 offers 2 x integrated 19-pin receptacle connector HDMI 2.0b interfaces. The HDMI link supports resolutions up to 4096x2160 @60 Hz.

**Figure 2.9 HDMI Connector****Table 2.14: HDMI Connector PIN Definition**

Pin	Signal Name
1	HDMI_TX2+
2	GND
3	HDMI_TX2-
4	HDMI_TX1+
5	GND
6	HDMI_TX1-
7	HDMI_TX0+
8	GND
9	HDMI_TX0-
10	HDMI_CLK+
11	GND
12	HDMI_CLK-
13	NC
14	NC
15	HDMI_DCLK
16	HDMI_DDAT
17	GND
18	+V5_HDMI-HPD
19	DDP0_HPDP

NC represents “No Connection”

## 2.4.8 DIO Connector

ARK-2251 provides 1 x 8-bit DIO connector.

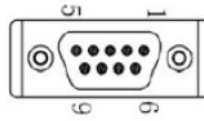


Figure 2.10 DIO Connector

Table 2.15: DIO Connector PIN Definition

Pin	Signal Name
1	DIO bit 0
2	DIO bit 1
3	DIO bit 2
4	DIO bit 3
5	DIO bit 4
6	DIO bit 5
7	DIO bit 6
8	DIO bit 7
9	GND

## 2.4.9 Remote Switch Connector

ARK-2251 provides a remote switch connector for power on/off via an external cable.

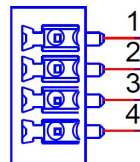


Figure 2.11 Remote Switch Connector

Table 2.16: Remote Switch Connector PIN Definition

Pin	Signal Name
1	WDT
2	PWRBTN
3	GND
4	SYSRST



## 2.4.10 CANBus

ARK-2251 provides a 6-pin terminal block for Canbus.

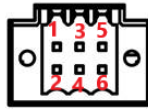


Figure 2.12 Canbus Connector

Table 2.17: CANBus Connector PIN Definition

Pin	Signal Name
1	CAN0_D-
2	CAN1_D+
3	GND
4	GND
5	CAN0_D+
6	CAN1_D-

## 2.5 Installation

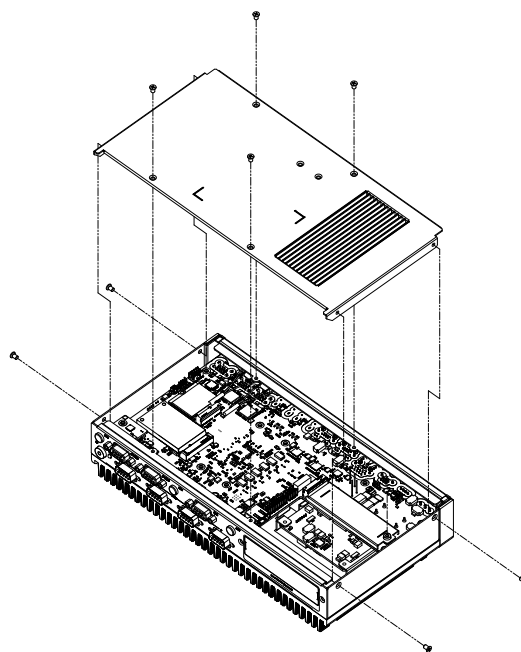
**Note!** This should be performed by skilled personnel.



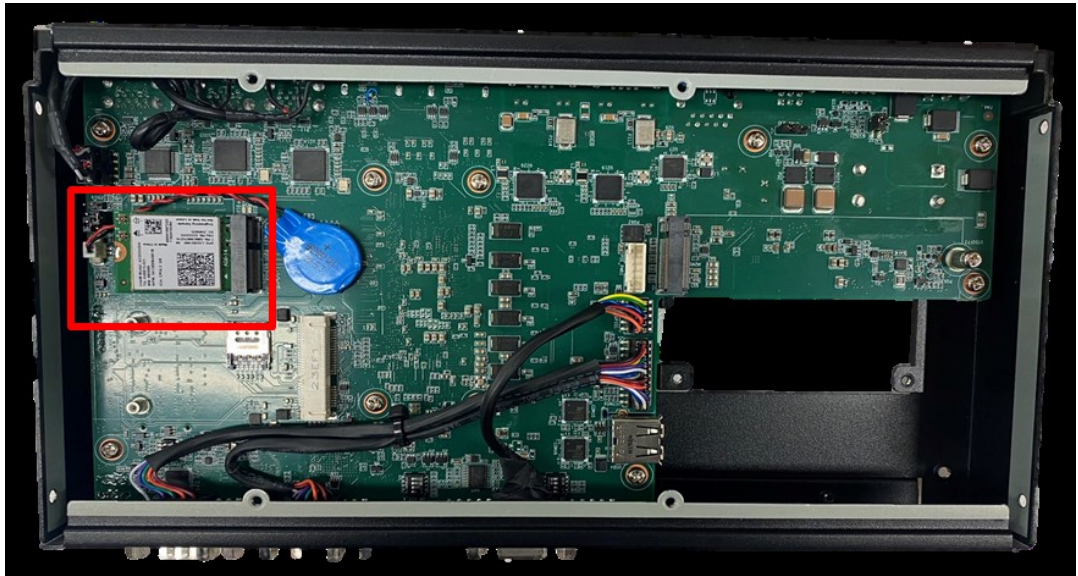
### 2.5.1 M.2 Installation

For the M.2 E KEY

1. Loosen the 8 x screws (M3x5L) on the bottom/sides and remove the bottom cover.

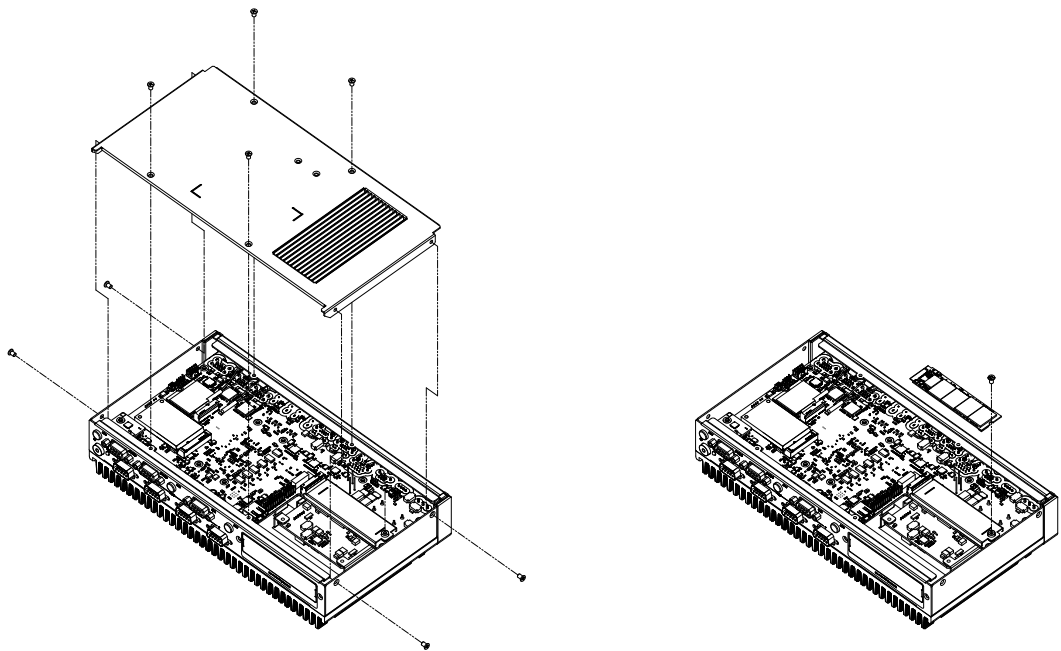


2. Install the M.2 E Key Module with the screw.
3. Put the bottom cover back and secure it with the 8 x screws (M3x5L).



For the M.2 M KEY

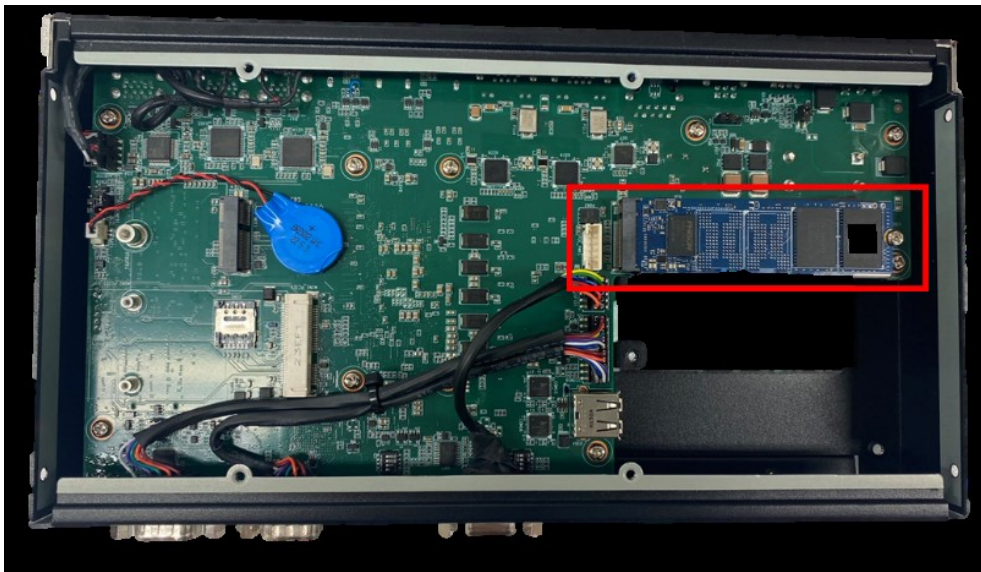
1. Loosen the 8 x screws on the front/sides and remove the bottom cover.



2. Take the bracket with thermal pad and the screw(M3\*5L) out from the accessory box then install it on the right position.



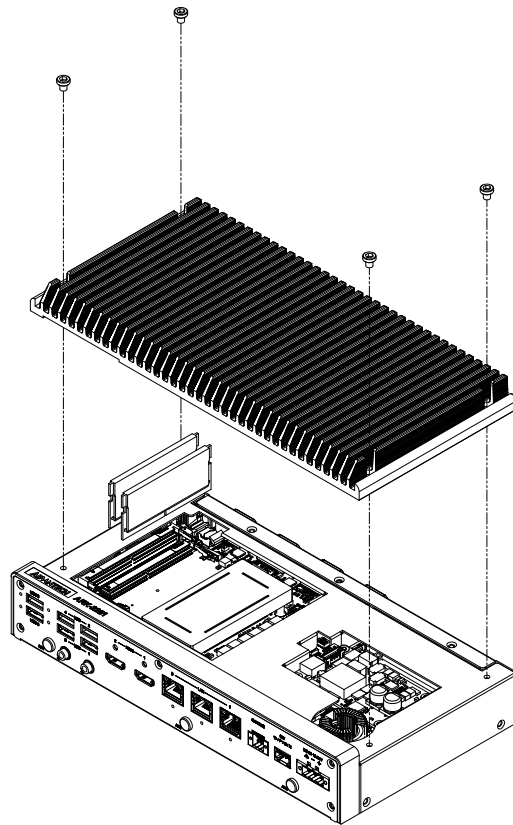
3. Install the M.2 M Key Device on the bracket.



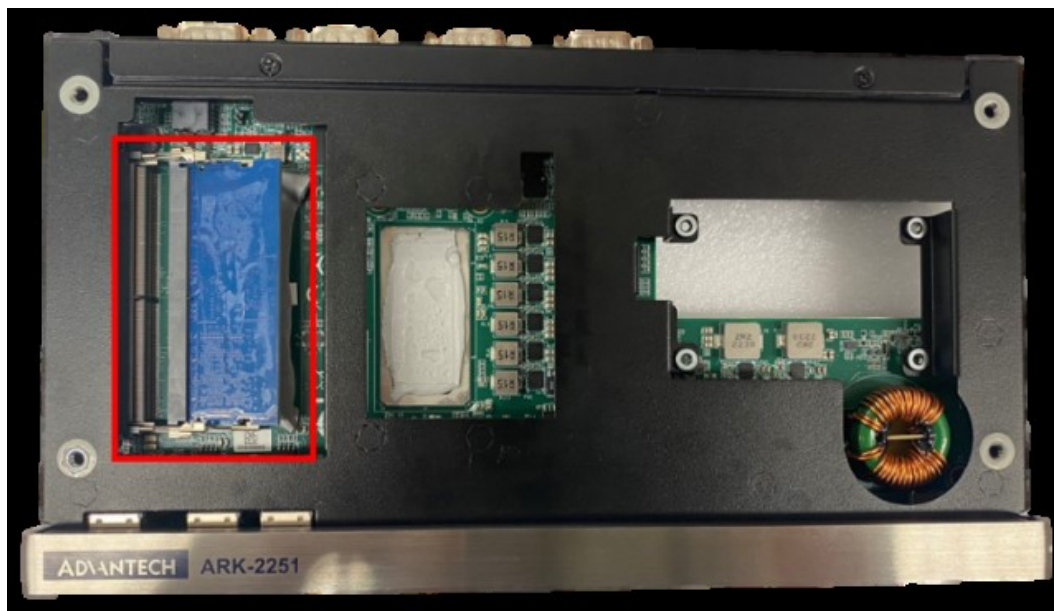
4. Put the bottom cover back and secure it with the 8 x screws.

## 2.5.2 Memory Installation

1. Remove the top cover with the wrench in the accessory box.

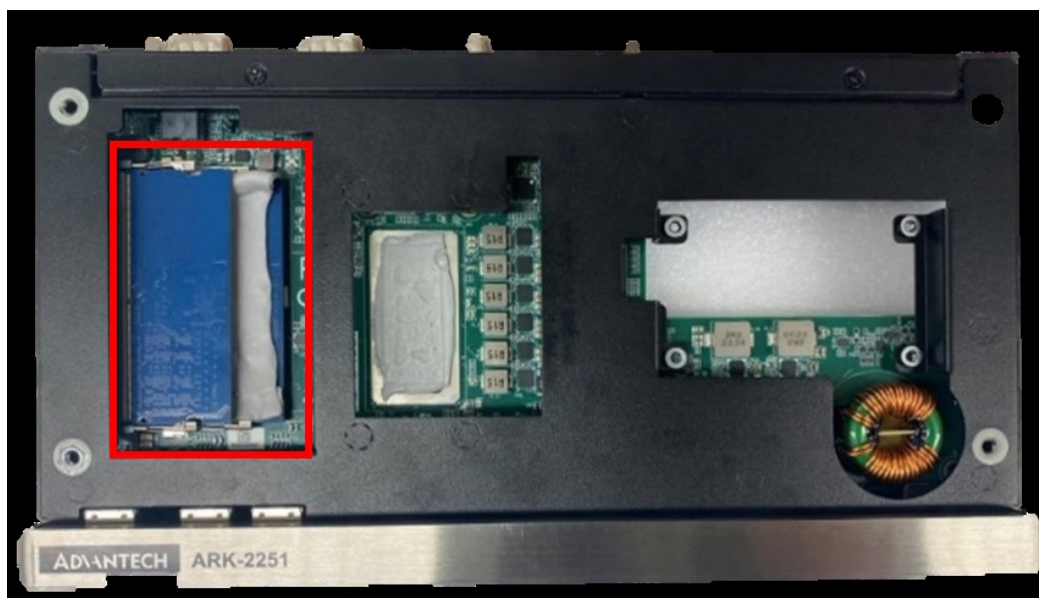


2. Carefully install RAM memory into the slots





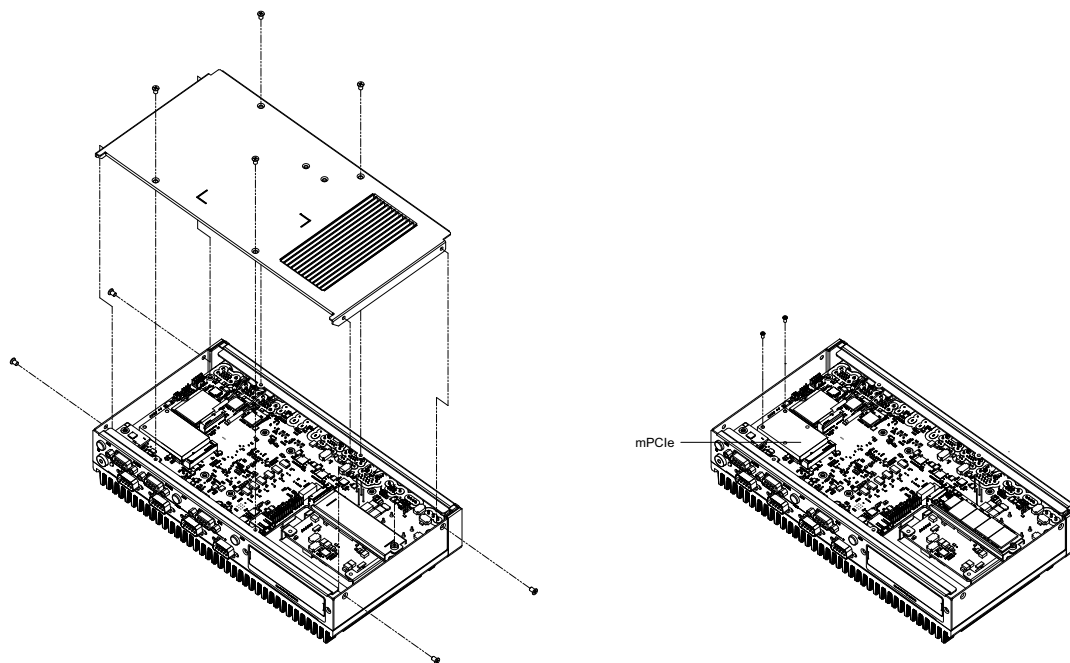
3. To install a second memory module, apply the thermal pad (located in the accessory box) before installing the memory.



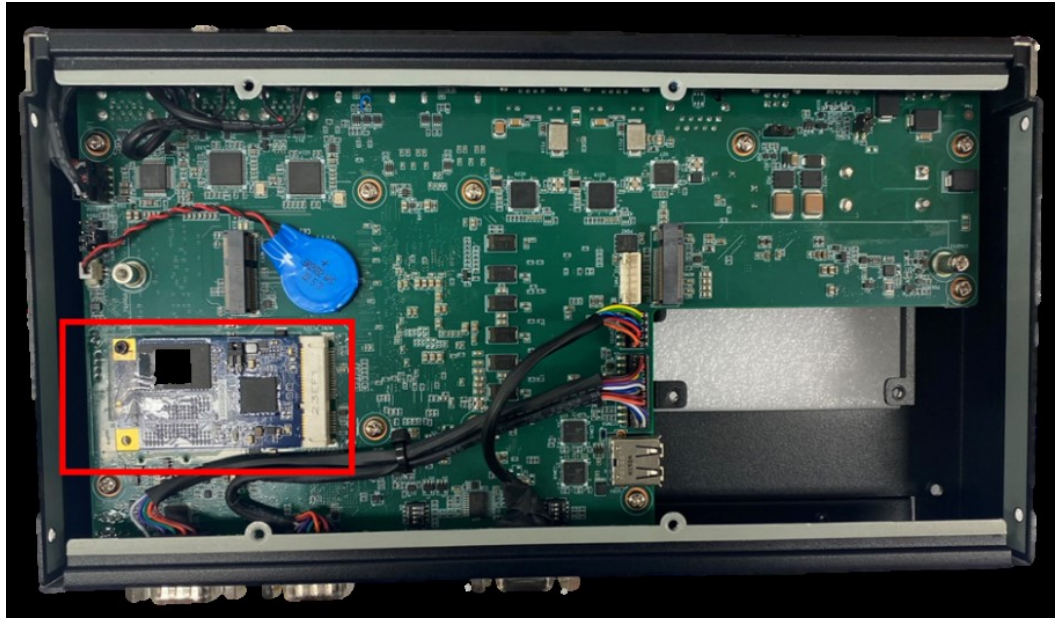
4. Put the top cover back and secure it with the 8x screws

### 2.5.3 mPCIe/mSATA Installation

1. Loosen the 8 x screws on the front/sides and remove the bottom cover.



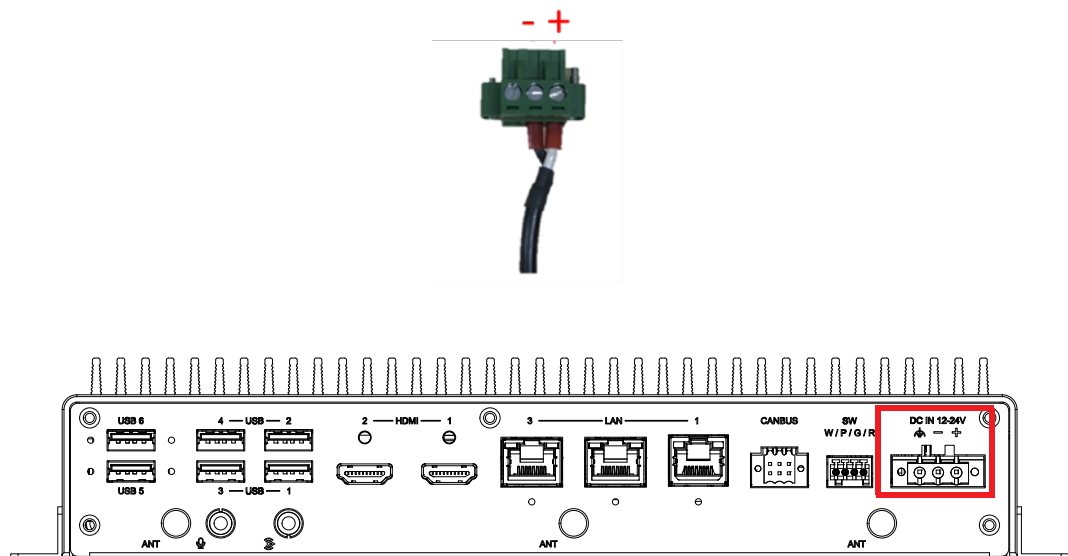
2. Install mPCIe/mSATA module.



3. Put the bottom cover back and secure it with the 8 x screws.

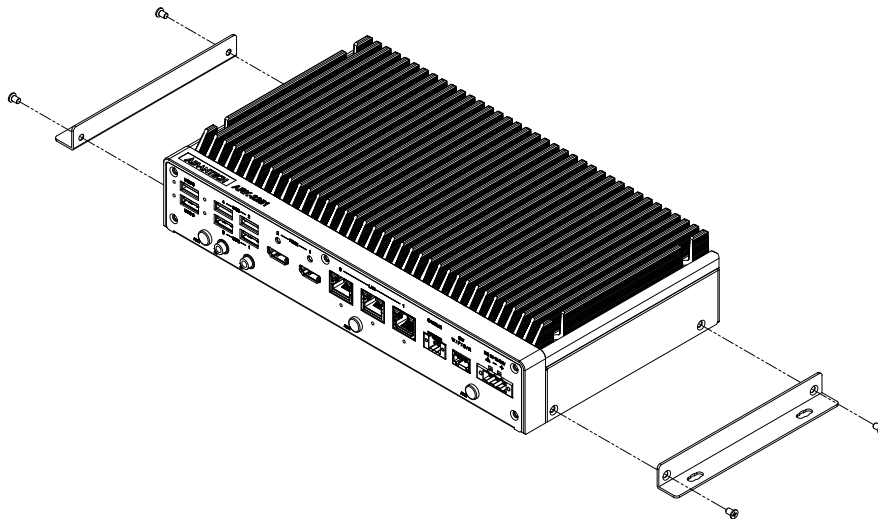
## 2.5.4 Adapter Installation

1. Connect the 3-pin Phoenix connector to the DC input.



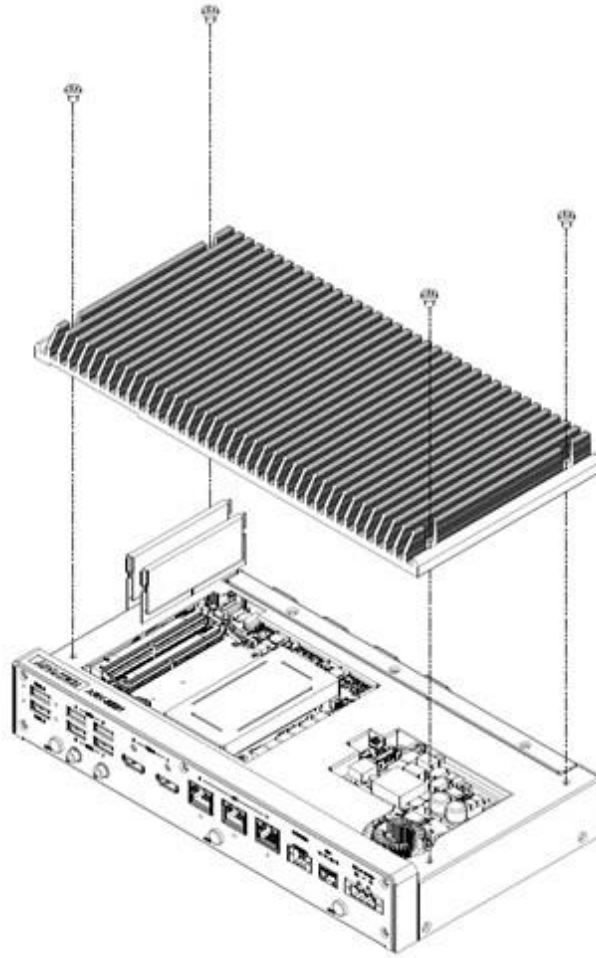
## 2.5.5 Wall Mount Installation

1. Unscrew the 4 x M3x5L screws on both sides of ARK- 2251.
2. Secure the wall mount brackets on both sides of ARK-2251 using the 4 x screws removed as shown in the above step.
1. Dévissez les 4x vis M3x5L ou des deux côtés de l'ARK-2251.
2. Vissez les supports de montage mural des deux côtés de l'ARK-2251 avec les quatre vis à l'arrière.



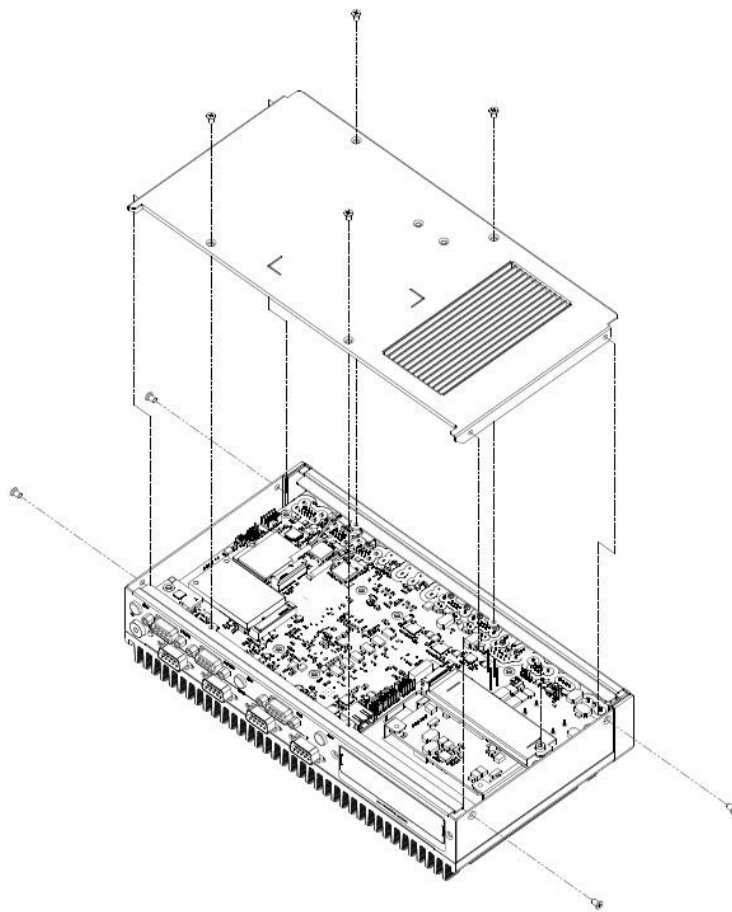
## 2.5.6 PoE Installation

1. Remove the top cover with the wrench in the accessory box.

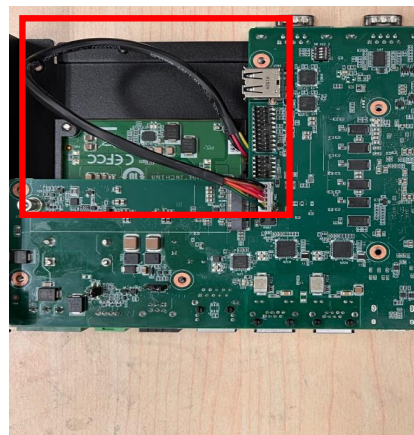
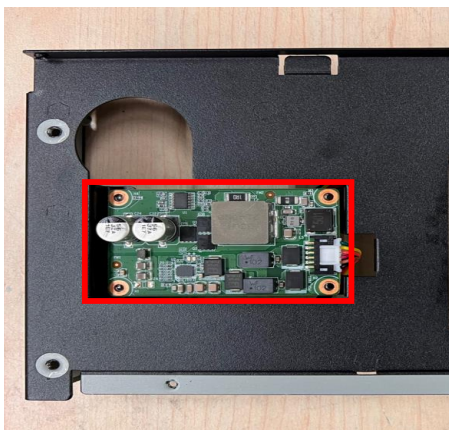




2. Loosen the 8 x screws on the front/sides and remove the bottom cover.



3. Attach the PoE module and then connect the cable to the ARK-2251.





# Chapter 3

## BIOS Settings

This chapter details instructions of setting BIOS configuration data.

## 3.1 Introduction

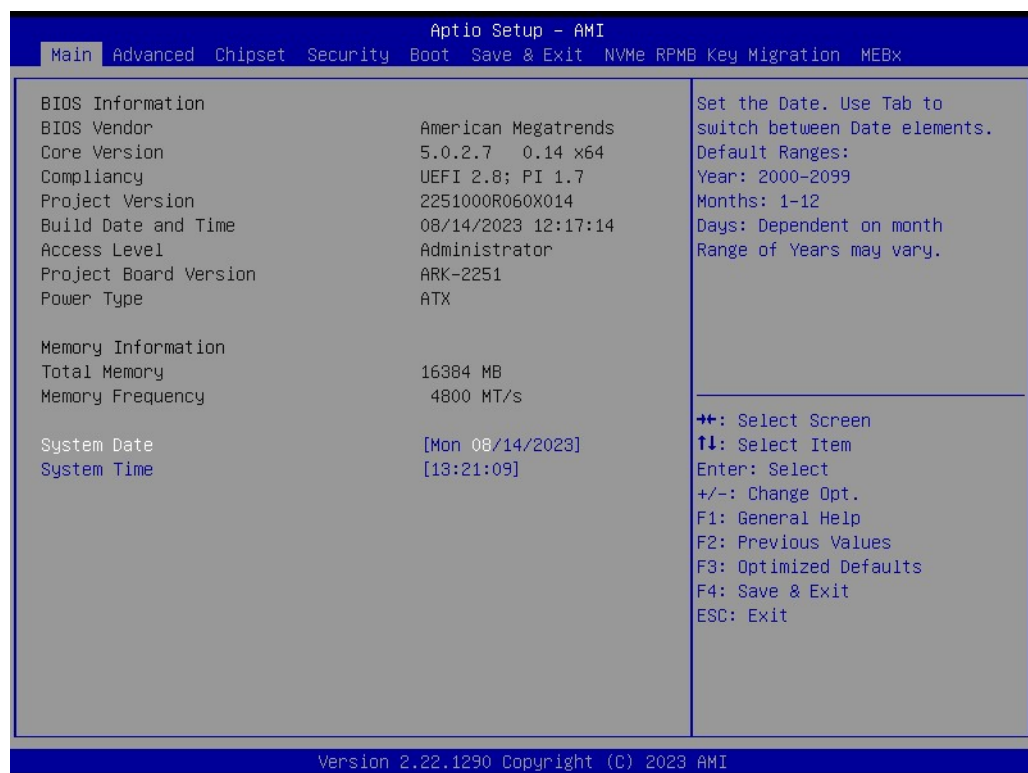
The AMI BIOS ROM has a built-in setup program - the BIOS Setup Utility - that allows users to modify the basic system configuration. All configuration data is stored in battery-backed CMOS to ensure the setup information is retained when the power is turned off. This chapter describes the basic navigation of the ARK-2251 BIOS setup screens.

## 3.2 Entering BIOS Setup

Turn on the computer and check for the patch code. If there is a number assigned to the patch code, it means that BIOS supports your CPU. If there is no number assigned to the patch code, please contact an Advantech application engineer to obtain an up-to-date patch code file. This will ensure that your CPU's system status is valid. After ensuring that you have a number assigned to the patch code, press <DEL> and you will immediately be allowed to enter Setup.

### 3.2.1 Main Setup

When users first enter the BIOS Setup Utility, they will enter the Main setup screen. Users can always return to the Main setup screen by selecting the Main tab. There are two Main Setup options. They are described in this section. The Main BIOS Setup screen is shown below.



The Main BIOS setup screen has two main frames. The left frame displays all the options that can be configured. Grayed-out options cannot be configured; options in blue can. The right frame displays the key legend.

Above the key legend is an area reserved for a text message. When an option is selected in the left frame, it is highlighted in white. Often a text message will accompany it.

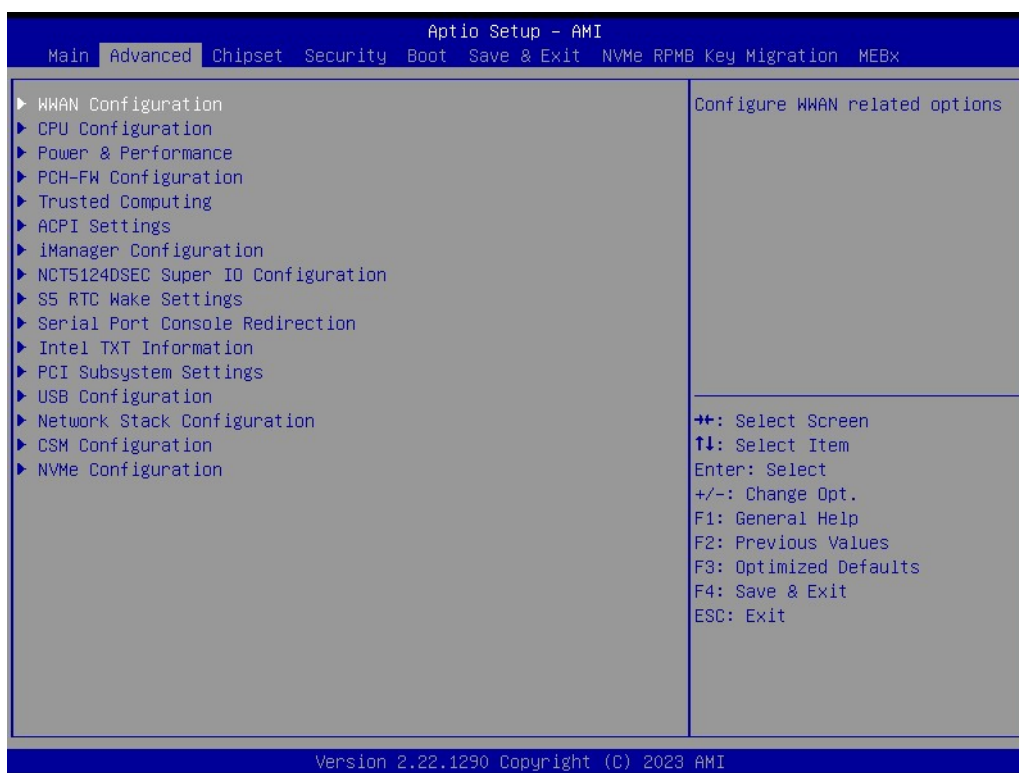
### System time / System date

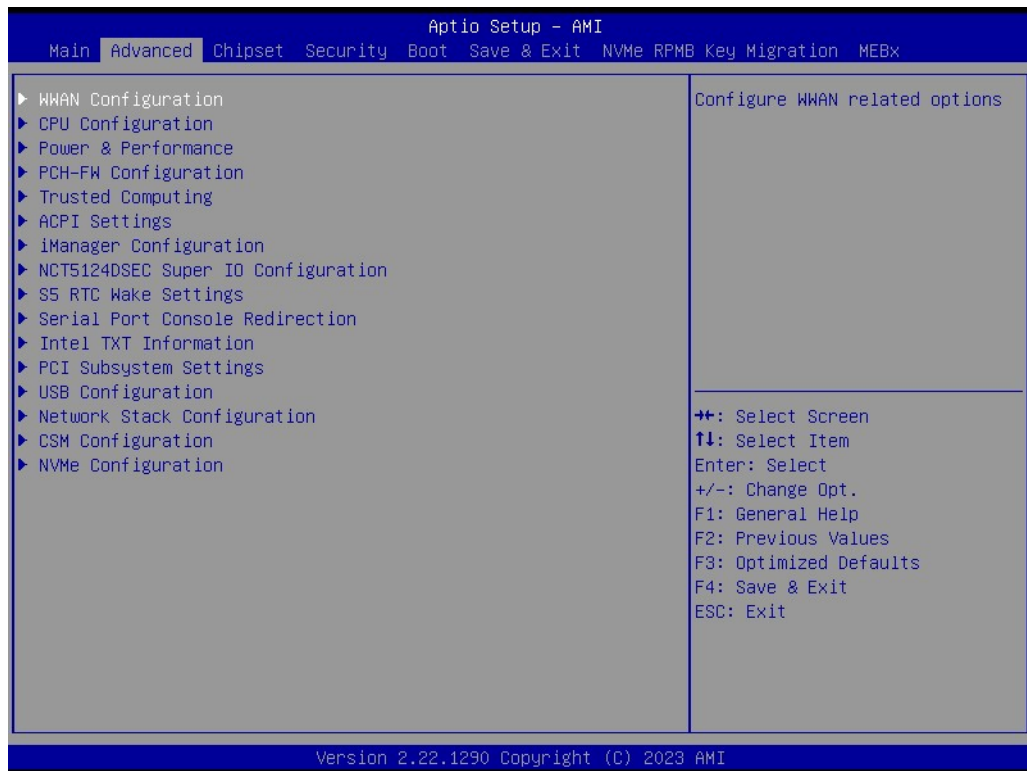
Use this option to change the system time and date. Highlight System Time or System Date using the <Arrow> keys. Enter new values through the keyboard. Press the <Tab> key or the <Arrow> keys to move between fields. The date must be entered in MM/DD/YY format. The time must be entered in HH:MM:SS format.

## 3.2.2 Advanced BIOS Features Setup

Select the Advanced tab from the ARK-2251 setup screen to enter the Advanced BIOS Setup screen. Users can select any item in the left frame of the screen, such as CPU Configuration, to go to the sub menu for that item. Users can display an Advanced BIOS Setup option by highlighting it using the <Arrow> keys. All Advanced BIOS Setup options are described in this section. The Advanced BIOS Setup screens are shown below. The sub menus are described on the following pages.

### 3.2.2.1 WWAN Configuration

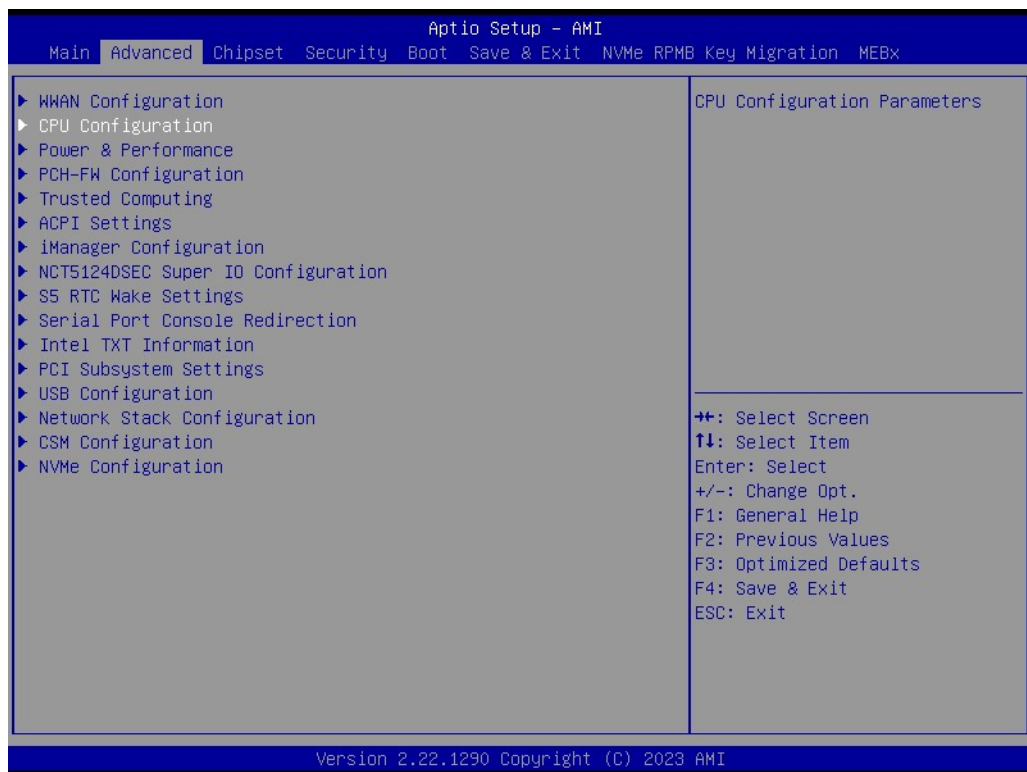




■ **WWAN DEVICE**

Select the M.2 WWAN Device options to enable 4G - 7360/7560 (Intel), 5G - M80 (MediaTek) Modems

**3.2.2.2 CPU Configuration**



## Efficient-core Information

Aptio Setup - AMI

Advanced

CPU Configuration		Displays the E-core Information
<ul style="list-style-type: none"> <li>▶ Efficient-core Information</li> <li>▶ Performance-core Information</li> </ul>		
Brand String	13th Gen Intel(R) Core(TM) i5-1335UE	<hr/> ++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
ID	0xB06A3	
Microcode Revision	4114	
VMX	Supported	
SMX/TXT	Supported	
TXT Crash Code	0x00000000	
TXT SPAD	0x9040000000000000	
Boot Guard Status	0xC0008000	
Boot Guard ACM Policy Status	0x0000000000000000	
Boot Guard SACM Information	0x0000001100000000	
C6DRAM	[Enabled]	
CPU Flex Ratio Override	[Disabled]	
CPU Flex Ratio Settings	25	
Hardware Prefetcher	[Enabled]	
Adjacent Cache Line Prefetch	[Enabled]	
Intel (VMX) Virtualization Technology	[Enabled]	
PECI	[Enabled]	

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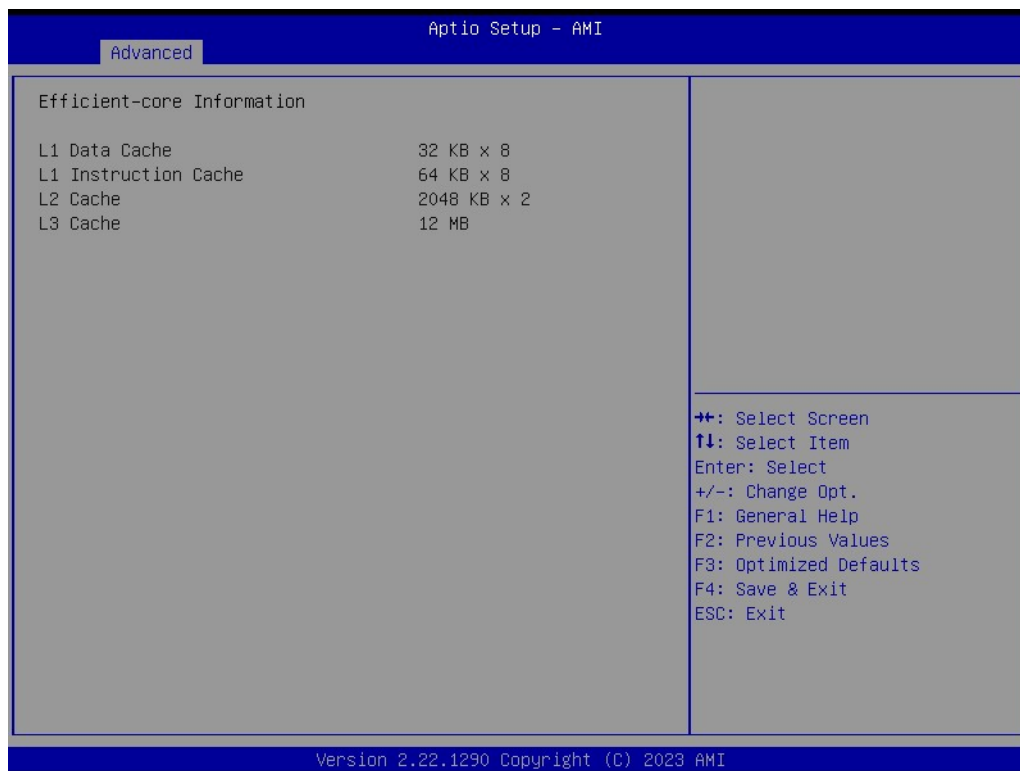
Aptio Setup - AMI

Advanced

Boot Guard ACM Policy Status 0x0000000000000000 Boot Guard SACM Information 0x0000001100000000		▲ Enable/Disable the Avx 2 Instructions. This is applicable for Performance-core only
C6DRAM [Enabled] CPU Flex Ratio Override [Disabled] CPU Flex Ratio Settings 25 Hardware Prefetcher [Enabled] Adjacent Cache Line Prefetch [Enabled] Intel (VMX) Virtualization Technology [Enabled] Peci [Enabled] AVX [Enabled] Active Performance-cores [All] Active Efficient-cores [All] Hyper-Threading [Enabled] BIST [Disabled] AP threads Idle Manner [MWAIT Loop] AES [Enabled] MachineCheck [Enabled] MonitorMwait [Enabled] Intel Trusted Execution Technology [Disabled] Alias Check Request [Disabled] DPR Memory Size (MB) 4 Reset AUX Content [no]		
▶ CPU SMM Enhancement		<hr/> ++: Select Screen ↑↓: Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit

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- **C6DRAM**  
Enable/Disable moving of DRAM contents to PRM memory when CPU is in C6 state.
- **CPU Flex Ratio Override**  
Enable/Disable CPU Flex Ratio Programming.
- **CPU Flex Ratio Settings**  
This value must be between Max Efficiency Ratio (LFM) and Maximum non-turbo ratio set by Hardware (HFM).
- **Hardware Prefetcher**  
To turn on/off the MLC streamer prefetcher.
- **Adjacent Cache Line Prefetch**  
To turn on/off prefetching of adjacent cache lines.
- **Intel (VMX) Virtualization Technology**  
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
- **PECI**  
Enable/Disable Peci.
- **AVX**  
Enable/Disable the Avx 2 Instructions. This is applicable for Performance-core only
- **Active Performance-Cores**  
Number of cores to enable in each processor package.
- **Active Efficient-cores**  
Enable/Disable Per Core Disable. When Per Core Disable Configuration is enabled, selection of Active Cores and Active Efficient-cores will be disabled.
- **Hyper-Threading**  
Enable/Disable Hyper-Threading Technology.



- **BIST**  
Enable/Disable BIST (Built-in Self Test) on reset
- **AP threads Idle Manner**  
AP threads Idle Manner for waiting signal to run.
- **AES**  
Enable/Disable AES (Advanced Encryption Standard)
- **MachineCheck**  
Enable/Disable Machine Check.
- **MonitorMWait**  
Enable/Disable MonitorMWait, if Disable MonitorMwait, the AP threads Idle Manner should not set in MWAIT Loop
- **Intel Trusted Execution Technology**  
Enables utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology.
- **Alias Check Request**  
Enables Txt Alias Checking capability.
- **DPR memory size (MB)**  
Reserve DPR memory size (0-255) MB
- **Reset AUX Content**  
Reset TPM Aux content. Txt may not functional after AUX content gets reset.
- **L1 Data Cache**  
Displays the Efficient-core L1 Data Cache size.
- **L1 Instruction Cache**  
Displays the Efficient-core L1 Instruction Cache size.
- **L2 Cache**  
Displays the Efficient-core L2 Cache size.
- **L3 Cache**  
Displays the Performance-core L3 Cache size.

## Power and Performance – CPU Power Management Control

Aptio Setup - AMI

Advanced

CPU Configuration

- ▶ Efficient-core Information
- ▶ Performance-core Information

Brand String	13th Gen Intel(R) Core(TM) i5-1335UE
ID	0xB06A3
Microcode Revision	4114
VMX	Supported
SMX/TXT	Supported
TXT Crash Code	0x00000000
TXT SPAD	0x9040000000000000
Boot Guard Status	0xC0008000
Boot Guard ACM Policy Status	0x0000000000000000
Boot Guard SADM Information	0x0000001100000000

---

C6DRAM	[Enabled]
CPU Flex Ratio Override	[Disabled]
CPU Flex Ratio Settings	25
Hardware Prefetcher	[Enabled]
Adjacent Cache Line Prefetch	[Enabled]
Intel (VMX) Virtualization Technology	[Enabled]
PECI	[Enabled]

Displays the P-core Information

⇄: Select Screen  
 ↑↓: Select Item  
 Enter: Select  
 +/-: Change Opt.  
 F1: General Help  
 F2: Previous Values  
 F3: Optimized Defaults  
 F4: Save & Exit  
 ESC: Exit

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Aptio Setup - AMI

Advanced

Boot Guard ACM Policy Status	0x0000000000000000
Boot Guard SADM Information	0x0000001100000000

---

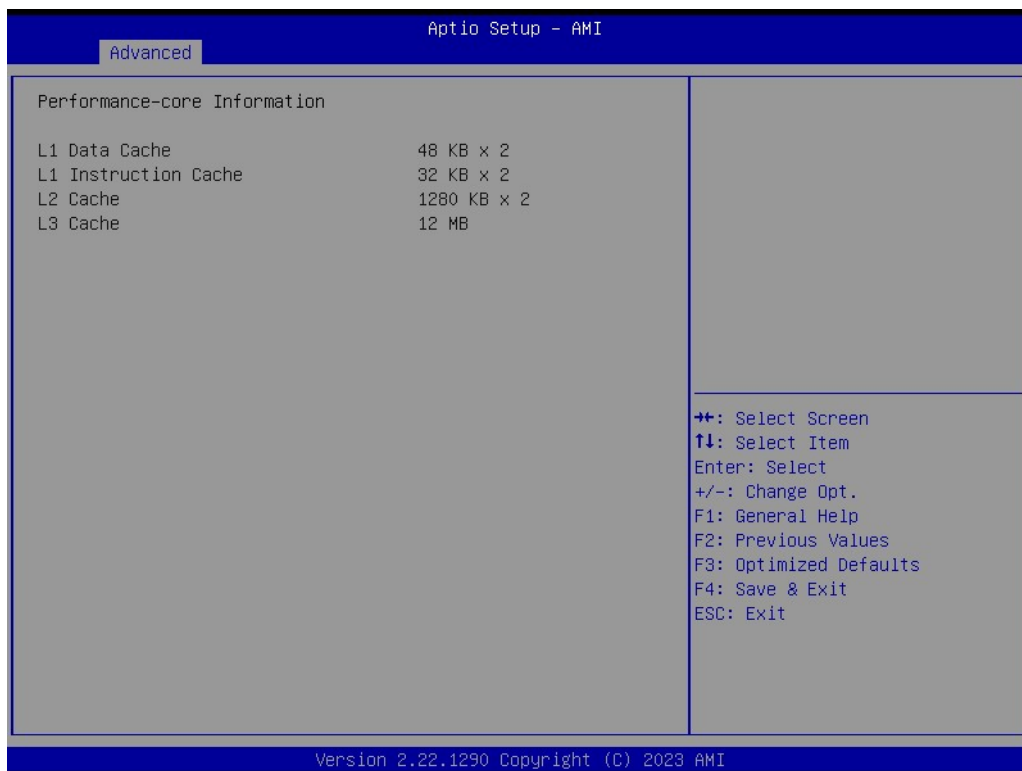
C6DRAM	[Enabled]
CPU Flex Ratio Override	[Disabled]
CPU Flex Ratio Settings	25
Hardware Prefetcher	[Enabled]
Adjacent Cache Line Prefetch	[Enabled]
Intel (VMX) Virtualization Technology	[Enabled]
PECI	[Enabled]
AVX	[Enabled]
Active Performance-cores	[All]
Active Efficient-cores	[All]
Hyper-Threading	[Enabled]
BIST	[Disabled]
AP threads Idle Manner	[MWAIT Loop]
AES	[Enabled]
MachineCheck	[Enabled]
MonitorMWait	[Enabled]
Intel Trusted Execution Technology	[Disabled]
Alias Check Request	[Disabled]
DPR Memory Size (MB)	4
Reset AUX Content	[no]

▶ CPU SMM Enhancement

CPU SMM Enhancement

⇄: Select Screen  
 ↑↓: Select Item  
 Enter: Select  
 +/-: Change Opt.  
 F1: General Help  
 F2: Previous Values  
 F3: Optimized Defaults  
 F4: Save & Exit  
 ESC: Exit

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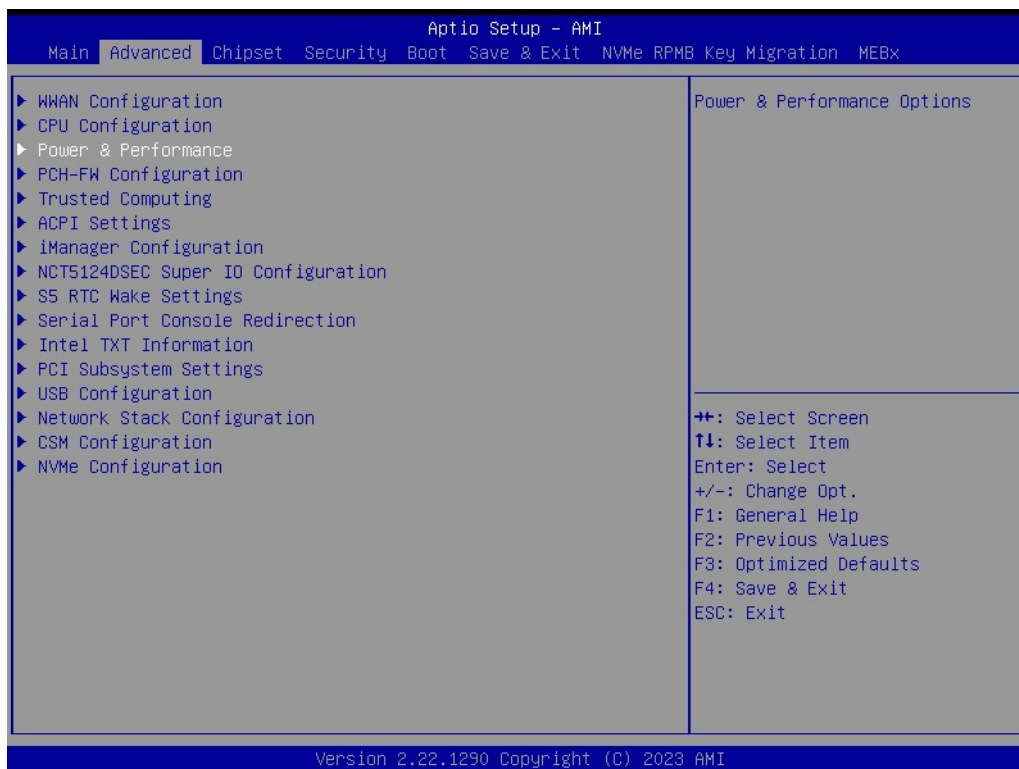
- **C6DRAM**  
Enable/Disable moving of DRAM contents to PRM memory when CPU is in C6 state.
- **CPU Flex Ratio Override**  
Enable/Disable CPU Flex Ratio Programming.

- **CPU Flex Ratio Settings**  
This value must be between Max Efficiency Ratio (LFM) and Maximum non-turbo ratio set by Hardware (HFM).
- **Hardware Prefetcher**  
To turn on/off the MLC streamer prefetcher.
- **Adjacent Cache Line Prefetch**  
To turn on/off prefetching of adjacent cache lines.
- **Intel (VMX) Virtualization Technology**  
When enabled, a VMM can utilize the additional hardware capabilities provided by Vanderpool Technology.
- **PECI**  
Enable/Disable Peci.
- **AVX**  
Enable/Disable the Avx 2 Instructions. This is applicable for Performance-core only
- **Active Performance-Cores**  
Number of cores to enable in each processor package.
- **Active Efficient-cores**  
Enable/Disable Per Core Disable. When Per Core Disable Configuration is enabled, selection of Active Cores and Active Efficient-cores will be disabled.
- **Hyper-Threading**  
Enable/Disable Hyper-Threading Technology.
- **BIST**  
Enable/Disable BIST (Built-in Self Test) on reset
- **AP threads Idle Manner**  
AP threads Idle Manner for waiting signal to run.
- **AES**  
Enable/Disable AES (Advanced Encryption Standard)
- **MachineCheck**  
Enable/Disable Machine Check.
- **MonitorMWait**  
Enable/Disable MonitorMWait, if Disable MonitorMwait, the AP threads Idle Manner should not set in MWAIT Loop
- **Intel Trusted Execution Technology**  
Enables utilization of additional hardware capabilities provided by Intel® Trusted Execution Technology.
- **Alias Check Request**  
Enables Txt Alias Checking capability.
- **DPR memory size (MB)**  
Reserve DPR memory size (0-255) MB
- **Reset AUX Content**  
Reset TPM Aux content. Txt may not functional after AUX content gets reset.
- **L1 Data Cache**  
Displays the Efficient-core L1 Data Cache size.
- **L1 Instruction Cache**  
Displays the Efficient-core L1 Instruction Cache size.
- **L2 Cache**  
Displays the Efficient-core L2 Cache size.

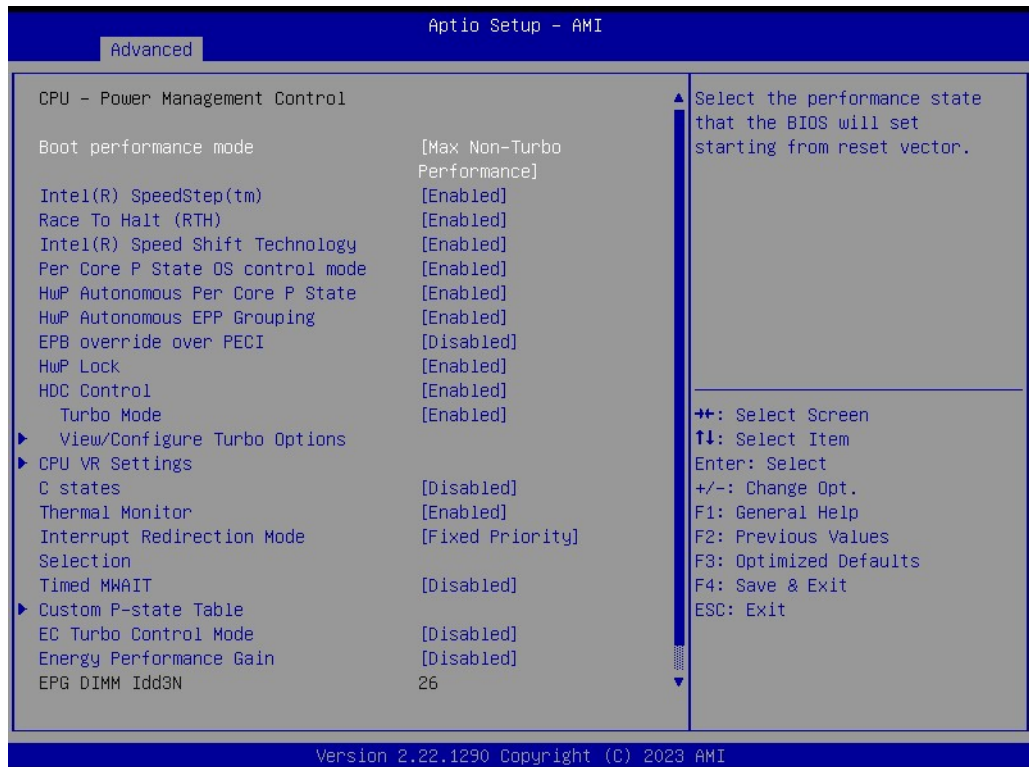
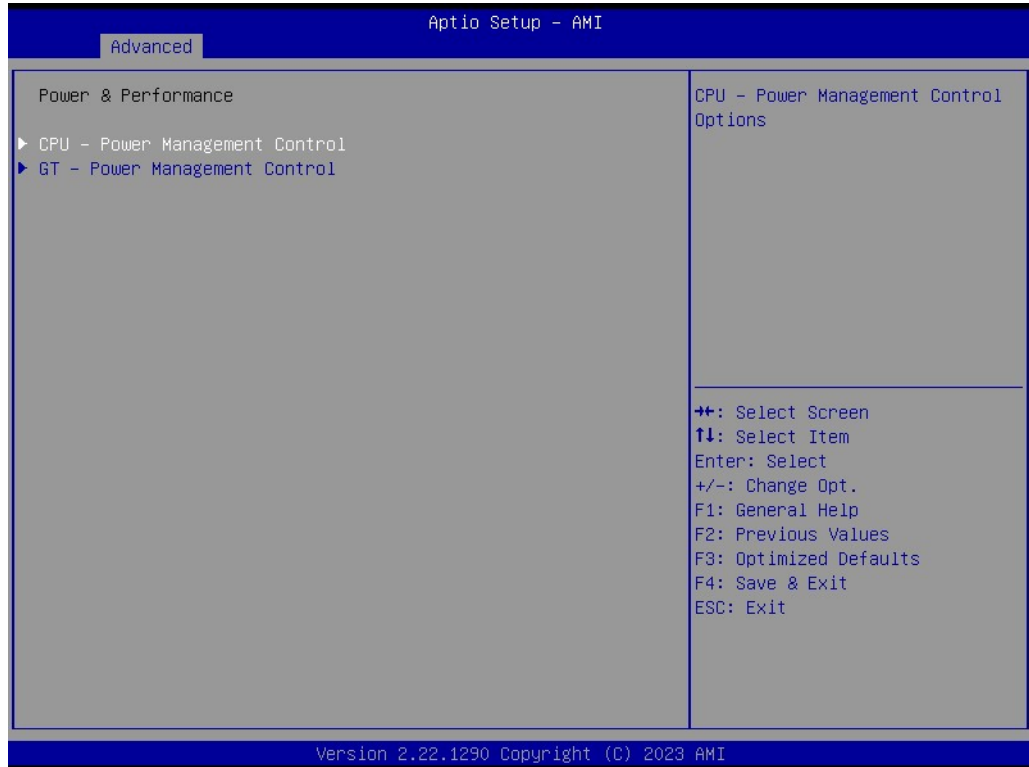
### ■ CPU SMM Enhancement

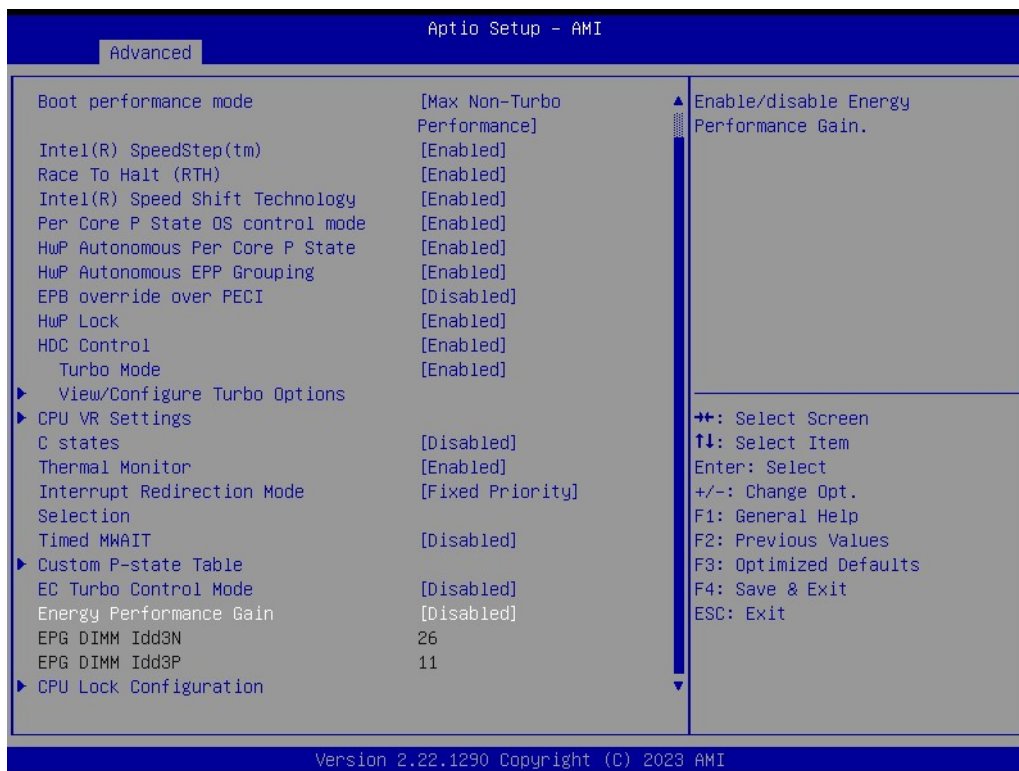
- SMM Use Delay Indication  
Enable/Disable usage of SMM\_DELAYED MSR for MP sync in SMI.
- SMM Use Block Indication  
Enable/Disable usage of SMM\_BLOCKED MSR for MP sync in SMI.
- SMM Use SMM en-US Indication  
Enable/Disable usage of SMM\_ENABLE MSR for MP sync in SMI

### 3.2.2.3 Power & Performance



## CPU - Power Management Control







Aptio Setup - AMI

Advanced

CPU VR Settings		PSYS Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x9.
Current VccIn Aux Icc Max	128	
PSYS Slope	0	<b>++</b> : Select Screen <b>↑↓</b> : Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
PSYS Offset	0	
PSYS Prefix	[+]	
PSYS PMax Power	0	
Min Voltage Override	[Disabled]	
VccIn Aux Icc Max	0	
VccIn Aux IMON Slope	100	
VccIN Aux IMON Offset	0	
VccIN Aux IMON Prefix	[+]	
Vsys/Psys Critical	[Disabled]	
Assertion Deglitch Mantissa	1	
Assertion Deglitch Exponent	0	
De assertion Deglitch Mantissa	13	
De assertion Deglitch Exponent	2	
VR Power Delivery Design	[AUTO]	
▶ Acoustic Noise Settings		
▶ Core/IA VR Settings		
▶ GT VR Settings		
▶ RFI Settings		

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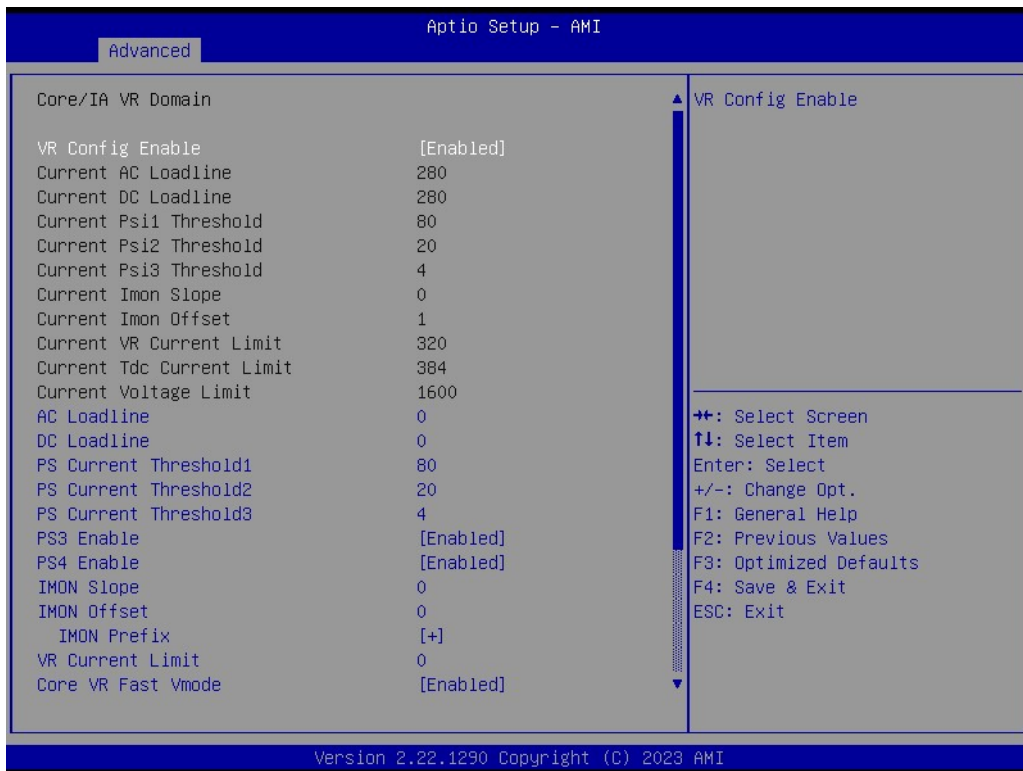
Aptio Setup - AMI

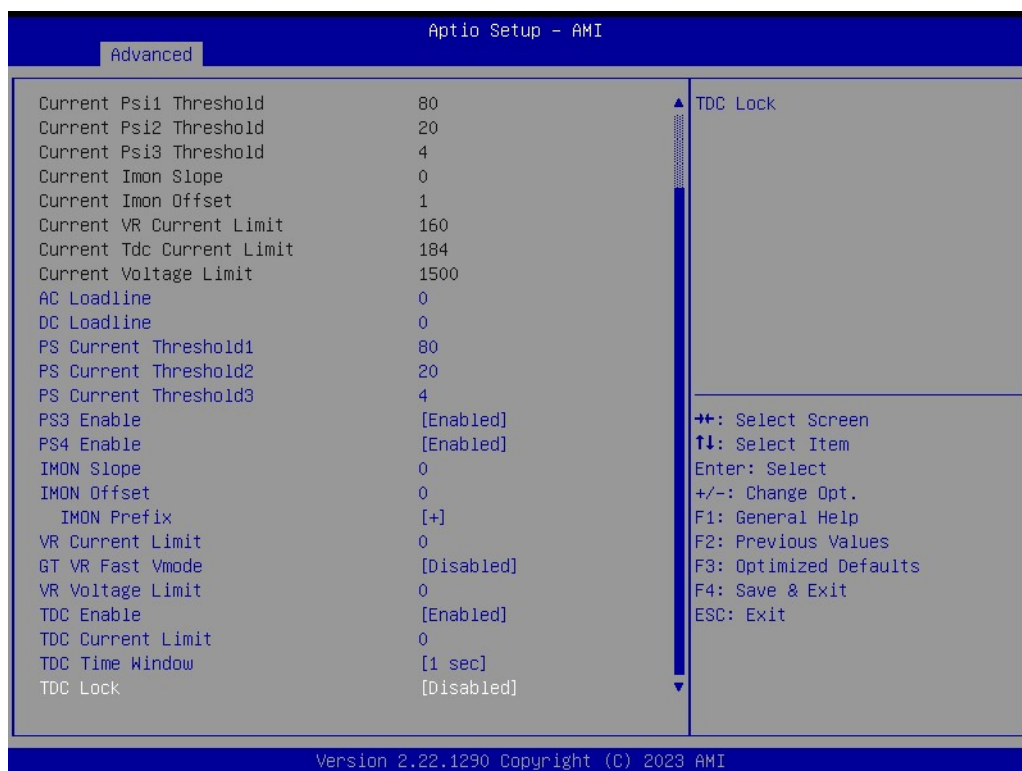
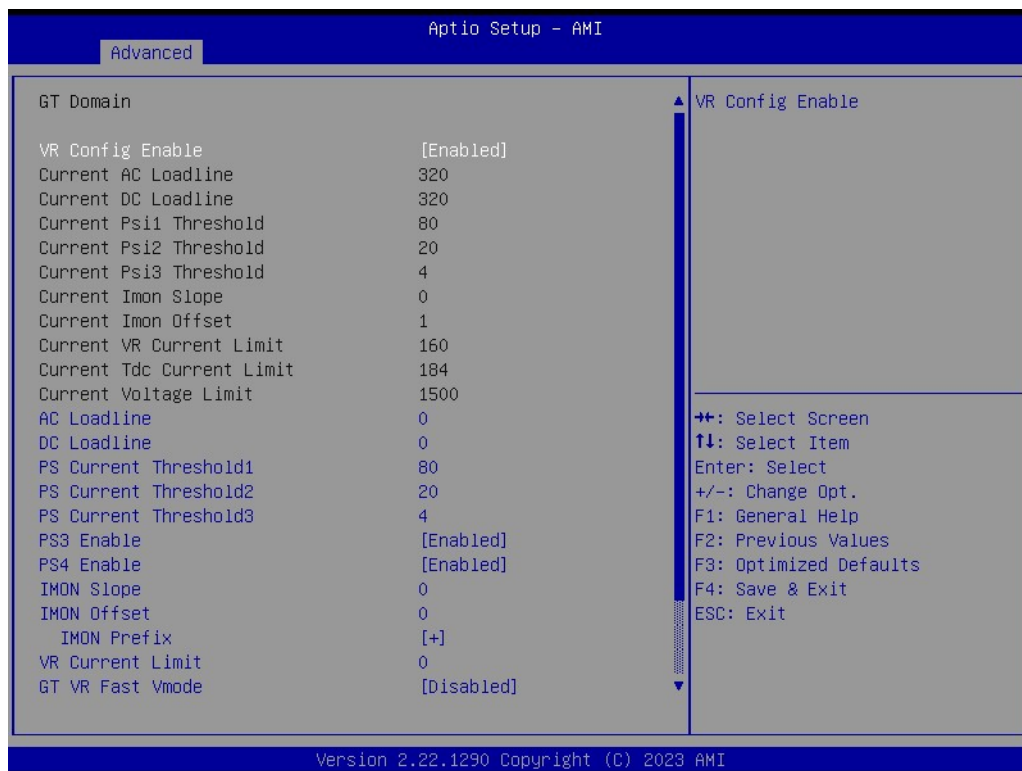
Advanced

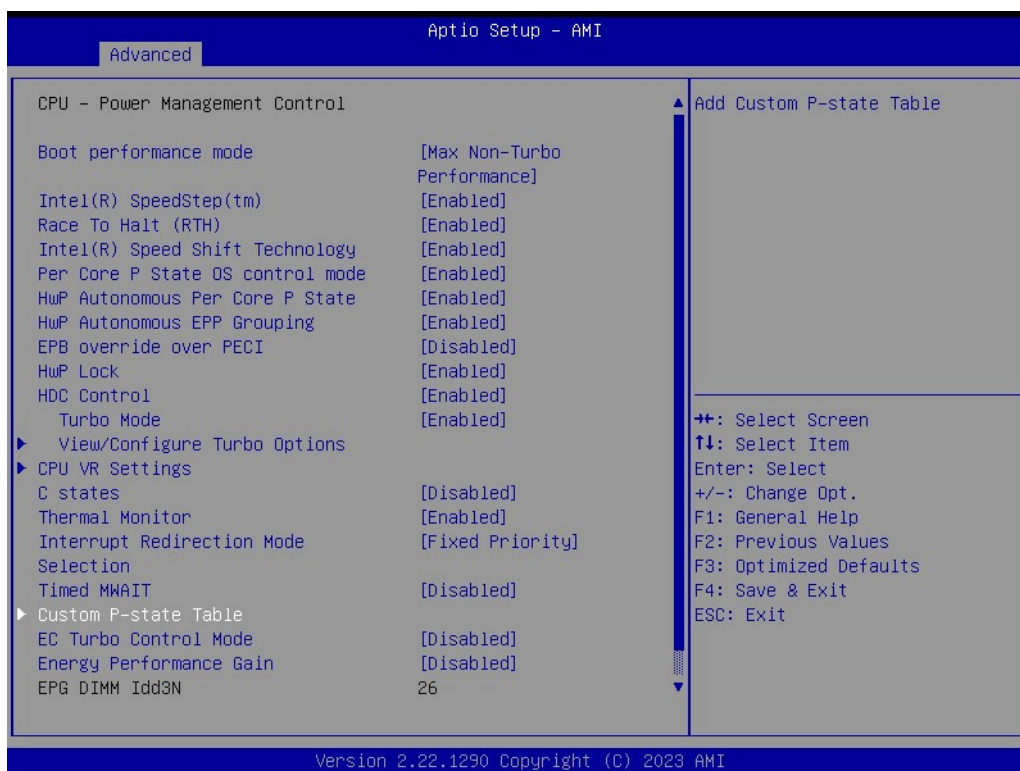
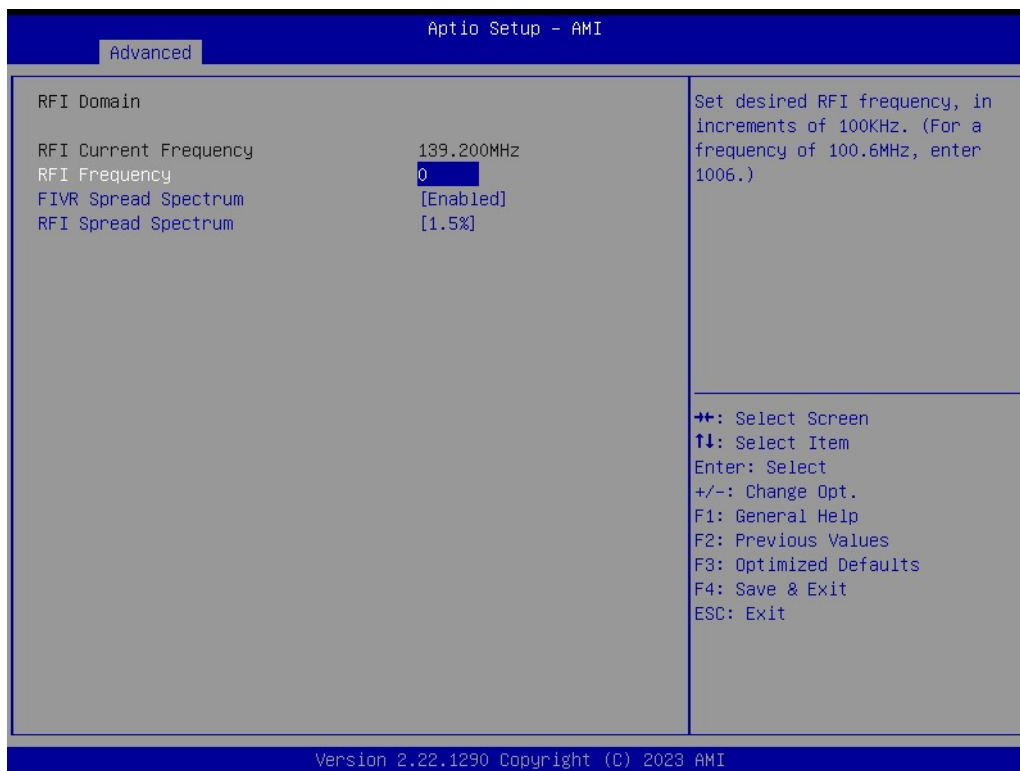
Acoustic Noise Settings		Enabling this option will help mitigate acoustic noise on certain SKUs when the CPU is in deeper C state
Acoustic Noise Mitigation	[Disabled]	
Pre Wake Time	0	<b>++</b> : Select Screen <b>↑↓</b> : Select Item Enter: Select +/-: Change Opt. F1: General Help F2: Previous Values F3: Optimized Defaults F4: Save & Exit ESC: Exit
Ramp Up Time	0	
Ramp Down Time	0	
IA VR Domain		
Disable Fast PKG C State Ramp for IA Domain	[FALSE]	
Slow Slew Rate for IA Domain	[Fast/2]	
GT VR Domain		
Disable Fast PKG C State Ramp for GT Domain	[FALSE]	
Slow Slew Rate for GT Domain	[Fast/2]	

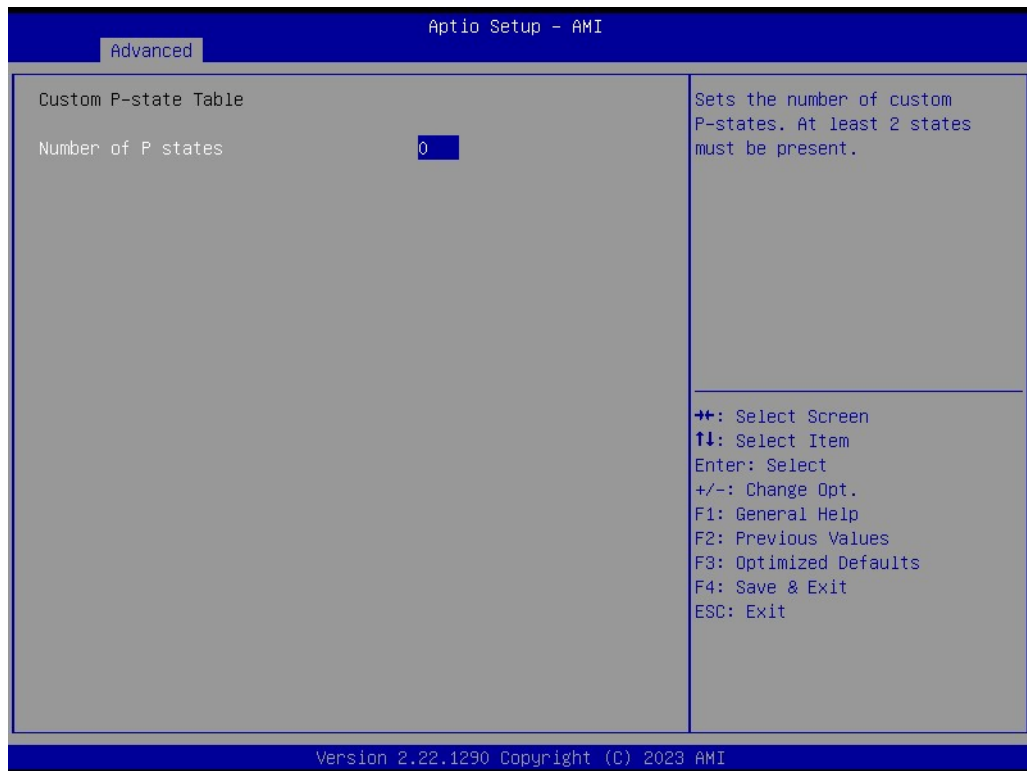
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- **Boot performance mode**  
Select the performance state that the BIOS will set before OS hand-off.
- **Intel® SpeedStep (tm)**  
Allows more than two frequency ranges to be supported.

- **Race To Halt (RTH)**  
Enable/Disable Race To Halt feature. RTH will dynamically increase CPU frequency in order to enter pkg C-State faster to reduce overall power. (RTH is controlled through MSR 1FC bit 20)
- **Intel® SpeedStep Shift Technology**  
Enable/Disable Intel® Speed Shift Technology support. Enabling will expose the CPPC v2 interface to allow for hardware controlled P-states.
- **Per Core P State OS Control mode**  
Enable/Disable Per Core P state OS control mode. Disabling will set Bit 31 = 1 command 0x06. When set, the highest core request is used for all other core requests.
- **HwP Autonomous Per Core P State**  
Disable Autonomous PCPS (Bit 30 = 1, command 0x11) Autonomous will request the same value for all cores all the time. Enable PCPS (default Bit 30 = 0, command 0x11)
- **HwP Autonomous EPP Grouping**  
Enable EPP grouping (default Bit 29 = 0, command 0x11) Autonomous will request the same values for all cores with same EPP. Disable EPP grouping (Bit 29 = 1, command 0x11) autonomous will not necessarily request same values for all cores with
- **EPB Override over PECI**  
Enable/Disable EPB override over PECI. Enable by sending pcode command 0x2b, subcommand 0x3 to 1. This will allow OOB EPB PECI override control
- **HwP Lock**  
Enable/Disable HWP Lock support in Misc Power Management MSR.
- **HDC Control**  
This option allows HDC configuration.
- **Turbo Mode**  
Enable/Disable processor Turbo Mode (requires Intel Speed Step or Intel Speed Shift to be available and enabled).
- **View/Configure Turbo Options**
  - Turbo Ratio Limit Options  
View/Configure Turbo Ratio Limit Options
  - Energy Efficient P-state  
Enable/Disable Energy Efficient P-state feature.
  - Package Power Limit MSR Lock  
Enable/Disable locking of Package Power Limit settings.
  - Energy Efficient Turbo  
Enable/Disable Energy Efficient Turbo Feature. This feature will opportunistically lower the turbo frequency to increase efficiency.
- **CPU VR Setting**
  - Current Vccln AUX Icc Max  
Current Vccln Aux Icc Max
  - PSYS Slope  
PSYS Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x9.
  - PSYS offset  
PSYS Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. PSYS Uses BIOS VR mailbox command 0x4.
  - PSYS Prefix  
Sets the offset value as positive or negative.

- PSYS Pmax Power  
PSYS PMax power, defined in 1/8 Watt increments. Range 0-8191. For a PMax of 125W, enter 1000. 0 = AUTO. Uses BIOS VR mailbox command 0xB.
- Min Voltage Override  
Min Voltage Override. Enable to override minimum voltage for runtime and for C8.
- Vccln Aux Icc Max  
Sets the Max Icc Vccln Aux value defined in 1/4A increments. Range is 0-512. For an IccMax 32A, enter 128(32\*4).
- Vccln Aux IMON Slope  
Vccln Aux IMON Slope defined in 1/100 increments. Range is 0-200. For a 1.25 slope, enter 125. 0 = AUTO. Uses BIOS VR mailbox command 0x18.
- Vccln Aux IMON Offset  
Vccln Aux IMON Offset defined in 1/1000 increments. Range is 0-63999. For an offset of 25.348, enter 25348. IMON Uses BIOS VR mailbox command 0x18.
- Vccln Aux IMON Prefix  
Sets the offset value as positive or negative.
- Vsys/Psys Critical  
Vsys Critical Enable/Disable.
- Assertion Deglitch Mantissa  
Assertion Deglitch Mantissa 0x4F[7-3]. Assertion Deglitch =  $2\mu\text{s} * \text{Mantissa} * 2^{(\text{Exponent})}$
- Assertion Deglitch Exponent  
Assertion Deglitch Exponent 0x4F[3-0]. Assertion Deglitch =  $2\mu\text{s} * \text{Mantissa} * 2^{(\text{Exponent})}$
- De assertion Deglitch Mantissa  
De Assertion Deglitch Mantissa 0x49[7-3]. Assertion Deglitch =  $2\mu\text{s} * \text{Mantissa} * 2^{(\text{Exponent})}$
- De assertion Deglitch Exponent  
De Assertion Deglitch Exponent 0x49[3-0]. Assertion Deglitch =  $2\mu\text{s} * \text{Mantissa} * 2^{(\text{Exponent})}$
- VR Power Delivery Design  
Specifies the ADL Desktop board design used for the VR settings override values. By default, BIOS will override the default Desktop VR settings based on the board design. A value of AUTO(0) will use the board ID to determine the board design. Any other value will override the board id logic to provide a custom VR Power Delivery Design value. This is intended primarily for validation.
- Acoustic Noise Settings
  - (i) Acoustic Noise Mitigation  
Enabling this option will help mitigate acoustic noise on certain SKUs when the CPU is in deeper C state
  - (ii) Pre Wake Time  
Set the maximum Pre Wake randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation Dynamic Periodicity Alteration (DPA) tuning.
  - (iii) Ramp Up Time  
Set the maximum Ramp Up randomization time in micro ticks. Range is 0-255. This is for acoustic noise mitigation Dynamic Periodicity Alteration (DPA) tuning
  - (iv) Ramp Down Time  
Set the maximum Ramp Down randomization time in micro ticks. Range is 0-



255. This is for acoustic noise mitigation Dynamic Periodicity Alteration (DPA) tuning.

(v) Disable Fast PKG C State Ramp for IA Domain

This option needs to be configured to reduce acoustic noise during deeper C states. False: Don't disable Fast ramp during deeper C states; True: Disable Fast ramp during deeper C state

(vi) Slow Slew Rate for IA Domain

Set VR IA Slow Slew Rate for Deep Package C State ramp time; Slow slew rate equals to Fast divided by number, the number is 2, 4, 8, 16 to slow down the slew rate to help minimize acoustic noise.

(vii) Disable Fast PKG C State Ramp for GT Domain

This option needs to be configured to reduce acoustic noise during deeper C states. False: Don't disable Fast ramp during deeper C states; True: Disable Fast ramp during deeper C state.

(viii) Slow Slew Rate for GT Domain

Set VR GT Slow Slew Rate for Deep Package C State ramp time; Slow slew rate equals to Fast divided by number, the number is 2, 4, 8 to slow down the slew rate to help minimize acoustic noise; divide by 16 is disabled

– Core/IA VR Settings

(i) VR Config Enable

(ii) Current AC loadline

(iii) Current DC loadline

(iv) Current Psi1 Threshold

(v) Current Psi2 Threshold

(vi) Current Psi3 Threshold

(vii) Current Imon Slope

(viii) Current Imon offset

(ix) Current VR Current Limit

Current VR Current Limit (Current IccMax Value)

(x) Current TDC Current Limit

(xi) Current Voltage Limit

(xii) AC Loadline

AC Loadline defined in 1/100 mOhms.

(xiii) DC Loadline

DC Loadline defined in 1/100 mOhms.

(xiv) PS Current Threshold1

PS Current Threshold1, defined in 1/4 A increments.

(xv) PS Current Threshold2

PS Current Threshold2, defined in 1/4 A increments.

(xvi) PS Current Threshold3

PS3 Enable/Disable. 0 - Disabled, 1 - Enabled. Uses BIOS VR mailbox command 0x3

(xvii) PS4 Enable

PS4 Enable/Disable. 0 - Disabled, 1 - Enabled. Uses BIOS VR mailbox command 0x3

(xviii) IMON Slope

IMON Slope defined in 1/100 increments.

(xix) IMON Offset

IMON Offset defined in 1/1000 increments.

(xx) IMON Prefix

Sets the offset value as positive or negative.

(xxi) VR Current Limit

Current VR Current Limit (Current IccMax Value)

(xxii) Core VR Fast Vmode

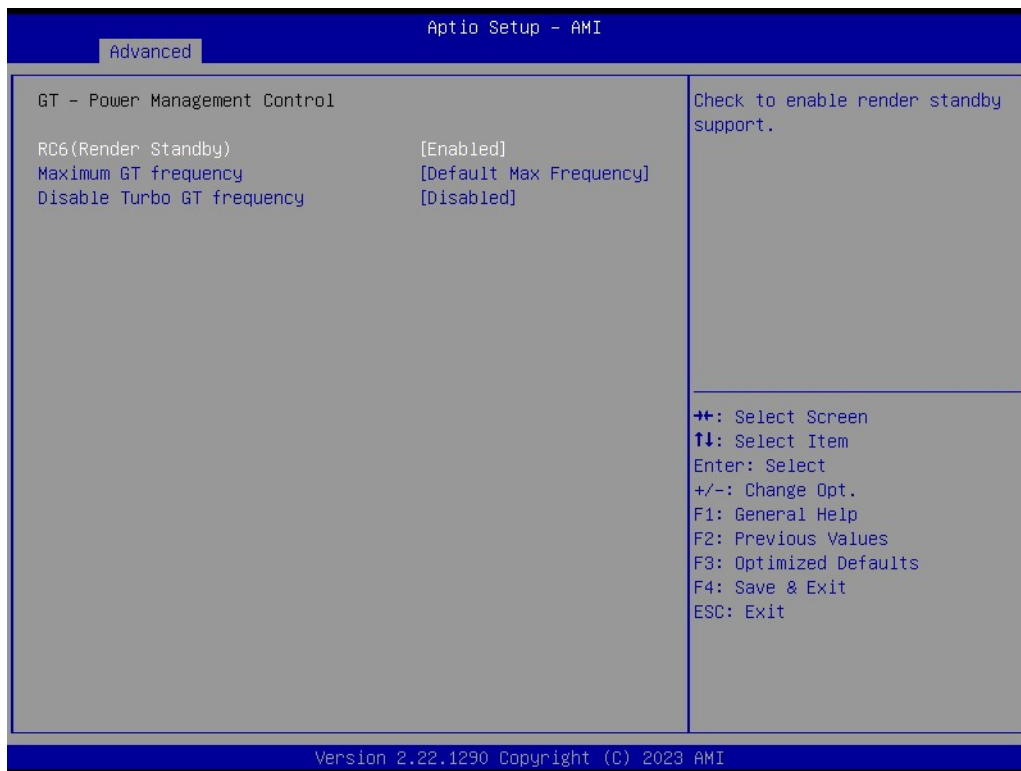
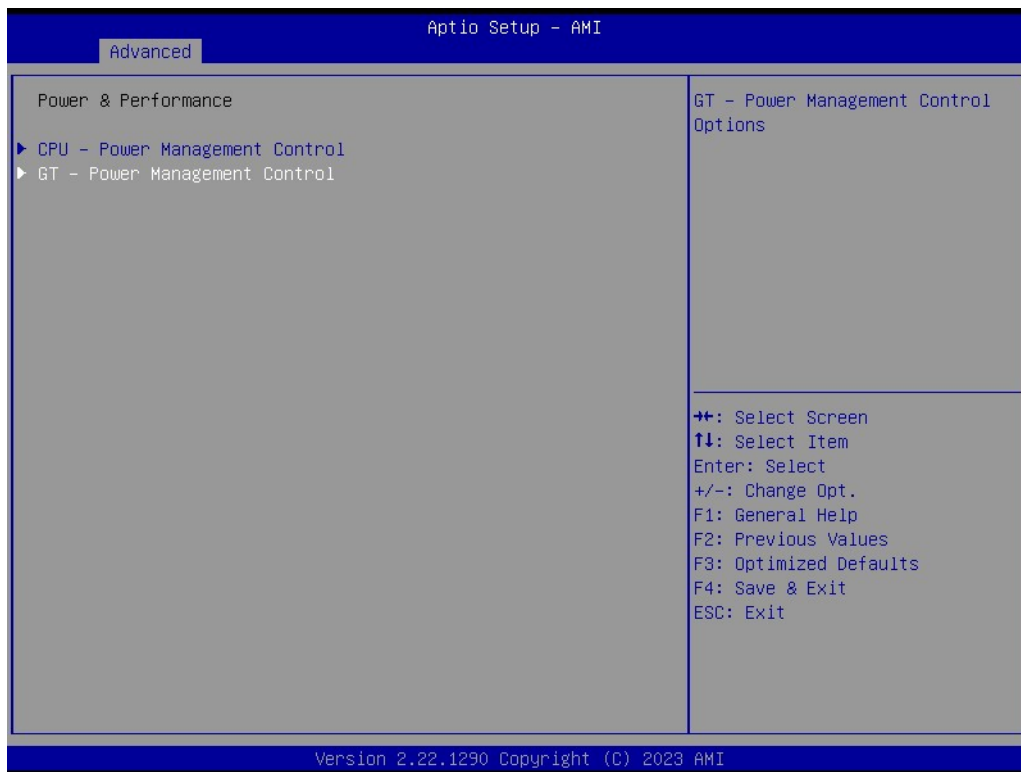
Core VR Fast Vmode. Use to control Core Fast Vmode Enable/Disable. The value will only be effective by enabling the corresponding CEP.

- (xxiii) Fast Vmode Itrip ICC Limit  
Voltage Regulator Fast Vmode Itrip ICC Limit.
- (xxiv) VR Voltage Limit  
Voltage Limit (VMAX). This value represents the Maximum instantaneous voltage allowed at any given time. Range is 0 - 7999mV. Uses BIOS VR mailbox command 0x8.
- (xxv) TDC Enable  
TDC Enable. 0- Disable, 1 - Enable
- (xxvi) TDC Current Limit  
TDC Current Limit, defined in 1/8A increments. Range 0-32767. For a TDC Current Limit of 125A, enter 1000. 0 = 0 Amps. Uses BIOS VR mailbox command 0x1A.
- (xxvii) TDC Time Window  
VR TDC Time Window, value in seconds. 1s is default. Range from 1s to 448s.
- (xxviii) TDC Lock
- (xxix) IRMS  
Enable/Disable IRMS - Current root mean square
- GT VR Settings
  - (i) VR Config Enable  
VR Config Enable
  - (ii) Current AC loadline
  - (iii) Current DC loadline
  - (iv) Current Psi1 Threshold
  - (v) Current Psi2 Threshold
  - (vi) Current Psi3 Threshold
  - (vii) Current Imon Slope
  - (viii) Current Imon offset
  - (ix) Current VR Current Limit  
Current VR Current Limit (Current IccMax Value)
  - (x) Current TDC Current Limit
  - (xi) Current Voltage Limit
  - (xii) AC Loadline  
AC Loadline defined in 1/100 mOhms.
  - (xiii) DC Loadline  
DC Loadline defined in 1/100 mOhms.
  - (xiv) PS Current Threshold1  
PS Current Threshold1, defined in 1/4 A increments.
  - (xv) PS Current Threshold2  
PS Current Threshold2, defined in 1/4 A increments.
  - (xvi) PS Current Threshold3  
PS Current Threshold3, defined in 1/4 A increments.
  - (xvii) PS4 Enable  
PS4 Enable/Disable. 0 - Disabled, 1 - Enabled. Uses BIOS VR mailbox command 0x3
  - (xviii) IMON Slope  
IMON Slope defined in 1/100 increments.
  - (xix) IMON Offset  
IMON Offset defined in 1/1000 increments.
  - (xx) IMON Prefix  
Sets the offset value as positive or negative.
  - (xxi) VR Current Limit  
Voltage Regulator Current Limit (IccMax).



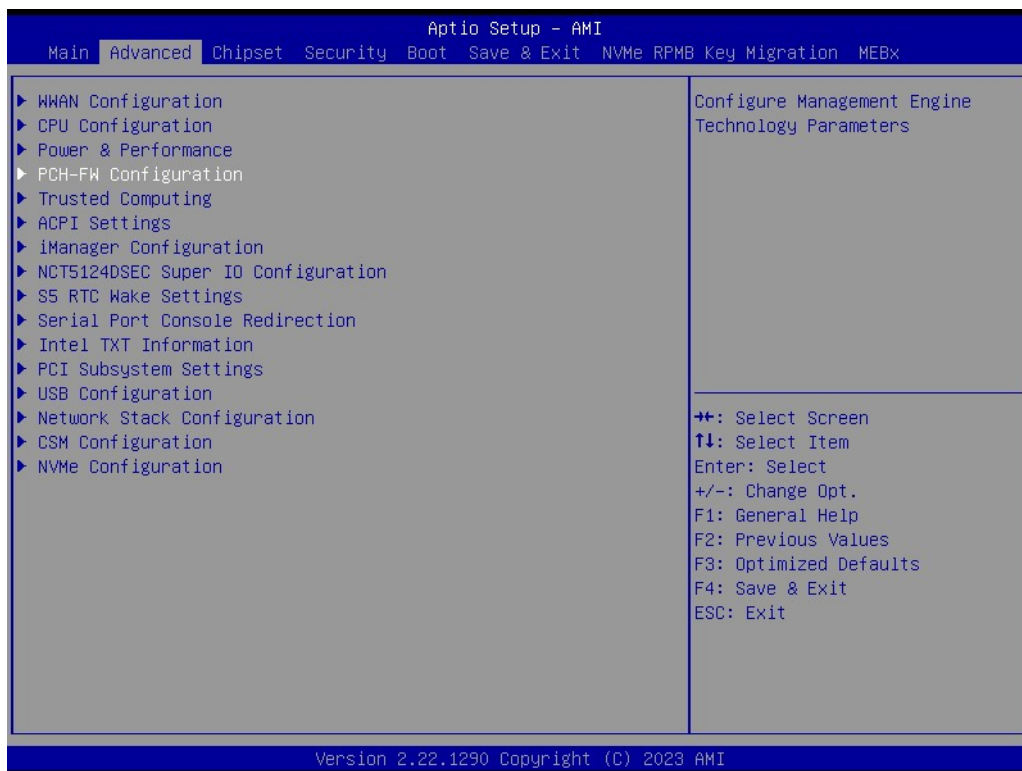
- (xxii) VR Voltage Limit  
Voltage Limit (VMAX). This value represents the Maximum instantaneous voltage allowed at any given time. Range is 0 - 7999mV. Uses BIOS VR mailbox command 0x8.
- (xxiii) TDC Enable  
TDC Enable. 0- Disable, 1 - Enable
- (xxiv) TDC Current Limit  
TDC Current Limit, defined in 1/8A increments. Range 0-32767. For a TDC Current Limit of 125A, enter 1000. 0 = 0 Amps. Uses BIOS VR mailbox command 0x1A.
- (xxv) TDC Time Window  
VR TDC Time Window, value in seconds. 1s is default. Range from 1s to 448s.
- (xxvi) TDC Lock
- RFI Settings
  - (i) RFI Current Frequency
  - (ii) RFI Frequency  
Set desired RFI frequency, in increments of 100KHz. (For a frequency of 100.6MHz, enter 1006.)
  - (iii) FIVR Spread Spectrum  
Enable/Disable the FIVR Spread Spectrum.
  - (iv) RFI Spread spectrum  
Set the Spread Spectrum.
- **C States**  
Enable/Disable CPU Power Management.
- **Thermal Monitor**  
Enable/Disable CPU Power Management.
- **Interrupt Redirection Mode**  
Enable/Disable Thermal Monitor
- **Timed MWAIT**  
Enable/Disable Timed MWAIT Support
- **Custom P-state Table**
  - Number of P states  
Sets the number of custom P-states. At least 2 states must be present.
- **EC Turbo Control Mode**  
Enable/Disable EC Turbo Control mode
- **Energy Performance Gain**  
Enable/disable Energy Performance Gain.
- **EPG DIM Idd3N**  
Active standby current (Idd3N) in milliamps from datasheet. Must be calculated on a per DIMM basis.
- **EPG DIM Idd3P**  
Active power-down current (Idd3P) in milliamps from datasheet. Must be calculated on a per DIMM basis.
- **CPU Lock Configuration**
  - CFG Lock  
Configure MSR 0xE2[15], CFG Lock bit.
  - Overclocking Lock  
Enable/Disable Overclocking Lock (BIT 20) in FLEX\_RATIO(194) MSR.

## GT - Power Management Control



- **RC6 (Render Standby)**  
Check to enable render standby support.
- **Maximum GT frequency**  
Maximum GT frequency limited by the user
- **Disable Turbo GT frequency**  
Enabled: Disables Turbo GT frequency. Disabled: GT frequency is not limited.

### 3.2.2.4 PCH-FW Configuration



#### ME State

When Disabled ME will be put into ME Temporarily Disabled Mode.

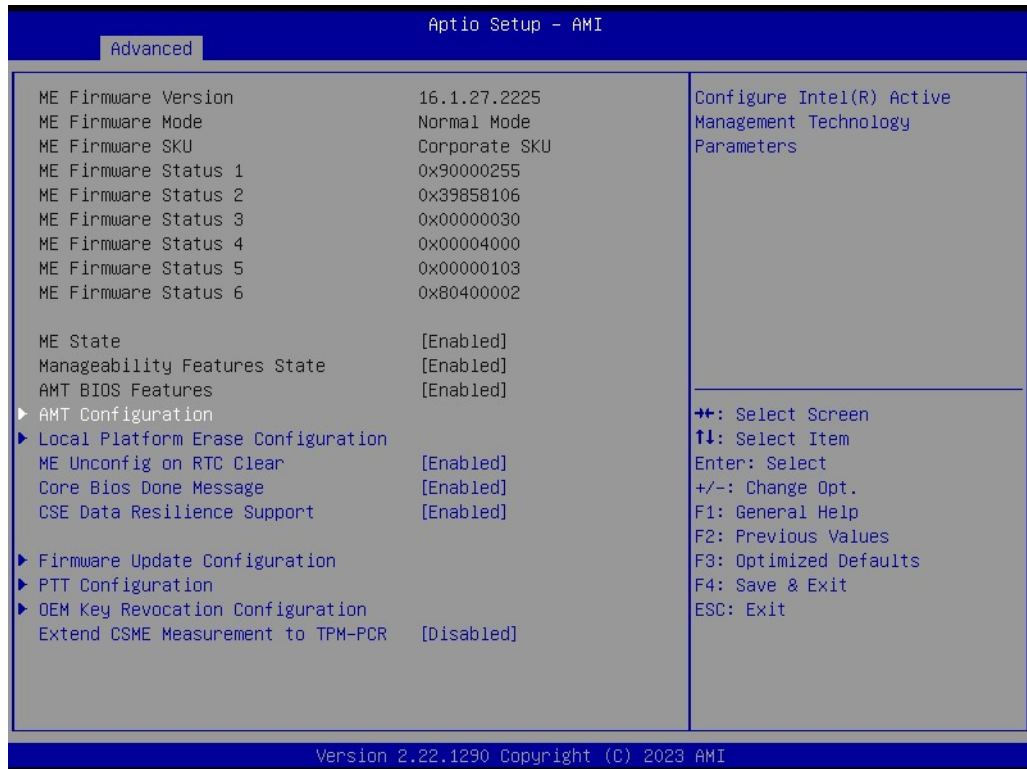
#### Manageability Features State

Enable/Disable Intel Manageability features.

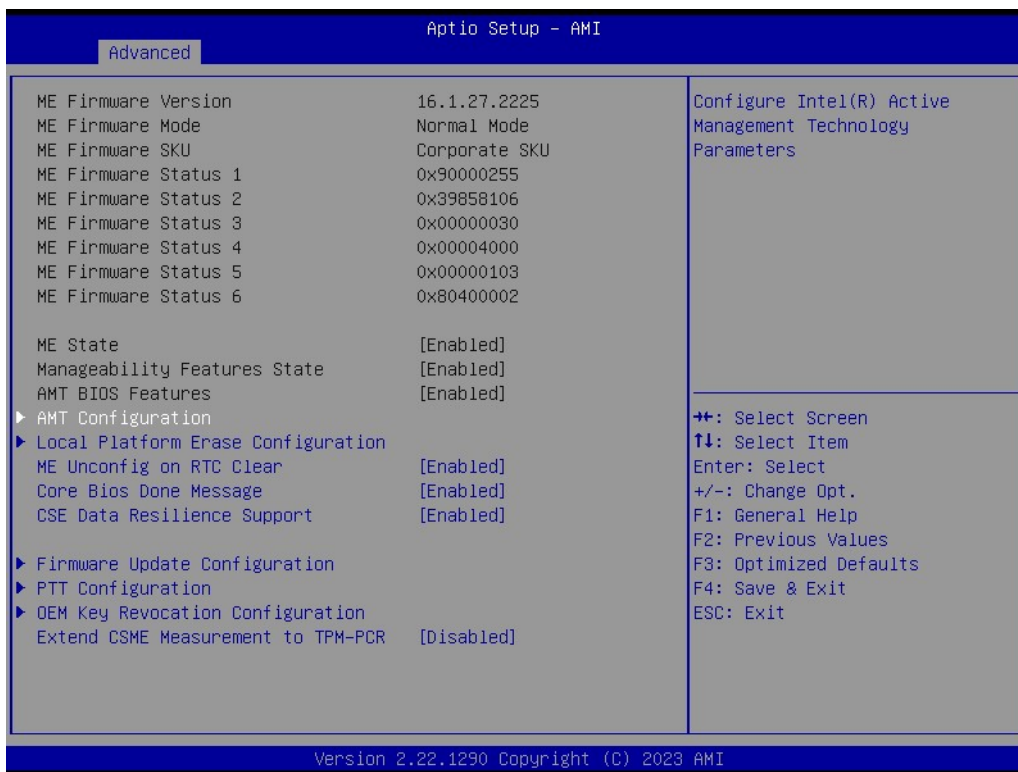
#### AMT BIOS Features

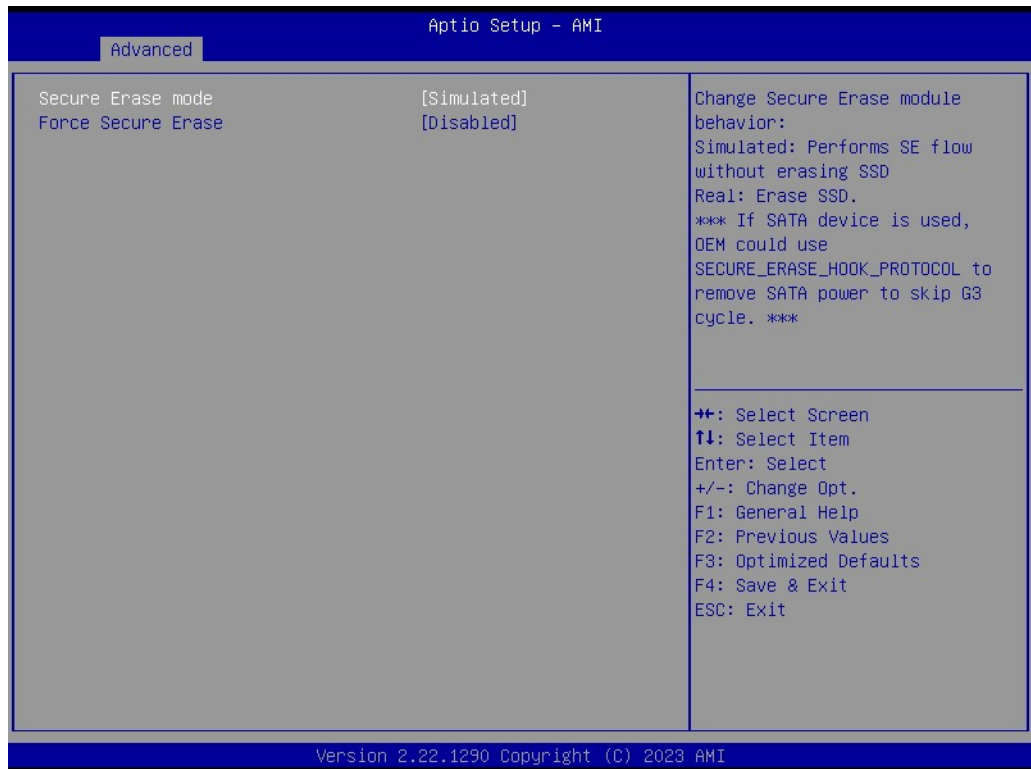
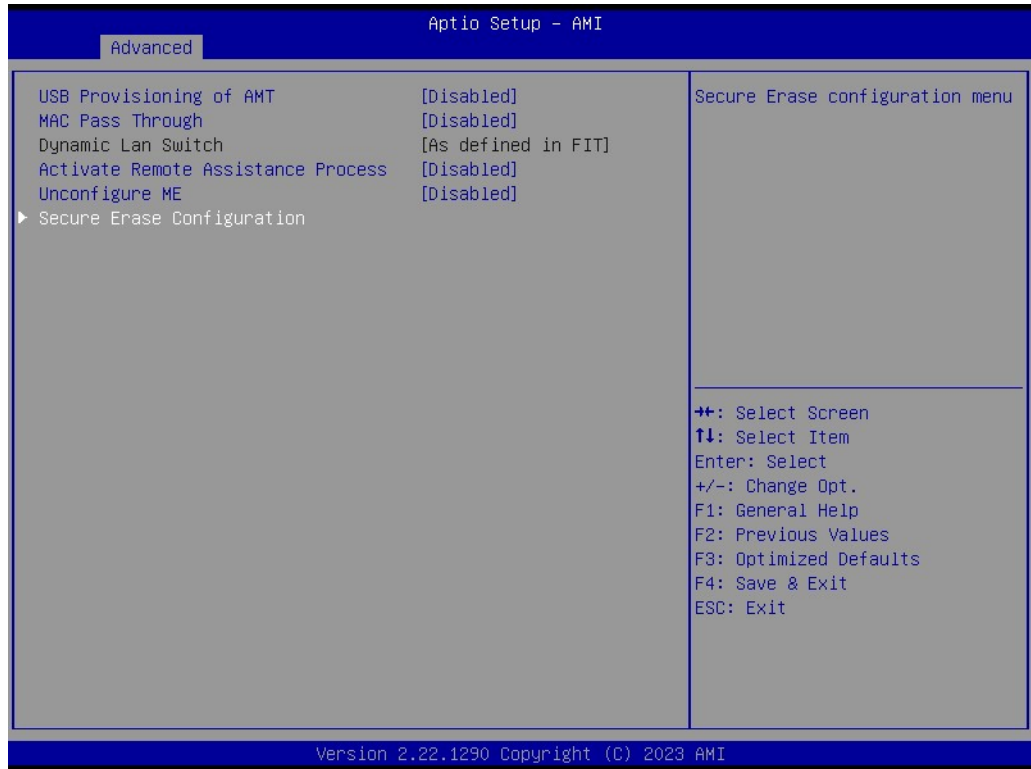
When disabled AMT BIOS Features are no longer supported and user is no longer able to access MEBx Setup.

## AMT Configuration



- **USB Provisioning of AMT**  
Enable/Disable of AMT USB Provisioning.
- **MAC Pass Through**  
Enable/Disable MAC Pass Through function.
- **Dynamic LAN Switch**  
Allow switching AMT support from Integrated LAN to Discrete LAN.
- **Activate Remote Assistance Process**  
Trigger CIRA boot\n\nNote:\nNetwork Access must be activated first from MEBx Setup.
- **Unconfigure ME**  
OEMFlag Bit 15. Unconfigure ME with resetting MEBx password to default.
- **Secure Erase Configuration**
  - Secure Erase mode  
Change Secure Erase module behavior. Simulated: Performs SE flow without erasing SSD\nReal: Erase SSD. If SATA device is used, OEM could use SECURE\_ERASE\_HOOK\_PROTOCOL to remove SATA power to skip G3 cycle.
  - Force Secure Erase  
Force Secure Erase on next boot





## Local Platform Erase Configuration



- **Perform Platform Erase Operations**  
Enabling this Feature will trigger Platform Erase Operations on the Next Boot

### ME Unconfig on RTC Clear

When Disabled ME will not be unconfigured on RTC Clear.

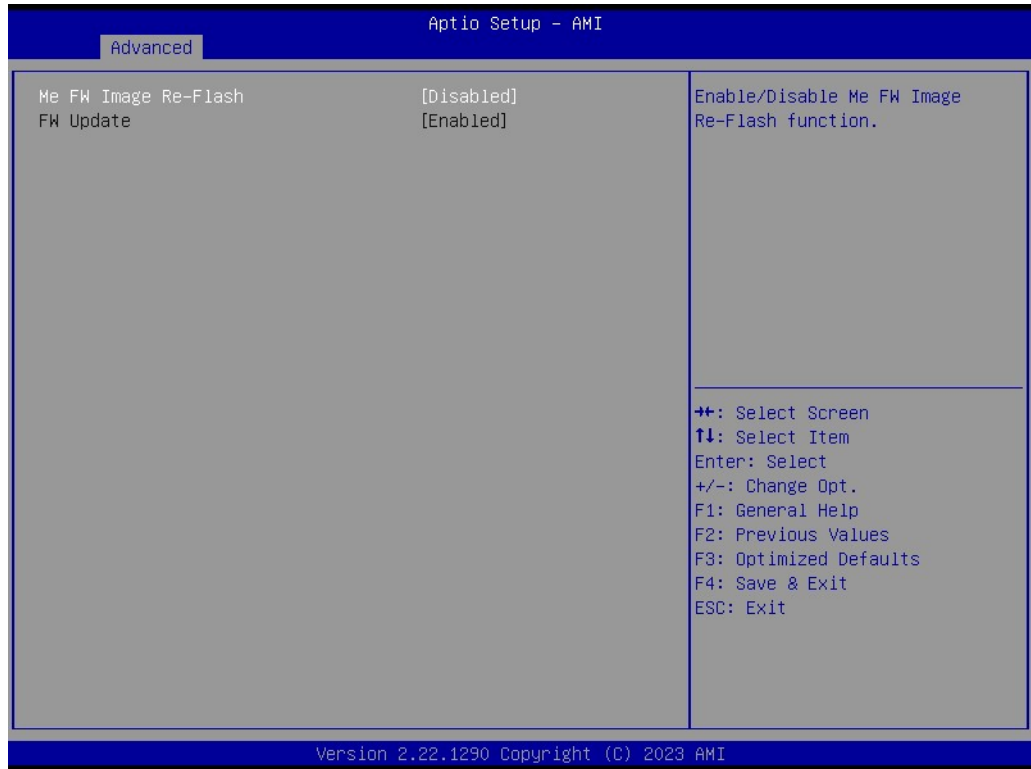
### Core Bios Done Message

Enable/Disable Core Bios Done message sent to ME

### CSE Data Resilience Support

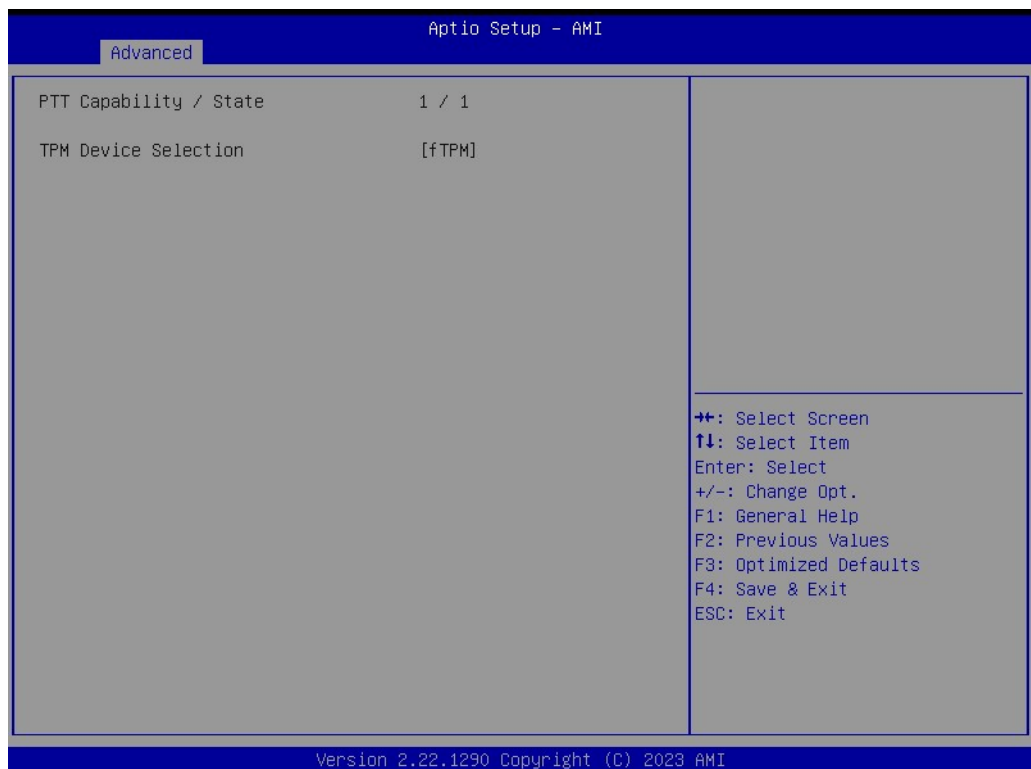
Enable/Disable CSE Data Resilience Support

## Firmware Update Configuration



- **ME FW Image Re-Flash**  
Enable/Disable Me FW Image Re-Flash function.
- **FW Update**  
Enable/Disable ME FW Update function.

## PTT Configuration



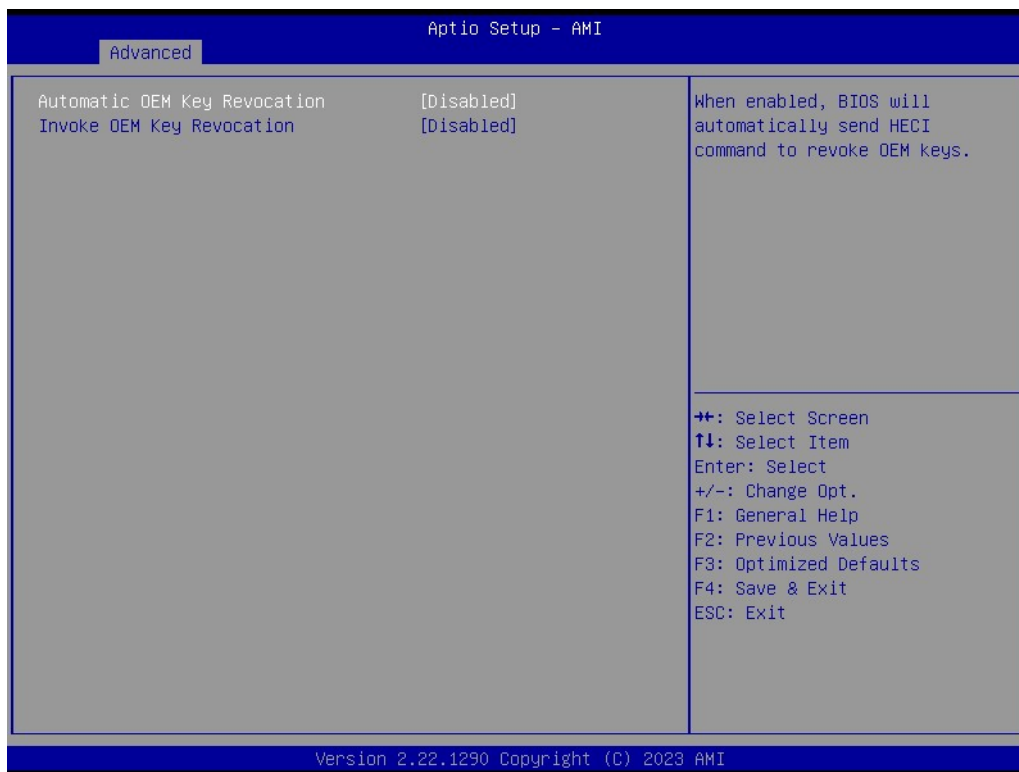


- **PTT Capability**
- **TPM Device Selection**  
Configure TPM device

### OEM Key Revocation configuration

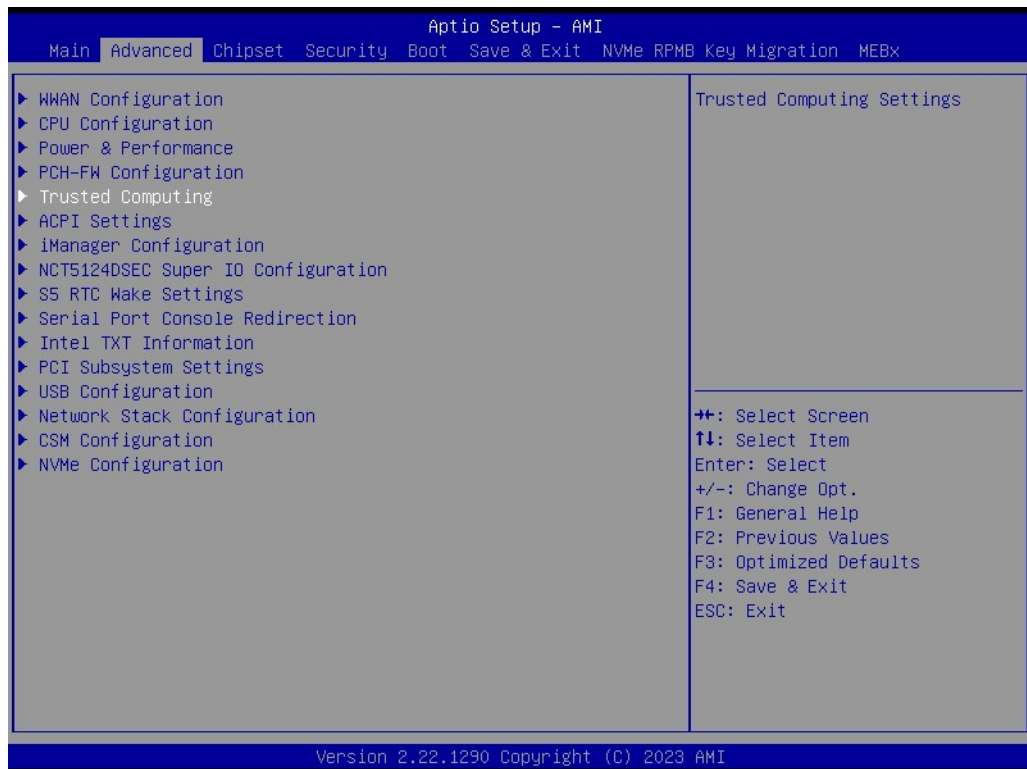
#### Extend CSME Measurement to TPM-PCR

Enable/Disable Extend CSME Measurement to TPM-PCR[0] and AMT Config to TPM-PCR[1]

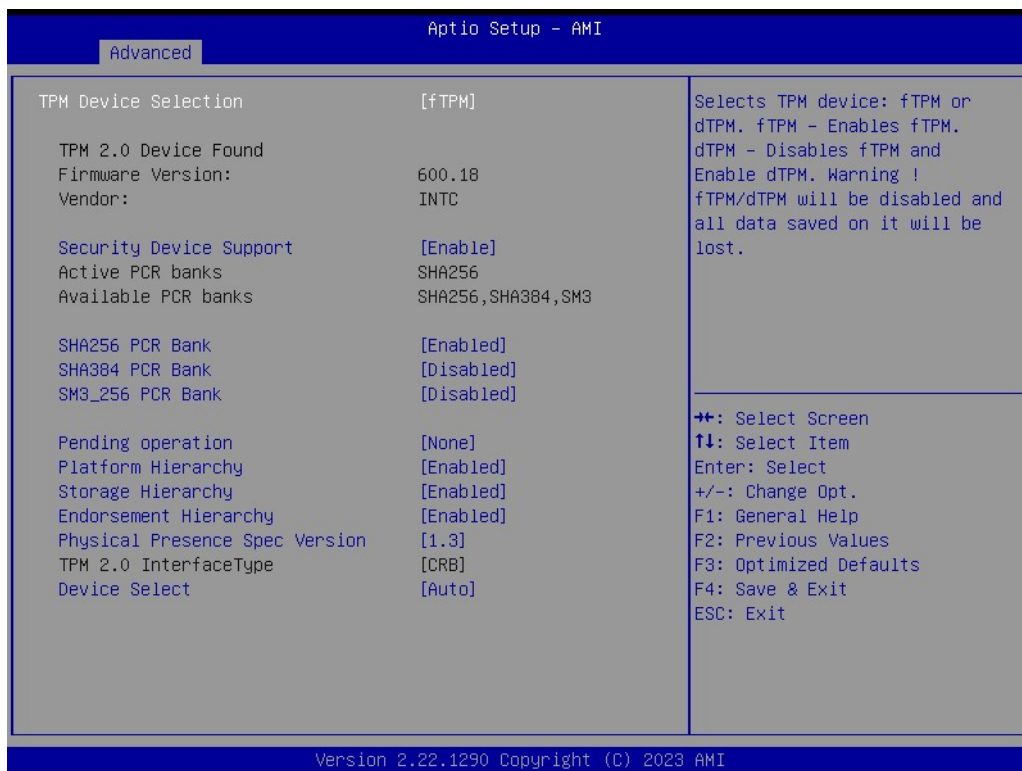


- **Automatic OEM Key Revocation**  
When enabled, BIOS will automatically send HECI command to revoke OEM keys.
- **Invoke OEM Key Revocation**  
A HECI command will be sent to revoke OEM key

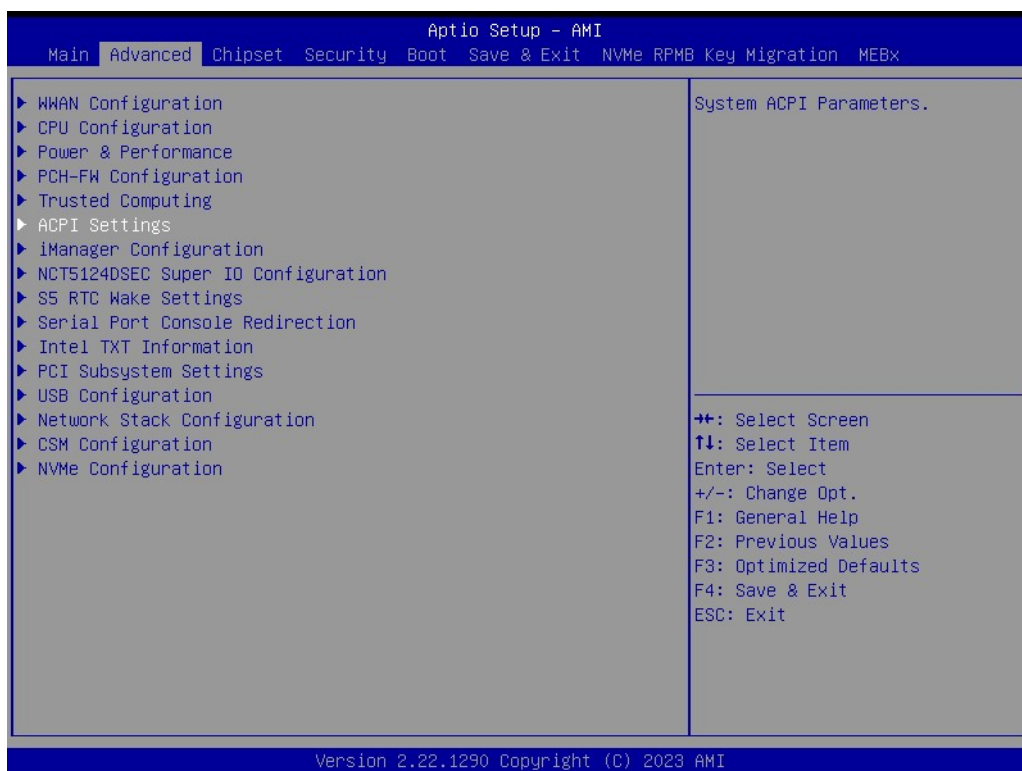
### 3.2.2.5 Trusted Computing



- **Security Device Support**  
Enable/Disable BIOS support for security device
- **Active PCR banks**
- **Available PCR banks**
- **SHA256 PCR Bank**  
Enable/Disable SHA256 PCR Bank
- **SHA384 PCR Bank**  
Enable/Disable SHA384 PCR Bank
- **SM3\_256 PCR Bank**  
Enable/Disable SM3\_256 PCR Bank
- **Pending Operation**  
Schedule an Operation for the security device
- **Platform Hierarchy**  
Enable/Disable Platform Hierarchy
- **Storage Hierarchy**  
Enable/Disable Storage Hierarchy
- **Endorsement Hierarchy**  
Enable/Disable Endorsement Hierarchy
- **Physical Presence Spec Version**  
Tells OS to support PPI Spec Version 1.2 or 1.3. Note some HCK tests might not support 1.3.
- **TPM 2.0 Interface Type**
- **Device Select**



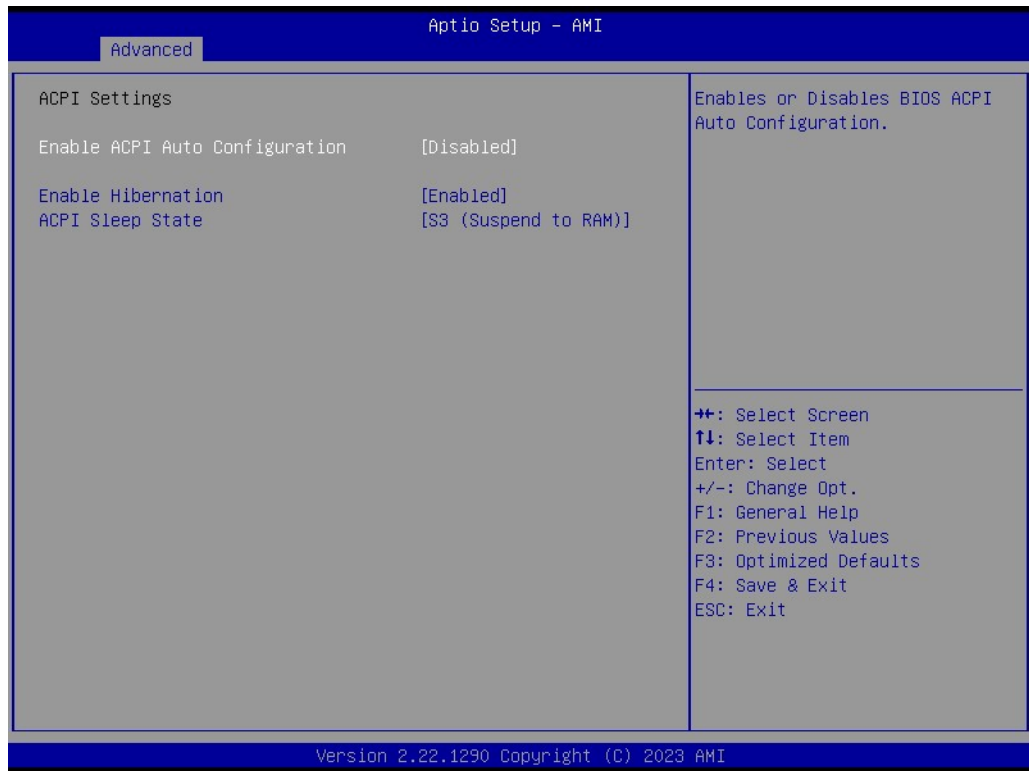
### 3.2.2.6 ACPI Settings



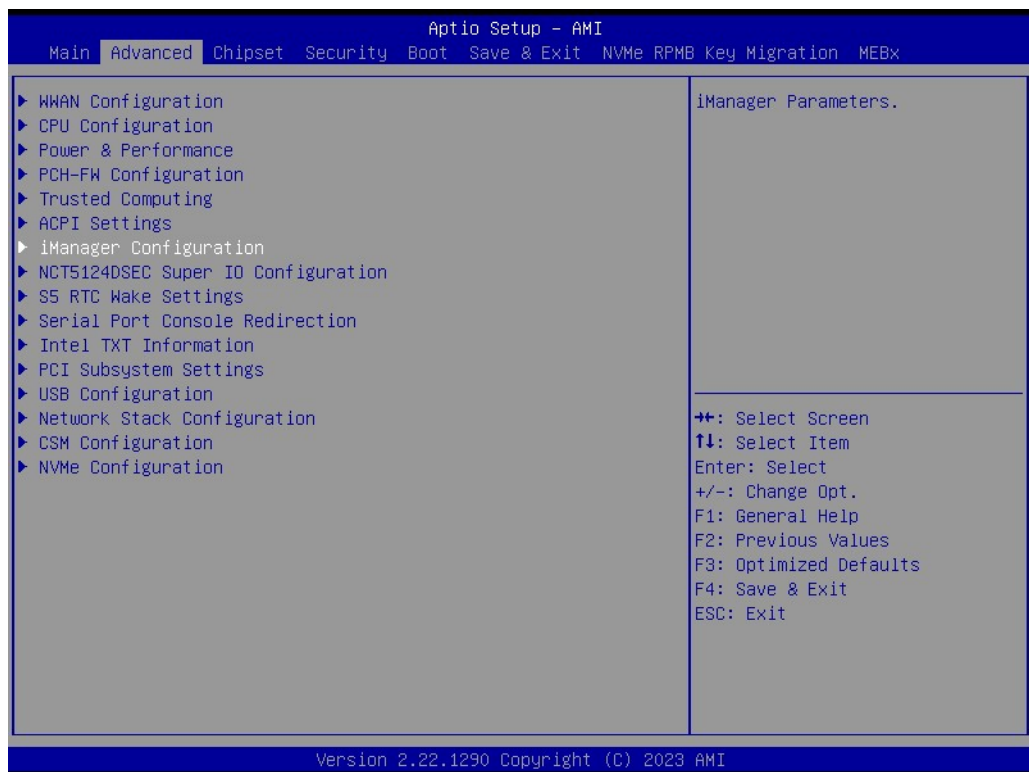
- **Enable ACPI Auto Configuration**  
Enables/Disables BIOS ACPI Auto Configuration.
- **Enable Hibernation**  
Enable/Disable System's ability to Hibernation (OS/S4 Sleep State)

■ **ACPI Sleep State**

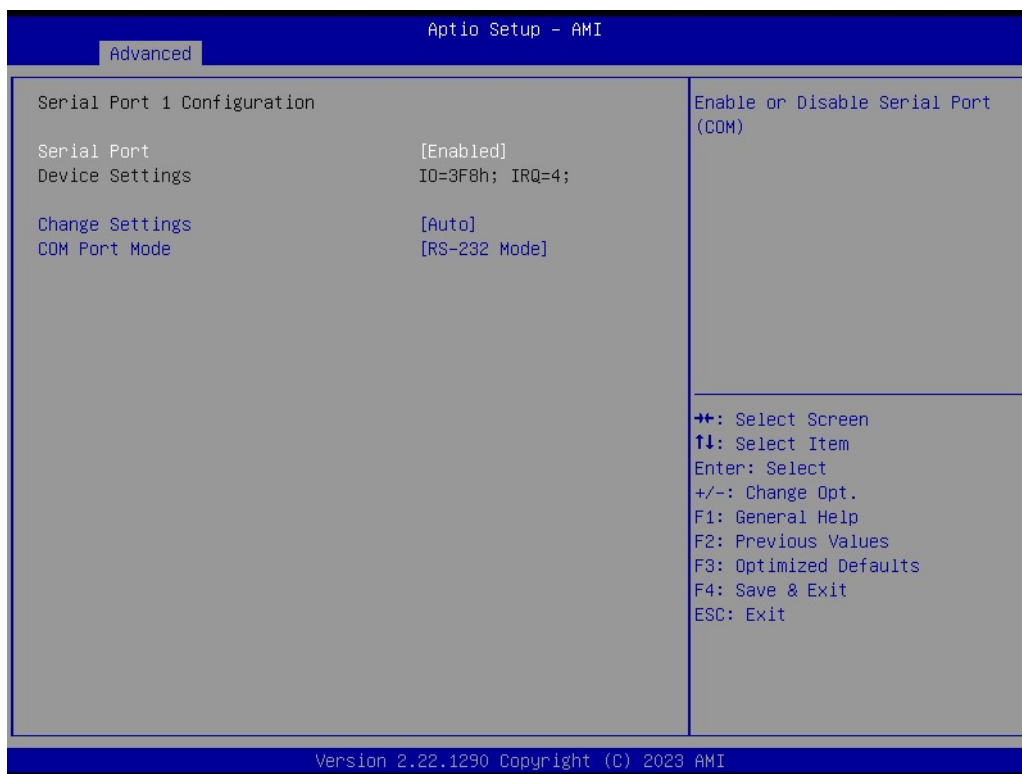
Select the highest ACPI sleep state the system will enter when the SUSPEND button is pressed.



**3.2.2.7 iManager Configuration**

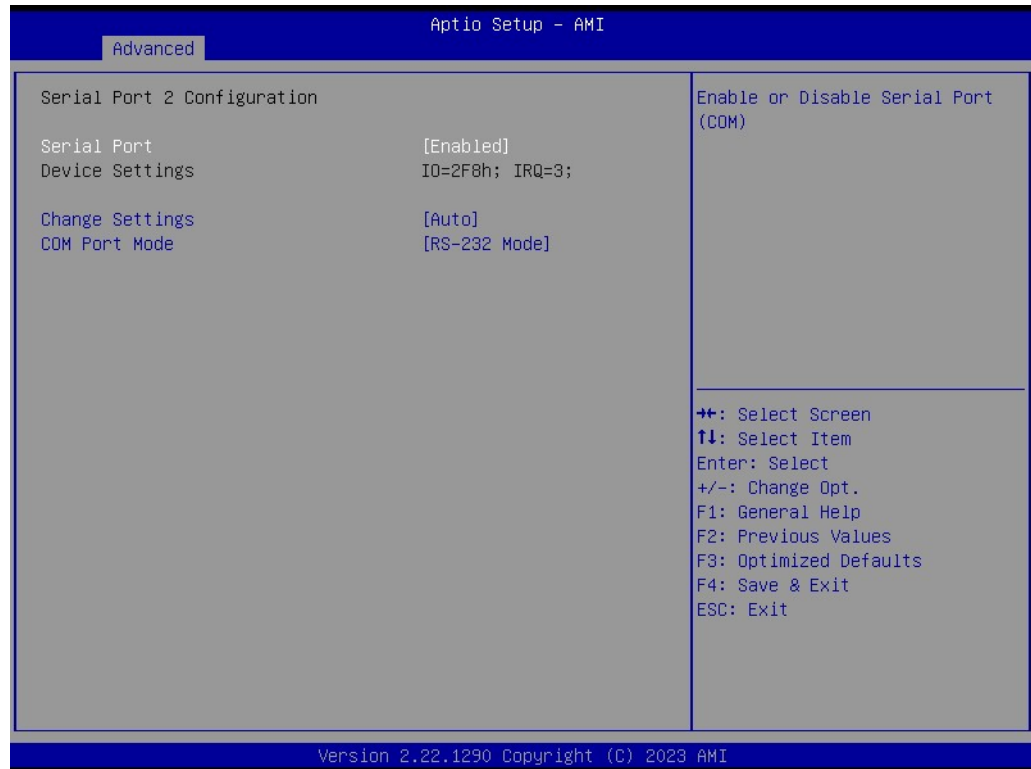


## Serial Port 1 Configuration



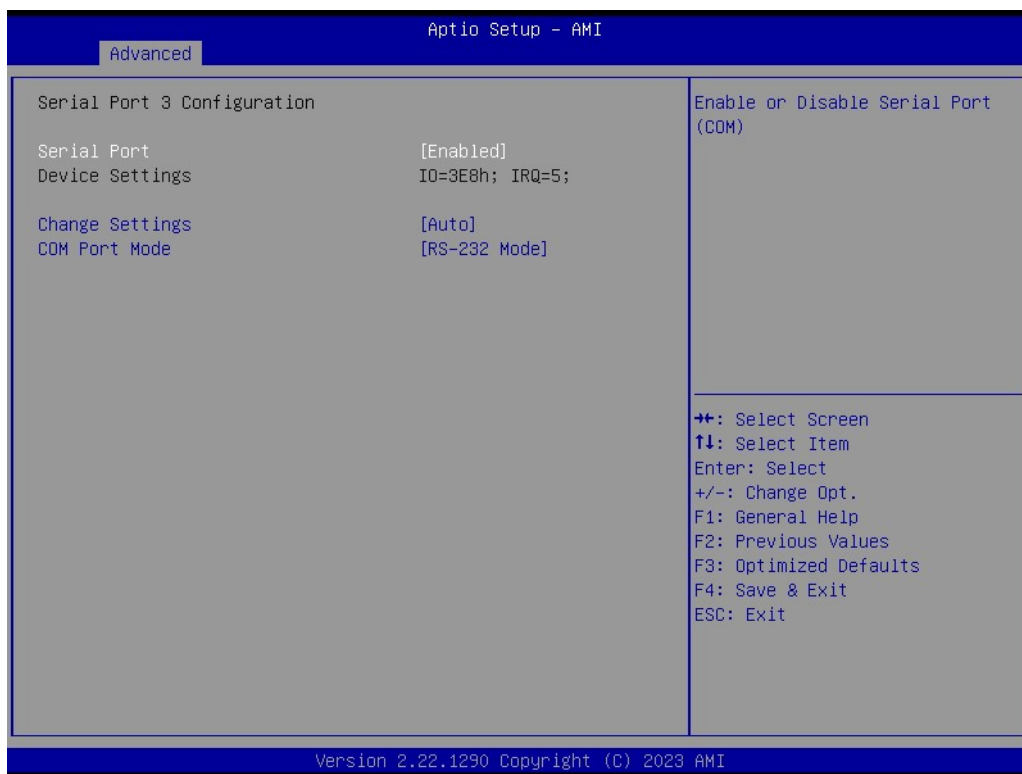
- **Serial Port**
- **Device Settings**
- **Change Settings**
- **COM Port Mode**

## Serial Port 2 Configuration



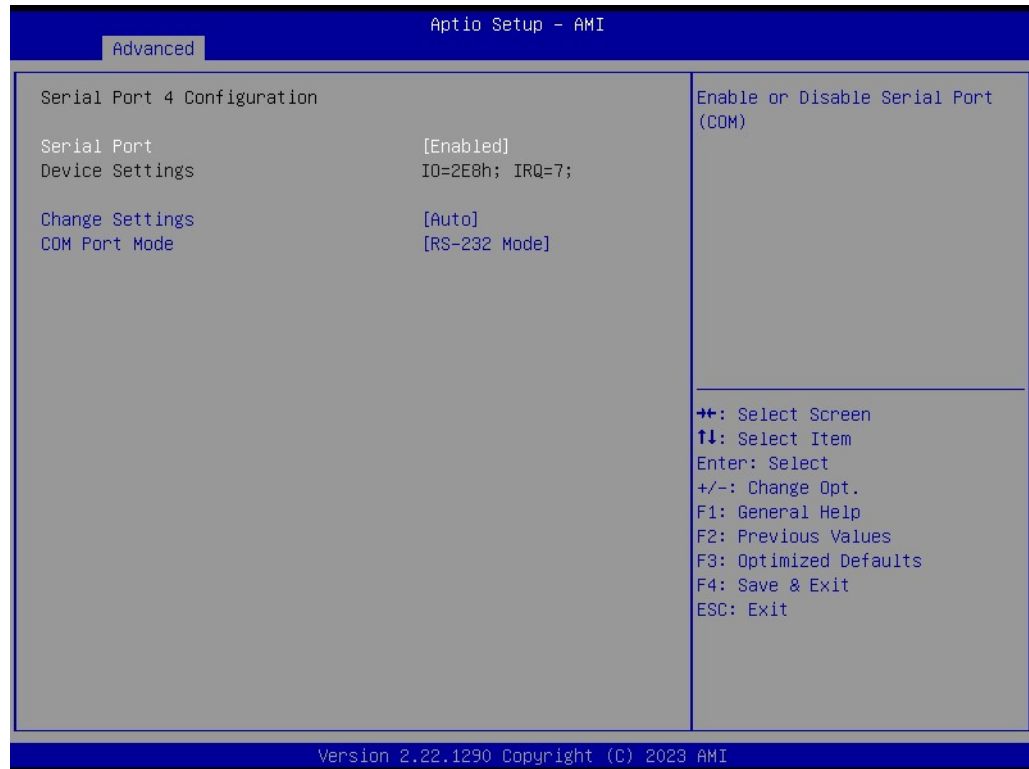
- **Serial Port**
- **Device Settings**
- **Change Settings**
- **COM Port Mode**

## Serial Port 3 Configuration



- **Serial Port**
- **Device Settings**
- **Change Settings**
- **COM Port Mode**

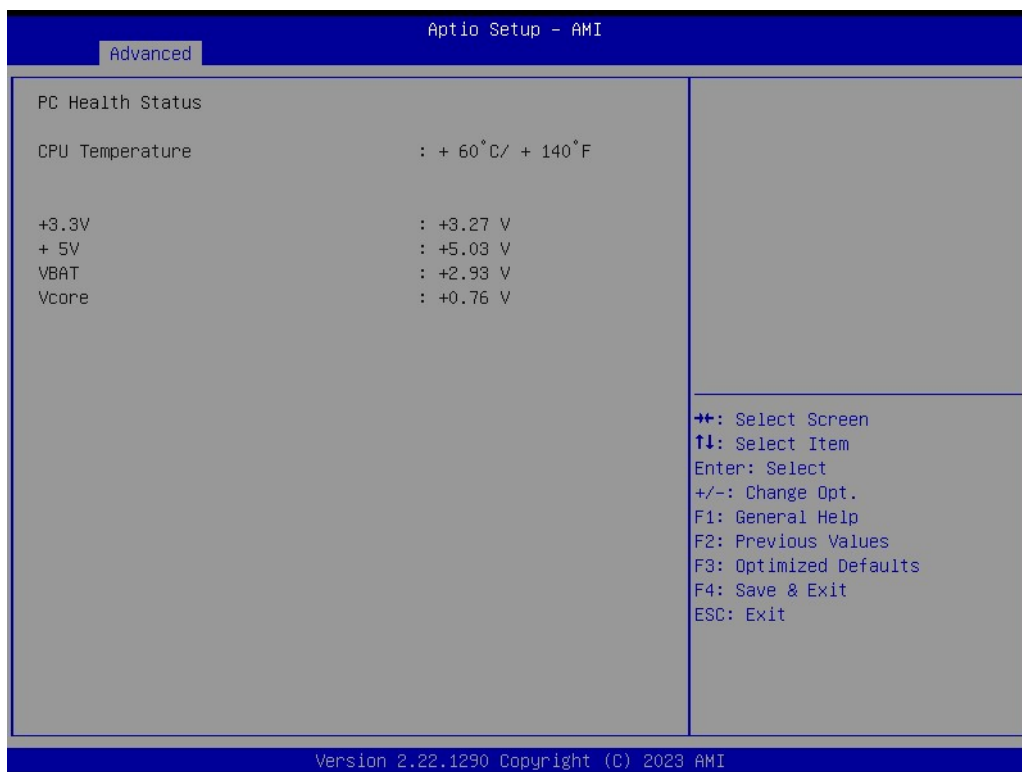
## Serial Port 4 Configuration



- **Serial Port**
- **Device Settings**
- **Change Settings**
- **COM Port Mode**



## Hardware Monitor



- **CPU Temperature**
- **+3.3V**
- **+5V**
- **VBAT**
- **Vcore**

## Watch Dog Timer Configuration



- **Watch Dog Timer Hidden**  
Enabled or Disabled Watch Dog Timer Hidden
- **Watch Dog Timer**  
Enabled or Disabled Watch Dog Timer function (Start before boot to OS and must stop by self)

## GPIO Configuration



- **GPIO Control Enable**  
Choose to control GPIO by EC or user override during POST stage.

## ACPI Report Method Configuration

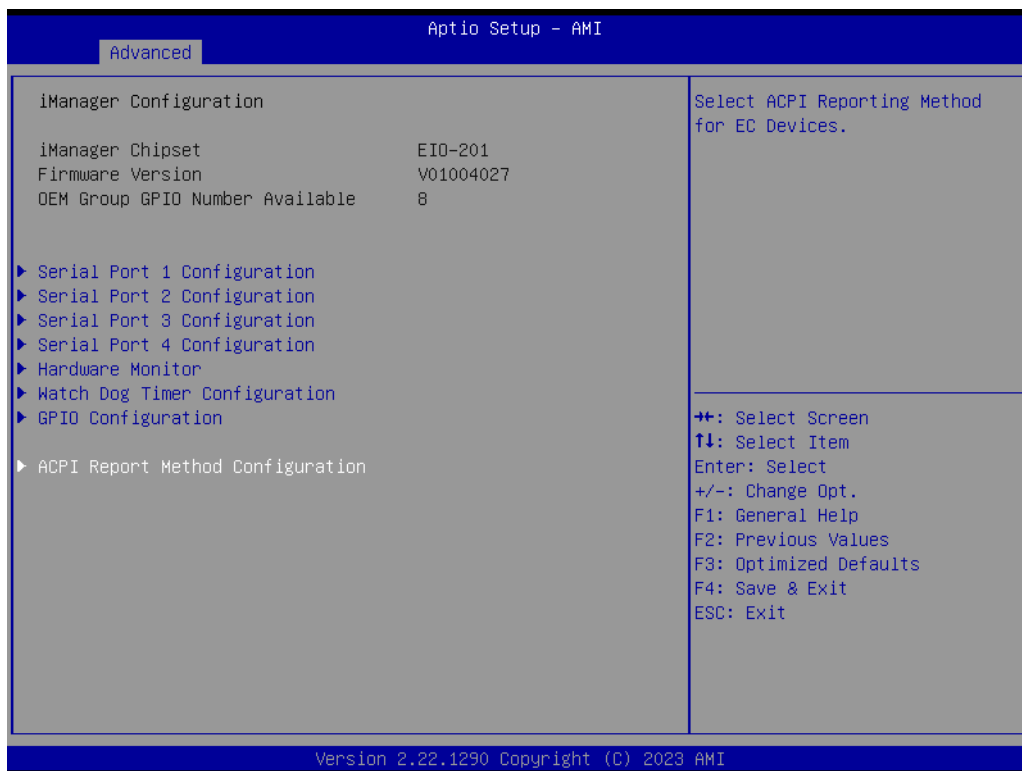


- **ACPI Report Method Control**  
Select ACPI Reporting Method for EC Devices.
- **Active High-Speed COM Port**  
Standard -> Standard COM Port. High Speed -> High Speed COM Port. (Driver installation is necessary.)

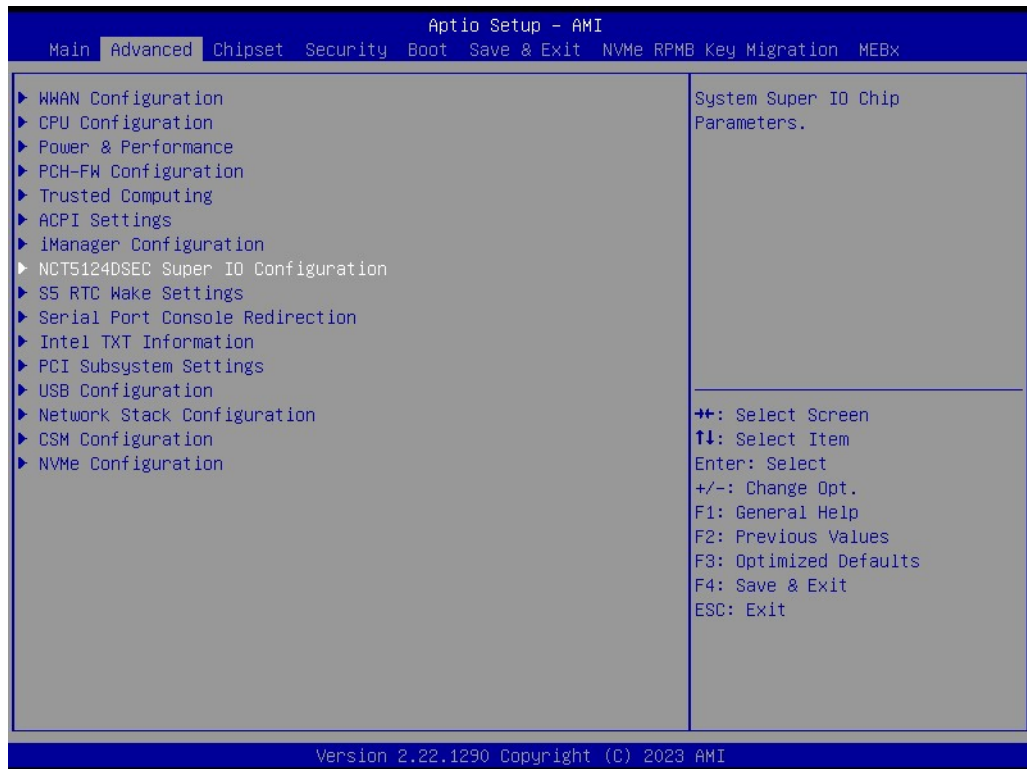
### iManager I2C0 Control

Enable/Disable SMBus0 controller on RDC

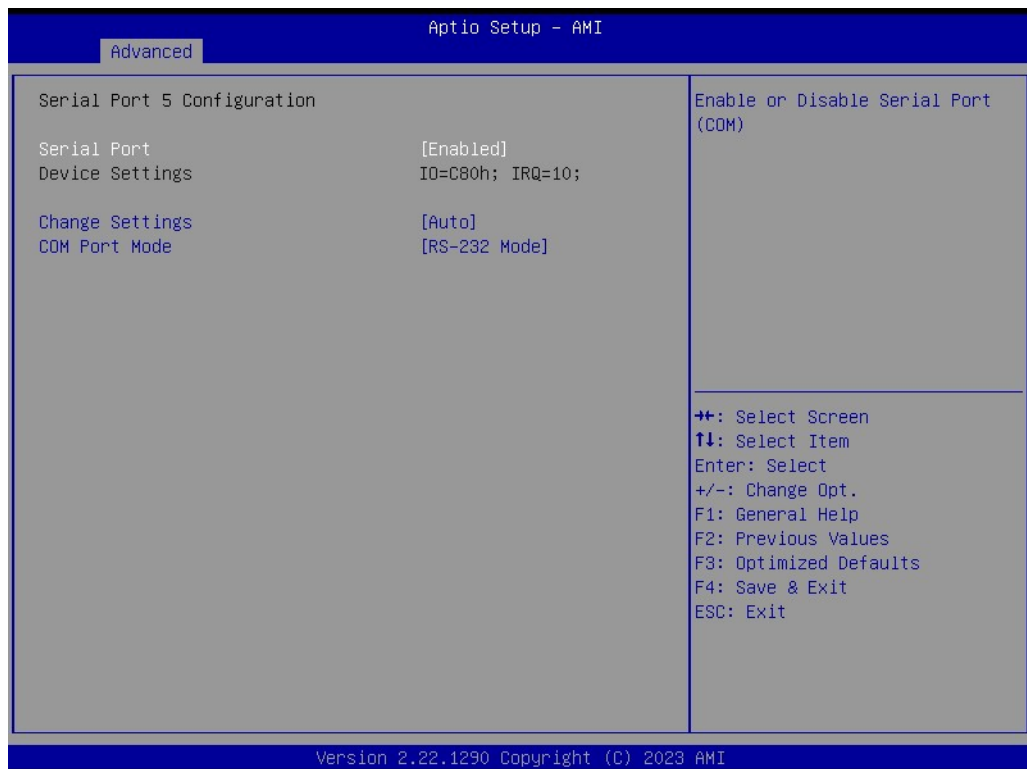
## iManager SMBus Control



### 3.2.2.8 NCT5124DSEC Super IO Configuration

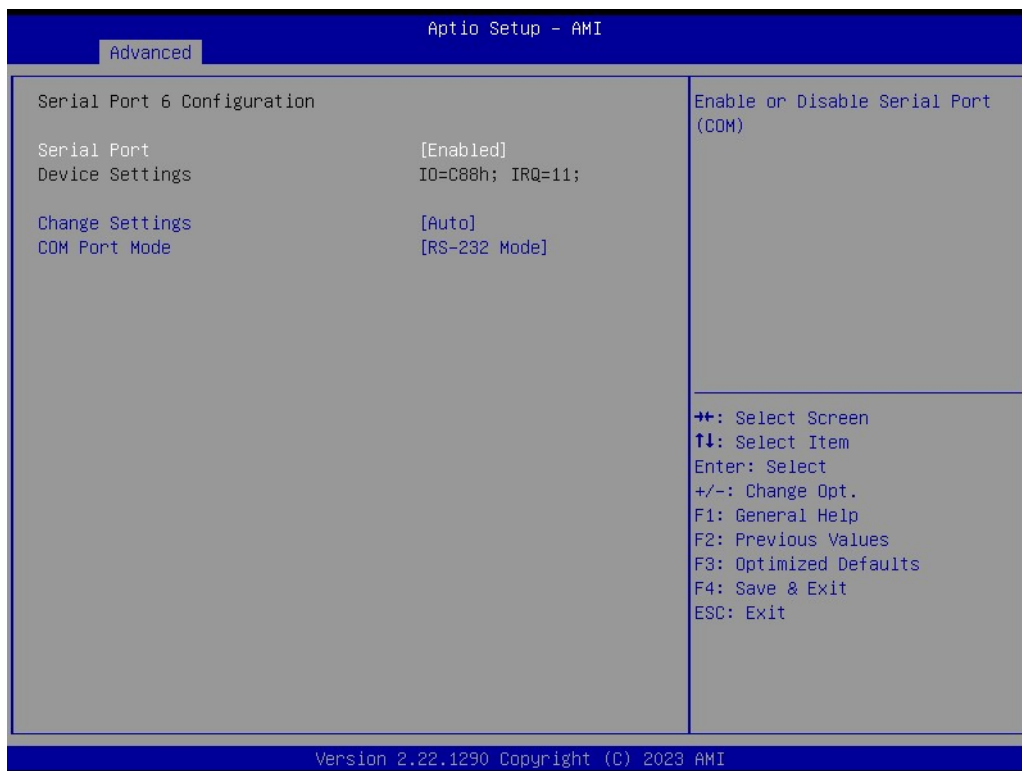


#### Super IO Chip Serial Port 5 Configuration



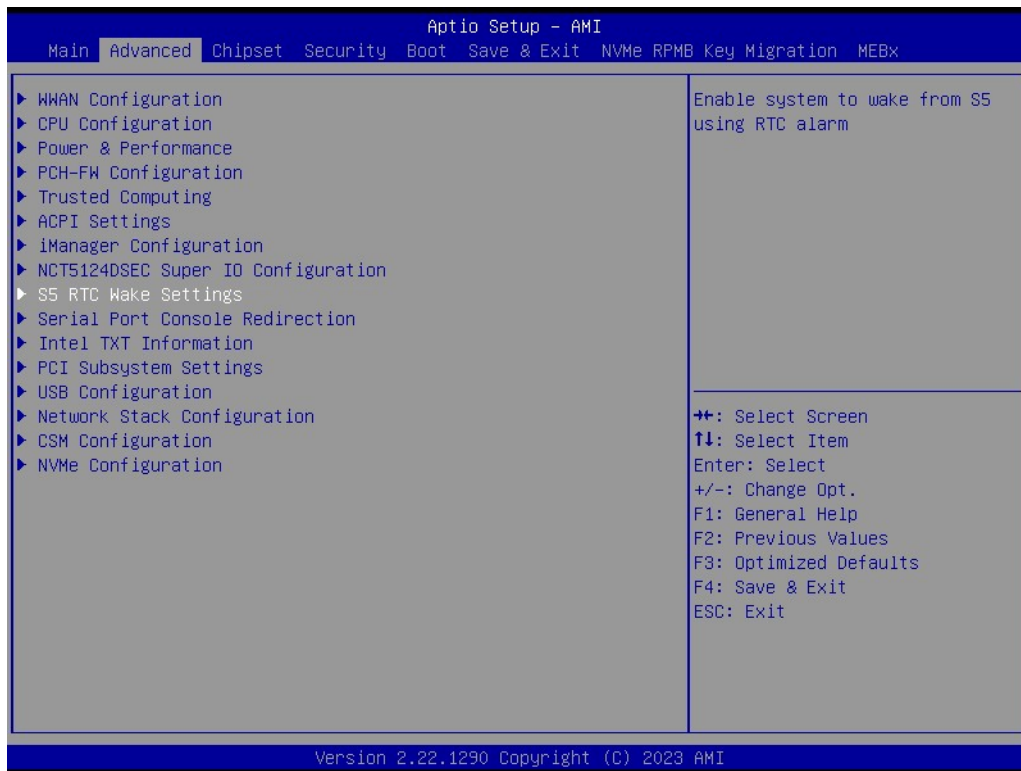
- **Serial Port**
- **Device Settings**
- **Change Settings**
- **COM Port Mode**

## Serial Port 6 Configuration



- **Serial Port**
- **Device Settings**
- **Change Settings**
- **COM Port Mode**

### 3.2.2.9 S5 RTC Wake Settings

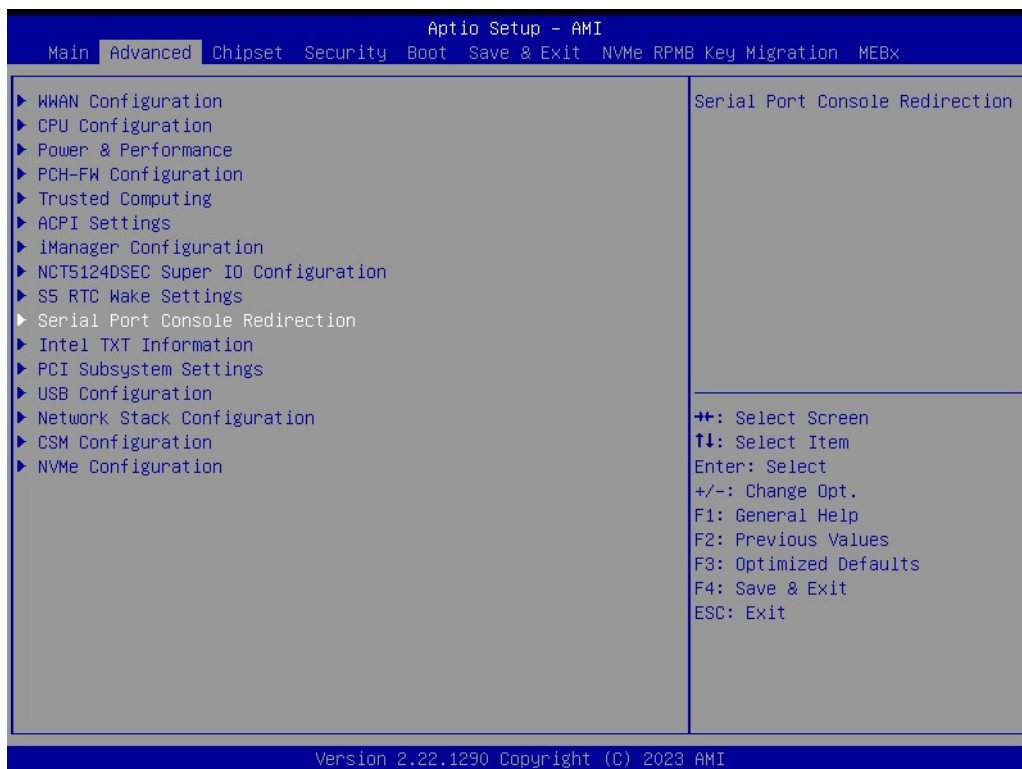


### Wake system from S5

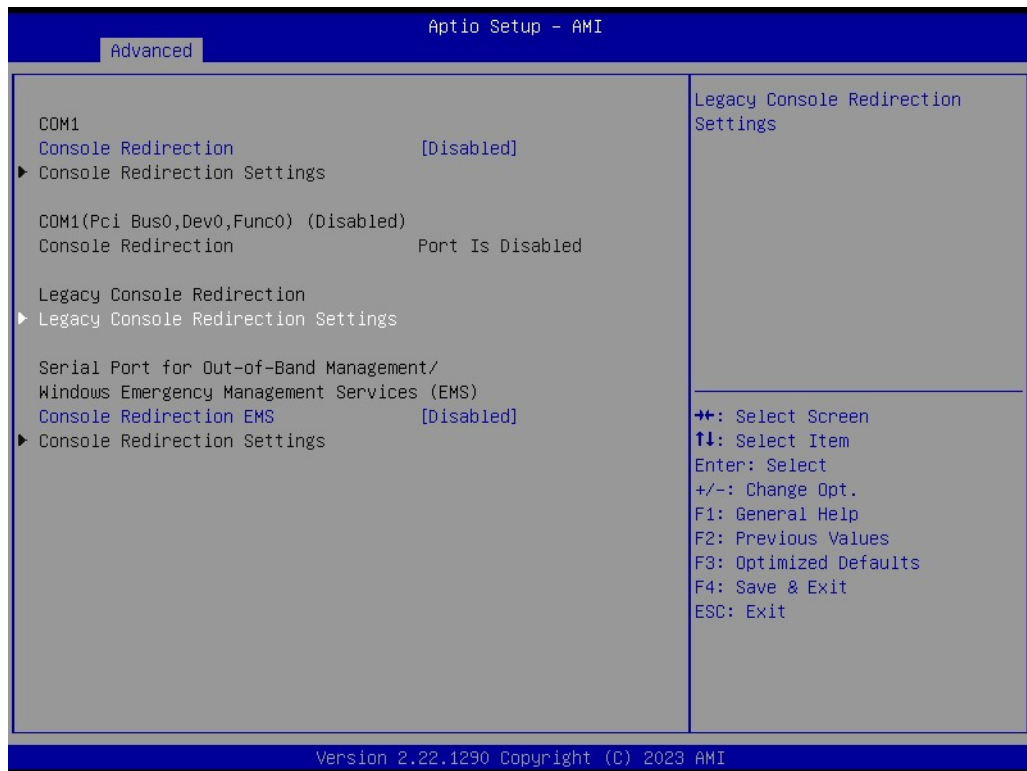




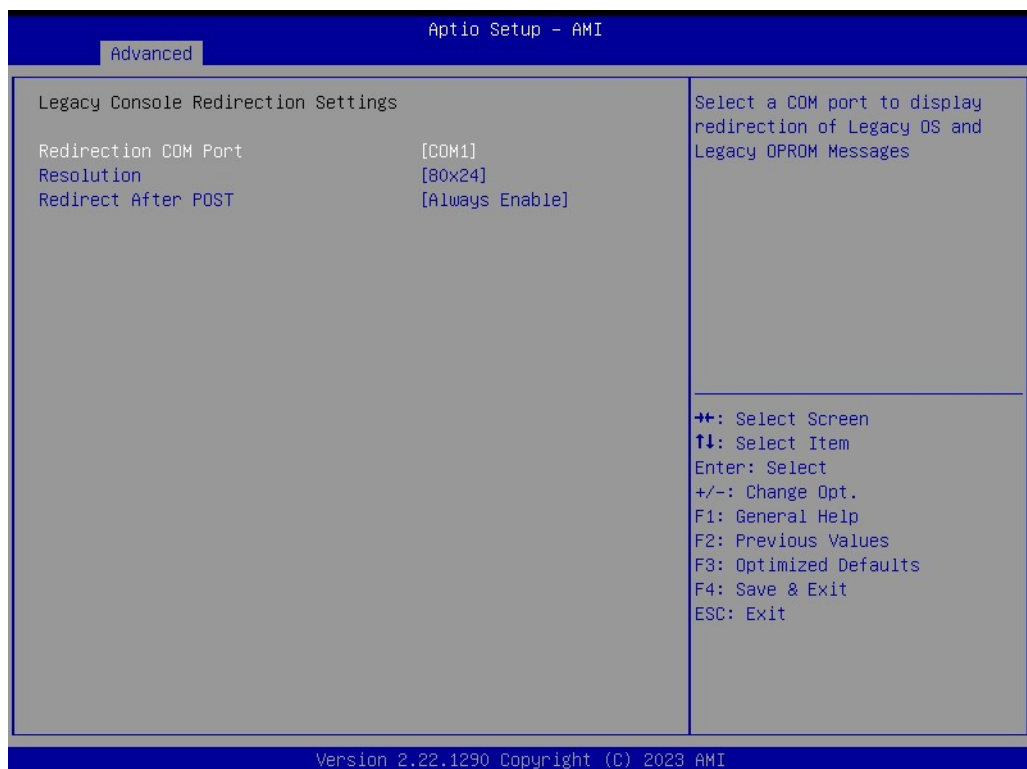
### 3.2.2.10 Serial Port Console Redirection



- **Console Redirection**  
Console Redirection Enable/Disable
- **Console Redirection Settings**  
The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.
- **COM1(Pci Bus, Dev0, Func0)**
- **Console Redirection**  
Console Redirection Enable/Disable.



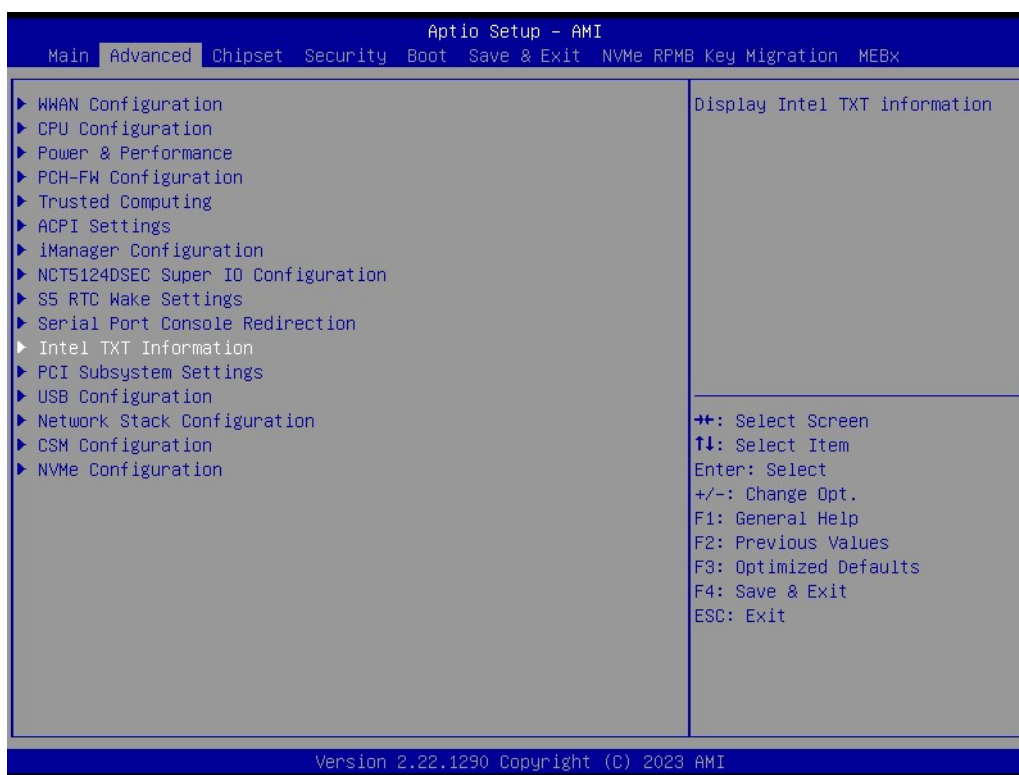
## ■ Legacy Console Redirection Settings



- Redirection COM Port  
Select a COM port to display redirection of Legacy OS and Legacy OPROM Messages
- Resolution  
Enable/Disable extended terminal resolution

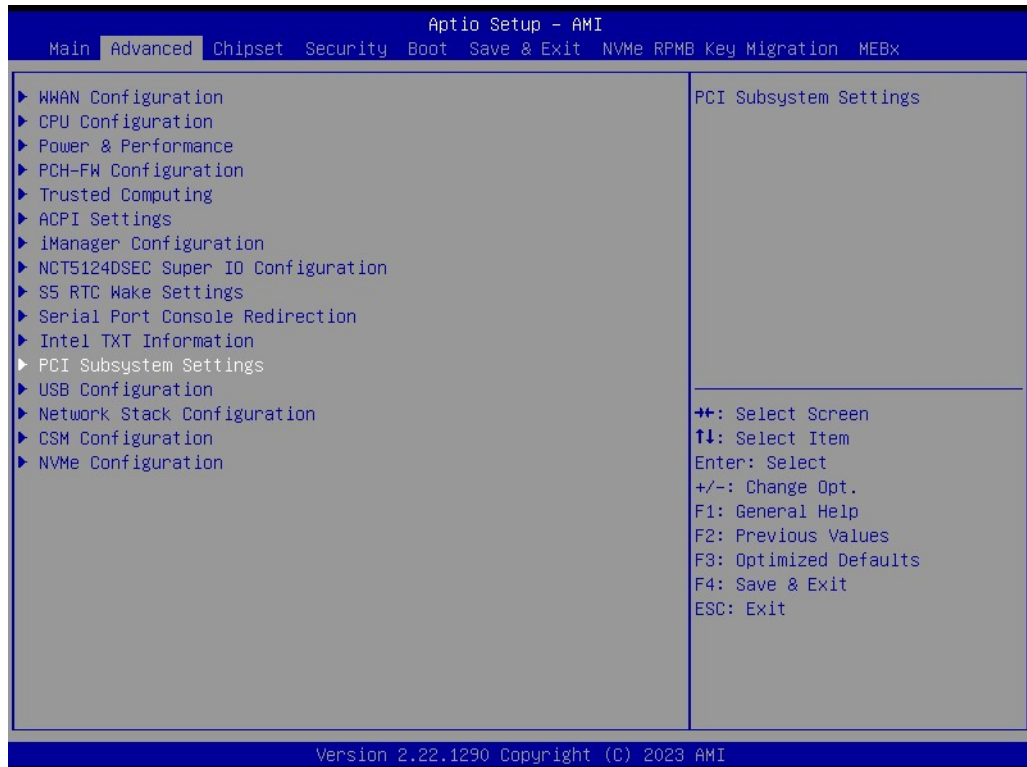
- Redirect After Post
  - When Bootloader is selected, then Legacy Console Redirection is disabled before booting to legacy OS. When Always Enable is selected, then Legacy Console Redirection is enabled for legacy OS. Default setting for this option is set to Always
- **Serial Port for Out-of-Band Management/Windows Emergency Management Services (EMS)**
- **Console Redirection EMS**  
Console Redirection Enable/Disable.
- **Console Redirection Settings**  
The settings specify how the host computer and the remote computer (which the user is using) will exchange data. Both computers should have the same or compatible settings.

### 3.2.2.11 Intel TXT Information

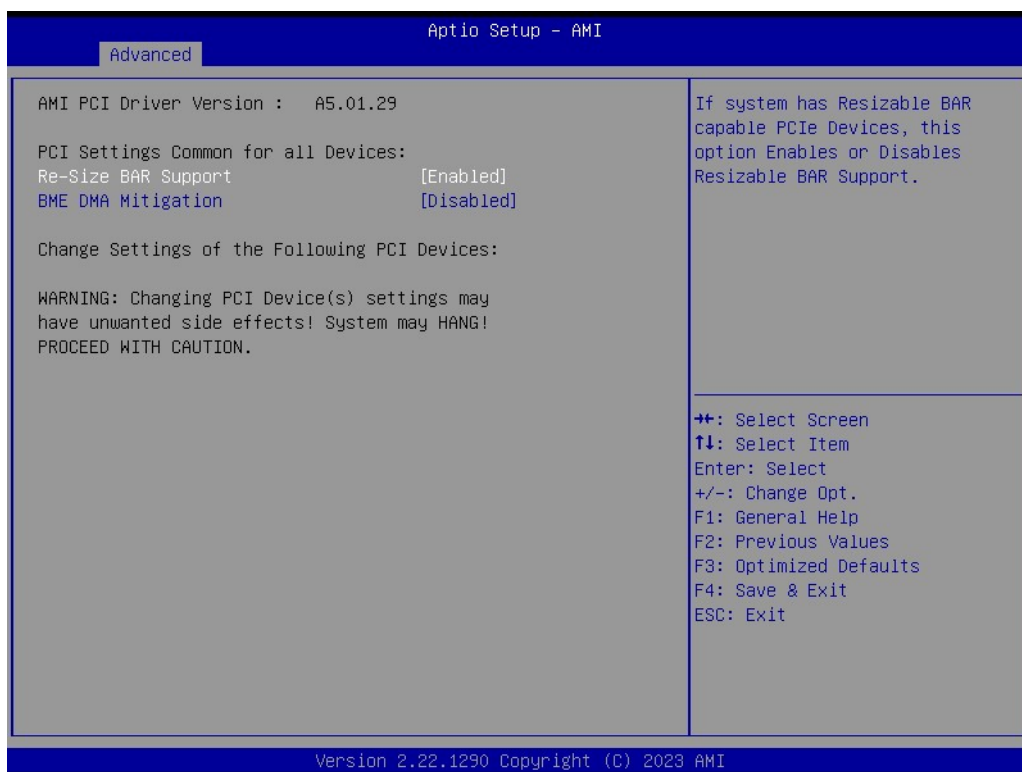


- **Chipset**
- **BiosAcm**
- **Chipset TxT**
- **CPU TxT**
- **Error Code**
- **Class Code**
- **Major Code**
- **Minor Code**

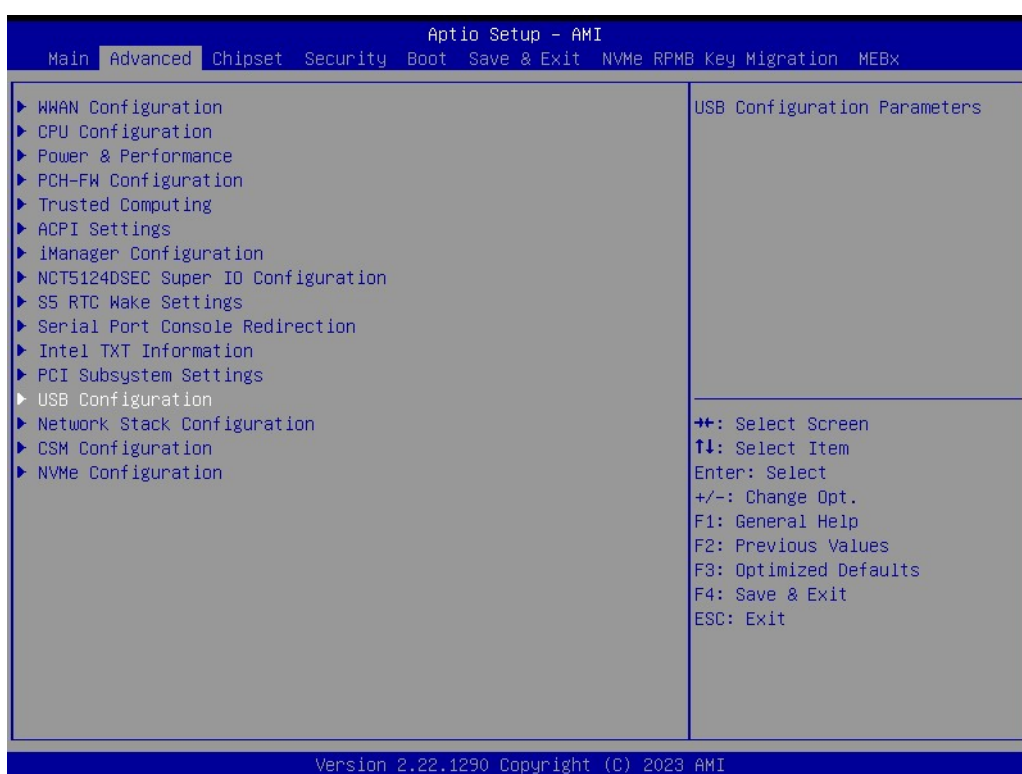
## ■ PCI Subsystem Settings



- Re-Sized BAR Support
- If system has Resizable BAR capable PCIe Devices, this option Enables or Disables Resizable BAR Support.
- BME DMA Mitigation  
Re-enable Bus Master Attribute disabled during PCI enumeration for PCI Bridges after SMM Locked

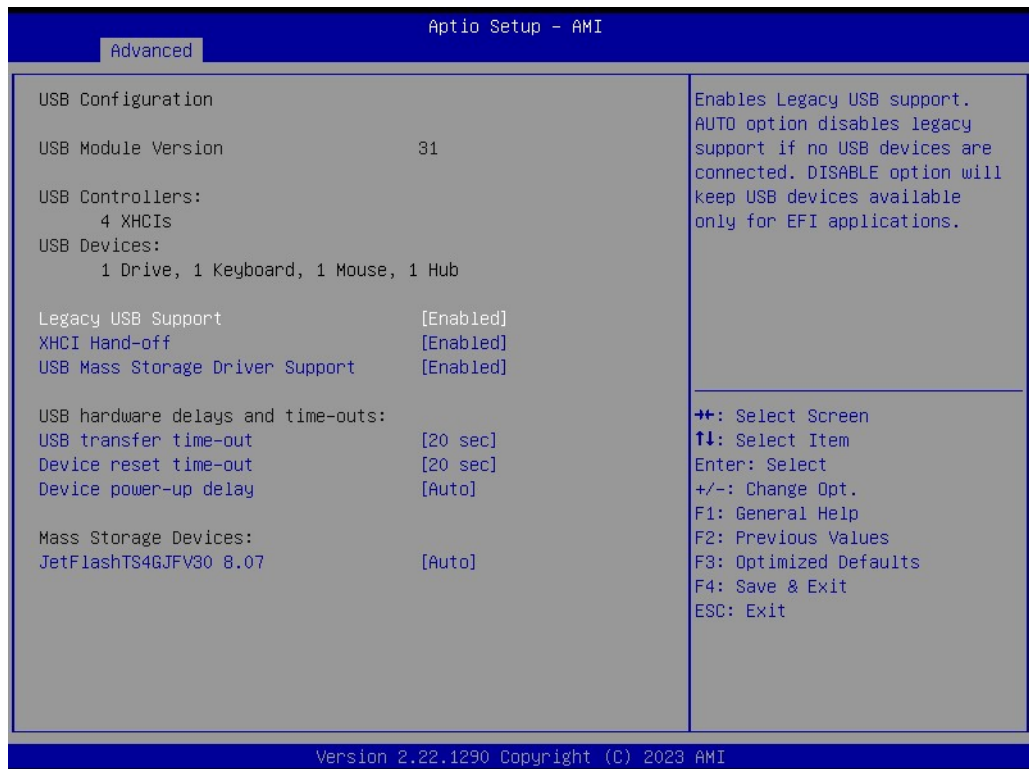


### 3.2.2.12 USB Configuration

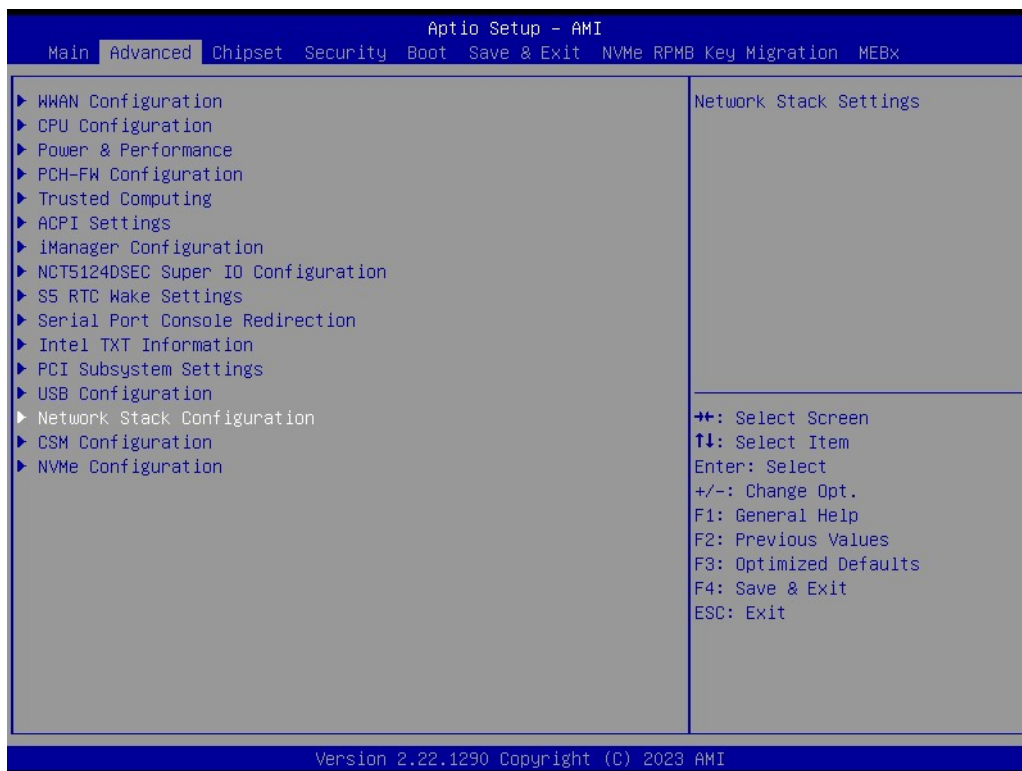


- **Legacy USB Support**  
Enables Legacy USB support.
- **XHCI Hand-off**  
This is a workaround for OS without XHCI hand-off support.

- **USB Mass Storage Device Configuration**  
Configure the USB Mass Storage Devices.
- **USB transfer time-out**  
The time-out value for Control, Bulk, and Interrupt transfers.
- **Device reset time-out**  
USB mass storage device Start Unit command time-out.
- **Device power-up delay**  
Maximum time the device will take before it properly reports itself to the Host Controller.
  
- **JetFlashTS4GJFV30 8.07**



### 3.2.2.13 Network Stack Configuration

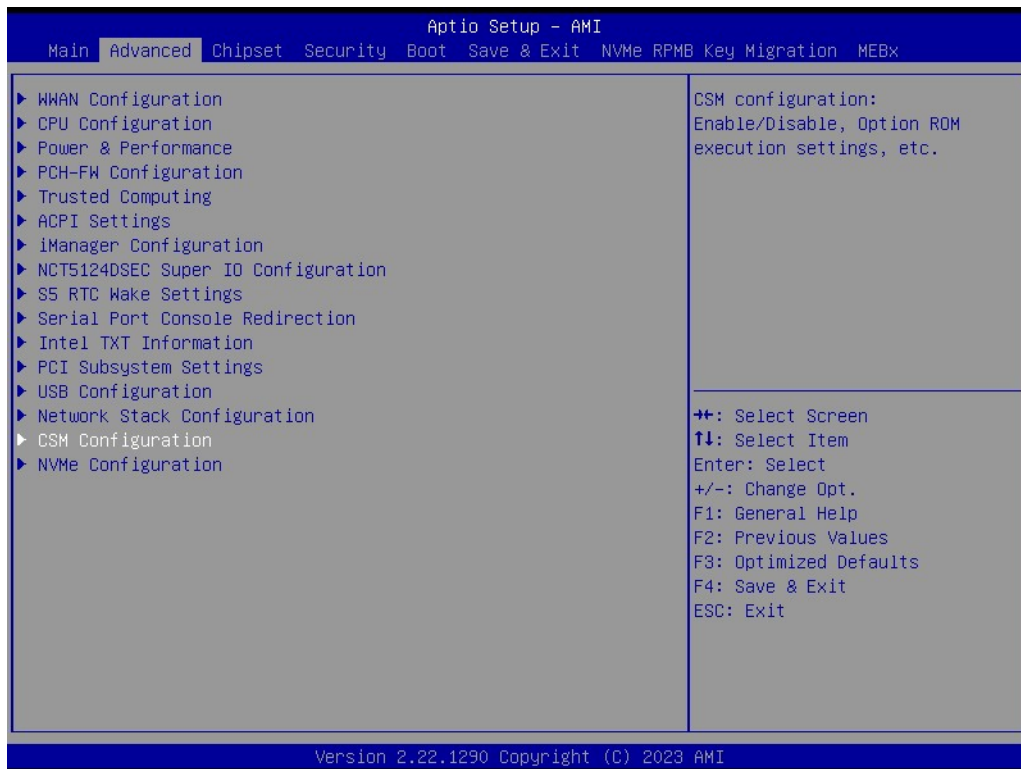


#### ■ Network Stack





### 3.2.2.14 CSM Configuration

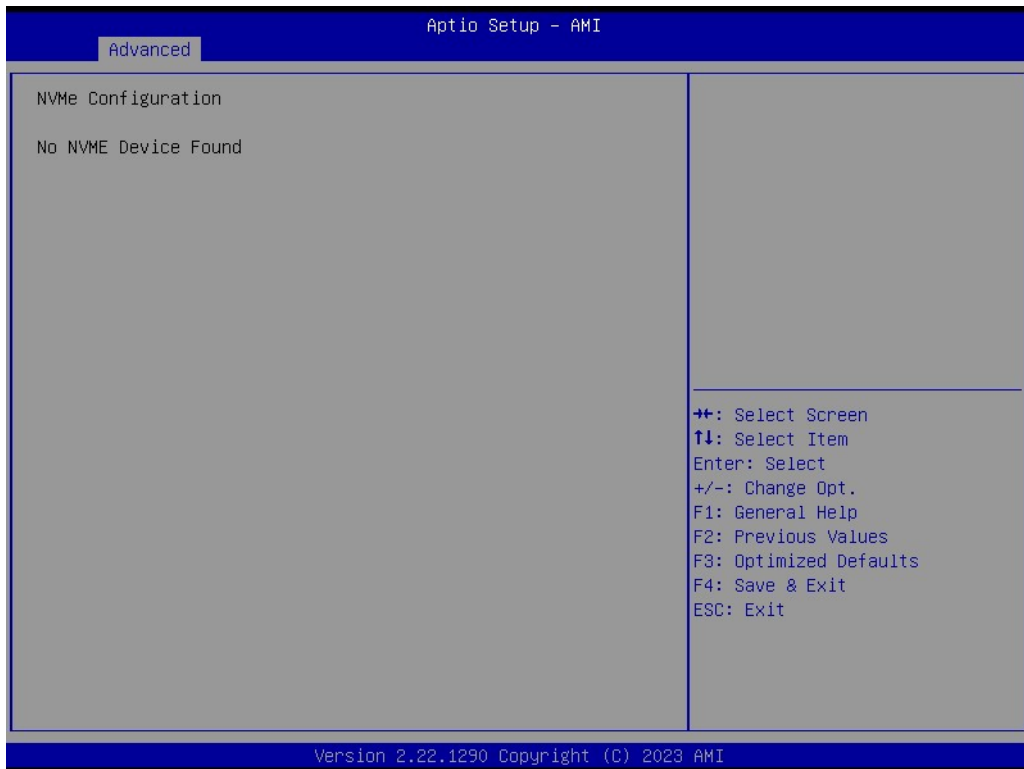
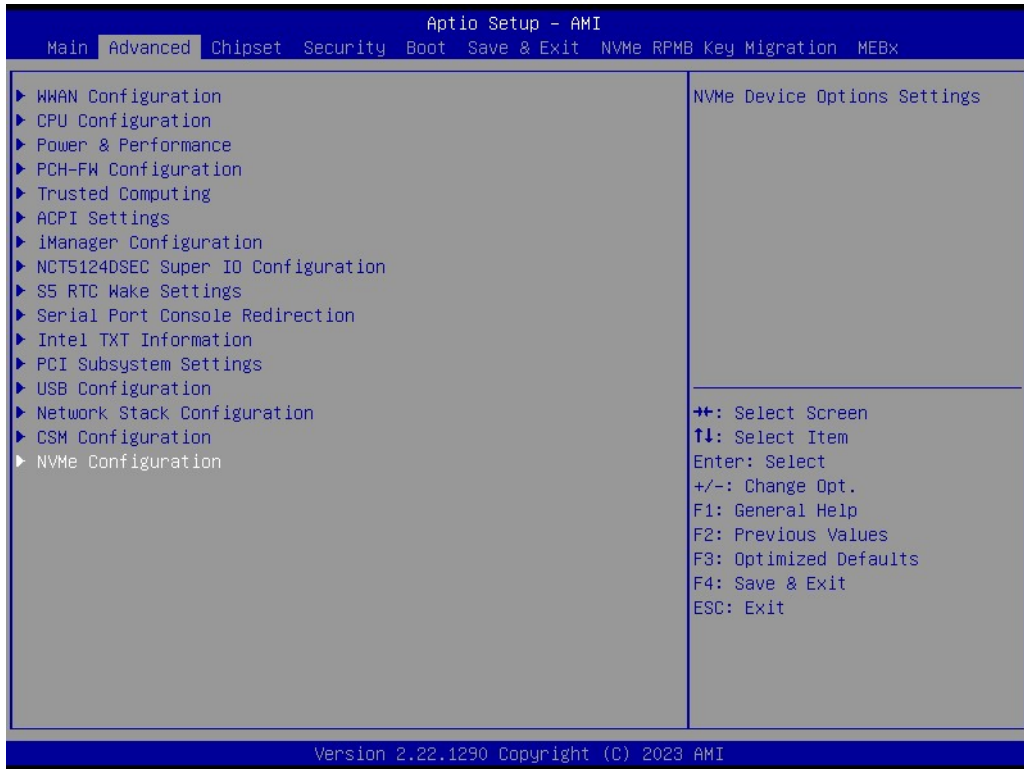


- **CSM Support**  
Enable/Disable CSM Support.





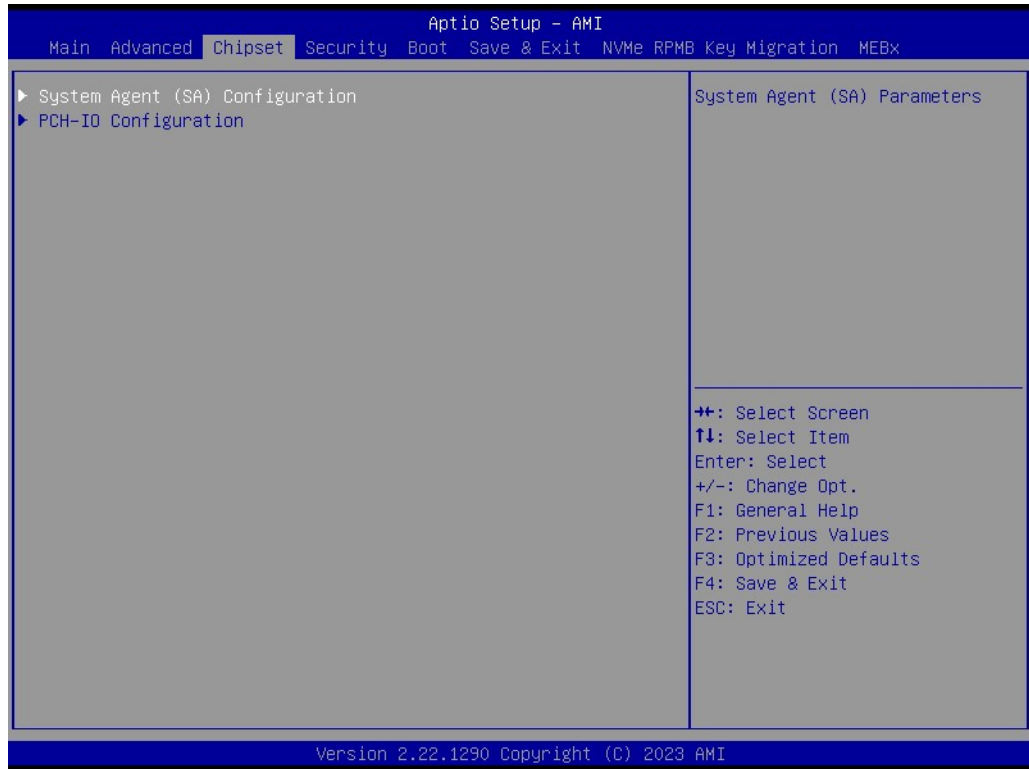
### 3.2.2.15 NVMe Configuration



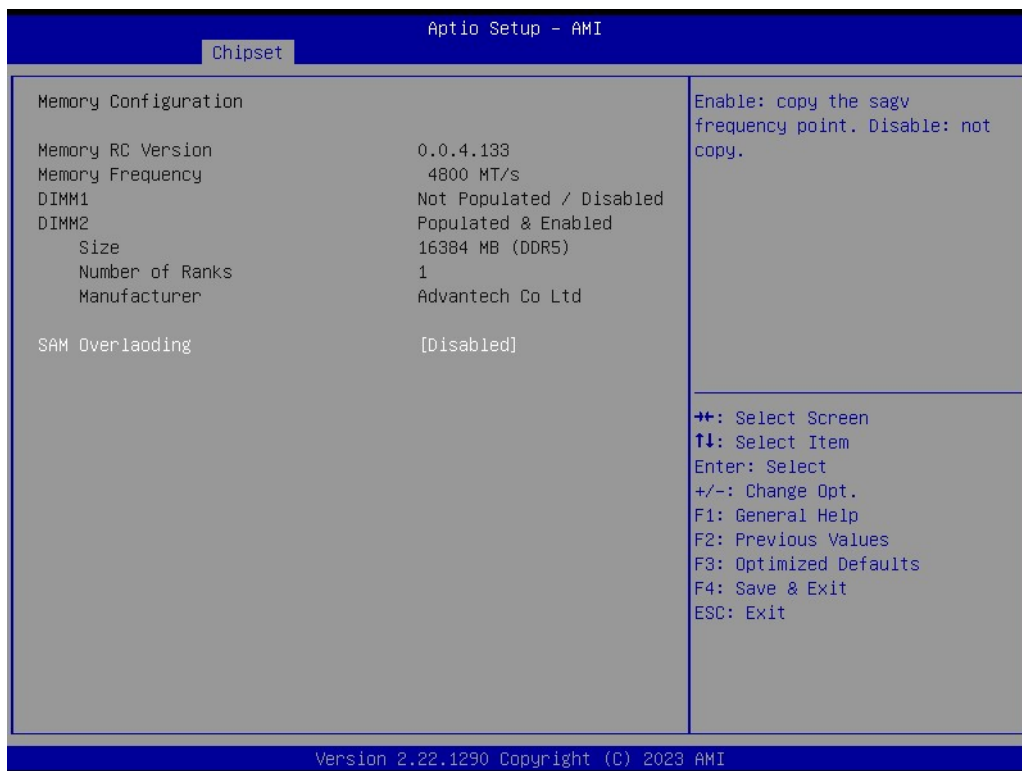
### 3.2.3 Chipset Configuration

Select the Chipset tab from the ARK-2251 setup screen to enter the Chipset BIOS Setup screen. You can display a Chipset BIOS Setup option by highlighting it using the <Arrow> keys. All Plug and Play BIOS Setup options are described in this section. The Plug and Play BIOS Setup screen is shown below.

#### 3.2.3.1 System Agent Configuration

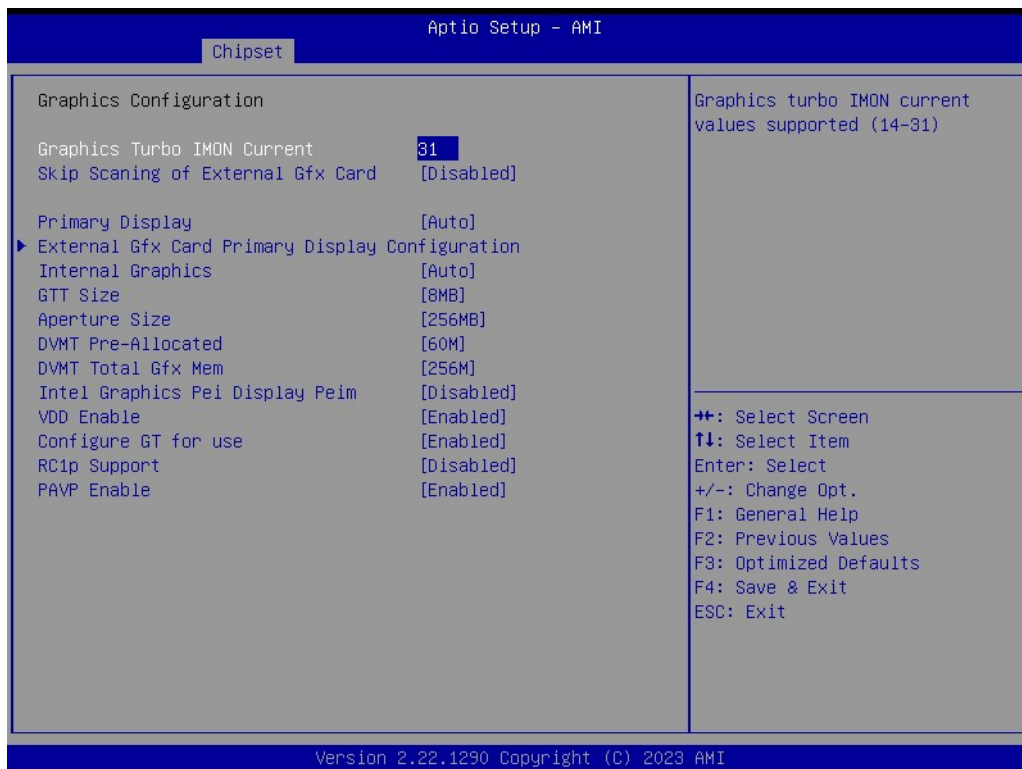


## ■ Memory Configuration



- SAM Overloading  
Enable/Disable SAM Overloading

## ■ Graphics Configuration



- 
- Graphics Turbo IMON current  
Graphics turbo IMON current values supported (14-31)
  - Skip Scanning of External Gfx Card  
If Enabled, it will not scan for External Gfx Card on PEG and PCH PCIE Ports.
  - Primary Display  
Select which of IGFX/PEG/PCI Graphics device should be Primary Display or select SG for Switchable Gfx.
  - External Gfx Card Primary Display Configuration  
Select the card used on the platform.
  - Internal Graphics  
Keep IGFX enabled based on the setup options.
  - GTT Size  
Select the GTT Size.
  - Aperture Size  
Select the Aperture Size.
  - Dvmt Pre-Allocated  
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
  - Dvmt Total Gfx Mem  
Select DVMT5.0 Total Graphic Memory size used by the Internal Graphics Device.
  - DVMT Pre-Allocated  
Select DVMT 5.0 Pre-Allocated (Fixed) Graphics Memory size used by the Internal Graphics Device.
  - Intel Graphics Pei Display Peim  
Enable/Disable Pei (Early) Display
  - VDD Enable  
Enable/Disable forcing of VDD in the BIOS
  - Configure GT for use  
Enable/Disable GT configuration in BIOS
  - RC1p Support  
Enable/Disable RC1p support. If RC1p is enabled, send a RC1p frequency request to PMA based other conditions being met
  - PAVP Enable  
Enable/Disable PAVP

## ■ VMD Setup Menu



- Enable VMD Controller  
 Enable/Disable to VMD controller

## ■ PCI Express Configuration

### ■ VT-d

VT-d capability

### ■ Control Iommu Pre-boot Behavior

Control Iommu Pre-boot Behavior

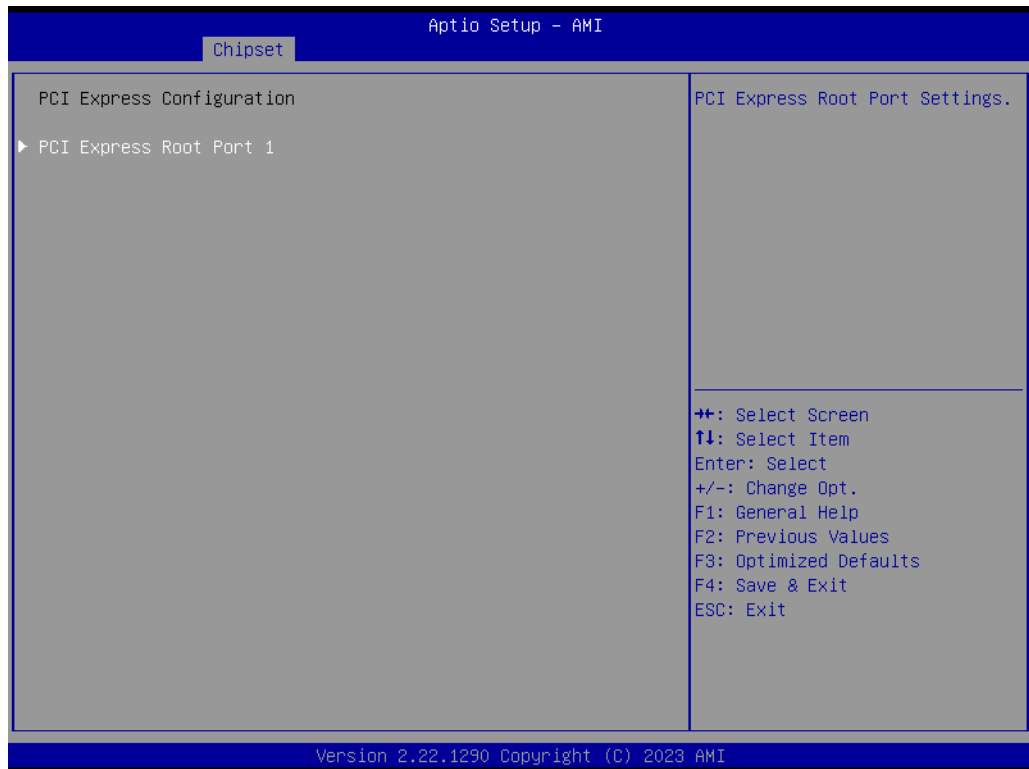
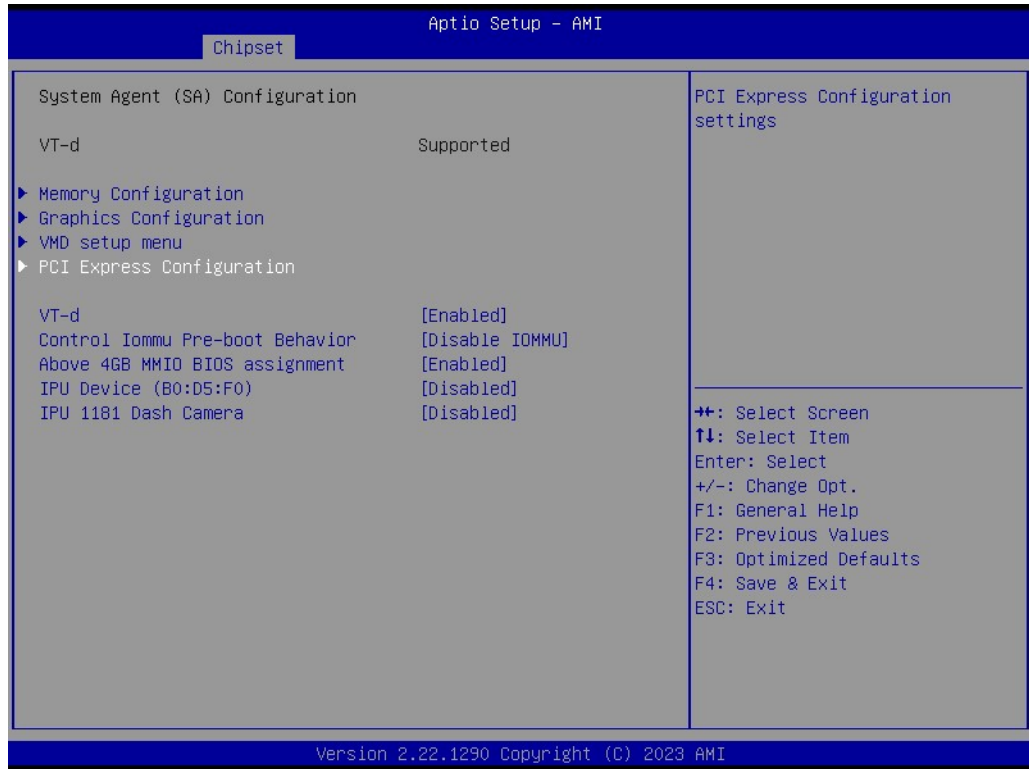
### ■ Above 4GB MMIO BIOS assignment

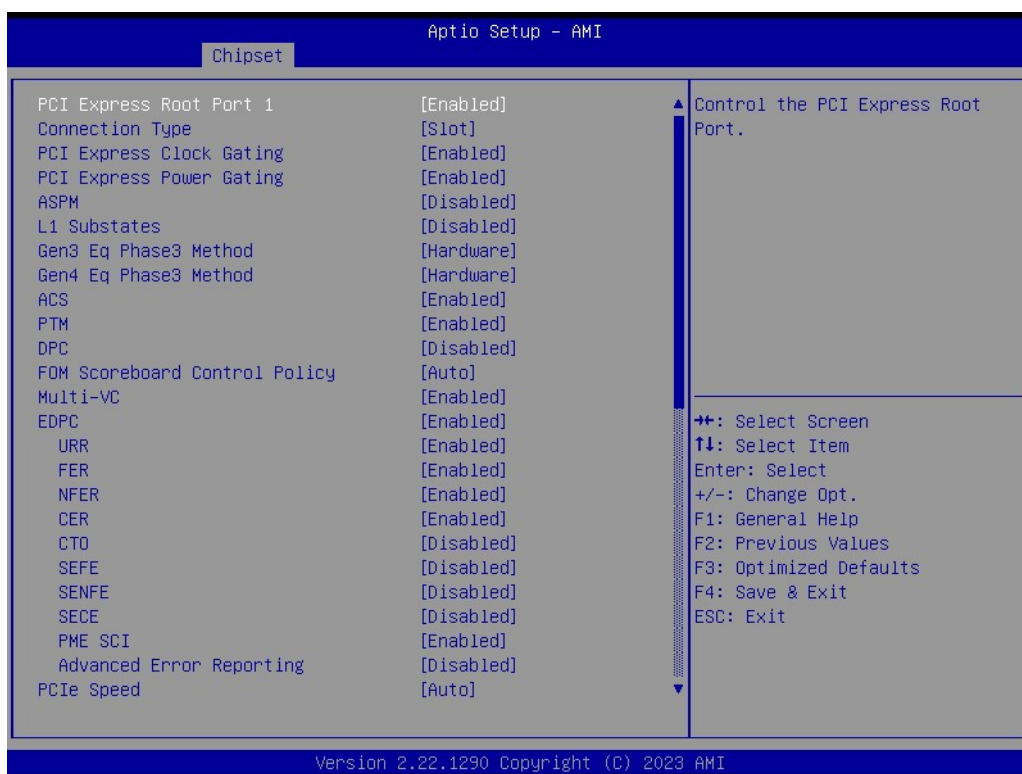
Enable/Disable above 4GB Memory Mapped I/O BIOS assignment. This is enabled automatically when Aperture Size is set to 2048MB.

### ■ IPU Device (B0:D5:F0)

Enable/Disable SA IPU Device.

■ IPU 1181 Dash Camera





- **PCI Express Root Port 1**
  - PCI Express Root Port 1  
Control the PCI Express Root Port.
  - Connection Type  
Built-In: a built-in device is connected to this rootport. SlotImplemented bit

---

will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.

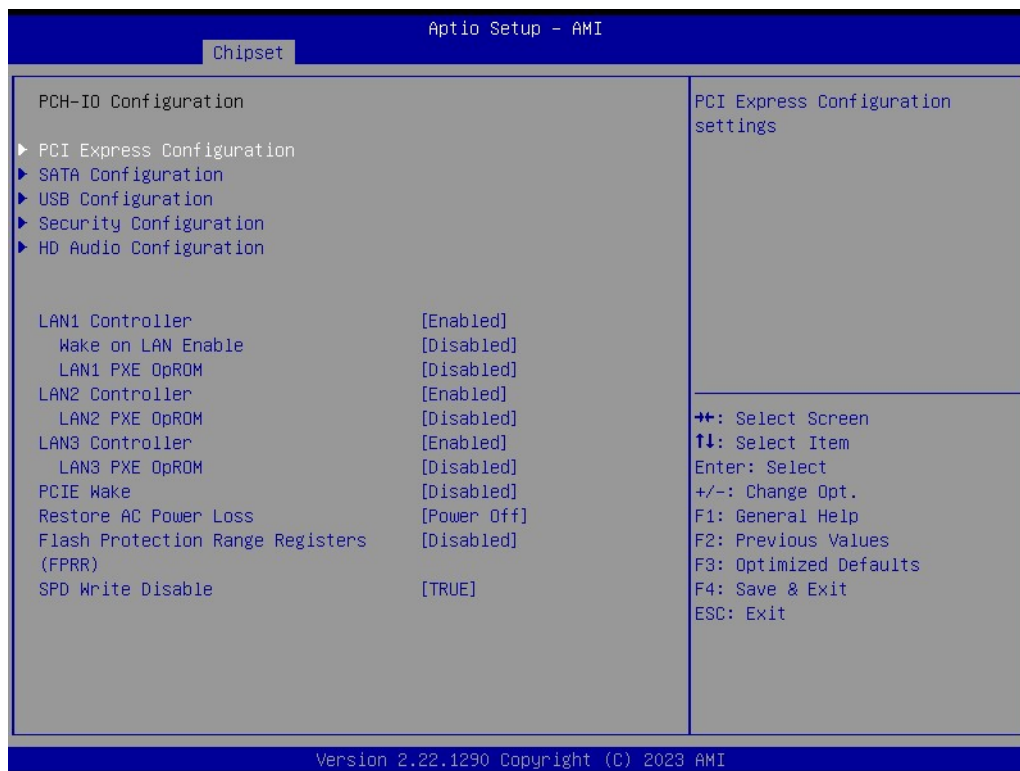
- PCI Express Clock Gating  
PCI Express Clock Gating Enable/Disable for each root port.
- PCI Express Power Gating  
PCI Express Power Gating Enable/Disable for each root port.
- ASPM  
PCI Express Active State Power Management settings
- L1 Substates  
PCI Express L1 Substates settings.L1SS cannot be enabled when CLKREQMSG is disabled
- Gen3 EQ Phase3 Method  
PCIe Gen3 Equalization Phase 3 Method
- Gen4 EQ Phase3 Method  
PCIe Gen4 Equalization Phase 3 Method
- ACS  
Enable/Disable Access Control Services Extended Capability
- PTM  
Enable/Disable Precision Time Measurement
- DPC  
Enable/Disable Downstream Port Containment
- FOM Scoreboard Control Policy  
Select the FOM Scoreboard Control Policy, when set to Auto, speed is based on TLS
- Multi-VC  
Enable/Disable Multi Virtual Channel
- EDPC  
Enable/Disable Rootport extensions for Downstream Port Containment
- URR  
PCI Express Unsupported Request Reporting Enable/Disable.
- FER  
PCI Express Device Fatal Error Reporting Enable/Disable.
- NFER  
PCI Express Device Non-Fatal Error Reporting Enable/Disable
- CER  
PCI Express Device Correctable Error Reporting Enable/Disable.
- CTO  
PCI Express Device Correctable Error Reporting Enable/Disable.
- SEFE  
Root PCI Express System Error on Fatal Error Enable/Disable.
- SENFE  
Root PCI Express System Error on Non-Fatal Error Enable/Disable.
- SECE  
Root PCI Express System Error on Correctable Error Enable/Disable
- PME SCI  
PCI Express PME SCI Enable/Disable.
- Advanced Error Reporting  
Advanced Error Reporting Enable/Disable.
- PCIe Speed  
Configure PCIe Speed
- Enable ClockReq Messaging  
Enable/Disable ClockReq Messaging



- Transmitter Half Swing  
Transmitter Half Swing Enable/Disable.
- Detect Timeout  
The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
- P2P Support  
Program P2P Support Registers according to setup option
- CPU PCIE Func0 Link Disable  
CPU PCIE Func0 Link Disable while Device attached into Port having Func0 and FuncN
- SA PCIe LTR Configuration  
SA PCIe Latency Reporting Enable/Disable
- LTR  
SA PCIe Latency Reporting Enable/Disable
- Snoop Latency Override  
Snoop Latency Override for SA PCIE.
- Non Snoop Latency Override  
Non Snoop Latency Override for SA PCIE.
- Force LTR Override  
Force LTR Override for SA PCIE.
- LTR Lock  
PCIE LTR Configuration Lock

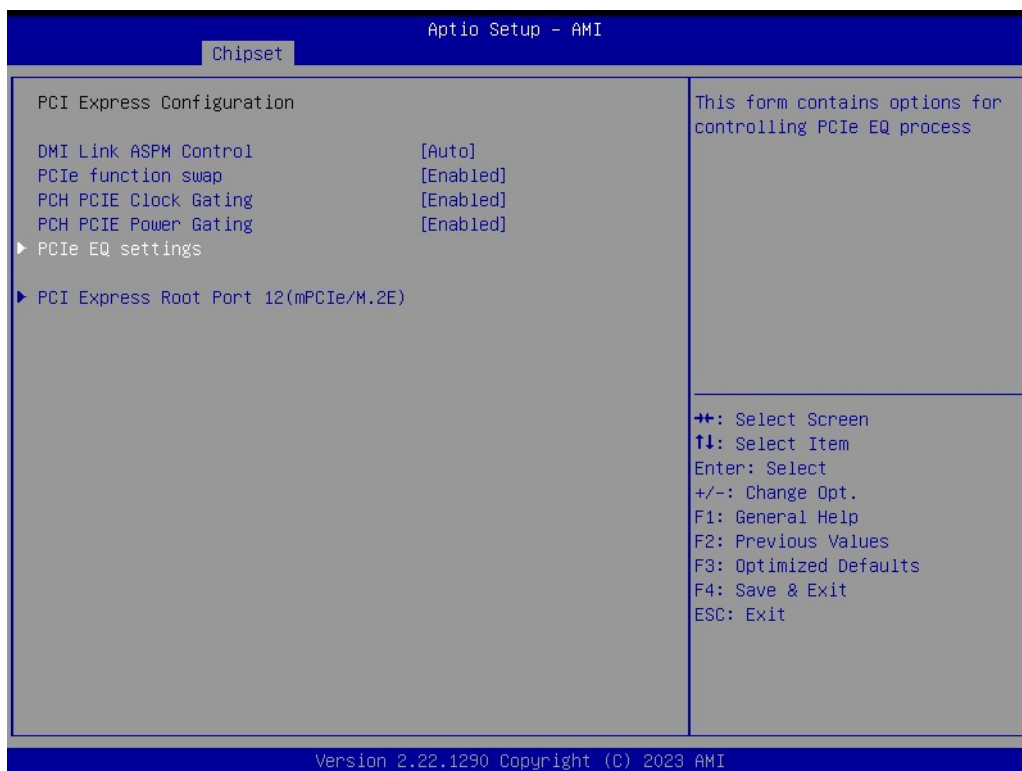
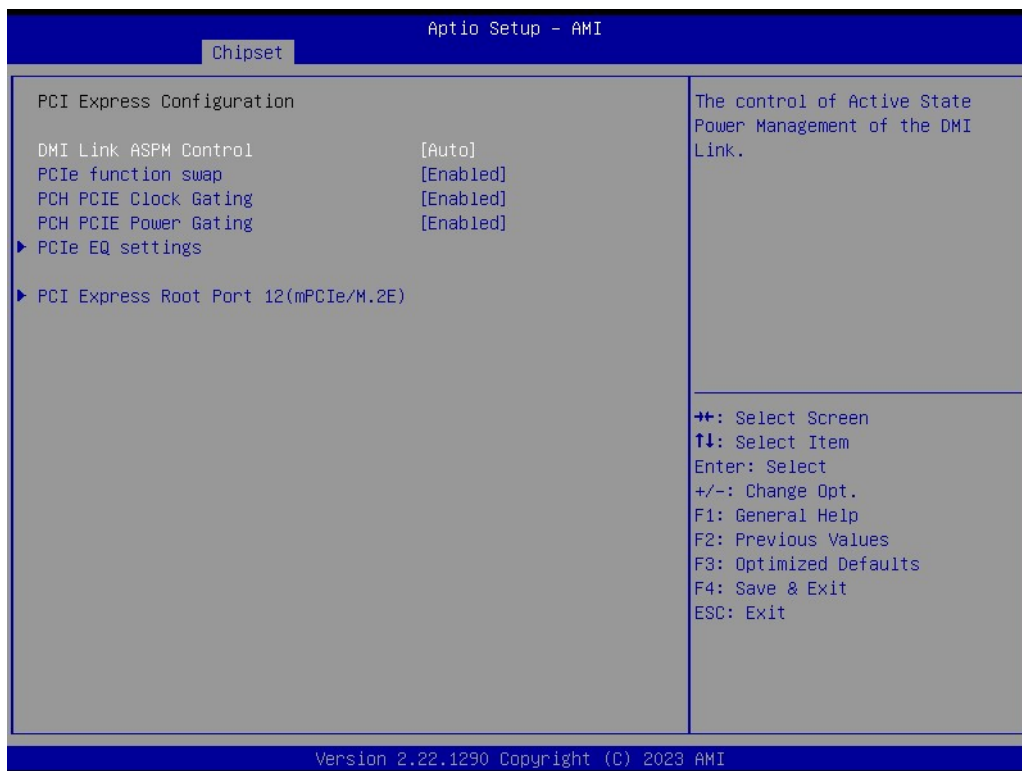
### 3.2.3.2 PCH-IO Configuration

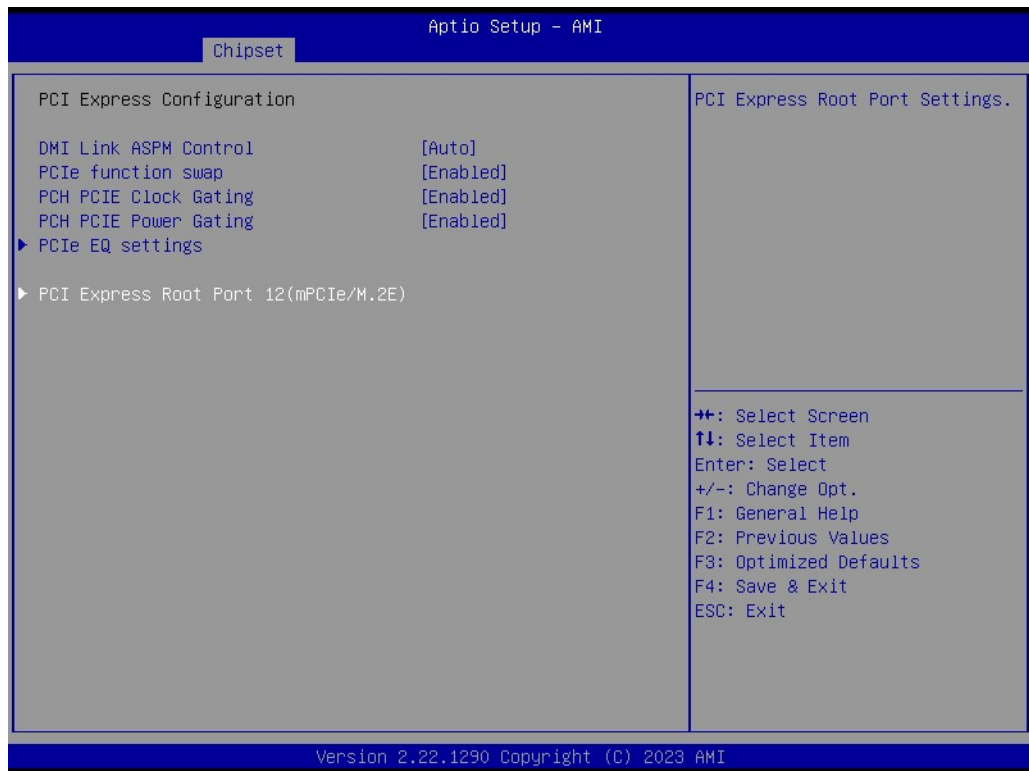
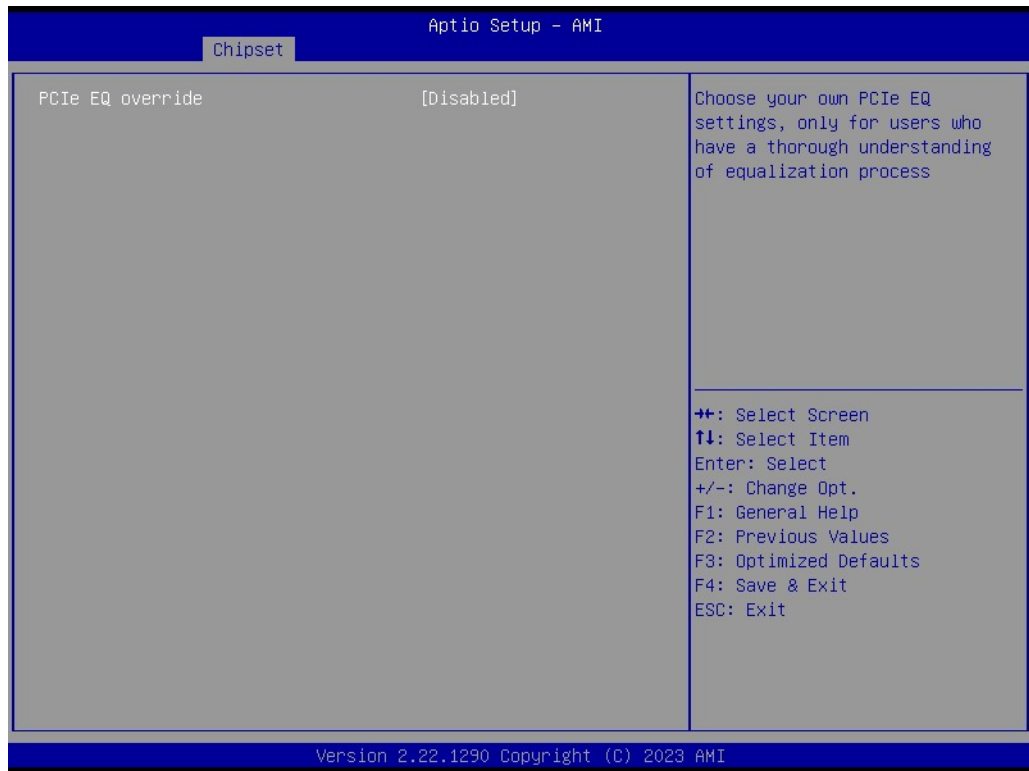


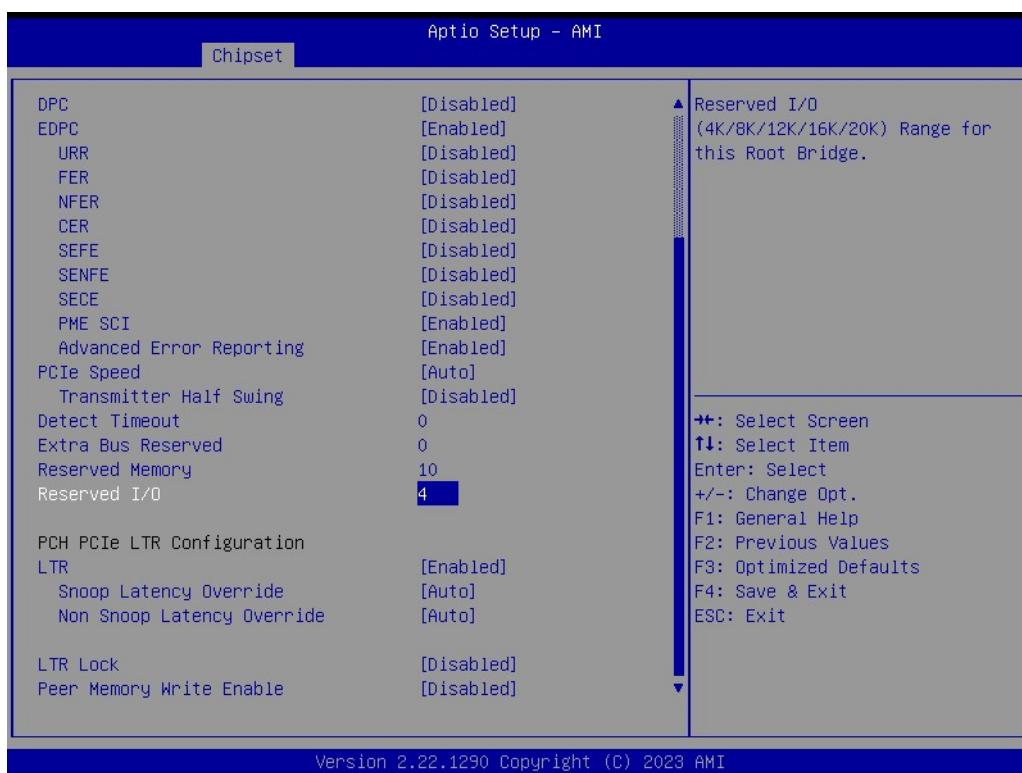
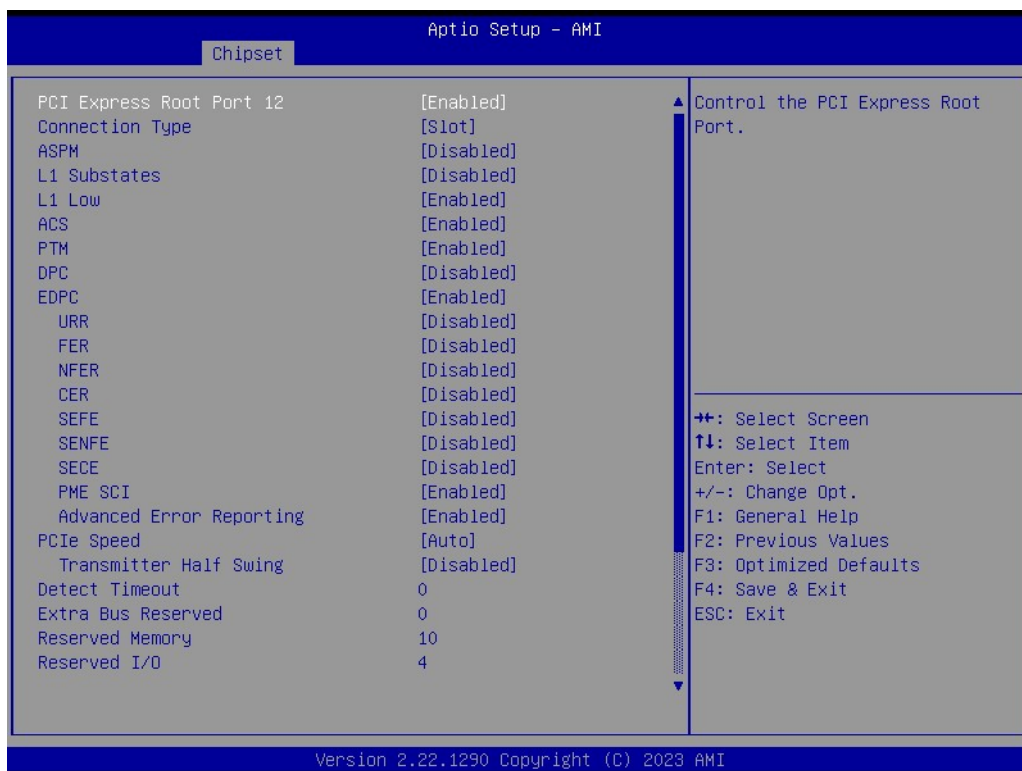


- **LAN1 Controller**  
Control Detection of the HD-Audio device.
- **Wake on LAN Enable**  
Enable/Disable integrated LAN to wake the system.
- **LAN1 PXE OpRom**  
Enable/Disable boot option rom for LAN1 Controller.
- **LAN2 Controller**  
Enable/Disable onboard LAN2
- **LAN2 PXE OpROM**  
Enable/Disable boot option rom for LAN2 Controller.
- **LAN3 Controller**  
Enable/Disable onboard LAN3
- **LAN3 PXE OpROM**  
Enable/Disable boot option ROM for LAN2 Controller.
- **PCIE Wake**  
Enable/Disable PCIE to wake the system from S5.
- **Restore AC Power Loss**  
Specify what state to go to when power is re-applied after a power failure (G3 state).
- **Flash Protection Range Registers (FPRR)**  
Enable Flash Protection Range Registers
- **SPD Write Disable**  
Enable/Disable setting SPD Write Disable. For security recommendations, SPD write disable bit must be set.

## ■ PCI Express Configuration





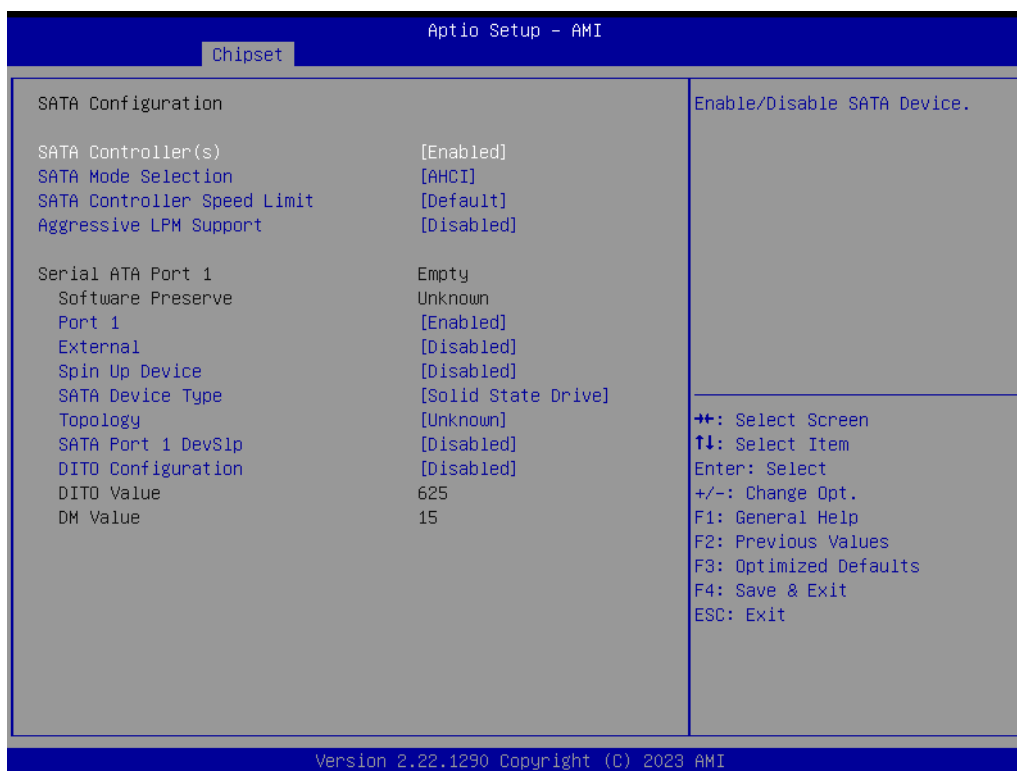


- DMI Link ASPM Control  
The control of Active State Power Management of the DMI Link.
- PCIe function swap  
Enable/Disable PCIe function swap
- PCH PCIE Clock Gating  
PCH PCI Express Clock Gating Enable/Disable for all port

- PCH PCIE Power Gating
  - PCH PCI Express Power Gating Enable/Disable for all port
- PCIe EQ settings
  - PCIe EQ override
    - Choose your own PCIe EQ settings, only for users who have a thorough understanding of equalization process
- PCI Express Root Port 12(mPCIe/M.2E)
  - PCI Express Root Port 12
    - Control the PCI Express Root Port.
  - Connection Type
    - Built-In: a built-in device is connected to this rootport. SlotImplemented bit will be clear. Slot: this rootport connects to user-accessible slot. SlotImplemented bit will be set.
  - ASPM
    - PCI Express Active State Power Management settings.
  - L1 Substates
    - PCI Express L1 Substates settings.L1SS cannot be enabled when CLKREQMSG is disabled
  - L1 Low
    - PCI Express L1 Low Substate Enable/Disable.
  - ACS
    - Enable/Disable Access Control Services Extended Capability
  - PTM
    - Enable/Disable Precision Time Measurement
  - DPC
    - Enable/Disable Downstream Port Containment
  - EDPC
    - Enable/Disable Rootport extensions for Downstream Port Containment
  - URR
    - PCI Express Unsupported Request Reporting Enable/Disable.
  - FER
    - PCI Express Device Fatal Error Reporting Enable/Disable.
  - NFER
    - PCI Express Device Non-Fatal Error Reporting Enable/Disable.
  - CER
    - PCI Express Device Correctable Error Reporting Enable/Disable
  - SEFE
    - Root PCI Express System Error on Fatal Error Enable/Disable
  - SENFE
    - Root PCI Express System Error on Non-Fatal Error Enable/Disable
  - SECE
    - Root PCI Express System Error on Correctable Error Enable/Disable.
  - PME SCI
    - PCI Express PME SCI Enable/Disable.
  - Advanced Error Reporting
    - Advanced Error Reporting Enable/Disable
  - PCIe Speed
    - Configure PCIe Speed
  - Transmitter Half Swing
    - Transmitter Half Swing Enable/Disable
  - Detect Timeout
    - The number of milliseconds reference code will wait for link to exit Detect state for enabled ports before assuming there is no device and potentially disabling the port.
  - Extra Bus Reserved

- Extra Bus Reserved (0-7) for bridges behind this Root Bridge.
- Reserved Memory
  - Reserved Memory for this Root Bridge (1-20) MB
- Reserved I/O
  - Reserved I/O (4K/8K/12K/16K/20K) Range for this Root Bridge.
- LTR
  - SA PCIE Latency Reporting Enable/Disable
- Snoop Latency Override
  - Snoop Latency Override for SA PCIE.
- Non Snoop Latency Override
  - Non Snoop Latency Override for SA PCIE
- LTR Lock
  - PCIE LTR Configuration Lock
- Peer Memory Write Enable
  - Peer Memory Write Enable/Disable

## ■ SATA Configuration



- SATA Controller(s)
  - Enable/Disable SATA Device.
- SATA Mode Selection
  - Determines how SATA controller(s) operate.
- SATA Controller Speed Limit
  - Indicates the maximum speed the SATA controller can support.
- Aggressive LPM Support
  - Enable PCH to aggressively enter link power state
- Serial ATA Port 1
- Software Preserve
- Port 1
- External

- Spin Up Device  
If enabled for any of ports Staggered Spin Up will be performed and only the drives which have this option enabled will spin up at boot. Otherwise all drives spin up at boot.
- SATA Device Type  
Identify the SATA port is connected to Solid State Drive or Hard Disk Drive
- Topology  
Identify the SATA Topology if it is Default or ISATA or Flex or DirectConnect or M2
- SATA Port 1 DevSlp  
Enable/Disable SATA Port 1 DevSlp. For DevSlp to work, both hard drive and SATA port need to support DevSlp function, otherwise an unexpected behavior might happen. Please check board design before enabling it.
- DITO Configuration
- Enable/Disable DITO Configuration
- DITO Value
- DM Value

## ■ USB Configuration



- DM Value  
Select 'Disabled' for pin-based debug. If pin-based debug is enabled but USB overcurrent is not disabled, USB DbC will not work.
- USB Overcurrent Lock  
Select 'Enabled' if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping data.
- USB Overcurrent Lock  
Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.



## ■ Security Configuration



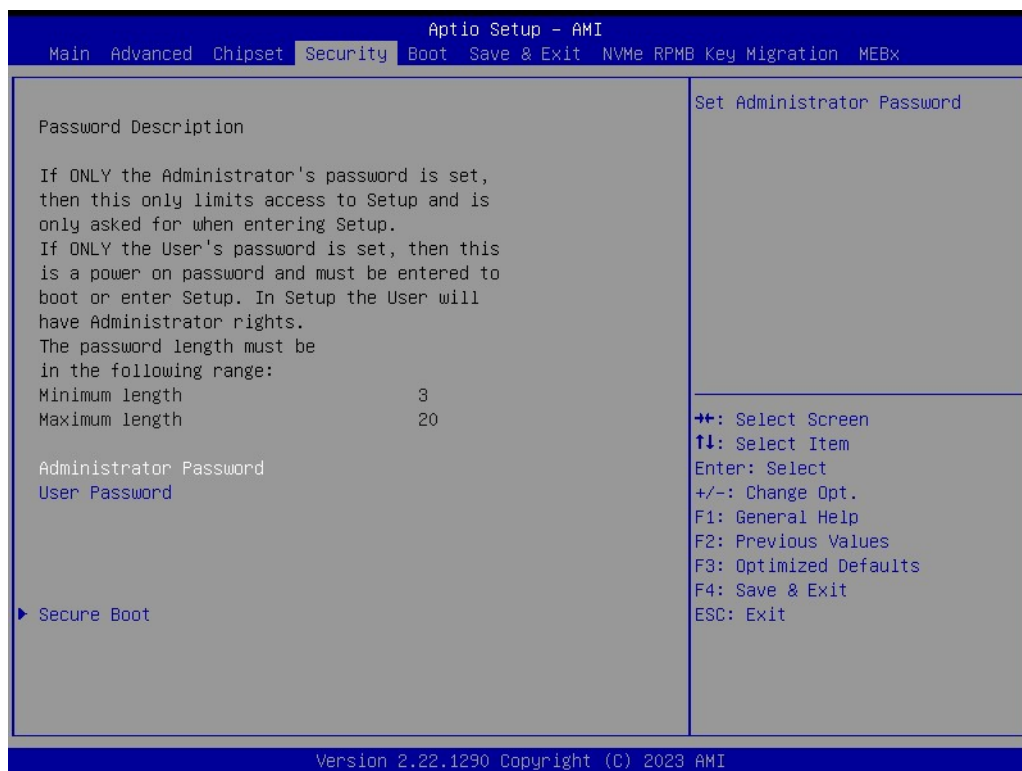
- DM Value  
Select 'Disabled' for pin-based debug. If pin-based debug is enabled but USB overcurrent is not disabled, USB D<sub>b</sub>C will not work.
- USB Overcurrent Lock  
Select 'Enabled' if Overcurrent functionality is used. Enabling this will make xHCI controller consume the Overcurrent mapping data.
- USB Overcurrent Lock  
Selectively Enable/Disable the corresponding USB port from reporting a Device Connection to the controller.

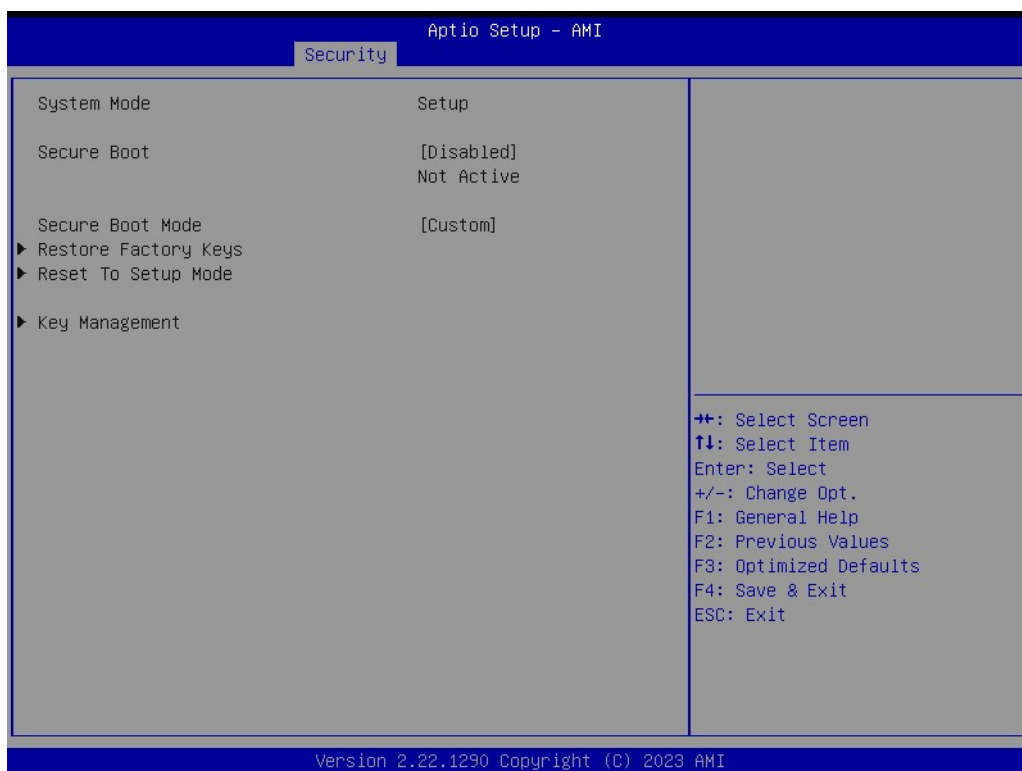
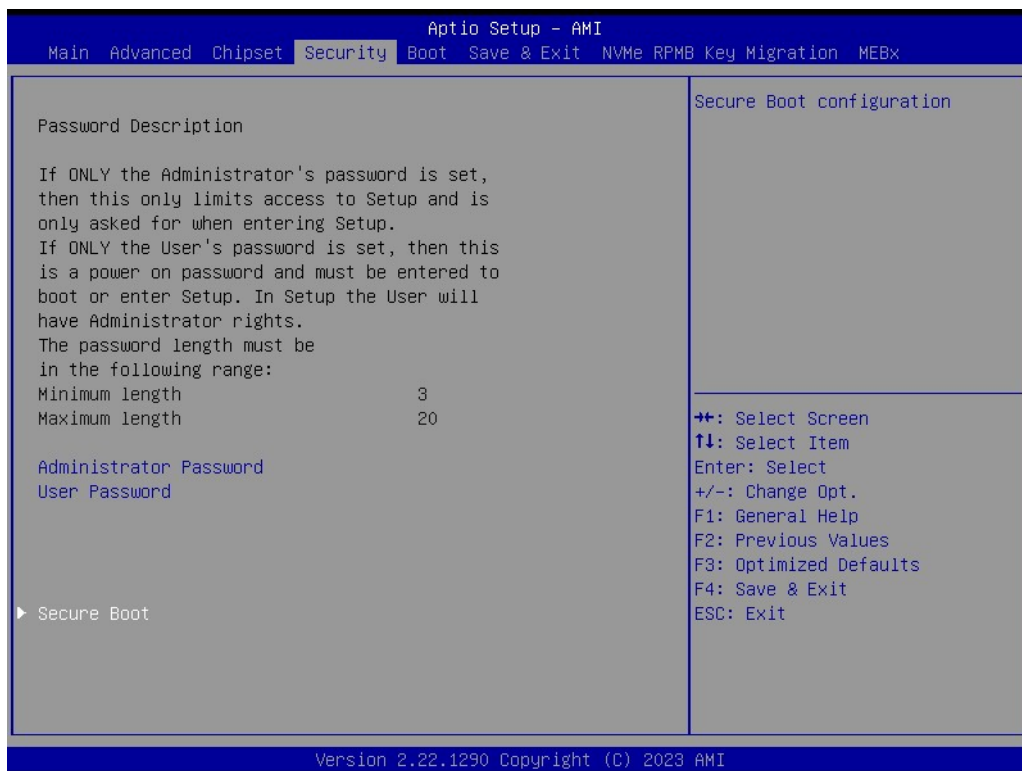
## ■ HD Audio Configuration



- HD Audio  
Control Detection of the HD-Audio device.

## 3.2.4 Security

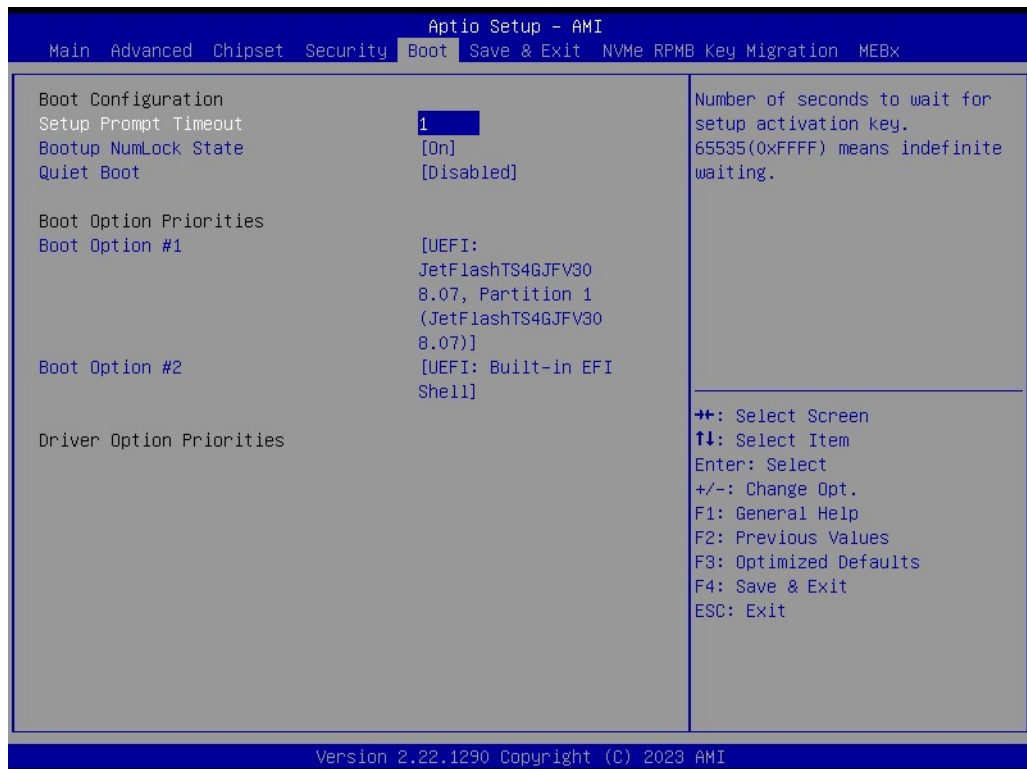




- **Administrator Password**  
Set Administrator Password
- **User Password**  
Set User Password
- **Secure Boot Mode**  
Secure Boot mode options: Standard or Custom.

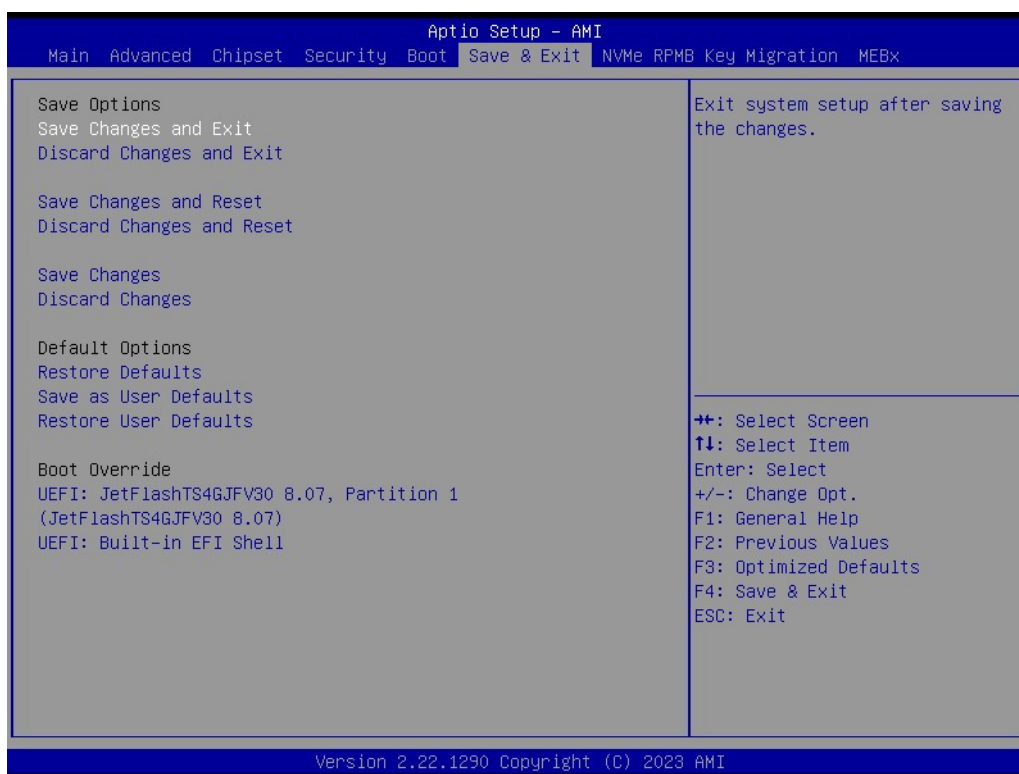
- **Restore Factory Keys**  
Force System to User Mode. Install factory default Secure Boot key databases
- **Reset To Setup Mode**  
Delete all Secure Boot key databases from NVRAM
- **Key Management**  
Enables expert users to modify Secure Boot Policy variables without variable authentication.

### 3.2.5 Boot



- **Setup Prompt Timeout**  
Number of seconds to wait for setup activation key. 65535 (0xFFFF) means indefinite waiting.
- **Bootup NumLock State**  
Select the keyboard NumLock state.
- **Quiet Boot**  
Enable/Disable Quiet Boot option.

### 3.2.6 Save & Exit



- **Save Changes and Exit**  
Exit system setup after saving the changes.
- **Discard Changes and Exit**  
Exit system setup without saving any changes.
- **Save Changes and Reset**  
Reset the system after saving the changes.
- **Discard Changes and Reset**  
Reset system setup without saving any changes.
- **Save Changes**  
Save Changes done so far to any of the setup options.
- **Discard Changes->Discard Changes done so far to any of the setup options**
- **Restore Defaults**  
Restore/Load Default values for all the setup options.
- **Save as User Defaults**  
Save the changes done so far as User Defaults.
- **Restore User Defaults**  
Restore the User Defaults to all the setup options.

## 3.2.7 MEBx



- **MEBx**  
Set ME configuration.



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