Approval Sheet

Customer	
Product Number	**ACT8GHR72P8J1333S-LV**
Module speed	**PC3-10600**
Pin	**240pin**
Cl-tRCD-tRP	**9-9-9**
Date	**27th June 2018**

ACT8GHR72P8J1333S-LV

8GB DDR3L-1333 Registered ECC Module Specification

Description

ACT8GHR72P8J1333S-LV is a high speed 8GB DDR3L-1333 Registered ECC DIMM. It is designed for mission critical application memory solution. This DIMM includes Error Checking and Correcting (ECC) for maximum reliability. The modules is constructed using 512Mx8 SDRAMs, and is fully compliant with JEDEC specifications. Decoupling capacitors are mounted on the PCB board for better signal integrity. The DIMM feature serial presence detect (SPD) based on a serial EEPROM device using the 2-pin I2C protocol.

Features

- 240-pin Registered Dual Inline Memory Module (RDIMM)
- Memory Module Organization 1Gx72
- Height: 30 mm
- CL-tRCD-tRP : 9-9-9
- JEDEC standard 1.5V (± 0.075V)
- VDDQ = 1.5V (± 0.075V)
- 8 independent internal bank
- Burst Length: 4, 8(Interleave/nibble sequential)
- Bi-directional Differential Data-Strobe
- On Die Termination (ODT)
- Eight-bit prefetch architecture
- Average Refresh Period 7.8us at lower than a T_{CASE} 85°C, 3.9us at 85°C < TCASE < 95 °C
- Programmable CAS Latency: 6,7,8,9
- RoHS Compliant

Address Range

Module Organization	Row address	Column Address	Bank Address	Auto Precharge
1Gx72	A0-A15	A0-A9	BA0-BA2	A10/AP

Pin Description

Pin Name	Description	Number	Pin Name	Description	Number
CK0	Clock Inputs, positive line	1	ODT[1:0]	On-die termination control	2
/CK0	Clock inputs, negative line	1	DQ[63:0]	Data Input/Output	64
CK1	Clock Inputs, positive line	1	CB[7:0]	Data check bits Input/Output	8
/CK1	Clock inputs, negative line	1	DQS[8:0]	Data strobes	9
CKE[1:0]	Clock Enables	2	/DQS[8:0]	Data strobes, negative line	9
/RAS	Row Address Strobe	1	DM[8:0] DQS[17:9], TDQS[17:9]	Data Masks / Data strobes, Termination data strobes	9
/CAS	Column Address Strobe	1	/DQS[17:9] /TDQS[17:9]	Data strobes, negative line, Termination data strobes	9
/WE	Write Enable	1	/EVENT	Reserved for optional hardware temperature sensing	1
/S[3:0]	Chip Selects	4	TEST	Memory bus test tool (Not Connected and Not Useable on DIMMs)	1
A[9:0],A11, A[15:13]	Address Inputs	14	/RESET	Register and SDRAM control pin	1
A10,AP	Address Input/Autoprecharge	1	VDD	Power Supply	22
A12,/BC	Address Input/Burst chop	1	VSS	Ground	59
BA[2:0]	SDRAM Bank Address	3	VREFDQ	Reference Voltage for DQ	1
SCL	Serial Presence Detect (SPD) Clock Input	1	VREFCA	Reference Voltage for CA	1
SDA	SPD Data Input/Output	1	VTT	Termination voltage	4
SA[2:0]	SPD Address Inputs	3	VDDSPD	SPD Power	1
Par_In	Parity bit for the Address and Control bus	1			
/Err_Out	Parity error found on the Address and Control bus	1			

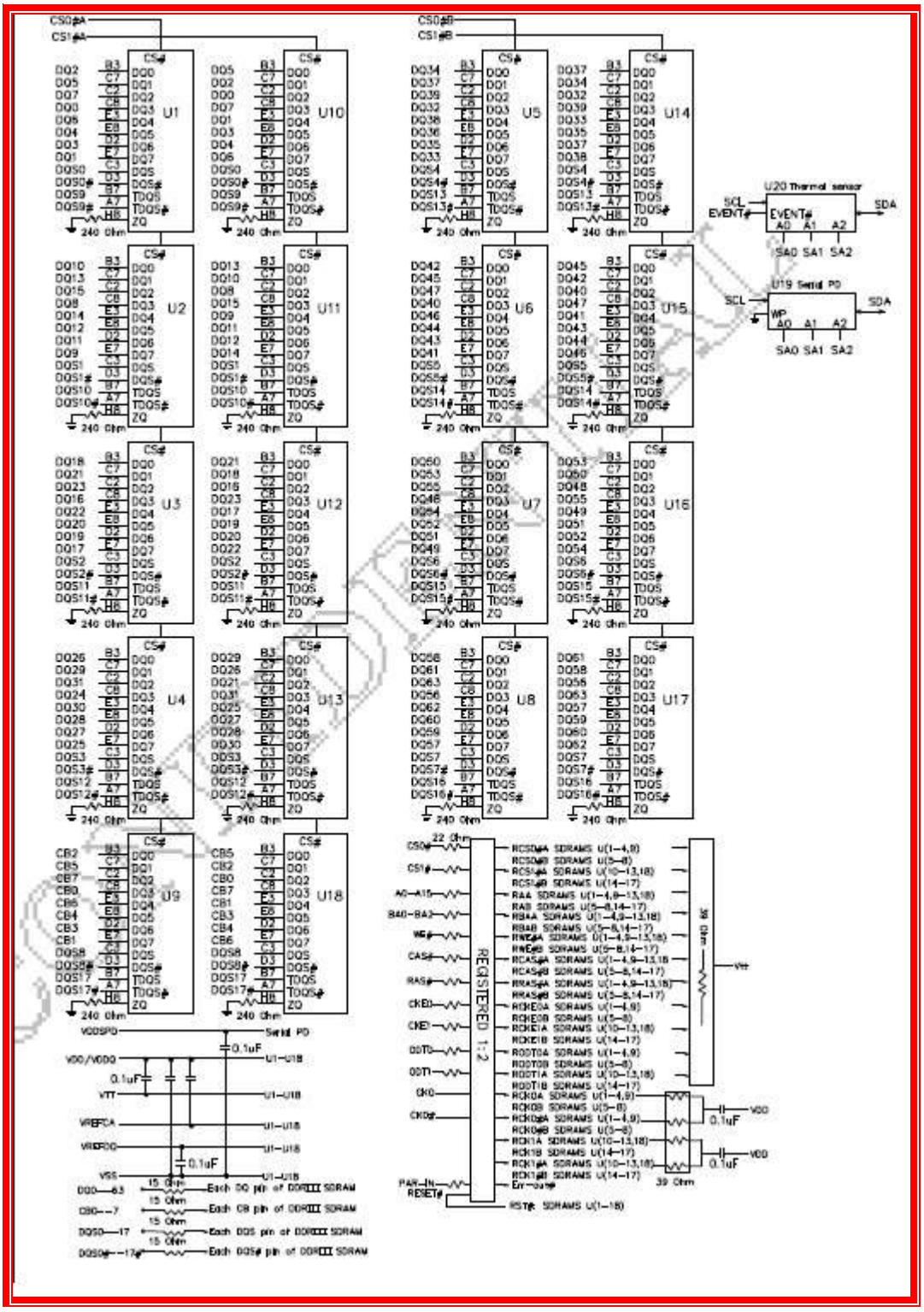
Pin Configuration (Front side/Back side)

Front								Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol
1	VREFDQ	31	DQ25	61	A2	91	DQ41	121	VSS	151	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	152	DM3/ TDQS12	182	VDD	212	DM5/ TDQS14
3	DQ0	33	/DQS3	63	NC,CK1	93	/DQS5	123	DQ5	153	NC, /TDQS12	183	VDD	213	NC, /TDQS14
4	DQ1	34	DQS3	64	NC,/CK1	94	DQS5	124	VSS	154	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0/ TDQS9	155	DQ30	185	/CK0	215	DQ46
6	/DQS0	36	DQ26	66	VDD	96	DQ42	126	NC, /TDQS9	156	DQ31	186	VDD	216	DQ47
7	DQS0	37	DQ27	67	VREFCA	97	DQ43	127	VSS	157	VSS	187	/EVENT	217	VSS
8	VSS	38	VSS	68	Par_In	98	VSS	128	DQ6	158	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	159	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	VSS	160	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0	101	VSS	131	DQ12	161	DM8/ TDQS17	191	VDD	221	DM6/ TDQS15
12	DQ8	42	/DQS8	72	VDD	102	/DQS6	132	DQ13	162	NC, /TDQS17	192	/RAS	222	NC, /TDQS15
13	DQ9	43	DQS8	73	/WE	103	DQS6	133	VSS	163	VSS	193	/S0	223	VSS
14	VSS	44	VSS	74	/CAS	104	VSS	134	DM1/ TDQS10	164	CB6	194	VDD	224	DQ54
15	/DQS1	45	CB2	75	VDD	105	DQ50	135	NC, /TDQS10	165	CB7	195	ODT0	225	DQ55
16	DQS1	46	CB3	76	/S1	106	DQ51	136	VSS	166	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1	107	VSS	137	DQ14	167	NC	197	VDD	227	DQ60
18	DQ10	48	VTT	78	VDD	108	DQ56	138	DQ15	168	/RESET	198	/S3	228	DQ61
19	DQ11	49	VTT	79	/S2	109	DQ57	139	VSS	169	CKE1	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ36	230	DM7/ TDQS16
21	DQ16	51	VDD	81	DQ32	111	/DQS7	141	DQ21	171	A15	201	DQ37	231	NC, /TDQS16
22	DQ17	52	BA2	82	DQ33	112	DQS7	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	/Err_Out	83	VSS	113	VSS	143	DM2/ TDQS11	173	VDD	203	DM4/ TDQS13	233	DQ62
24	/DQS2	54	VDD	84	/DQS4	114	DQ58	144	NC, /TDQS11	174	A12	204	NC, /TDQS13	234	DQ63
25	DQS2	55	A11	85	DQS4	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDDSPD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A5	88	DQ35	118	SCL	148	VSS	178	A6	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	SA2	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

Ordering Information

DDR3L RDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
ACT8GHR72P8J1333S-LV	8GB	PC3-10600	1Gx72	18	2	Y

Block Diagram



IDD Specification Parameter

(IDD values are for full operating range of Voltage and Temperature)
Reference only

Symbol	Proposed Conditions	Value	Units
IDD0	**Operating one bank active-precharge current;** CKE: High; External clock: On; tCK, nRC, nRAS, CL; BL: 8[a]; AL: 0; CS: High between ACT and PRE; Command, Address, Bank Address Inputs: partially toggling ; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Pattern Details	522	mA
IDD1	**Operating one bank active-read-precharge current;** CKE: High; External clock: On; tCK, nRC, nRAS, nRCD, CL; BL: 8[a]; AL: 0; CS: High between ACT, RD and PRE; Command, Address, Bank Address Inputs, Data IO: partially toggling ; DM:stable at 0; Bank Activity: Cycling with one bank active at a time: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0;	720	mA
IDD2P0	**Precharge power-down current;** CKE: Low; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO:MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Slow Exit	198	mA
IDD2P1	**Precharge power-down current;** CKE: Low; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO:MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0; Precharge Power Down Mode: Fast Exit	198	mA
IDD2Q	**Precharge quiet standby current;** CKE: High; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO: MID-LEVEL; DM:stable at 0;Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	216	mA
IDD2N	**Precharge standby current;** CKE: High; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0; Bank Activity: all banks closed; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	234	mA
IDD3P	**Active power-down current;** CKE: Low; External clock: On; tCK, CL: AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: stable at 0; Data IO:MID-LEVEL;DM:stable at 0; Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	198	mA
IDD3N	**Active standby current;** CKE: High; External clock: On; AL: 0; CS: stable at 1; Command, Address, Bank Address Inputs: partially toggling; Data IO: MID-LEVEL; DM:stable at 0;Bank Activity: all banks open; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	378	mA
IDD4W	**Operating burst write current;** CKE: High; External clock: On; AL: 0; CS: High between WR; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless write data burst with different data between one burst and the next one; DM: stable at 0; Bank Activity: all banks open, WR commands cycling through banks: 0,0,1,1,2,2,... ; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at HIGH	1170	mA
IDD4R	**Operating burst read current;** CKE: High; External clock: On; AL: 0; CS: High between RD; Command, Address, Bank Address Inputs: partially toggling; Data IO: seamless read data burst with different data between one burst and the next one; DM:stable at 0; Bank Activity: all banks open, RD commands cycling through banks: 0,0,1,1,2,2,...; Output Buffer and RTT: Enabled in Mode Registers; ODT Signal: stable at 0	1170	mA
IDD5B	**Burst refresh current;** CKE: High; External clock: On; AL: 0; CS: High between REF; Command, Address, Bank Address Inputs: partially toggling ; Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: REF command every nRFC ; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	3600	mA
IDD6	**Self refresh current;** TCASE: 0 - 85°C; Auto Self-Refresh (ASR): Disabled[d]; Self-Refresh Temperature Range (SRT): Normal[e]; CKE: Low; External clock: Off; CK and CK: LOW; AL: 0; CS, Command, Address, Bank Address, Data IO: MID-LEVEL;DM:stable at 0; Bank Activity: Self-Refresh operation; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: MID-LEVEL	270	mA
IDD7	**Operating bank interleave read current;** CKE: High; External clock: On; AL: CL-1; CS: High between ACT and RDA; Command, Address, Bank Address Inputs: partially toggling; Data IO: read data bursts with different data between one burst and the next one; DM:stable at 0; Bank Activity: two times interleaved cycling through banks (0, 1, ...7) with different addressing; Output Buffer and RTT: Enabled in Mode Registers[b]; ODT Signal: stable at 0	2358	mA
IDD8	**RESET Low Current** RESET : Low; External clock : off; CK and CK : LOW; CKE : FLOATING ; CS, Command, Address, Bank Address, Data IO : FLOATING ; ODT Signal : FLOATING	270	mA

Absolute Maximum DC ratings

Symbol	Parameter	Rating	Units	Notes
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}	-0.4V ~ 1.80V	V	1,3
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}	-0.4V ~ 1.80V	V	1,3
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}	-0.4V ~ 1.80V	V	1
T_{STG}	Storage Temperature	-55 ~ +100	^{0}C	1, 2

Note:
1) Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2) Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.
3) 3. V_{DD} and V_{DDQ} must be within 300mV of each other at all times;and V_{REF} must be not greater than 0.6 x V_{DDQ}, When V_{DD} and V_{DDQ} are less than 500mV; V_{REF} may be equal to or less than 300mV.

AC and DC Operating Conditions

Recommended DC Operating Conditions

Symbol	Parameter	Rating			Units	Notes
		Min.	Typ.	Max.		
V_{DD}	Supply Voltage	1.283	1.35	1.45	V	1,2
V_{DDQ}	Supply Voltage for Output	1.283	1.35	1.45	V	1,2
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage for Output	1.425	1.5	1.575	V	1,2

Note :
1) Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2) V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together.

Input/Output Capacitance

Symbol	Parameter	Max.	Units
C_{CK}	Input capacitance, CK and /CK	1.4	pF
C_I	Input capacitance (All other input only pins)	1.2	
C_{ZQ}	Input/output capacitance of ZQ pin	3	
C_{IO}	Input/output capacitance (DQ, DM, DQS, /DQS, TDQS, /TDQS)	2.2	

Timing Parameters

Symbol	Parameter	PC3-10600		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.5	<1.875	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-80	80	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-70	70	Ps
JIT (CC)	Cycle to Cycle Period Jitter	160		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	140		Ps
TERR (2per)	Cumulative error across 2 cycle	-118	118	Ps
TERR (3per)	Cumulative error across 3 cycle	-140	140	Ps
TERR (4per)	Cumulative error across 4 cycle	-155	155	Ps
TERR (5per)	Cumulative error across 5 cycle	-168	168	Ps
TERR (6per)	Cumulative error across 6 cycle	-177	177	Ps
TERR (7per)	Cumulative error across 7 cycle	-186	186	Ps
TERR (8per)	Cumulative error across 3 cycle	-193	193	Ps
TERR (9per)	Cumulative error across 4 cycle	-200	200	Ps
TERR (10per)	Cumulative error across 5 cycle	-205	205	Ps
TERR (11per)	Cumulative error across 6 cycle	-210	210	Ps

TERR (12per)	Cumulative error across 7 cycle	-215	215	Ps
TERR (nper)	Cumulative error across 13~50 cycle	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max		Ps
Data Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDQSQ	DQS, DQS# to DQ skew, per group, per access	-	125	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-500	250	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	250	Ps
1.35V				
tDS(base) AC160	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC135		45	-	Ps
tDS(base) AC125		-	-	Ps
tDH(base) DC90	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	75	-	Ps
1.5V				
tDS(base) AC175	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	-	-	Ps
tDS(base) AC150		30	-	Ps
tDS(base) AC135		-	-	Ps
tDH(base) DC100	Data hold time from DQS, DQS# referenced to VIH(DC)VIL(DC) levels	65	-	Ps
Data Strobe Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)

tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSCK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps
tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-500	250	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	250	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.45	0.55	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.45	0.55	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.25	0.25	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.2	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.2	-	tCK(avg)
Command and Address Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			

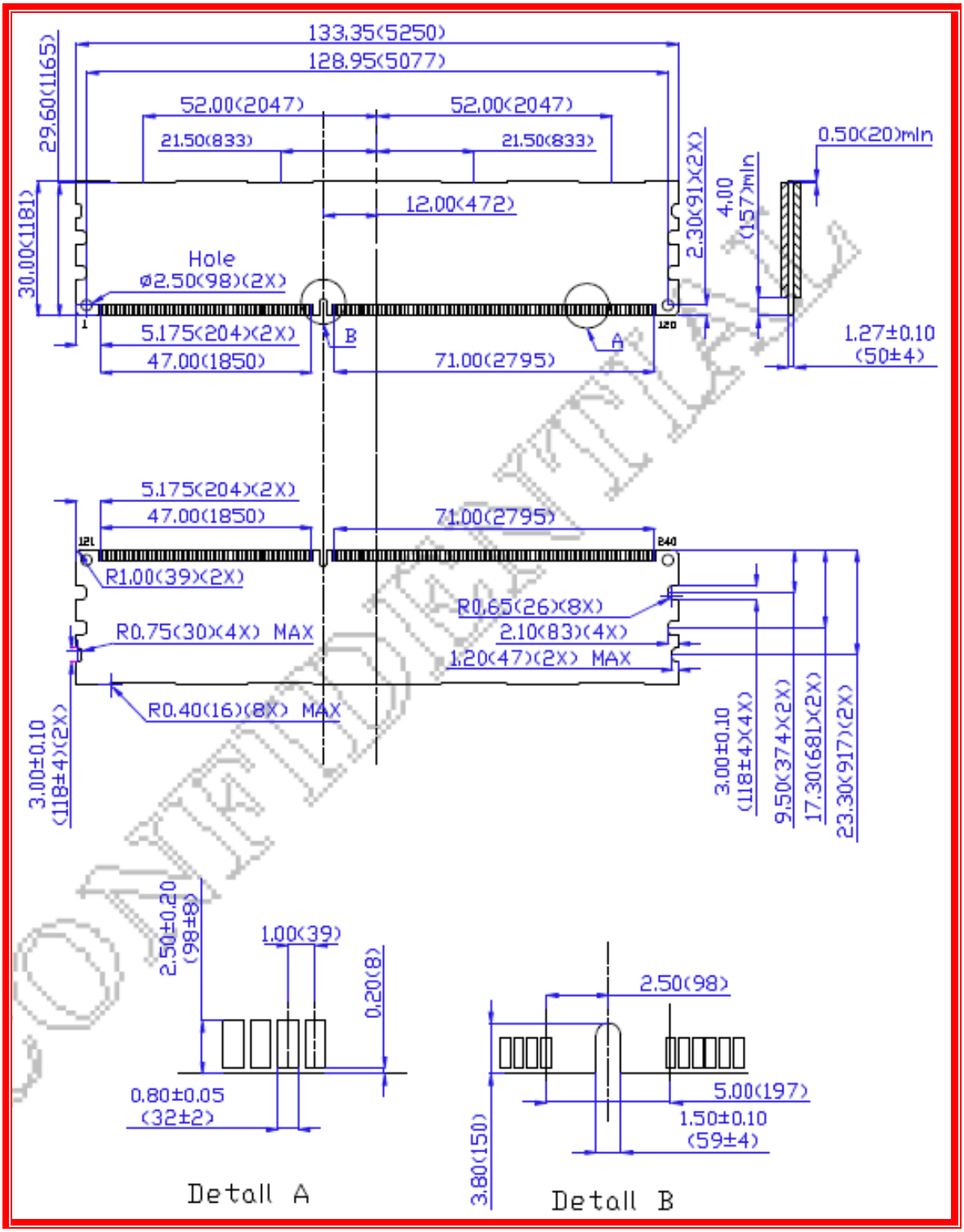
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK
tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	36	9 tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	45	-	ns
1.35V				
tIS(base) AC160	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	80	-	Ps
tIS(base) AC135		205	-	Ps
tIS(base) AC125		-	-	Ps
tIH(base) DC90	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	150	-	Ps
1.5V				
tIS(base) AC175	Command and Address setup time to CK, CK# referenced to VIH(AC) / VIL(AC) levels	65	-	Ps
tIS(base) AC150		190	-	Ps
tIS(base) AC135		-	-	Ps
tIS(base) AC125		-	-	Ps
tIH(base) DC100	Command and Address hold time from CK, CK# referenced to VIH(DC) / VIL(DC) levels	140	-	Ps

Calibration Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tZQinit	Power-up and RESET calibration time	512	-	nCK
tZQoper	Normal operation Full calibration time	256	-	nCK
tZQCS	Normal operation Short calibration time	64	-	nCK
Reset Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK,tRFC+10ns)	-	
Self Refresh Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC+10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE9min)+1tCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK,10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK,10ns)	-	
Power Down Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	

tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10 nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK,5.625 ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCKE(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK
tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(min)	-	nCK
ODT Timings				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK

tAONPD	Asynchronous RTT turn-on delay (Powe-Down with DLL frozen)	2	8.5	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	2	8.5	ns
tAON	RTT-turn-on	-250	250	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.3	0.7	tCK(avg)
Write Leveling Timing				
Symbol	**Parameter**	**Min.**	**Max.**	**Unit**
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	195	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	195	-	ps
tWLO	Write leveling output delay	0	9	ns
tWLOE	Write leveling output error	0	2	ns

Physical Dimension



Note: All dimensions are in millimeters (mils) and should be kept within a tolerance of ±0.15 (6), unless otherwise specified.

RoHS Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: http://www.innodisk.com/

RoHS 自我宣告書 (RoHS Declaration of Conformity)

Manufacturer Product: All Innodisk EM Flash and Dram products

一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。

Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。

Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
鉛 (Pb)	< 1000 ppm
汞 (Hg)	< 1000 ppm
鎘 (Cd)	< 100 ppm
六價鉻 (Cr 6+)	< 1000 ppm
多溴聯苯 (PBBs)	< 1000 ppm
多溴二苯醚 (PBDEs)	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯 (DEHP)	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯 (BBP)	< 1000 ppm
鄰苯二甲酸二丁酯 (DBP)	< 1000 ppm
鄰苯二甲酸二異丁酯 (DIBP)	< 1000 ppm

立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Randy Chien 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2017 / 01 / 18

Revision Log

Rev	Date	Modification
0.1	27th June 2018	Preliminary Edition
1.0	27th June 2018	Official released.