

# Approval Sheet

Customer	
Product Number	M3UW-8GSSACN9-D
Module speed	PC3-10600
Pin	240 pin
CI-tRCD-tRP	9-9-9
DRAM Operating Temp	0°C ~85°C
Date	28 <sup>th</sup> August 2014

Approval by Customer

P/N:

Signature:

Date:

Sales: \_\_\_\_\_ Sr. Technical Manager: John Hsieh

Rev 1.0

## 1. Features

### Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)
		CL=7	CL=9	CL=11			
PC3-10600	N	1066	1333	1333	13.5	13.5	13.5

- JEDEC Standard 240-pin Dual In-Line Memory Module
- Intend for PC3-1333 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt (-0.075/+0.1V)
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- Golden Connector (Au:30u")
- 8 bit pre-fetch
- Two different termination values (Rtt\_Nom & Rtt\_WR)
- Auto & self refresh 7.8μs (TA ≤ +85°C)
- 16/10/2 Addressing (row/column/rank)-8GB
- SDRAM operating temperature range 0°C ≤ TA ≤ +85°C
- Programmable Device Operation:
  - Burst Type: Sequential or Interleave
  - Device CAS# Latency: 7, 9, 11
  - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant (*Section 13*)

## 2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
<b>TOPR</b>	Operating Temperature (ambient)	0 to +85	°C	1
<b>TSTG</b>	Storage Temperature	-50 to +100	°C	
<b>HOPR</b>	Operating Humidity (relative)	10 to 90	%	
<b>HSTG</b>	Storage Humidity (without condensation)	5 to 95	%	
<b>PBAR</b>	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.  
 2. Up to 9850 ft.

## 3. DRAM Parameters by device density

RTT_Nom Setting	Parameter	4Gb	Units
tRFC	REF command ACT or REF command time	260	ns
tREFI	Average periodic refresh interval	0°C ≤ Tcase ≤ 85°C	7.8 μs
		85°C ≤ Tcase ≤ 95°C	3.9 μs

#### 4. Ordering Information

DDR3 UDIMM						
Part Number	Density	Speed	DIMM Organization	Number of DRAM	Number of rank	ECC
<b>M3UW-8GSSACN9-D</b>	8GB	PC3-10600	1Gx64	16	2	N

## 5. Pin Configurations (Front side/Back side)

X64 UDIMM

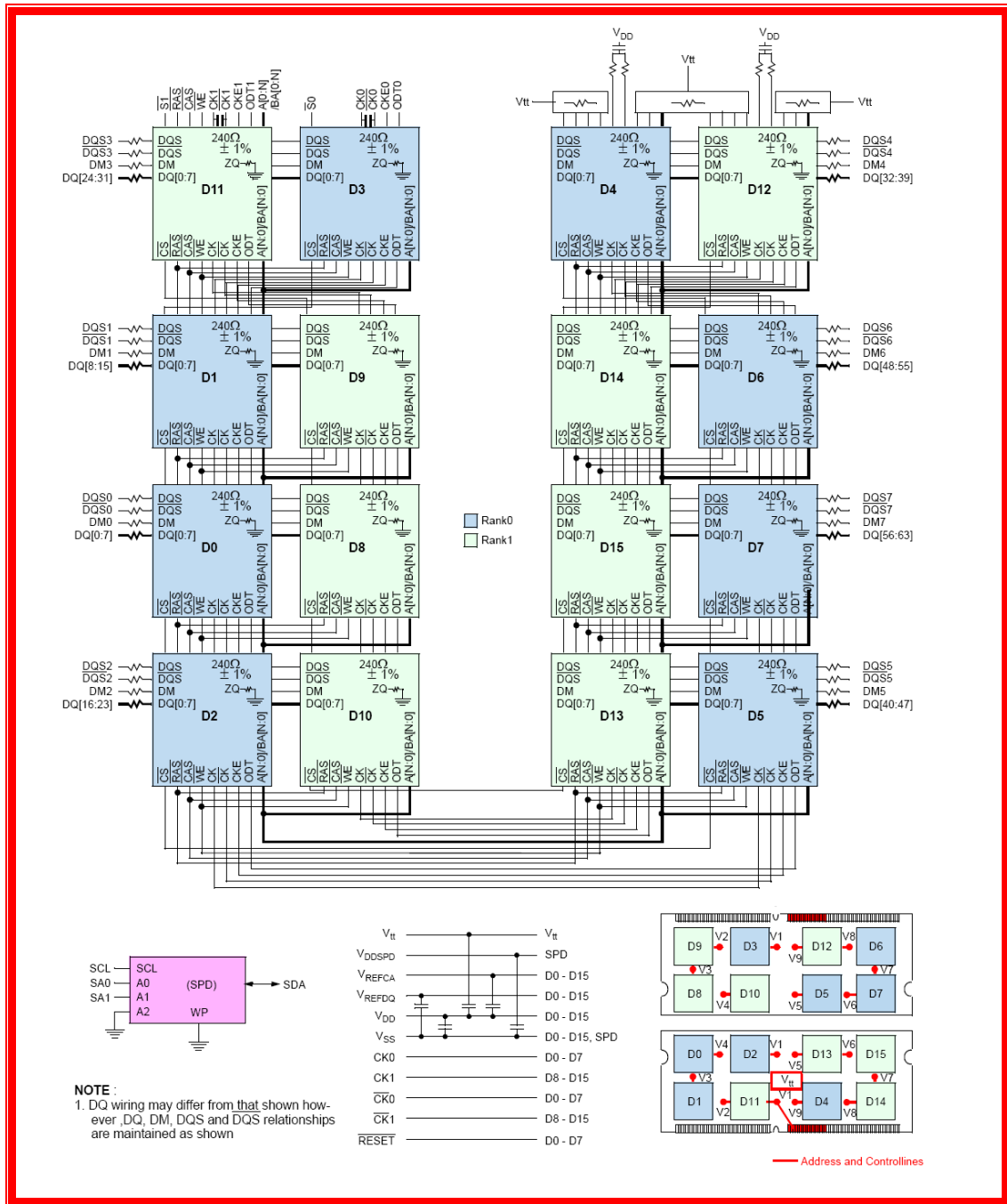
DDRIII-240pins DIMM Front								DDRIII-240pins DIMM Back							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	31	DQ26	61	A2	91	DQ41	121	VSS	161	VSS	181	A1	211	VSS
2	VSS	32	VSS	62	VDD	92	VSS	122	DQ4	162	DM3	182	VDD	212	DM6
3	DQ0	33	/DQ33	63	CK1/NC	93	/DQ35	123	DQ6	163	NC	183	VDD	213	NC
4	DQ1	34	DQ33	64	/CK1/NC	94	DQ35	124	VSS	164	VSS	184	CK0	214	VSS
5	VSS	35	VSS	65	VDD	95	VSS	125	DM0	165	DQ30	185	/CK0	215	DQ48
6	/DQ30	36	DQ28	66	VDD	96	DQ42	126	NC	166	DQ31	186	VDD	216	DQ47
7	DQ30	37	DQ27	67	VREFCA	97	DQ43	127	VSS	167	VSS	187	NC	217	VSS
8	VSS	38	VSS	68	NC	98	VSS	128	DQ6	168	CB4	188	A0	218	DQ52
9	DQ2	39	CB0	69	VDD	99	DQ48	129	DQ7	169	CB5	189	VDD	219	DQ53
10	DQ3	40	CB1	70	A10	100	DQ49	130	VSS	180	VSS	190	BA1	220	VSS
11	VSS	41	VSS	71	BA0/BA1	101	VSS	131	DQ12	181	DM8	191	VDD	221	DM8
12	DQ8	42	NC, /DQ38	72	VDD	102	/DQ38	132	DQ13	182	NC	192	RA3	222	NC
13	DQ9	43	NC DQ38	73	WE	103	DQ38	133	VSS	183	VSS	193	C30	223	VSS
14	VSS	44	VSS	74	CA3	104	VSS	134	DM1	184	CB8	194	VDD	224	DQ54
15	/DQ31	45	CB2	75	VDD	105	DQ50	135	NC	185	CB7	195	ODT0	225	DQ56
16	DQ31	46	CB3	76	CS1	106	DQ51	136	VSS	186	VSS	196	A13	226	VSS
17	VSS	47	VSS	77	ODT1	107	VSS	137	DQ14	187	NC,TEST	197	VDD	227	DQ60
18	DQ10	48	NC	78	VDD	108	DQ58	138	DQ15	188	RESET	198	NC	228	DQ61
19	DQ11	49	NC	79	NC/SA2	109	DQ57	139	VSS	189	NC CKE1	199	VSS	229	VSS
20	VSS	50	CKE0	80	VSS	110	VSS	140	DQ20	170	VDD	200	DQ38	230	DM7
21	DQ16	51	VDD	81	DQ32	111	/DQ37	141	DQ21	171	A15/BA3	201	DQ37	231	NC
22	DQ17	52	BA2	82	DQ33	112	DQ37	142	VSS	172	A14	202	VSS	232	VSS
23	VSS	53	NC	83	VSS	113	VSS	143	DM2	173	VDD	203	DM4	233	DQ62
24	/DQ32	54	VDD	84	/DQ34	114	DQ58	144	NC	174	A12/NC	204	NC	234	DQ63
25	DQ32	55	A11	85	DQ34	115	DQ59	145	VSS	175	A9	205	VSS	235	VSS
26	VSS	56	A7	86	VSS	116	VSS	146	DQ22	176	VDD	206	DQ38	236	VDD3PD
27	DQ18	57	VDD	87	DQ34	117	SA0	147	DQ23	177	A8	207	DQ39	237	SA1
28	DQ19	58	A6	88	DQ36	118	SCL	148	VSS	178	A8	208	VSS	238	SDA
29	VSS	59	A4	89	VSS	119	VSS	149	DQ28	179	VDD	209	DQ44	239	VSS
30	DQ24	60	VDD	90	DQ40	120	VTT	150	DQ29	180	A3	210	DQ45	240	VTT

## 6. Architecture

### Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	V <sub>DD</sub>	Power Supply
/WE	SDRAM write enable	V <sub>DDID</sub>	V <sub>DD</sub> Identification Flag
/S0 - /S1	DIMM Rank Select Lines	V <sub>DDQ</sub>	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	V <sub>REFDQ</sub>	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	V <sub>REFCA</sub>	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	V <sub>SS</sub>	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	V <sub>DDSPD</sub>	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	V <sub>TT</sub>	SDRAM I/O termination supply.

### 7. Function Block Diagram: - (8GB, 2 Ranks 512Mx8 DDR3 SDRAMs)



## 8. SDRAM Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note	
T <sub>OPER</sub>	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T <sub>STG</sub>	Storage Temperature	-55 to 100	°C	4,5	
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pins relative to V <sub>ss</sub>	-0.4 to +1.975	V	4	
V <sub>DD</sub>	Voltage on VDD supply relative to V <sub>ss</sub>	-0.4 to +1.975	V	4,6	
V <sub>DDQ</sub>	Voltage on VDDQ supply relative to V <sub>ss</sub>	-0.4 to +1.975	V	4,6	

### Note:

1. Operating Temperature T<sub>OPER</sub> is the case surface temperature on the center / top side of the DRAM.

For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

- a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
- b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. V<sub>DD</sub> and V<sub>DDQ</sub> must be within 300 mV of each other at all times;and V<sub>REF</sub> must be not greater than 0.6 x V<sub>DDQ</sub>, When V<sub>DD</sub> and V<sub>DDQ</sub> are less than 500 mV; V<sub>REF</sub> may be equal to or less than 300 mV



## 9. DRAM AC &amp; DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
<b>Recommended DC Operating Conditions</b>						
<b>V<sub>DD</sub></b>	Supply Voltage	1.425	1.5	1.6	V	1,2
<b>V<sub>DDQ</sub></b>	Supply Voltage	1.425	1.5	1.6	V	1,2
<b>Single Ended AC/DC Input Levels</b>						
<b>V<sub>IH</sub> (DC)</b>	DC Input High (Logic1) Voltage	$V_{REF} + 0.1$	-	V <sub>DD</sub>	V	3
<b>V<sub>IL</sub> (DC)</b>	DC Input Low (Logic 0) Voltage	V <sub>SS</sub>	-	$V_{REF} - 0.1$	V	3
<b>V<sub>IH</sub> (AC)</b>	AC Input High (Logic1) Voltage	$V_{REF} + 0.175$	-	-	V	3
<b>V<sub>IL</sub> (AC)</b>	AC Input Low (Logic 0) Voltage	-	-	$V_{REF} - 0.175$	V	3
<b>V<sub>REFDQ</sub> (DC)</b>	Reference Voltage for DQ, DM inputs	0.49V <sub>DDQ</sub>	0.5V <sub>DDQ</sub>	0.51V <sub>DDQ</sub>	V	4,5
<b>V<sub>REFCA</sub> (DC)</b>	Reference Voltage for ADD,CMD inputs	0.49V <sub>DDQ</sub>	0.5V <sub>DDQ</sub>	0.51V <sub>DDQ</sub>	V	4,5
<b>Single Ended AC/DC output Levels</b>						
<b>V<sub>OH</sub> (DC)</b>	DC output high measurement level (for IV curve linearity)	-	0.8 x V <sub>DDQ</sub>	-	V	
<b>V<sub>OM</sub> (DC)</b>	DC output mid measurement level (for IV curve linearity)	-	0.5 x V <sub>DDQ</sub>	-	V	
<b>V<sub>OL</sub> (DC)</b>	DC output low measurement level (for IV curve linearity)	-	0.2 x V <sub>DDQ</sub>	-	V	
<b>V<sub>OH</sub> (AC)</b>	AC output high measurement level (for output SR)	-	$V_{TT} + 0.1 \times V_{DDQ}$	-	V	6
<b>V<sub>OL</sub> (AC)</b>	AC output low measurement level (for output SR)	-	$V_{TT} - 0.1 \times V_{DDQ}$	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
<b>Differential AC/DC Input Levels</b>						
<b>VIHdiff</b>	Differential Input high	+0.2	-	Note 9	V	7
<b>VILdiff</b>	Differential Input logic Low	Note 9	-	-0.2	V	7
<b>VIHdiff(ac)</b>	Differential Input high ac	2* (VIH (AC)- VREF)	-	Note 9	V	8
<b>VILdiff(ac)</b>	Differential Input logic Low ac	Note 9	-	2* (VREF- VIL (AC) )	V	8
<b>Differential AC and DC Output Levels</b>						
<b>VOHdiff(AC)</b>	AC differential output high measurement level (for output SR)	-	+ 0.2 x VDDQ	-	V	10
<b>VOLdiff(AC)</b>	AC differential output low measurement level (for output SR)	-	- 0.2 x VDDQ	-	V	10
<b>Note:</b>						
<ol style="list-style-type: none"> <li>Under all conditions VDDQ must be less than or equal to VDD.</li> <li>VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.</li> <li>For DQ and DM, Vref = VrefDQ. For input only pins except RESET#, Vref = VrefCA.</li> <li>The ac peak noise on VRef may not allow VRef to deviate from VRef(DC) by more than +/-1% VDD (for reference: approx. +/- 15 mV).</li> <li>For reference: approx. VDD/2 +/- 15 mV.</li> <li>The swing of <math>\pm 0.1 \times VDDQ</math> is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of <math>40 \Omega</math> and an effective test load of <math>25 \Omega</math> to <math>V_{TT} = VDDQ/2</math></li> <li>Used to define a differential signal slew-rate.</li> <li>For CK - CK# use VIH/VIL(ac) of ADD/CMD and VREFCA; for DQS - DQS#, DQSL, DQSL#, DQSU, DQSU# use VIH/VIL(ac) of DQs and VREFDQ; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here.</li> <li>These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (VIH(dc) max, VIL(dc)min) for single- ended signals as well as the limitations for overshoot and undershoot.</li> <li>The swing of <math>\pm 0.2 \times VDDQ</math> is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of <math>40 \Omega</math> and an effective test load of <math>25 \Omega</math> to <math>V_{TT} = VDDQ/2</math> at each of the differential outputs.</li> </ol>						

## 10. Operating, Standby, and Refresh Currents

- 8GB SODIMM (2 Ranks, 512Mx8 DDR3 SDRAMs  $T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$ )

Symbol	Parameter/Condition	PC3-8500	Unit
I DD0	One bank; Active - Precharge	520	mA
I DD1	One bank; Active - Read - Precharge	600	mA
I DD2N	Precharge Standby Current	320	mA
I DD2P	Precharge Power Down Current	240	mA
I DD2Q	Precharge Quiet Standby Current	320	mA
I DD3N	Active Standby Current	400	mA
I DD3P	Active Power-Down Current	Fast	320 mA
		Slow	320 mA
I DD4R	Operating Current Burst Read	960	mA
I DD4W	Operating Current Burst Write	1040	mA
I DD5B	Burst Refresh Current	1320	mA
I DD6	Self-Refresh Current: Normal Temperature Range	240	mA
I DD7	Operating Bank Interleave Read Current	1530	mA
IDD8	Reset Low-Current	240	mA

## 11. Timing Parameters

(T<sub>CASE</sub> = 0 °C ~ 70 °C; V<sub>DDQ</sub> = V<sub>DD</sub>, See AC Characteristics)

Symbol	Parameter	PC3-10600		Unit
		Min.	Max.	
<b>Clock Timing</b>				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.5	3.3	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-80	80	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-70	70	Ps
JIT (CC)	Cycle to Cycle Period Jitter	160		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	140		Ps
TJIT (duty)		-	-	Ps
TERR (2per)	Cumulative error across 2 cycle	-118	118	Ps
TERR (3per)	Cumulative error across 3 cycle	-140	140	Ps
TERR (4per)	Cumulative error across 4 cycle	-155	155	Ps
TERR (5per)	Cumulative error across 5 cycle	-168	168	Ps
TERR (6per)	Cumulative error across 6 cycle	-177	177	Ps
TERR (7per)	Cumulative error across 7 cycle	-186	186	Ps
TERR (8per)	Cumulative error across 3 cycle	-193	193	Ps
TERR (9per)	Cumulative error across 4 cycle	-200	200	Ps
TERR (10per)	Cumulative error across 5 cycle	-205	205	Ps

TERR (11per)	Cumulative error across 6 cycle	-210	210	Ps
TERR (12per)	Cumulative error across 7 cycle	-215	215	Ps
TERR (nper)	Cumulative error across 13~50 cycle	$tERR(nper)min = (1 + 0.68ln(n)) *$ $tJIT(per)min$ $tERR(nper)max = (1 + 0.68ln(n)) *$ $tJIT(per)max$		Ps
<b>Data Timing</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tDSQ	DQS, DQS# to DQ skew, per group, per access	-	125	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-500	250	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	250	Ps
tDS(base) AC150	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	30	-	Ps
tDH(base) DC 100	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	65	-	Ps
<b>Data Strobe Timing</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tRPRE	DQS, DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps

tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.4	0.6	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.4	0.6	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.25	0.25	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.2	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.2	-	tCK(avg)
<b>Command and Address Timing</b>				
Symbol	Parameter	Min.	Max.	Unit
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK

tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	36	9 tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	45	-	ns
tIS (base)	Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	65		ns
tIH(base)	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	140		ps
tIS(base) AC150	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	65+125		ps
<b>Calibration Timing</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tZQinit	Power-up and RESET calibration time	512	-	nCK
tZQoper	Normal operation Full calibration time	256	-	nCK
tZQCS	Normal operation Short calibration time	64	-	nCK
<b>Reset Timing</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK, tRFC(min) + 10ns)	-	
<b>Self Refresh Timings</b>				

Symbol	Parameter	Min.	Max.	Unit
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC(min) +10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE9min) +1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK, ,10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK, ,10ns)	-	
<b>Power Down Timings</b>				
Symbol	Parameter	Min.	Max.	Unit
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK, 5.625ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCK(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK

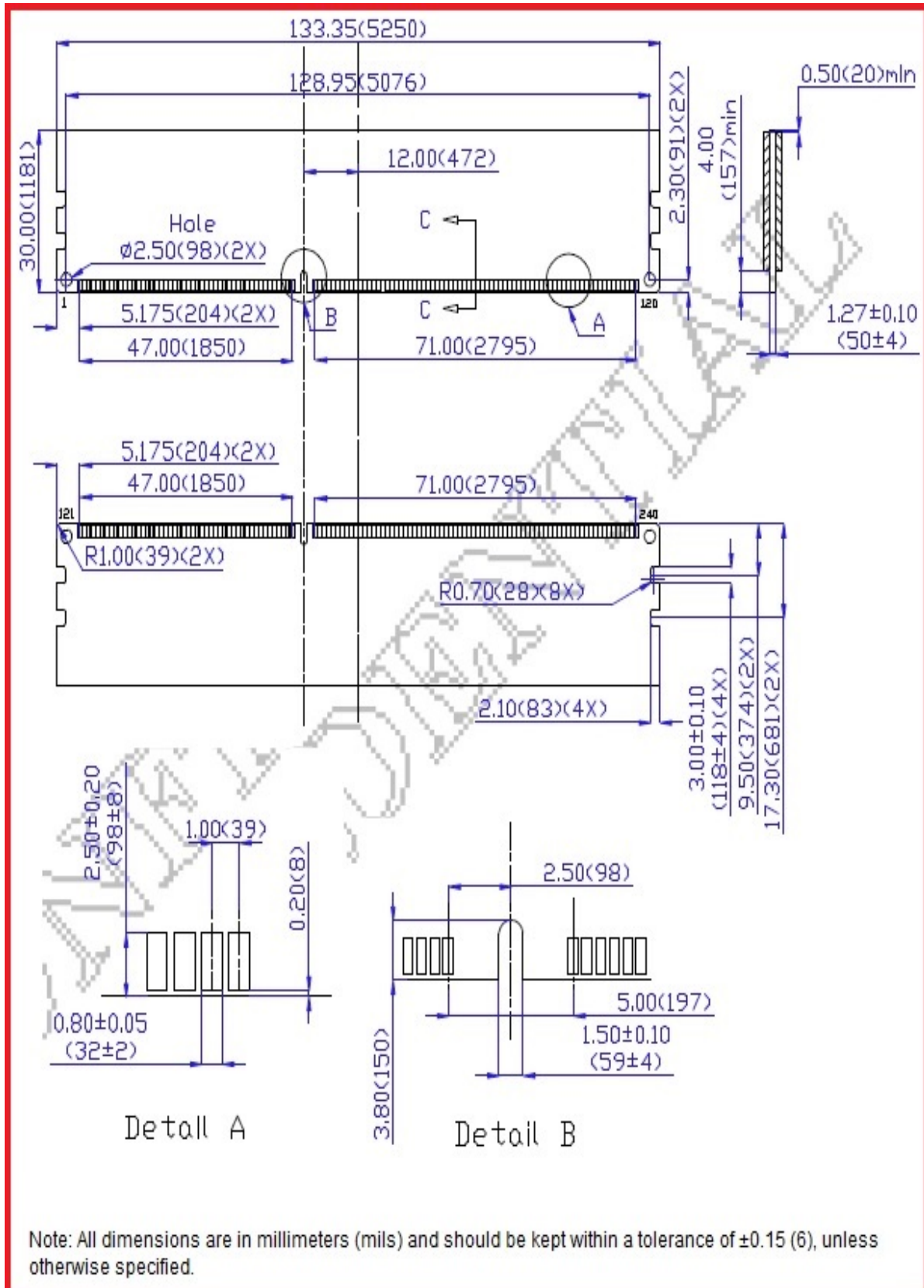


tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg) )	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg) )	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(mi n)	-	nCK
<b>ODT Timings</b>				
<b>Symbol</b>	<b>Parameter</b>	<b>Min.</b>	<b>Max.</b>	<b>Unit</b>
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	1	9	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	1	9	ns
tAON	RTT-turn-on	-250	250	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.30.7		tCK(avg)

Write Leveling Timing				
Symbol	Parameter	Min.	Max.	Unit
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	195	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	195	-	ps
tWLO	Write leveling output delay	0	9	ns
tWLOE	Write leveling output error	0	2	ns

## 12. PACKAGE DIMENSION

- (8GB, 2 Ranks 512Mx8 DDR3 base UDIMM)



### 13. RoHS Declaration



#### Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M3UW-8GSSACN9/-(X) complies with the requirement of RoHS directives 2011/65/EU and 2006/12/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3<sup>rd</sup> party test reports of the component/ raw materials used in the manufacture of products.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI (Cr+6)	< 1000 ppm
Polybromodiphenyl ether (PBDE)	< 1000 ppm
Polybrominated Biphenyls (PBB)	< 1000 ppm
Perfluorooctane Sulfonate (PFOS)	Not Contained

Date issued: 2014/01/22

Manufacturer: : InnoDisk Co., Ltd.  
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Authorized Signature :

QA Dept. Director – Ryan Tsai

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## Revision Log

Rev	Date	Modification
0.1	28 <sup>th</sup> August 2014	Preliminary Edition
1.0	28 <sup>th</sup> August 2014	Official released.