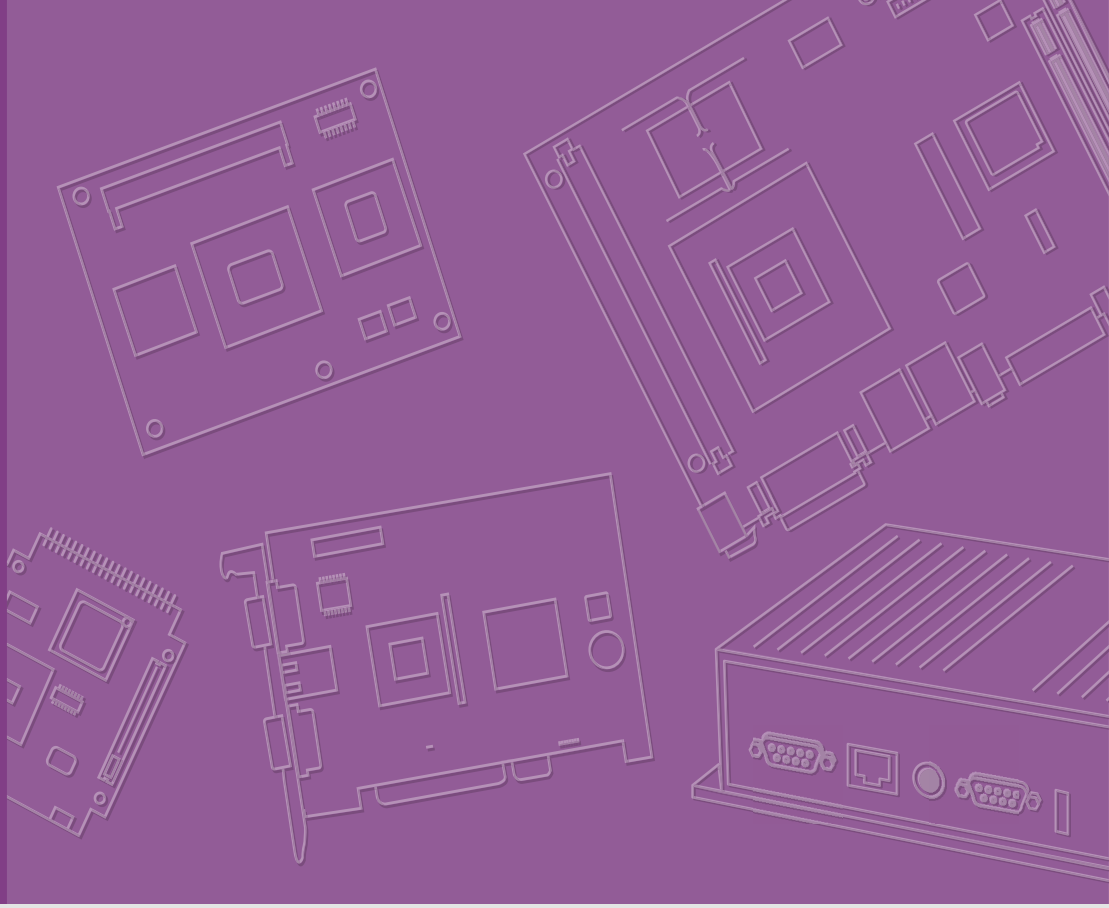


User Manual

SOM-DB5830

Development Board for COM Express® Type 6 Pinout Modules

ADVANTECH

Enabling an Intelligent Planet

Copyright

Acknowledgments

Intel and Pentium are trademarks of Intel Corporation.

Microsoft Windows and MS-DOS are registered trademarks of Microsoft Corp.

All other product names or trademarks are properties of their respective owners.

Product Warranty (2 Years)

Advantech warrants the original purchaser that each of its products will be free from defects in materials and workmanship for two years from the date of purchase.

This warranty does not apply to any products that have been repaired or altered by persons other than repair personnel authorized by Advantech, or products that have been subject to misuse, abuse, accident, or improper installation. Advantech assumes no liability under the terms of this warranty as a consequence of such events.

Because of Advantech's high quality-control standards and rigorous testing, most customers never need to use our repair service. If an Advantech product is defective, it will be repaired or replaced free of charge during the warranty period. For out-of-warranty repairs, customers will be billed according to the cost of replacement materials, service time, and freight. Please consult your dealer for more details.

If you believe your product to be defective, follow the steps outlined below.

1. Collect all the information about the problem encountered. (For example, CPU speed, Advantech products used, other hardware and software used, etc.) Note anything abnormal and list any onscreen messages displayed when the problem occurs.
2. Call your dealer and describe the problem. Please have your manual, product, and any helpful information readily available.
3. If your product is diagnosed as defective, obtain a return merchandise authorization (RMA) number from your dealer. This allows us to process your return more quickly.
4. Carefully pack the defective product, a completed Repair and Replacement Order Card, and a proof of purchase date (such as a photocopy of your sales receipt) into a shippable container. Products returned without a proof of purchase date are not eligible for warranty service.
5. Write the RMA number clearly on the outside of the package and ship the package prepaid to your dealer.

Part No. 2006583003 Edition 4

Printed in Taiwan August 2024

Declaration of Conformity

CE

This product has passed the CE test for environmental specifications when shielded cables are used for external wiring. We recommend the use of shielded cables. This type of cable is available from Advantech. Please contact your local supplier for ordering information.

Test conditions for passing also include the equipment being operated within an industrial enclosure. In order to protect the product from damage caused by electrostatic discharge (ESD) and EMI leakage, we strongly recommend the use of CE-compliant industrial enclosure products.

FCC Class B

This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for assistance.

Technical Support and Assistance

1. Visit the Advantech website at www.advantech.com/support to obtain the latest product information.
2. Contact your distributor, sales representative, or Advantech's customer service center for technical support if you need additional assistance. Please have the following information ready before calling:
   - Product name and serial number
   - Description of your peripheral attachments
   - Description of your software (operating system, version, application software, etc.)
   - A complete description of the problem
   - The exact wording of any error messages

Warnings, Cautions, and Notes

Warning! *Warnings indicate conditions that, if not observed, can result in personal injury.*

Caution! *Cautions are included to help prevent hardware damage and data losses. For example,*

"Batteries are at risk of exploding if incorrectly installed. Do not attempt to recharge, force open, or heat the battery. Replace the battery only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions."

Note! *Notes provide optional additional information.*

Document Feedback

To assist us with improving this manual, we welcome all comments and constructive criticism. Please send all feedback in writing to support@advantech.com.

Selection Guide

Part Number	Description
SOM-DB5830-00A1	COM Express R3.0 development board for Type 6 pinout modules
SOM-DB5830-00A2	COM Express R3.0 development board for Type 6 pinout modules
SOM-DB5830-00A3	COM Express R3.1 development board for Type 6 pinout modules

Pin Description

Advantech provides useful checklists regarding schematic design and layout routing. The schematic checklist provides details about each pin's electrical properties and connection method for various usage scenarios. The layout checklist specifies the layout constraints and recommendations in terms of trace length, impedance, and other necessary information during the design process.

Contact your nearest Advantech office for design documents and advanced technical support.

Packing List

SOM-DB5830-00A1

Part Number	Description	Quantity
SOM-EA10	PCIe x4-to-4 x PCIe x1 riser card	1
SOM-EA00	N/A	N/A
SOM-EA30 A2	N/A	N/A
1700008941	Serial ATA cable 7P/7P, 32cm	2
1701100300	Flat COM port cable	2
1960077251T000	I/O bracket for SOM-DB5830	1
1910001675	Post M2.5 x 4L 2.5 x 5L 2.5 2.1 5 5 Cu Ni	5
1920001128	NUT M D = 5 5 2.1 3 Cu Ni	5

SOM-DB5830-00A2

Part Number	Description	Quantity
SOM-EA10	PCIe x4 to 4 x PCIe x1 riser card	1
SOM-EA00 A3	Type 6 to Type 10 Middle Board Rev. 3.0	1
SOM-EA30 A2	Type 6 Extension Card, Max.16G	1
1700008941	Serial ATA cable 7P/7P, 32cm	2
1701100300	Flat COM port cable	2
1960077251T000	I/O bracket for SOM-DB5830	1
1910001675	Post M2.5 x 4L 2.5 x 5L 2.5 2.1 5 5 Cu Ni	5
1920001128	NUT M D = 5 5 2.1 3 Cu Ni	5

SOM-DB5830-00A3

Part Number	Description	Quantity
SOM-EA00 A4	Type 6 to Type 10 Middle Board Rev. 3.1	1
SOM-EA30 A2	Type 6 Extension Card, Max.16G	1
1700008941	Serial ATA cable 7P/7P, 32 cm	2
1701100300	Flat COM port cable	2
1960077251T000	I/O bracket for SOM-DB5830	1
1910001675	Post M2.5 x 4L 2.5 x 5L 2.5 2.1 5 5 Cu Ni	5
1920001128	NUT M D = 5 5 2.1 3 Cu Ni	5

Safety Instructions

1. Read these safety instructions carefully.
2. Retain this user manual for future reference.
3. Disconnect the equipment from all power outlets before cleaning. Use only a damp cloth for cleaning. Do not use liquid or spray detergents.
4. For pluggable equipment, the power outlet socket must be located near the equipment and easily accessible.
5. Protect the equipment from humidity.
6. Place the equipment on a reliable surface during installation. Dropping or letting the equipment fall may cause damage.
7. The openings on the enclosure are for air convection. Protect the equipment from overheating. Do not cover the openings.
8. Ensure that the voltage of the power source is correct before connecting the equipment to a power outlet.
9. Position the power cord away from high-traffic areas. Do not place anything over the power cord.
10. All cautions and warnings on the equipment should be noted.
11. If the equipment is not used for a long time, disconnect it from the power source to avoid damage from transient overvoltage.
12. Never pour liquid into an opening. This may cause fire or electrical shock.
13. Never open the equipment. For safety reasons, the equipment should be opened only by qualified service personnel.
14. If any of the following occurs, have the equipment checked by service personnel:
    - The power cord or plug is damaged.
    - Liquid has penetrated the equipment.
    - The equipment has been exposed to moisture.
    - The equipment is malfunctioning, or does not operate according to the user manual.
    - The equipment has been dropped and damaged.
    - The equipment shows obvious signs of breakage.
15. Do not leave the equipment in an environment with a storage temperature of below -20°C (-4°F) or above 60°C (140°F) as this may damage the components. The equipment should be kept in a controlled environment.
16. CAUTION: Batteries are at risk of exploding if incorrectly replaced. Replace only with the same or equivalent type as recommended by the manufacturer. Discard used batteries according to the manufacturer's instructions.
17. In accordance with IEC 704-1:1982 specifications, the sound pressure level at the operator's position should not exceed 70 dB (A).

DISCLAIMER: These instructions are provided according to IEC 704-1 standards. Advantech disclaims all responsibility for the accuracy of any statements contained herein.

Safety Precautions - Static Electricity

Follow these simple precautions to protect yourself from harm and the products from damage.

- To avoid electrical shock, always disconnect the power from the PC chassis before manual handling. Do not touch any components on the CPU card or other cards while the PC is powered on.
- Disconnect the power before making any configuration changes. A sudden rush of power after connecting a jumper or installing a card may damage sensitive electronic components.

Contents

Chapter 1

General Information

- Introduction
- Functional Block Diagram

1.1 Introduction

SOM-DB5830 is a new carrier board that complies with PICMG COM.0 Revision 3.0 Type 6 pinouts. The differences in the main features compared with that for COM.0 Revision 2.1 are listed below (refer to PICMG COM.0 Revision 3.0 specifications for further details).

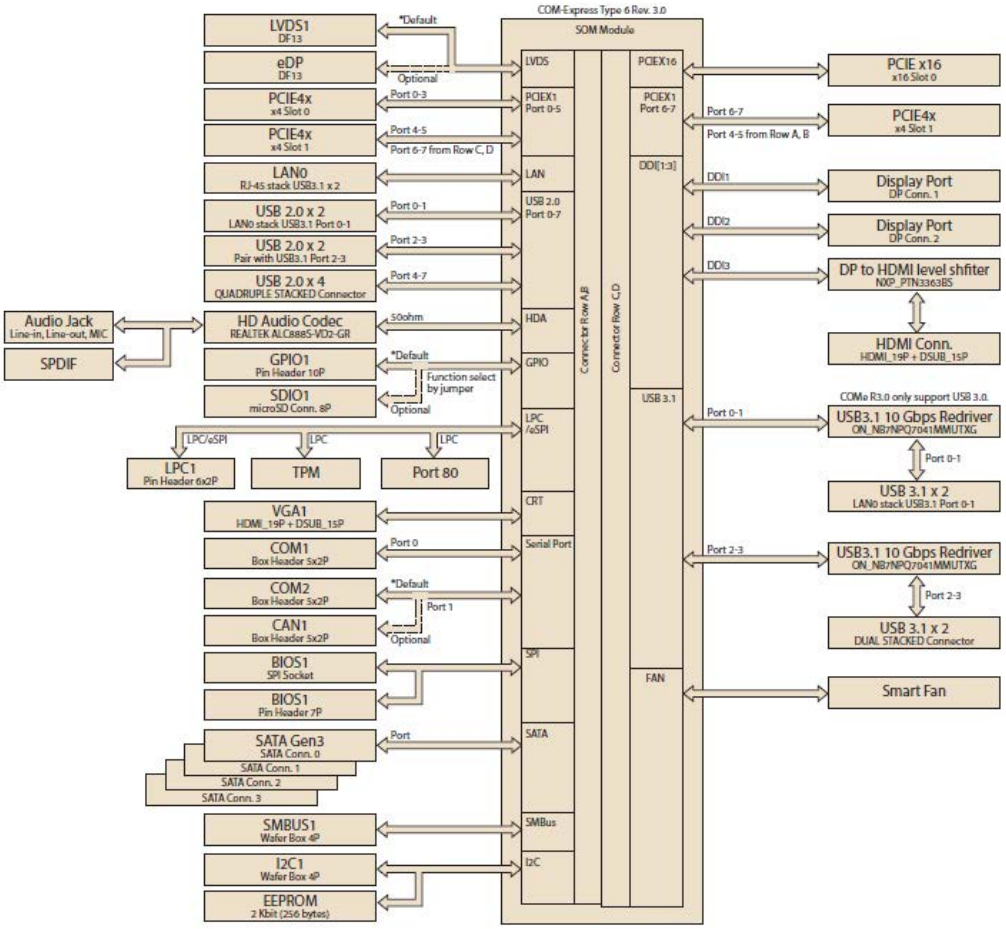
- Express card no longer supported
- AC'97 removed
- Added rapid shutdown support
- Left pin header of the eSPI interface is multiplexed over LPC

USB 3.1 Gen2 is a common feature of computing platforms. Thus, SOM-DB5830 has been equipped with a driver for USB 3.1 Gen2 at a transfer rate of 10 Gbit/s, which exceeds that for COM Express.

Customers can use SOM-DB5830 as a reference design board to emulate required functions or as an application board integrated directly into products.

Acronyms	
Term	**Definition**
ACPI	Advanced Configuration Power Interface is a standard for implementing power-saving modes in PC-AT systems.
BIOS	Basic Input/Output System is firmware on PC-AT systems that initializes system components before relinquishing control to the operating system.
CAN	Controller area network (CAN or CAN bus) is a vehicle bus standard designed to allow micro-controllers to communicate with each other within a vehicle without a host computer.
DDI	Digital Display Interface is a convergence specification comprising DisplayPort, HDMI/DVI, and SDVO.
EAPI	Embedded Application Programmable Interface Software interface for COM Express®-specific industrial functions ■ System Information ■ Watchdog Timer ■ I2C Bus ■ Flat Panel Brightness Control ■ User Storage Area ■ GPIO
GbE	Gigabit Ethernet
GPIO	General Purpose Input/Output
HDA	Intel® High Definition Audio (HD Audio) refers to the 2004 specification for delivering high-definition audio that enables the playback of more channels at higher quality compared to AC'97
I2C	Inter Integrated Circuit is a 2-wire (clock and data) signaling scheme that allows communication between integrated circuits and is primarily used to read and load register values.
ME	Management Engine
PC-AT	Personal Computer - Advanced Technology is an IBM-trademarked term used to refer to Intel-based personal computers in the 1990s.
PEG	PCI Express Graphics
RTC	Real-Time Clock refers to a battery-backed circuit in PC-AT systems that maintains the system time and date, as well as specific setup parameters.
SPD	Serial Presence Detect is configuration information stored on a serial EEPROM chip on DRAM modules.
TPM	Trusted Platform Module is chip technology designed to provide hardware-based, security-related functions.
UEFI	Unified Extensible Firmware Interface
WDT	Watchdog Timer

1.2 Block Diagram



Chapter 2

Mechanical Information

- Board Information
- Mechanical Drawings
- Assembly Drawing

2.1 Board Information

The main chips on the COM Express® carrier board are shown below.

A1

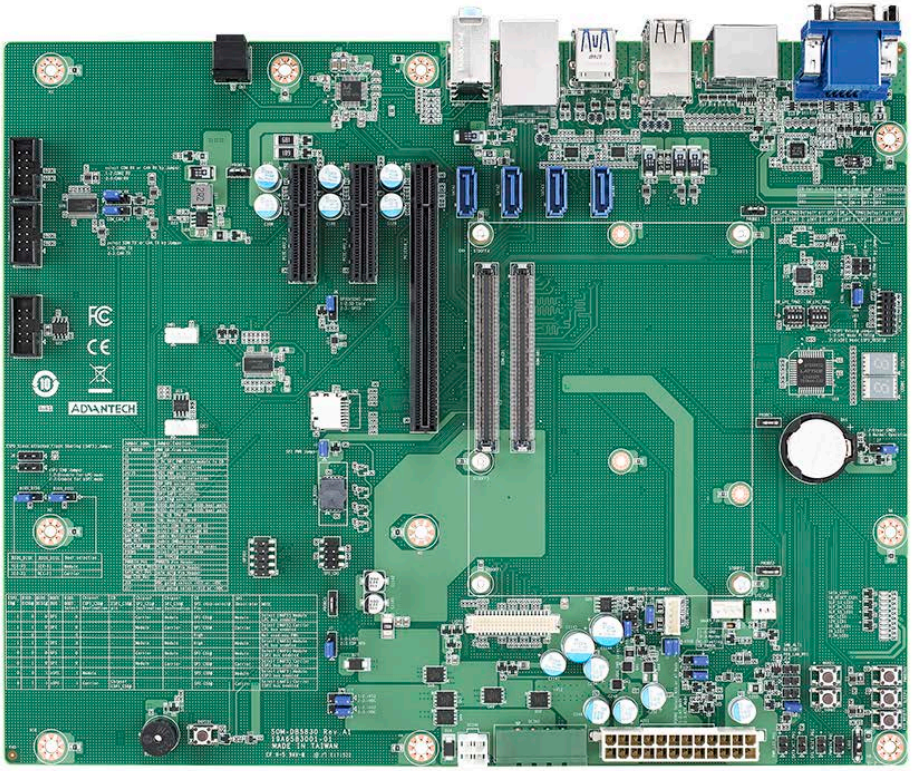


Figure 2.1 Main Chips on Board - Top View (A1)

A2

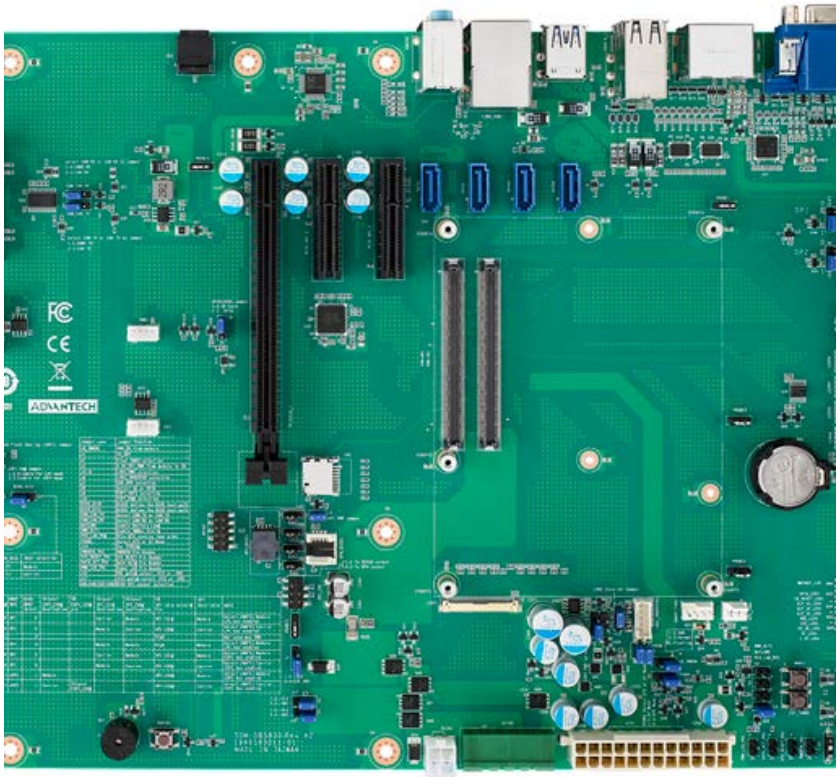


Figure 2.2 Main Chips on Board - Top View (A2)

A3

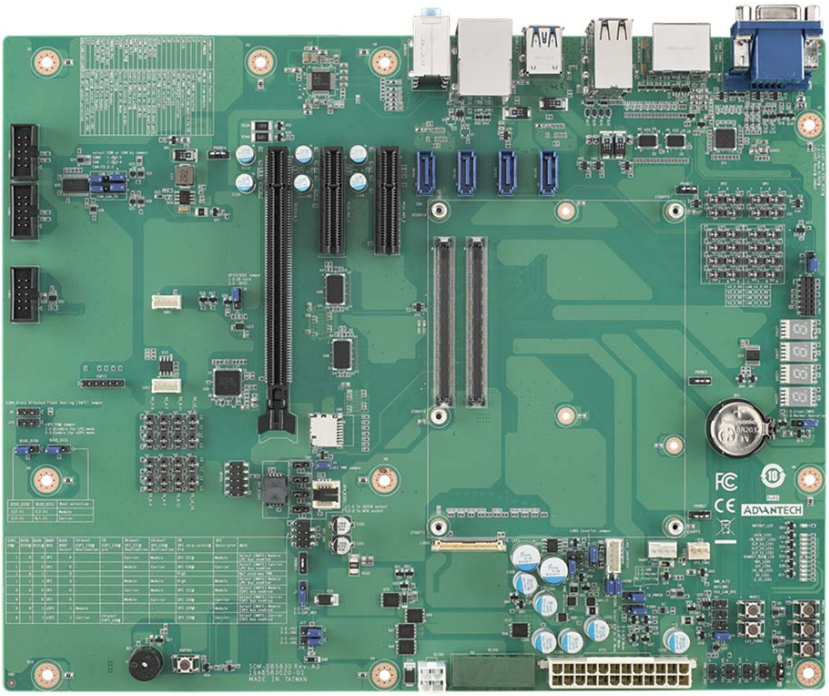


Figure 2.3 Main Chips on Board - Top View (A3)

2.2 Mechanical Drawings

To obtain more details about 2D/3D models, visit the Advantech COM support website at http://com.advantech.com.

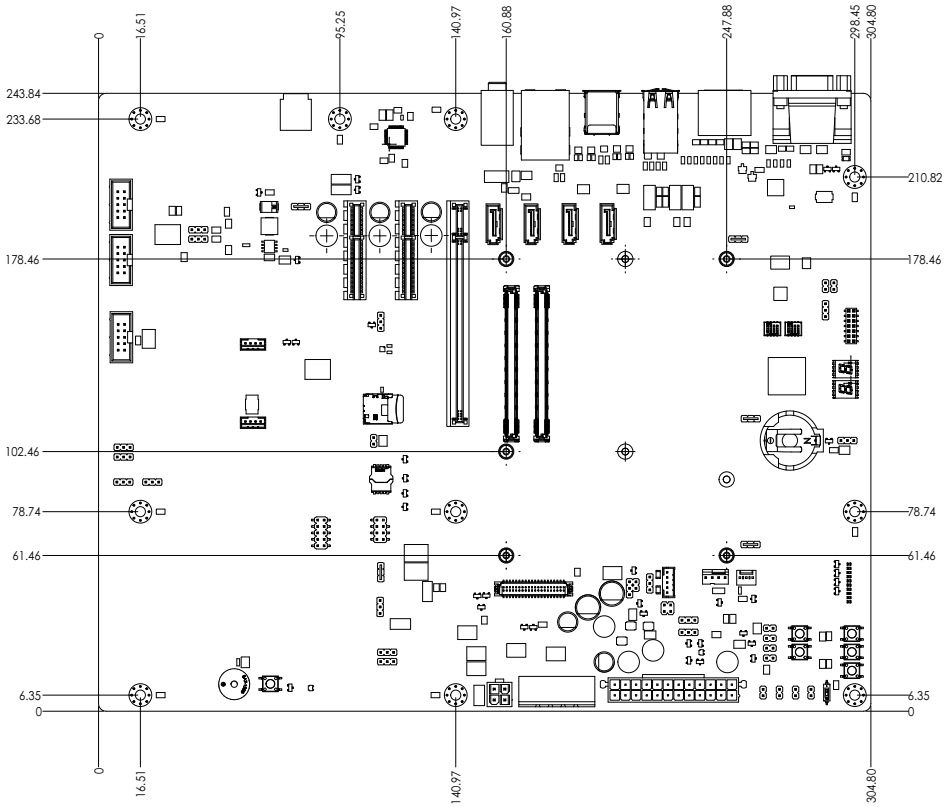


Figure 2.4 SOM-DB5830 Board - Top View

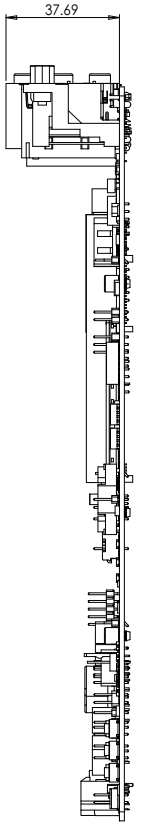


Figure 2.5 SOM-DB5830 Mechanical Drawing - Side View

2.3 Assembly Drawing

These figures demonstrate the assembly order from the thermal module, COM Express Basic module to the carrier board.

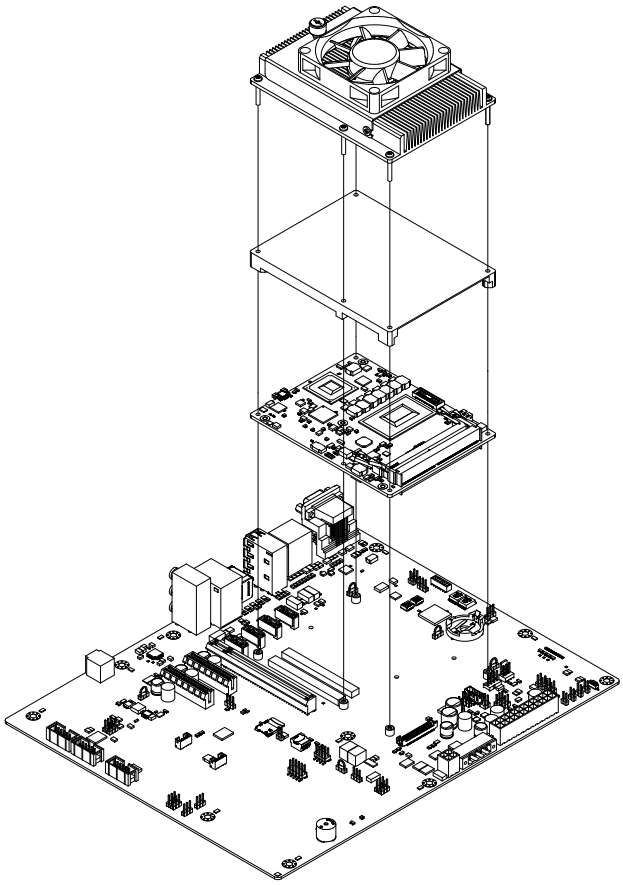


Figure 2.6 COM Express to SOM-DB5830

Chapter 3

Connector and Jumper Settings

3.1 Connector and Jumper Settings

3.1.1 Connector Layout

A1

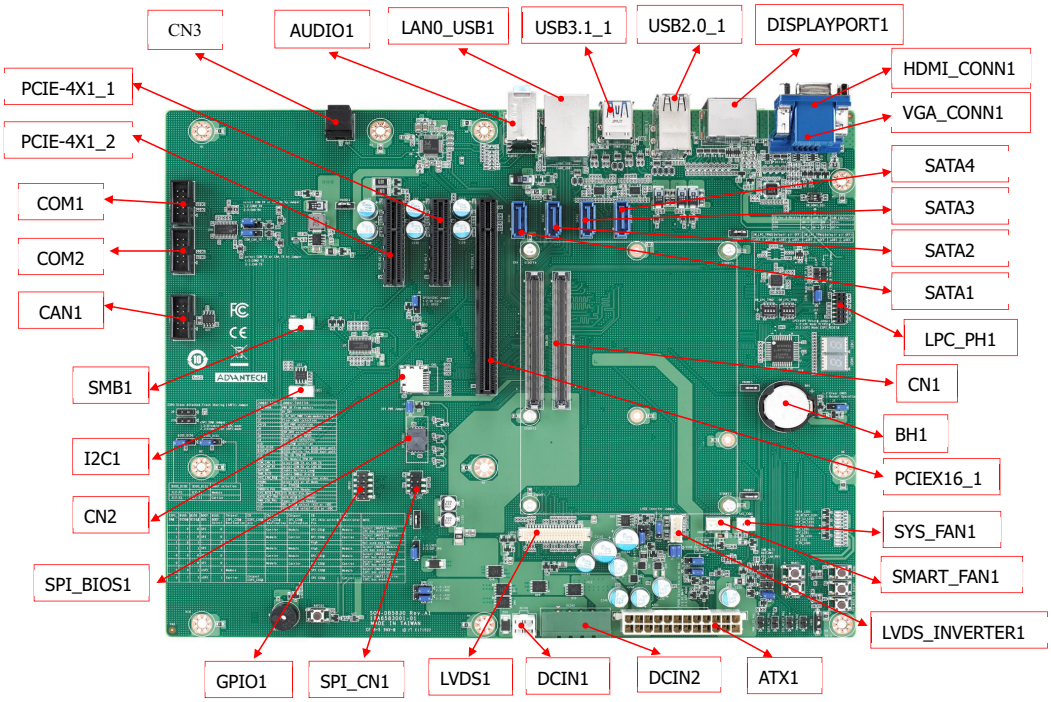


Figure 3.1 Board Connector Layout (A1)

A2

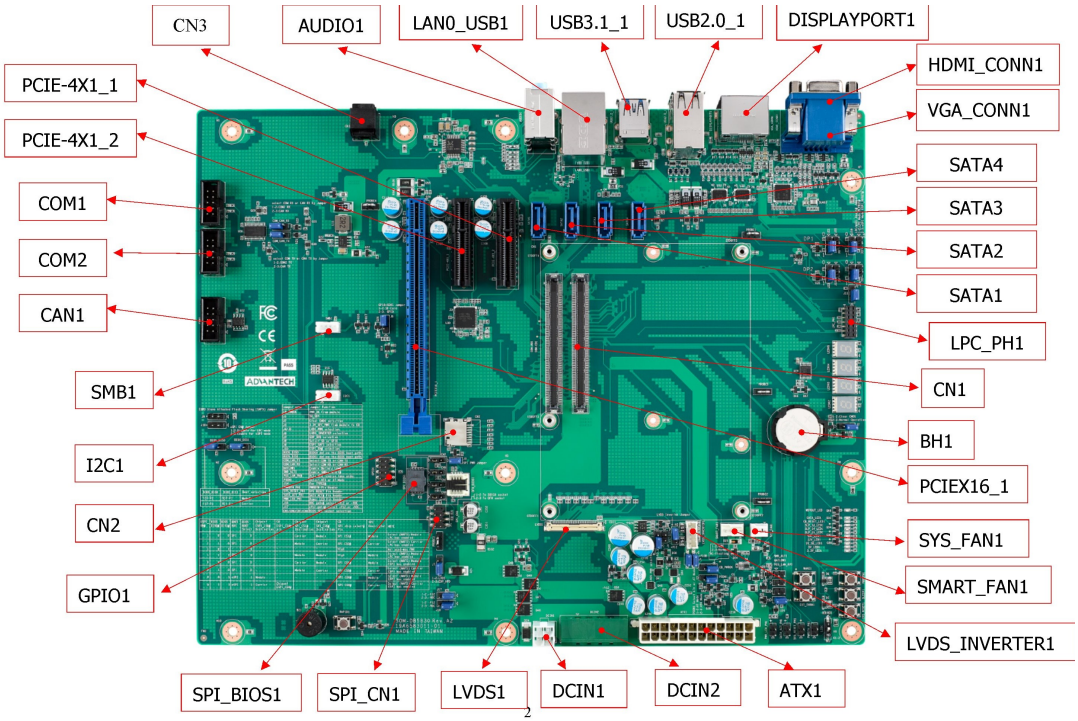


Figure 3.2 Board Connector Layout (A2)

A3

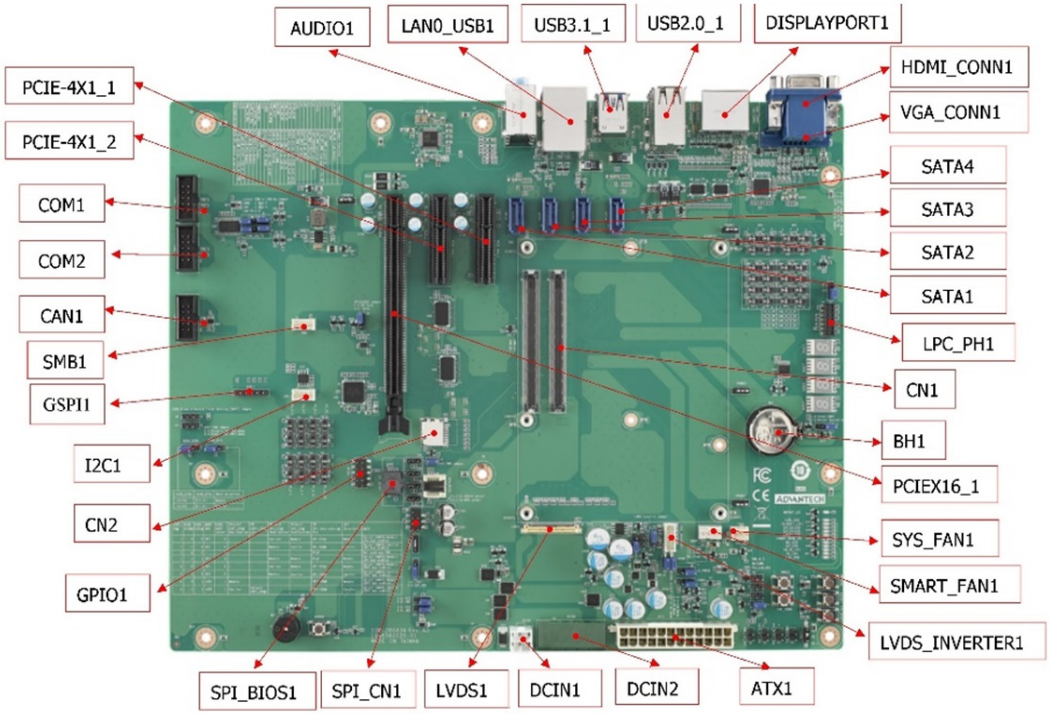


Figure 3.3 Board Connector Layout (A3)

3.1.2 I/O Layout

A1

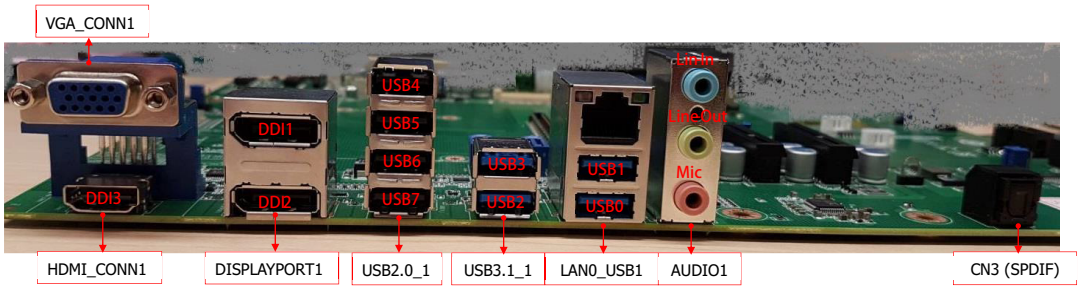


Figure 3.4 I/O Layout (A1)

A2

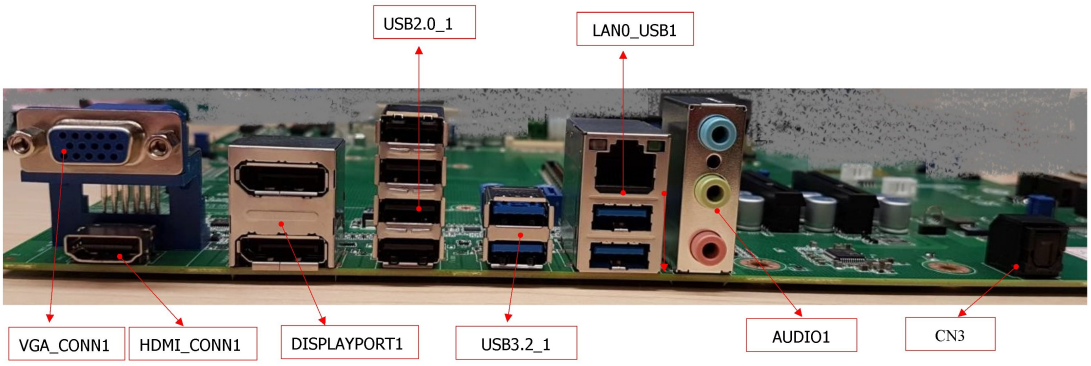


Figure 3.5 I/O Layout (A2)

A3

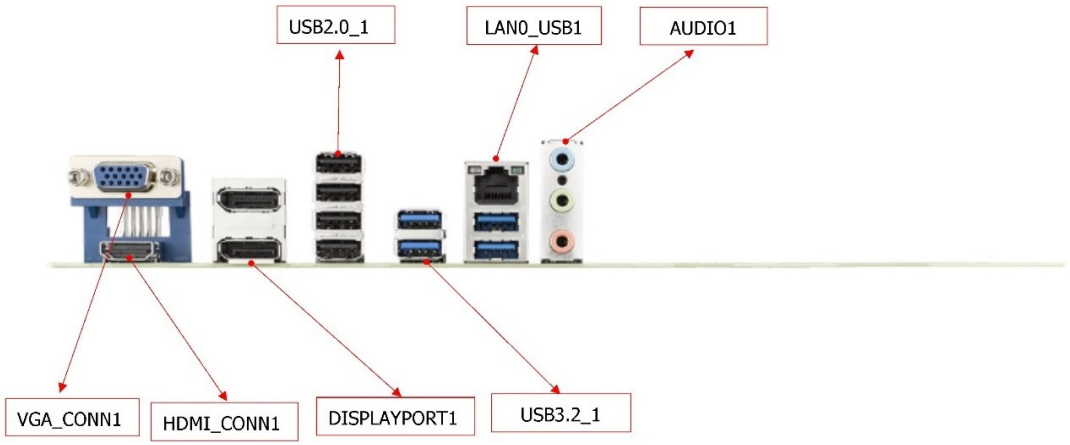


Figure 3.6 I/O Layout (A3)

3.1.3 LED Layout (A1)

A1

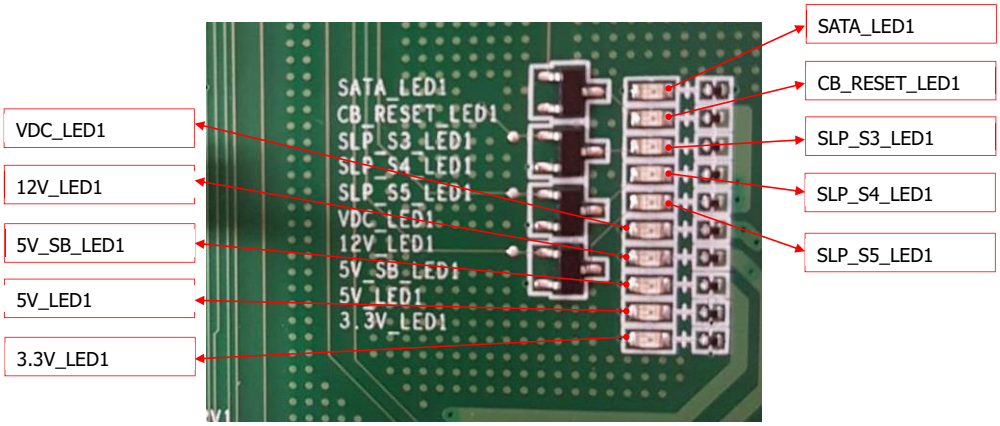


Figure 3.7 LED Layout (A1)

A2

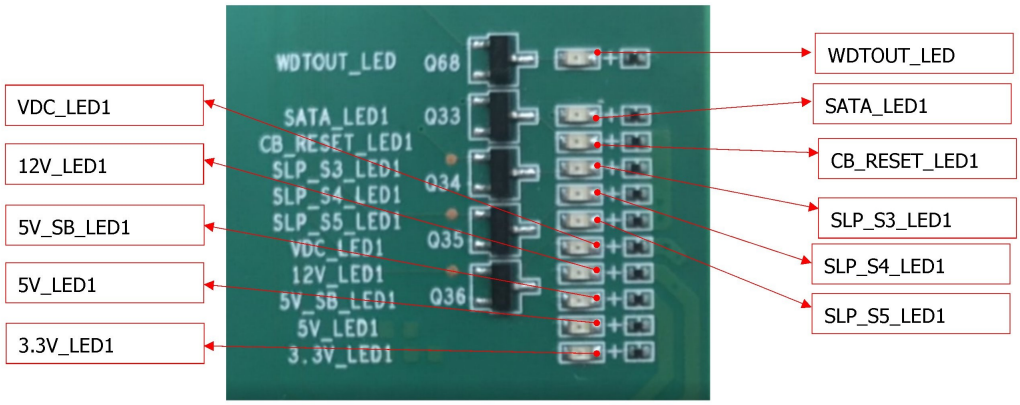


Figure 3.8 LED Layout (A2)

A3

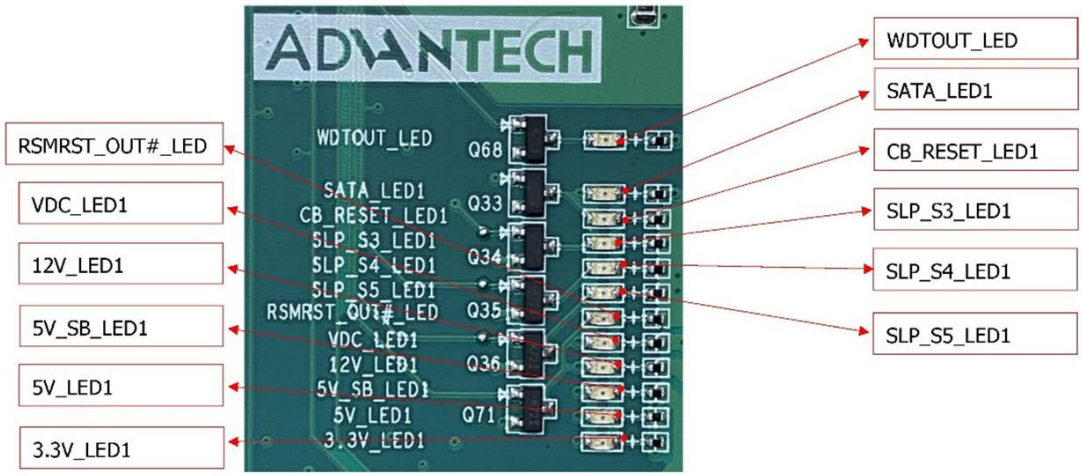


Figure 3.9 LED Layout (A3)

3.1.4 Jumper and Switch Layout

A1

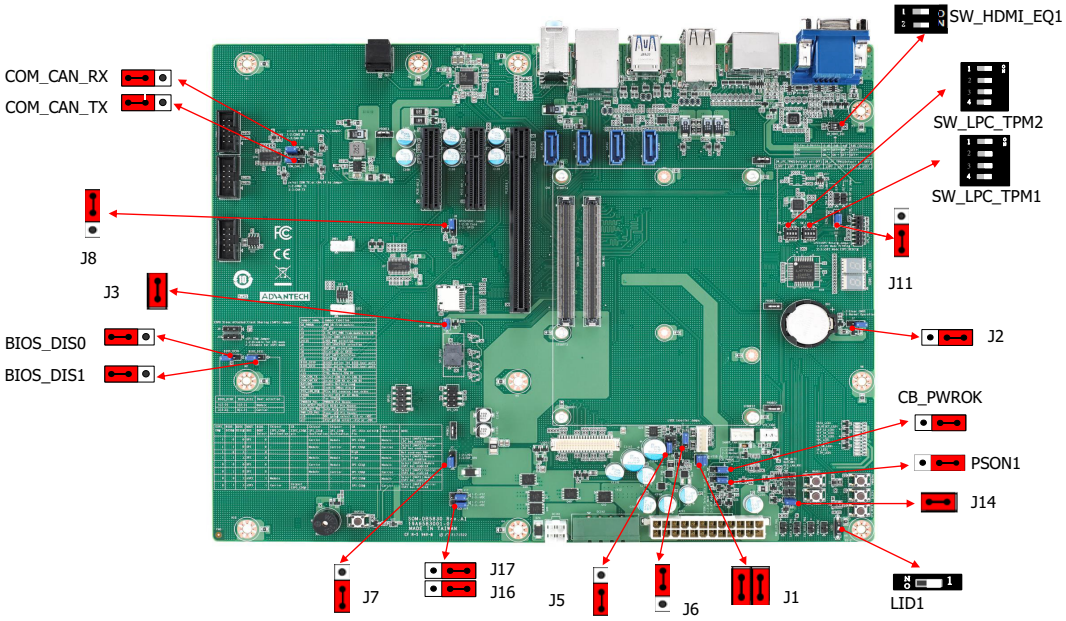


Figure 3.10 Default Jumper Settings (A1)

A2

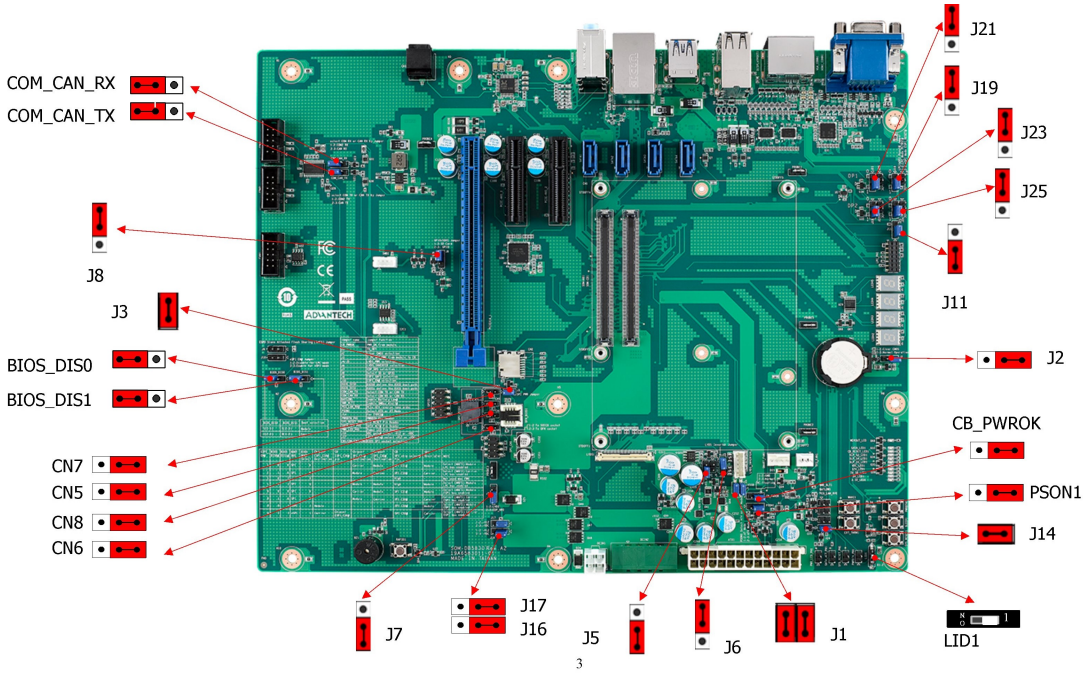


Figure 3.11 Default Jumper Settings (A2)

A3

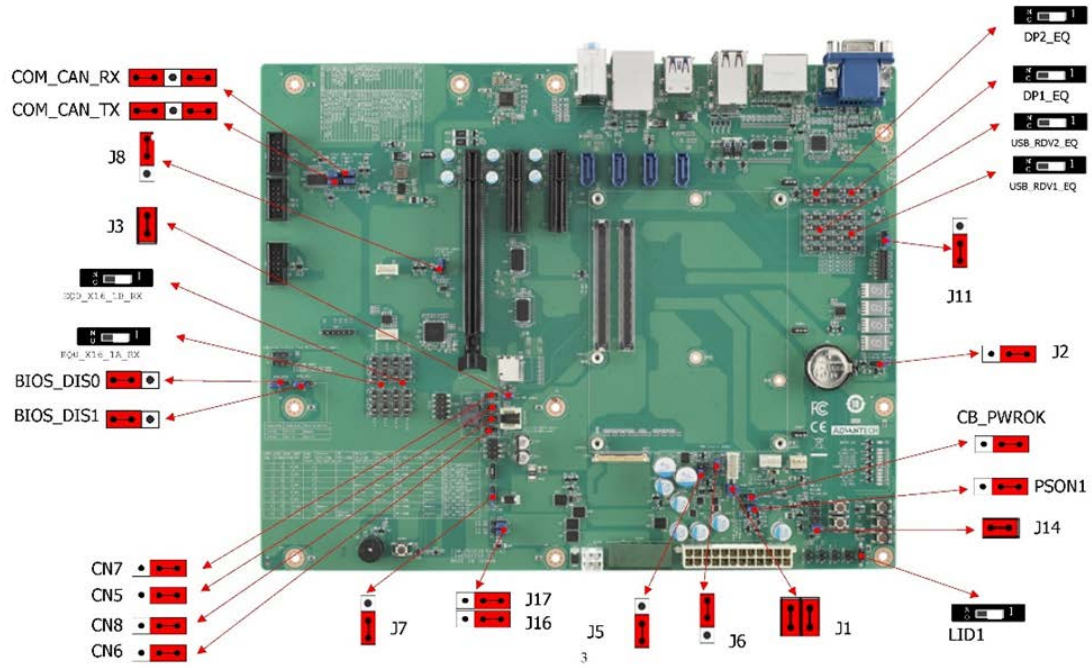


Figure 3.12 Default Jumper Settings (A3)

3.1.5 Connector List

Table 3.1: Connector List (A1)

Label	Function	Label	Function
ATX1	ATX connector	BH1	RTC battery connector
CN1	COM Express connector	SMART_FAN1	Smart fan connector
COM1	COM Port 1 connector (Tx, Rx)	SMB1	SMBus wafer box
COM2	COM Port 2 connector (Tx, Rx)	SYS_FAN1	System fan connector
DCIN1	Wide-range DC input connector 1	SPI_CN1	SPI BIOS pin header
GPIO1	GPIO pin header	CAN1	CAN bus connector
I2C1	I2C wafer box	SPI_BIOS1	SPI BIOS socket
LAN0_USB1	LAN, USB 3.1/2.0 Port 0 and Port 1 connector	DCIN2	Wide-range DC input connector 2
LPC_PH1	Low-pin count pin header	PCIE-4X1_1	PCIe x4 Slot 1
PCIEX16_1	PCIe x16 Slot 1	SATA1	SATA Port 0 connector
PCIE-4X1_2	PCIe x4 Slot 2	SATA2	SATA Port 1 connector
LVDS_INVERTER1	LVDS inverter connector	SATA3	SATA Port 2 connector
CN3	S/PDIF connector	SATA4	SATA Port 3 connector
DISPLAYPORT1	DisplayPort 1 and 2 connector	HDMI_CONN1	HDMI connector
USB2.0_1	USB 2.0 Port 4 ~ 7 connector	VGA_CONN1	CRT connector
USB3.1_1	USB 3.1 Port 2 ~ 3 connector	AUDIO1	Audio jack
CN2	Micro SD card connector	LVDS1	LVDS connector

Table 3.2: Connector List (A2)

Label	Function	Label	Function
ATX1	ATX Connector	BH1	RTC Battery Connector
CN1	COM Express Connector	SMART_FAN1	Smart Fan Connector
COM1	COM Port1 Connector (Tx, Rx)	SMB1	SMBus Wafer Box
COM2	COM Port2 Connector (Tx, Rx)	SYS_FAN1	System Fan Connector
DCIN1	Wide Range DC Input Connector1	SPI_CN1	SPI BIOS PIN HEADER
GPIO1	GPIO Pin Header	CAN1	CAN Bus Connector
I2C1	I2C Wafer Box	SPI_BIOS1	SPI BIOS Socket
LAN0_USB1	LAN, USB 3.2/2.0 Port0 and Port1 Connector	DCIN2	Wide Range DC Input Connector2
LPC_PH1	Low Pin Count Pin Header	PCIE-4X1_1	PCIe x4 slot1
PCIEX16_1	PCIe x16 slot	SATA1	SATA Port0 Connector
PCIE-4X1_2	PCIe x4 slot2	SATA2	SATA Port1 Connector
LVDS_INVERTER1	LVDS INVERTER Connector	SATA3	SATA Port2 Connector
CN3	S/PDIF Connector	SATA4	SATA Port3 Connector
DISPLAYPORT1	Display Port1&2 Connector	HDMI_CONN1	HDMI Connector
USB2.0_1	USB 2.0 Port4~7 Connector	VGA_CONN1	CRT Connector
USB3.2_1	USB 3.2 Port2~3 Connector	AUDIO1	AUDIO Jack
CN2	Micro SD Card Connector	LVDS1	LVDS Connector

Table 3.3: Connector List (A3)			
Label	**Function**	**Label**	**Function**
ATX1	ATX Connector	BH1	RTC Battery Connector
CN1	COM Express Connector	SMART_FAN1	Smart Fan Connector
COM1	COM Port1 Connector (Tx, Rx)	SMB1	SMBus Wafer Box
COM2	COM Port2 Connector (Tx, Rx)	SYS_FAN1	System Fan Connector
DCIN1	Wide Range DC Input Connector1	SPI_CN1	SPI BIOS PIN HEADER
GPIO1	GPIO Pin Header	CAN1	CAN Bus Connector
I2C1	I2C Wafer Box	SPI_BIOS1	SPI BIOS Socket
LAN0_USB1	LAN, USB 3.2/2.0 Port0 and Port1 Connector	DCIN2	Wide Range DC Input Connector2
LPC_PH1	Low Pin Count Pin Header	PCIE-4X1_1	PCIe x4 slot1
PCIEX16_1	PCIe x16 slot	SATA1	SATA Port0 Connector
PCIE-4X1_2	PCIe x4 slot2	SATA2	SATA Port1 Connector
LVDS_INVERTER1	LVDS INVERTER Connector	SATA3	SATA Port2 Connector
DISPLAYPORT1	Display Port1&2 Connector	SATA4	SATA Port3 Connector
		HDMI_CONN1	HDMI Connector
		VGA_CONN1	CRT Connector
		AUDIO1	AUDIO Jack
		LVDS1	LVDS Connector
		GSPI1	GSPI pin header

3.1.6 Jumper, Switch, and Button List

Table 3.4: Jumper, Switch, and Button List (A1)

Label	Function	Label	Function
J16, J17	SOM-DB5830 voltage input (VIN) selection	SW_LPC_TPM1	TPM enable/disable switch
J1	COMe module +V5SB supply	SW_LPC_TPM2	TPM enable/disable switch
PSON1	ATX/AT mode selection	CB_PWROK	PWROK signal pull down/floating selection
J3	Carrier board SPI power supply	PWRBTN1	Power button
J2	Normal operation/clear CMOS selection	SYS_RESET1	Reset button
J9	eSPI_SAFS selection	SLEEP1	Sleep button
J10	eSPI_EN# selection	EXT_THRM1	External thermal trip button
J11	LPC/eSPI reset# jumper selection	WAKE1	Wake button
J12	CTRL CB TPM PP selection	LID1	LID button
J13	CTRL module TPM PP selection	RAPID1	Rapid shutdown button
J14	COMe R3.0 support type SEL	SW_HDMI_EQ1	HDMI level shifter EQ SEL
J4, J5	LVDS_PWR selection		
J6	LVDS_inverter selection		
J8	GPIO/SDIO SEL		
J7	EDP/LVDS HPD selection		
BIOS_DIS0	BIOS disable 0		
BIOS_DIS1	BIOS disable 1		
CB_PWROK	PWR_OK from module SEL		
COM_CAN_TX	COM TX/CAN TX SEL		
COM_CAN_RX	COM RX/CAN RX SEL		
BATLOW1	Enable battery low#		
SMB_ALT1	Enable SMBus alert#		
PEG_LAN_RV1	PCIe GFX reverse lane order		
PWRBTN_PH1	PWRBTN pin header		
SYS_RESET_PH1	SYS reset pin header		
SATA_ACT_PH1	SATA ACT# pin header		
PWR_LED_PH1	Power LED pin header		

Table 3.5: Jumper, Switch, and Button List (A2)			
Label	**Function**	**Label**	**Function**
J16, J17	SOM-DB5830 Voltage Input (VIN) Selection	CB_PWROK	PWROK Signal Pull Down or Floating Selection
J1	COMe Module +V5SB supply	PWRBTN1	Power Button
PSON1	ATX / AT Mode Selection	SYS_RESET1	Reset Button
J3	Carrier Board SPI power supply	SLEEP1	Sleep Button
J2	Normal Operation / Clear CMOS Selection	EXT_THRM1	External Thermal Trip Button
J9	eSPI_SAFS Selection	WAKE1	Wake Button
J10	eSPI_EN# Selection	LID1	LID Button
J11	LPC / eSPI Reset# Jumper Selection	RAPID1	Rapid shutdown button
J12	CTRL CB TPM PP Selection	J18/J19	DISPLAYPORT1A Equalization Setting
J13	CTRL Module TPM PP Selection	J20/J21	DISPLAYPORT1A Equalization Setting
J14	COMe R3.0 support Type SEL	J22/J23	DISPLAYPORT1B Equalization Setting
J4, J5	LVDS_PWR selection	J24/J25	DISPLAYPORT1B Equalization Setting
J6	LVDS_INVERTER selection	CN5	BIOS Socket Select
J8	GPIO / SDIO SEL	CN6	BIOS Socket Select
J7	EDP / LVDS HPD selection	CN7	BIOS Socket Select
BIOS_DIS0	BIOS Disable0	CN8	BIOS Socket Select
BIOS_DIS1	BIOS Disable1		
CB_PWROK	PWR_OK from module SEL		
COM_CAN_TX	COM TX / CAN TX SEL		
COM_CAN_RX	COM RX / CAN RX SEL		
BATLOW1	Enable Battery Low#		
SMB_ALT1	Enable SMBus Alert#		
PEG_LAN_RV1	PCIe GFX reverse lane order		
PWRBTN_PH1	PWRBTN Pin Header		
SYS_RESET_PH1	SYS RESET Pin Header		
SATA_ACT_PH1	SATA ACT# Pin Header		
PWR_LED_PH1	Power LED Pin Header		

Table 3.6: Jumper, Switch, and Button List (A3)			
Label	**Function**	**Label**	**Function**
J16, J17	SOM-DB5830 Voltage Input (VIN) Selection	CB_PWROK	PWROK Signal Pull Down or Floating Selection
J1	COMe Module +V5SB supply	PWRBTN1	Power Button
PSON1	ATX / AT Mode Selection	SYS_RESET1	Reset Button
J3	Carrier Board SPI power supply	SLEEP1	Sleep Button
J2	Normal Operation / Clear CMOS Selection	EXT_THRM1	External Thermal Trip Button
J9	eSPI_SAFS Selection	WAKE1	Wake Button
J10	eSPI_EN# Selection	LID1	LID Button
J11	LPC / eSPI Reset# Jumper Selection	RAPID1	Rapid shutdown button
J12	CTRL CB TPM PP Selection	CN5	BIOS Socket Solect
J13	CTRL Module TPM PP Selection	CN6	BIOS Socket Solect
J14	COMe R3.0 support Type SEL	CN7	BIOS Socket Solect
J4, J5	LVDS_PWR selection	CN8	BIOS Socket Solect
J6	LVDS_INVERTER selection	USB3_RDVx	USB 3.2 Gen2 Redriiver EQ setting switch
J8	GPIO / SDIO SEL	DPx_EQx_x	DP1/DP2 Re-driver EQ setting switch
J7	EDP / LVDS HPD selection	EQ0_X-16_1x_RX_xx_x	PCIe x16 Gen4 Redriver EQ setting switch
BIOS_DIS0	BIOS Disable0		
BIOS_DIS1	BIOS Disable1		
CB_PWROK	PWR_OK from module SEL		
COM_CAN_TX	COM TX / CAN TX SEL		
COM_CAN_RX	COM RX / CAN RX SEL		
BATLOW1	Enable Battery Low#		
SMB_ALT1	Enable SMBus Alert#		
PEG_LAN_RV1	PCIe GFX reverse lane order		
PWRBTN_PH1	PWRBTN Pin Header		
SYS_RESET_PH1	SYS RESET Pin Header		
SATA_ACT_PH1	SATA ACT# Pin Header		
PWR_LED_PH1	Power LED Pin Header		

3.1.7 Switch Settings

3.1.7.1 (A1)

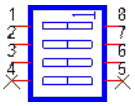


Table 3.7: SW_LPC_TPM1 and SW_LPC_TPM2: TPM Enable/Disable Switch

Dip Switch	1-8	2-7	3-6	4-5	Function
SW_LPC_TPM1 ~ SW_LPC_TPM2	ON	ON	ON	ON	TPM enable
	OFF	OFF	OFF	OFF	TPM disable [default]

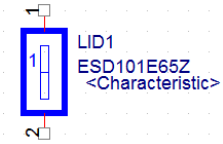


Table 3.8: LID1 LID Button Enable/Disable Switch

Dip Switch	1-2	Function
LID1	ON	LID# enable
	OFF	LID# disable [default]

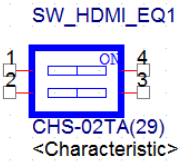


Table 3.9: SW_HDMI_EQ1 HDMI Level Shifter EQ SEL

Dip Switch	1-4	2-3	Function
SW_HDMI_EQ1	ON	ON	EQ set to 0dB
	OFF	ON	EQ set to 2dB
	ON	OFF	EQ set to 4dB
	OFF	OFF	EQ set to 6dB [default]

3.1.7.2 A2 & A3

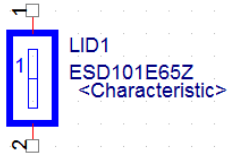


Table 3.10: LID1 LID Button Enable/Disable Switch

Dip Switch	1-2	Function
LID1	ON	LID# Enable
	OFF	LID# Disable [Default]

Table 3.11: BATLOW1 BATLOW#

Pin	Function
1-2	Battery low
1-X	Normal [default]

Table 3.12: BATLOW1 BATLOW# (A2 & A3)

Pin	Function
1-2	Battery Low
1-X	Normal [Default]

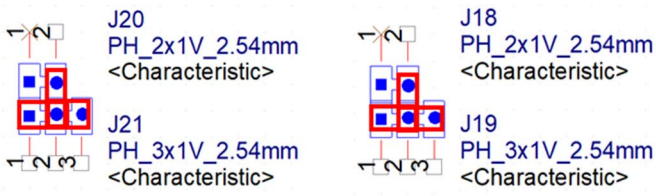


Table 3.13: DISPLAYPORT1A EQ GPOP Control (A2)

Equalization Setting	DPEQ1 Level	DPEQ0 Level	EQ GAIN at 4.05G Hz (dB)
0	J19(2,1)	J21(2,1)	1.0
1	J19(2,1)	J21(2,2)	3.3
2	J19(2,1)	J21(2-X)	4.9
3	J19(2,1)	J21(2-3)	6.5
4	J19(2,2)	J21(2,1)	7.5
5	J19(2,2)	J21(2,2)	8.6
6	J19(2,2)	J21(2-X)	9.5
7	J19(2,2)	J21(2-3)	10.4
8	J19(2,X)	J21(2,1)	11.1
9	J19(2,X)	J21(2,2)	11.7
10	J19(2,X)	J21(2-X)	12.3

Table 3.13: DISPLAYPORT1A EQ GPOP Control (A2)			
11	J19(2,X)	J21(2-3)	12.8
12	J19(2,3)	J21(2,1)	13.2
13	J19(2,3)	J21(2,2)	13.6
14	J19(2,3)	J21(2-X)	14.0
15	J19(2,3)	J21(2-3)	14.4

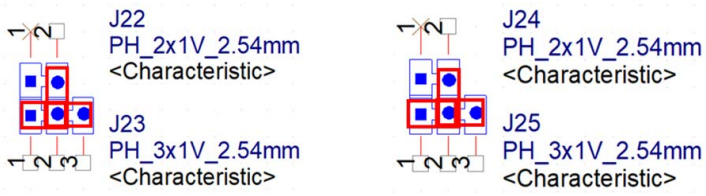


Table 3.14: DISPLAYPORT1B EQ GPOP Control (A2)			
Equalization Setting	**DPEQ1 Level**	**DPEQ0 Level**	**EQ GAIN at 4.05G Hz (dB)**
0	J23(2,1)	J25(2,1)	1.0
1	J23(2,1)	J25(2,2)	3.3
2	J23(2,1)	J25(2-X)	4.9
3	J23(2,1)	J25(2-3)	6.5
4	J23(2,2)	J25(2,1)	7.5
5	J23(2,2)	J25(2,2)	8.6
6	J23(2,2)	J25(2-X)	9.5
7	J23(2,2)	J25(2-3)	10.4
8	J23(2,X)	J25(2,1)	11.1
9	J23(2,X)	J25(2,2)	11.7
10	J23(2,X)	J25(2-X)	12.3
11	J23(2,X)	J25(2-3)	12.8
12	J23(2,3)	J25(2,1)	13.2
13	J23(2,3)	J25(2,2)	13.6
14	J23(2,3)	J25(2-X)	14.0
15	J23(2,3)	J25(2-3)	14.4

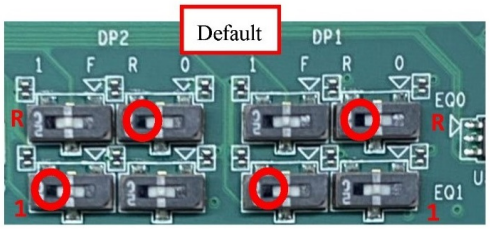


Table 3.15: DISPLAYPORT1A EQ GPOP Control (A3)

Equalization Setting	DPEQ1 Level	DPEQ0 Level	EQ GAIN at 4.05G Hz (dB)
0	0	0	1.0
1	0	R	3.3
2	0	F	4.9
3	0	1	6.5
4	R	0	7.5
5	R	R	8.6
6	R	F	9.5
7	R	1	10.4
8	F	0	11.1
9	F	R	11.7
10	F	F	12.3
11	F	1	12.8
12	1	0	13.2
13	1	R	13.6
14	1	F	14.0
15	1	1	14.4

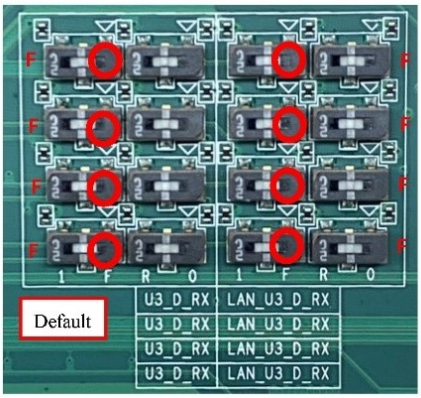


Table 3.16: USB 3.2 Gen2 Re-driver EQ Settings (A3)

	Equalizer setting (dB)	
EQA/B/C/D	@2.5GHz	@5GHz
0	6.7	12.4
R	3.5	8.0
F	5.3	10.6
1	8.4	14.6

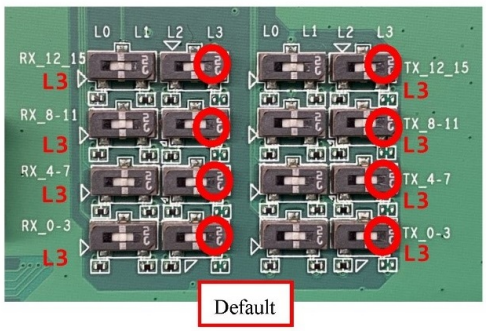


Table 3.17: PCIe x16 TX/RX EQ Settings (A3)

	Equalization setting		TYPICAL EQ BOOST(dB)	
EQ INDEX	EQ1_0 EQ1_1	EQ0_0 EQ0_1	@4GHz	@8GHz
0	L0	L0	-0.25	-0.5
1	L0	L1	2.0	4.0
2	L0	L2	2.5	5.0
3	L0	L3	3.0	6.0
4	L1	L0	4.0	7.0
5	L1	L1	4.5	7.5
6	L1	L2	5.0	8.0
7	L1	L3	6.0	9.5
8	L2	L0	7.0	10
9	L2	L1	8.0	11
10	L2	L2	8.5	12.5
11	L2	L3	9.0	13
12	L3	L0	9.5	14.5
13	L3	L1	10.0	15
14	L3	L2	10.5	16
15	L3	L3	12.0	18

3.1.8 Connector Pin Definitions

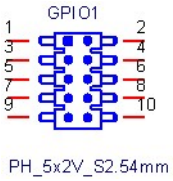


Table 3.18: GPIO1 GPIO Pin Header (A1)

Pin	Signal	Pin	Signal
1	GPI0	2	GPO0
3	GPI1	4	GPO1
5	GPI2	6	GPO2
7	GPO1	8	GPO3
9	GPI3	10	GND

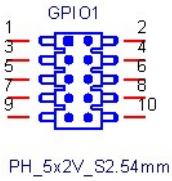


Table 3.19: GPIO1 GPIO Pin Header (A2 & A3)

Pin	Signal	Pin	Signal
1	GPI0	2	GPO0
3	GPI1	4	GPO1
5	GPI2	6	GPO2
7	GPI3	8	GPO3
9	GND	10	GND

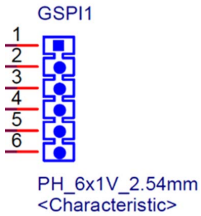


Table 3.20: GSPI1 GSPI Pin Header (A3)

Pin	Signal
1	+V3.3
2	GND
3	GSPI_CK
4	GSPI_MOSI
5	GSPI_CS#
6	GSPI_MISO

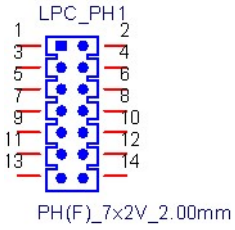


Table 3.21: LPC_PH1 Low-Pin Count Pin Header (A1)

Pin	Signal	Pin	Signal
1	CLK33M_PH	2	LPC_PH_AD1
3	ESPI_LPC_RST#	4	LPC_PH_AD0
5	LPC_PH_FRAME#	6	+V3.3
7	LPC_PH_AD3	8	GND
9	LPC_PH_AD2	10	Pull-up via 10K ohm to +V3.3
11	SERIRQ_PH	12	ESPI_LPC_RST#
13	+V5_DUAL	14	+V5

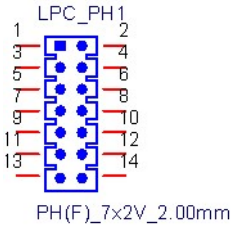


Table 3.22: LPC_PH1 Low Pin Count Pin Header (A2 & A3)			
Pin	**Signal**	**Pin**	**Signal**
1	CLK33M_PH	2	LPC_PH_AD1
3	ESPI_LPC_RST#	4	LPC_PH_AD0
5	LPC_PH_FRAME#	6	+V3.3
7	LPC_PH_AD3	8	GND
9	LPC_PH_AD2	10	Pull-up via 10K ohm to +V3.3
11	SERIRQ_PH	12	ESPI_LPC_RST#
13	+V5_DUAL	14	+V5

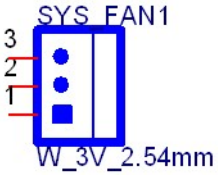


Table 3.23: SYS_FAN1 System Fan Connector (A1)	
Pin	**Signal**
1	GND
2	+V12
3	SYS_FAN_SENSE

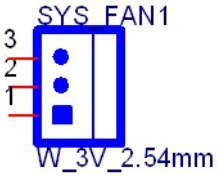


Table 3.24: SYS_FAN1 System Fan Connector (A2 & A3)	
Pin	**Signal**
1	GND
2	+V12
3	SYS_FAN_SENSE

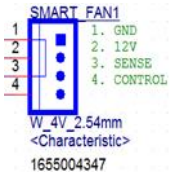


Table 3.25: SMART_FAN1 Smart Fan Connector (A1)

Pin	Signal
1	GND
2	+V_FAN
3	FANTACH_R1
4	FANPWM_R

Table 3.26: SMART_FAN1 Smart Fan Connector (A2 & A3)

Pin	Signal
1	GND
2	+V12
3	FANTACH_R1
4	FANPWM_R

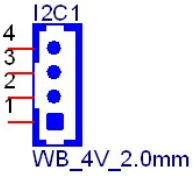


Table 3.27: I^2C1 I^2C Wafer Box (A1)

Pin	Signal
1	GND
2	I2C_DAT
3	I2C_CLK
4	+V3.3_DUAL

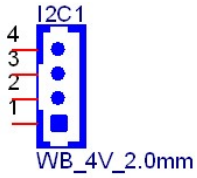


Table 3.28: I²C Wafer Box (A2 & A3)	
Pin	**Signal**
1	GND
2	I2C_DAT
3	I2C_CLK
4	+V3.3_DUAL

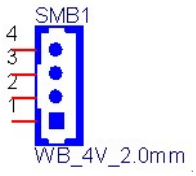


Table 3.29: SMB1 SMBus Wafer Box (A1)	
Pin	**Signal**
1	GND
2	SMB_DAT
3	SMB_CLK
4	+V3.3_DUAL

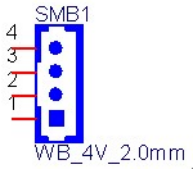


Table 3.30: SMB1 SMBus Wafer Box (A2 & A3)	
Pin	**Signal**
1	GND
2	SMB_DAT
3	SMB_CLK
4	+V3.3_DUAL

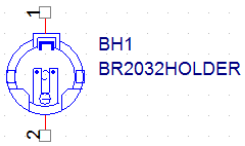


Table 3.31: BH1 RTC Battery Connector (A1)	
Pin	**Signal**
1	3SMB_CLK
2	4+V3.3_DUAL

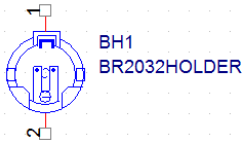


Table 3.32: BH1 RTC Battery Connector (A2 & A3)	
Pin	**Signal**
1	+VBAT_BH
2	GND

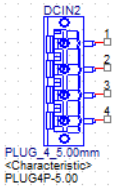


Table 3.33: DCIN2 Wide-Range DC Input Connector 2 (A1)	
Pin	**Signal**
1	GND
2	+VDC
3	+VDC
4	GND

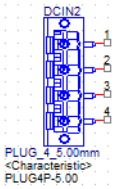


Table 3.34: DCIN2 Wide Range DC Input Connector2 (A2 & A3)	
Pin	**Signal**
1	GND
2	+VDC
3	+VDC
4	GND

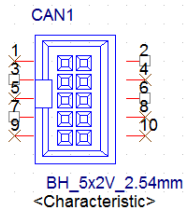


Table 3.35: CAN1 CAN Bus Connector (A1)

Pin	Signal	Pin	Signal
1	NC	2	CAN1_D-
3	GND	4	NC
5	NC	6	GND
7	CAN1_D+	8	NC
9	NC	10	NC

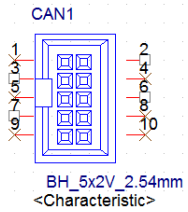


Table 3.36: CAN1 CAN Bus Connector (A2 & A3)

Pin	Signal	Pin	Signal
1	NC	2	CAN1_D-
3	GND	4	NC
5	NC	6	GND
7	CAN1_D+	8	NC
9	NC	10	NC

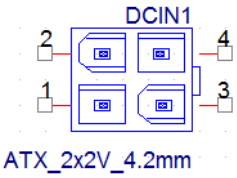


Table 3.37: DCIN1 Wide-Range DC Input Connector 1 (A1)

Pin	Signal	Pin	Signal
1	GND	3	+VDC
2	GND	4	+VDC

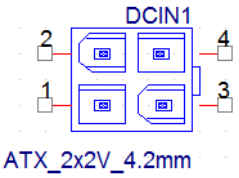


Table 3.38: DCIN1 Wide-Range DC Input Connector1 (A2 & A3)			
Pin	Signal	Pin	Signal
1	GND	3	+VDC
2	GND	4	+VDC

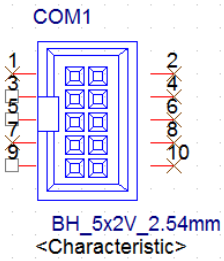


Table 3.39: COM1 COM Port 1 Connector (A1)			
Pin	**Signal**	**Pin**	**Signal**
1	NC	2	NC
3	COM1_RX	4	NC
5	COM1_TX	6	NC
7	NC	8	NC
9	GND	10	NC

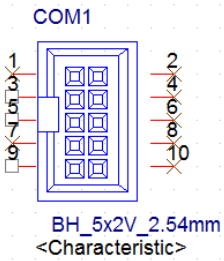


Table 3.40: COM1 COM Port1 Connector (A2 & A3)			
Pin	**Signal**	**Pin**	**Signal**
1	NC	2	NC
3	COM1_RX	4	NC
5	COM1_TX	6	NC
7	NC	8	NC
9	GND	10	NC

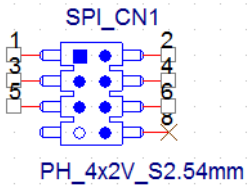


Table 3.41: SPI_CN1 SPI BIOS Pin Header (A1)

Pin	Signal	Pin	Signal
1	+V3.3M_SPI_J	2	GND
3	Q_SPI_PH_CS#	4	Q_SPI_PH_CLK
5	Q_SPI_PH_MISO	6	Q_SPI_PH_MOSI
X		8	NC

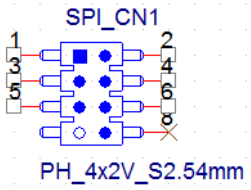


Table 3.42: SPI_CN1 SPI BIOS Pin Header (A2 & A3)

Pin	Signal	Pin	Signal
1	+V3.3M_SPI_J	2	GND
3	Q_SPI_PH_CS#	4	Q_SPI_PH_CLK
5	Q_SPI_PH_MISO	6	Q_SPI_PH_MOSI
X		8	NC

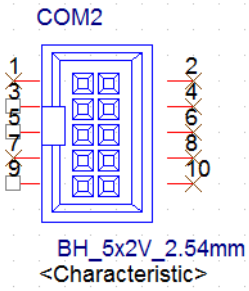


Table 3.43: COM2 COM Port 2 Connector (A1)

Pin	Signal	Pin	Signal
1	NC	2	NC
3	COM2_RX	4	NC
5	COM2_TX	6	NC
7	NC	8	NC
9	GND	10	NC

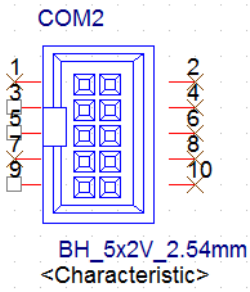


Table 3.44: COM2 COM Port2 Connector (A2 & A3)

Pin	Signal	Pin	Signal
1	NC	2	NC
3	COM2_RX	4	NC
5	COM2_TX	6	NC
7	NC	8	NC
9	GND	10	NC

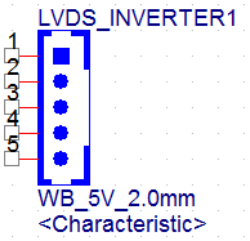


Table 3.45: LVDS_INVERTER1 LVDS Inverter Connector (A1)

Pin	Signal
1	+V12_Z_LVDS
2	GND
3	LVDS_BKLT_Z_EN#
4	LVDS_Z_VBR
5	+V5_LVDS

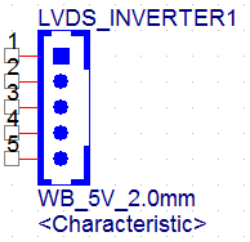


Table 3.46: LVDS_INVERTER1 LVDS INVERTER Connector (A2 & A3)

Pin	Signal
1	+V12_Z_LVDS
2	GND
3	LVDS_BKLT_Z_EN#
4	LVDS_Z_VBR
5	+V5_LVDS

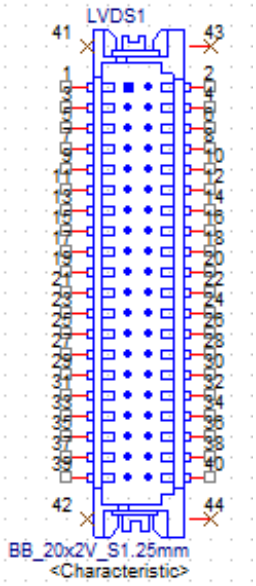


Table 3.47: LVDS1 LVDS Connector (A1)

Pin	Signal	Pin	Signal
1	+VLVDS_PANEL_PWR	2	+VLVDS_PANEL_PWR
3	GND	4	GND
5	+VLVDS_PANEL_PWR	6	+VLVDS_PANEL_PWR
7	LVDS0_Z_D0-	8	LVDS1_Z_D0-
9	LVDS0_Z_D0+	10	LVDS1_Z_D0+
11	GND	12	GND
13	LVDS0_Z_D1-	14	LVDS1_Z_D1-
15	LVDS0_Z_D1+	16	LVDS1_Z_D1+
17	GND	18	GND
19	LVDS0_Z_D2-	20	LVDS1_Z_D2-
21	LVDS0_Z_D2+	22	LVDS1_Z_D2+
23	GND	24	GND
25	LVDS0_Z_CLK-	26	LVDS1_Z_CLK-
27	LVDS0_Z_CLK+	28	LVDS1_Z_CLK+
29	GND	30	GND
31	LVDS_Z_DDC_CLK_eDP_AUX+	32	LVDS_Z_DDC_DAT_eDP_AUX-
33	GND	34	EDP_HDP_A
35	LVDS0_Z_D3-	36	LVDS1_Z_D3-
37	LVDS0_Z_D3+	38	LVDS1_Z_D3+
39	Pull-low via 4.7Kohm to GND	40	LVDS1_CTRL

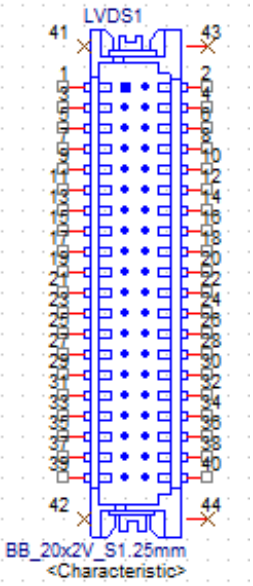


Table 3.48: LVDS1 LVDS Connector (A2)

Pin	Signal	Pin	Signal
1	+VLVDS_PANEL_PWR	2	+VLVDS_PANEL_PWR
3	+VLVDS_PANEL_PWR	4	+VLVDS_PANEL_PWR
5	GND	6	GND
7	LVDS1_Z_CLK-	8	LVDS1_Z_CLK+
9	GND	10	LVDS1_Z_D3-
11	LVDS1_Z_D3+	12	GND
13	LVDS1_Z_D2-	14	LVDS1_Z_D2+
15	GND	16	LVDS1_Z_D1-
17	LVDS1_Z_D1+	18	GND
19	LVDS1_Z_D0-	20	LVDS1_Z_D0+
21	EDP_HDP_A	22	LVDS1_CTRL
23	LVDS_Z_DDC_CLK_eD-P_AUX+	24	LVDS_Z_DDC_DAT_eD-P_AUX-
25	GND	26	LVDS0_Z_CLK+
27	LVDS0_Z_CLK-	28	GND
29	LVDS0_Z_D3-	30	LVDS0_Z_D3+
31	GND	32	LVDS0_Z_D2-
33	LVDS0_Z_D2+	34	GND
35	LVDS0_Z_D1-	36	LVDS0_Z_D1+
37	GND	38	LVDS0_Z_D0-
39	LVDS0_Z_D0+	40	Pull-low via 4.7Kohm to GND

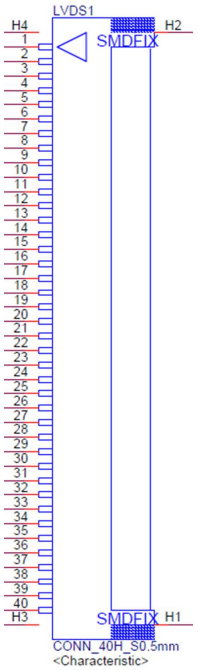


Table 3.49: LVDS1 LVDS Connector (A3)

Pin	Signal	Pin	Signal
1	LVDS1_CTRL	2	GND
3	LVDS1_Z_CLK-	4	LVDS1_Z_CLK+
5	GND	6	LVDS1_Z_D0-
7	LVDS1_Z_D0+	8	GND
9	LVDS1_Z_D1-	10	LVDS1_Z_D1+
11	GND	12	LVDS1_Z_D2-
13	LVDS1_Z_D2+	14	GND
15	LVDS_Z_DDC_CLK_eD-P_AUX+	16	LVDS_Z_DDC_CLK_eD-P_AUX-
17	GND	18	LVDS1_Z_D3-
19	LVDS1_Z_D3+	20	GND
21	LVDS0_Z_CLK+	22	LVDS0_Z_CLK-
23	GND	24	LVDS0_Z_D3-
25	LVDS0_Z_D3+	26	GND
27	LVDS0_Z_D2-	28	LVDS0_Z_D2+
29	GND	30	LVDS0_Z_D1-
31	LVDS0_Z_D1+	32	GND
33	LVDS0_Z_D0-	34	LVDS0_Z_D0+
35	EDP_HPD_A	36	Pull-low via 4.7Kohm to GND
37	+VLVDS_PANEL_PWR	38	+VLVDS_PANEL_PWR
39	+VLVDS_PANEL_PWR	40	+VLVDS_PANEL_PWR

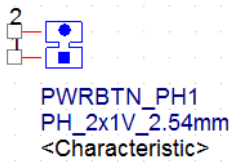


Table 3.50: PWRBTN_PH1 PWRBTN Pin Header (A1)

Pin	Signal
1	GND
2	PWRBTN#

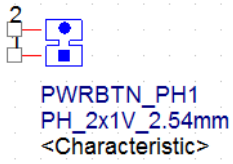


Table 3.51: PWRBTN_PH1 PWRBTN Pin Header (A2 & A3)

Pin	Signal
1	GND
2	PWRBTN#

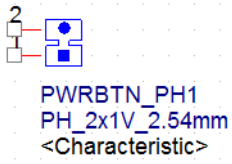


Table 3.52: SYS_RESET_PH1 SYS Reset Pin Header (A1)

Pin	Signal
1	GND
2	PM_EXTRST#

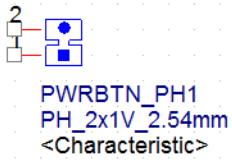


Table 3.53: SYS_RESET_PH1 SYS RESET Pin Header (A2 & A3)

Pin	Signal
1	GND
2	PM_EXTRST#

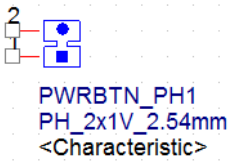


Table 3.54: SATA_ACT_PH1 SATA ACT# Pin Header (A1)

Pin	Signal
1	SATA_ACT#
2	Pull-up via 330 ohm to +V3.3

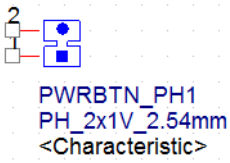


Table 3.55: SATA_ACT_PH1 SATA ACT# Pin Header (A2 & A3)

Pin	Signal
1	SATA_ACT#
2	Pull-up via 330 ohm to +V3.3

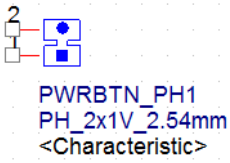


Table 3.56: PWR_LED_PH1 Power LED Pin Header (A1)

Pin	Signal
1	GND
2	Pull-up via 330 ohm to +V5

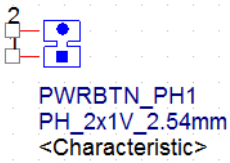


Table 3.57: PWR_LED_PH1 Power LED Pin Header (A2 & A3)

Pin	Signal
1	GND
2	Pull-up via 330 ohm to +V5

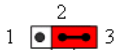


Table 3.58: CN7/CN5/CN8/CN6 BIOS Selection (A2)	
Pin	**Function**
1-2	To SOIC8 Socket
2-3	To QFN Socket [Default]

3.1.9 Jumper Settings

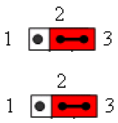


Table 3.59: BIOS_DIS0/BIOS_DIS1 BIOS Disable 0/BIOS Disable 1 (A1)						
BIOS_DIS1# (BIOS_DIS1)	**BIOS_DIS0# (BIOS_DIS0)**	**Chipset SPI CS1# Destination**	**Chipset SPI CS0# Destination**	**Carrier SPI_CS#**	**SPI Descriptor**	**BIOS Entry**
2-3 (1)	2-3 (1)	Module	Module	High	Module	SPI0/SPI1 [default]
1-2 (0)	2-3 (1)	Module	Carrier	SPI0	Carrier	SPI0/SPI1
1-2 (0)	1-2 (0)	Carrier	Module	SPI1	Module	SPI0/SPI1

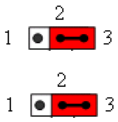


Table 3.60: BIOS_DIS0/BIOS_DIS1 BIOS Disable0, BIOS Disable1 (A2 & A3)						
BIOS_DIS1# (BIOS_DIS1)	BIOS_DIS0# (BIOS_DIS0)	Chipset SPI CS1# Destination	Chipset SPI CS0# Destination	Carrier SPI_CS#	SPI Descriptor	BIOS Entry
2-3 (1)	2-3 (1)	Module	Module	High	Module	SPI0/SPI1 [Default]
1-2 (0)	2-3 (1)	Module	Carrier	SPI0	Carrier	SPI0/SPI1
1-2 (0)	1-2 (0)	Carrier	Module	SPI1	Module	SPI0/SPI1

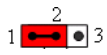


Table 3.61: J16, J17 SOM-DB5830 Voltage Input (VIN) Selection (A1)	
Pin	**Function**
J16 1-2 J17 1-2	Supply ATX (+V12) to VIN [default]
J16 2-3 J17 2-3	Supply DCIN (+VDC) to VIN

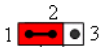


Table 3.62: J16, J17 SOM-DB5830 Voltage Input (VIN) Selection (A2 & A3)	
Pin	**Function**
J16 1-2 J17 1-2	Supply ATX (+V12) to VIN [Default]
J16 2-3 J17 2-3	Supply DCIN (+VDC) to VIN

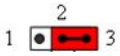


Table 3.63: PSON1 ATX/AT Mode Selection (A1)	
Pin	**Function**
1-2	AT Mode
2-3	ATX Mode [default]

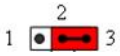


Table 3.64: PSON1 ATX / AT Mode Selection (A2 & A3)	
Pin	**Function**
1-2	AT Mode
2-3	ATX Mode [Default]

Table 3.65: J1 COMe Module +V5SB Supply (A1)	
Pin	**Function**
1-X 3-X	Not supply +V5SB to COMe module
1-2 3-4	Supply +V5SB to COMe module [default]

Table 3.66: J1 COMe Module +V5SB Supply (A2 & A3)	
Pin	**Function**
1-X 3-X	Not supply +V5SB to COMe Module
1-2 3-4	Supply +V5SB to COMe Module [Default]

Table 3.67: J3 Carrier Board SPI Power Supply (A1)	
Pin	**Function**
1-2	Carrier board SPI power supply [default]
1-X	Carrier board SPI no power

Table 3.68: J3 Carrier Board SPI power supply (A2 & A3)	
Pin	**Function**
1-2	Carrier Board SPI power supply [Default]
1-X	Carrier Board SPI no power

Table 3.69: J13 COMe Module TPM Disable (A1)	
Pin	**Function**
1-X	COMe module TPM enable [default]
1-2	COMe module TPM disable

Table 3.70: J13 COMe Module TPM Disable (A2 & A3)	
Pin	**Function**
1-X	COMe Module TPM Enable [Default]
1-2	COMe Module TPM Disable

Table 3.71: J12 Carrier Board TPM Disable (A1)	
Pin	**Function**
1-X	Carrier board TPM enable [default]
1-2	Carrier board TPM disable

Table 3.72: J12 Carrier Board TPM Disable (A2 & A3)	
Pin	**Function**
1-X	Carrier Board TPM Enable [Default]
1-2	Carrier Board TPM Disable

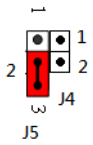


Table 3.73: J4, J5 LVDS_PWR Selection (A1)	
Pin	**Function**
J5 2-3	LVDS_PWR is +V3.3 [default]
J5 1-2	LVDS_PWR is +V5
J4 2 - J5 2	LVDS_PWR is +V12

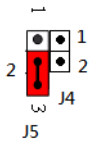


Table 3.74: J4, J5 LVDS_PWR selection (A2 & A3)	
Pin	**Function**
J5 2-3	LVDS_PWR is +V3.3 [Default]
J5 1-2	LVDS_PWR is +V5
J4 2 - J5 2	LVDS_PWR is +V12

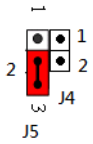


Table 3.75: J4, J5 LVDS_PWR selection (A2 & A3)	
Pin	**Function**
J5 2-3	LVDS_PWR is +V3.3 [Default]
J5 1-2	LVDS_PWR is +V5
J4 2 - J5 2	LVDS_PWR is +V12

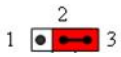


Table 3.76: J2 Normal Operation / Clear CMOS Selection (A1)	
Pin	**Function**
1-2	Clear CMOS
2-3	Normal operation [default]

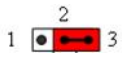


Table 3.77: J2 Normal Operation / Clear CMOS Selection (A2 & A3)	
Pin	**Function**
1-2	Clear CMOS
2-3	Normal Operation [Default]

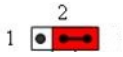


Table 3.78: CB_PWROK Power OK Signal Pull Down \ Floating Selection (A1)	
Pin	**Function**
1-2	POWROK signal pull down
2-3	POWROK signal connect to module [default]
2-X	POWROK signal floating

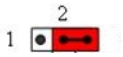


Table 3.79: CB_PWROK Power PK Signal Pull Down \ Floating Selection (A2 & A3)	
Pin	**Function**
1-2	POWROK Signal Pull Down
2-3	POWROK Signal connect to Module [Default]
2-X	POWROK Signal Floating

Table 3.80: J7 EDP/LVDS HPD Selection (A1)	
Pin	**Function**
1-2	LVDS HPD [default]
2-3	EDP HPD

Table 3.81: J7 EDP / LVDS HPD Selection (A2 & A3)	
Pin	**Function**
1-2	LVDS HPD [Default]
2-3	EDP HPD

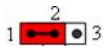


Table 3.82: COM_CAN_TX COM TX/CAN TX SEL (A1)

Pin	Function
1-2	COM port TX [default]
2-3	CAN bus TX

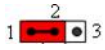


Table 3.83: COM_CAN_TX COM TX / CAN TX SEL (A2 & A3)

Pin	Function
1-2	COM port TX [Default]
2-3	CAN BUS TX

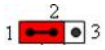


Table 3.84: COM_CAN_RX COM RX/CAN RX SEL (A1)

Pin	Function
1-2	COM port RX [default]
2-3	CAN bus RX

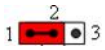


Table 3.85: COM_CAN_RX COM RX / CAN RX SEL (A2 & A3)

Pin	Function
1-2	COM port RX [Default]
2-3	CAN BUS RX

Table 3.86: J6 LVDS_Inverter Selection (A1)

Pin	Function
1-2	Inverter is +V5 [default]
2-3	Inverter is +V12

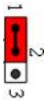


Table 3.87: J6 LVDS_INVERTER Selection (A2 & A3)

Pin	Function
1-2	INVERTER is +V5 [Default]
2-3	INVERTER is +V12

Table 3.88: J8 GPIO_SDIO_SEL (A1)

Pin	Function
1-2	SD card
2-3	GPIO [default]

Table 3.89: J8 GPIO_SDIO_SEL (A2 & A3)

Pin	Function
1-2	SD card
2-3	GPIO [Default]

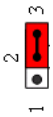


Table 3.90: J11 ESPI Reset SEL (A1)

Pin	Function
1-2	PLRST# [default]
2-3	ESPI reset#

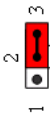


Table 3.91: J11 ESPI Reset SEL (A2 & A3)

Pin	Function
1-2	PLRST# [Default]
2-3	ESPI RESET#

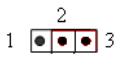


Table 3.92: J10 ESPI EN and Disable SEL (A1)

Pin	Function
1-2	ESPI disable
2-3	ESPI EN
1-X	LPC [default]

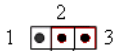


Table 3.93: J10 ESPI EN & Disable SEL (A2 & A3)	
Pin	**Function**
1-2	ESPI EN
2-3	ESPI Disable

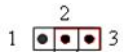


Table 3.94: J9 ESPI_SAFS Selection (A1)	
Pin	**Function**
1-2	ESPI_SAFS mode
2-3	ESPI_SAFS disable

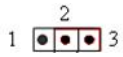


Table 3.95: J9 ESPI_SAFS Selection (A2 & A3)	
Pin	**Function**
1-2	ESPI_SAFS mode
2-3	ESPI_SAFS disable

Table 3.96: PEG_LAN_RV1 PCIe GFX Reverse Lane Order (A1)	
Pin	**Function**
1-2	PCIe GFX lane reverse
1-X	Normal [default]

Table 3.97: PEG_LAN_RV1 PCIe GFX Reverse Lane Order (A2 & A3)	
Pin	**Function**
1-2	PCIe GFX lane reverse
1-X	Normal [Default]

Table 3.98: SMB_ALT1 SMB_ALT# (A1)	
Pin	**Function**
1-2	SMBus alert
1-X	Normal [default]

Table 3.99: SMB_ALT1 SMB_ALT# (A2 & A3)	
Pin	**Function**
1-2	SMBus Alert
1-X	Normal [Default]

Table 3.100: J14 COMe R3.0 Support Type SEL (Type 6 / Type 10) (A1)	
Pin	**Function**
1-2	Support type enable [default]
1-X	Support type disable (for Type 10 module)

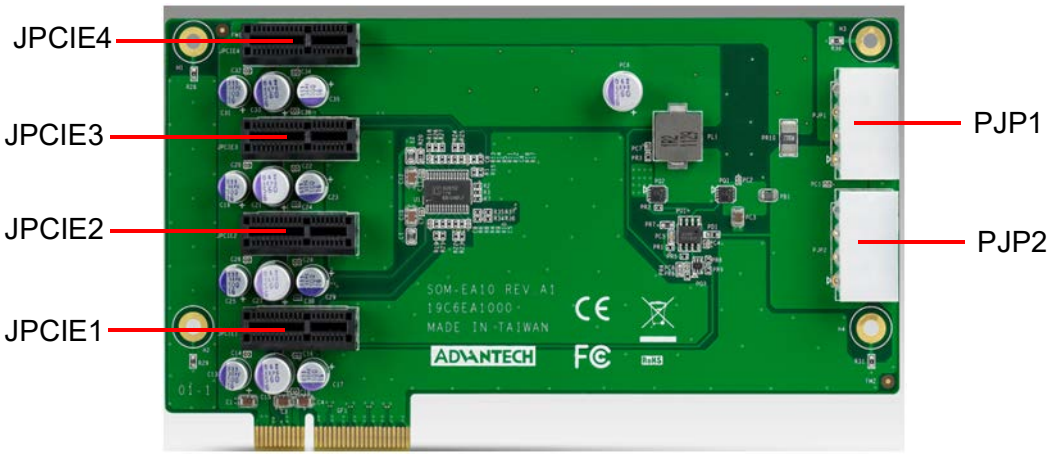
Table 3.101: J14 COMe R3.0 support Type SEL (A2 & A3)	
Pin	**Function**
1-2	Support Type enable [Default]
1-X	Support Type disable

Chapter 4

SOM-EA10

4.1 SOM-EA10

4.1.1 Connector Layout

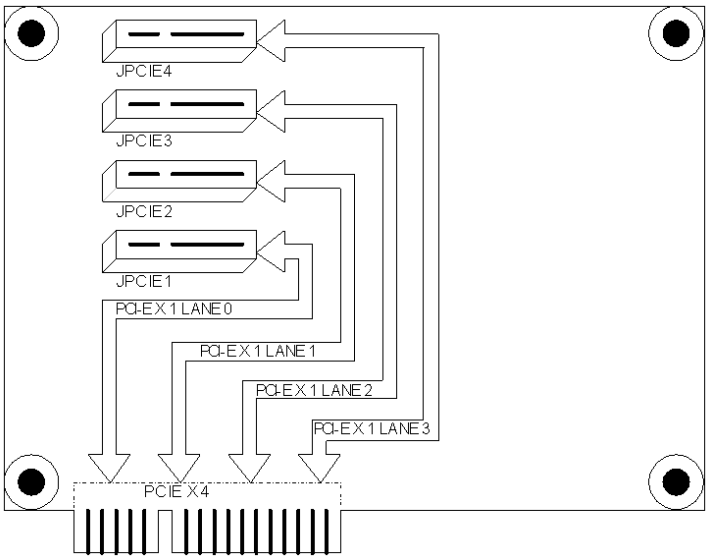


4.1.2 Connector List

Table 4.1: Connector List

Label	Function
JPCIE1	PCIe x1 Port 1 connector
JPCIE2	PCIe x1 Port 2 connector
JPCIE3	PCIe x1 Port 3 connector
JPCIE4	PCIe x1 Port 4 connector
PJP1	4P power connector
PJP2	4P power connector

4.1.3 SOM-EA10 Block Diagram



ADVANTECH

Enabling an Intelligent Planet

www.advantech.com

Please verify specifications before quoting. This guide is intended for reference purposes only.