

Approval Sheet

Customer	
Product Number	M3U0-4GSJACN9
Module speed	PC3-10600
Pin	240pin
Cl-tRCD-tRP	9-9-9
SDRAM Operating Temp	0°C ~85°C
Date	19 th December 2013

Approval by Customer

P/N:

Signature:

Date:

Sales: _____

Sr. Technical Manager: John Hsieh

Rev 1.0

1. Features

Key Parameter

Industry Nomenclature	Speed Grade	Data Rate MT/s			tAA (ns)	tRCD (ns)	tRP (ns)	tRC (ns)
		CL=7	CL=9	CL=11				
PC3-10600	N	1066	1333	1333	13.5	13.5	13.5	49.5

- JEDEC Standard 240-pin Dual In-Line Memory Module
- Intend for PC3-10600 applications
- Inputs and Outputs are SSTL-15 compatible
- VDD=VDDQ= 1.5 Volt \pm 0.075
- Bi-directional Differential Data Strobe
- DLL aligns DQ and DQS transition with CK transition
- SDRAMs have 8 internal banks for concurrent operation
- Normal and Dynamic On-Die Termination support.
- SDRAMs are 78-ball BGA Package
- 8 bit pre-fetch
- Two different termination values (Rtt_Nom & Rtt_WR)
- Auto & self refresh 7.8 μ s ($T_A \leq +85^\circ\text{C}$)
- 15/10/2 Addressing (row/column/rank)-4GB
- SDRAM operating temperature range $0^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$
- Programmable Device Operation:
 - Burst Type: Sequential or Interleave
 - Device CAS# Latency: 7, 9
 - Burst Length: switch on-the-fly: BL=8 or BC 4
- RoHS Compliant (*Section 14*)

2. Environmental Requirements

iDIMM are intended for use in standard office environments that have limited capacity for heating and air conditioning.

Symbol	Parameter	Rating	Units	Notes
TOPR	Operating Temperature (ambient)	0 to +65	°C	1
TSTG	Storage Temperature	-55 to +150	°C	
HOPR	Operating Humidity (relative)	10 to 90	%	
HSTG	Storage Humidity (without condensation)	5 to 95	%	
PBAR	Barometric Pressure (operating & storage)	105 to 69	K Pascal	1,2

1. The component maximum case temperature (Tcase) shall not exceed the value specified in the DDR DRAM component specification.
 2. Up to 9850 ft.

3. SDRAM Parameters by device density

RTT_Nom Setting	Parameter	2Gb	Units
tRFC	REF command ACT or REF command time	160	ns
tREFI	Average periodic refresh interval	0°C ≤ TCASE ≤ 85°C	7.8 μs
		85°C ≤ TCASE ≤ 95°C	3.9 μs

4. Ordering Information

UDIMM						
Part Number	Density	Speed	Organization	Number of DRAM	Number of rank	ECC
M3U0-4GSJACN9	4GB	PC3-10600	512Mx64	16	2	N

5. Pin Configurations (Front side/Back side) X64 UDIMM

Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back	Pin	Front	Pin	Back
1	VREFDQ	121	VSS	31	DQ25	151	VSS	61	A2	181	A1	91	DQ41	211	VSS
2	VSS	122	DQ4	32	VSS	152	DM3, DQS12, TDQS12	62	VDD	182	VDD	92	VSS	212	DM5, DQS14, TDQS14
3	DQ0	123	DQ5	33	DQS3#	153	NC, DQS12#, TDQS12#	63	NC, CK1	183	VDD	93	DQS5#	213	NC, DQS14#, TDQS14#
4	DQ1	124	VSS	34	DQS3	154	VSS	64	NC, CK1#	184	CK0	94	DQS5	214	VSS
5	VSS	125	DM0, DQS9, TDQS9	35	VSS	155	DQ30	65	VDD	185	CK#0	95	VSS	215	DQ46
6	DQS0#	126	NC, DQS9#, TDQS9#	36	DQ26	156	DQ31	66	VDD	186	VDD	96	DQ42	216	DQ47
7	DQS0	127	VSS	37	DQ27	157	VSS	67	VREFCA	187	EVENT#, NC	97	DQ43	217	VSS
8	VSS	128	DQ6	38	VSS	158	CB4,NC	68	PAR_IN,NC	188	A0	98	VSS	218	DQ52
9	DQ2	129	DQ7	39	CB0,NC	159	CB5,NC	69	VDD	189	VDD	99	DQ48	219	DQ53
10	DQ3	130	VSS	40	CB1,NC	160	VSS	70	A10/AP	190	BA1	100	DQ49	220	VSS
11	VSS	131	DQ12	41	VSS	161	DM8, DQS17, TDQS17	71	BA0	191	VDD	101	VSS	221	DM6, DQS15, TDQS15
12	DQ8	132	DQ13	42	DQS8#	162	NC, DQS17#, TDQS17#	72	VDD	192	RAS#	102	DQS6#	222	NC, DQS15#, TDQS15#
13	DQ9	133	VSS	43	DQS8	163	VSS	73	WE#	193	S0#	103	DQS6	223	VSS
14	VSS	134	DM1, DQS10, TDQS10	44	VSS	164	CB6,NC	74	CAS#	194	VDD	104	VSS	224	DQ54
15	DQS1#	135	NC, DQS10#, TDQS10#	45	CB2,NC	165	CB7,NC	75	VDD	195	ODT0	105	DQ50	225	DQ55
16	DQS1	136	VSS	46	CB3,NC	166	VSS	76	S1#,NC	196	A13	106	DQ51	226	VSS
17	VSS	137	DQ14	47	VSS	167	NC	77	ODT1,NC	197	VDD	107	VSS	227	DQ60
18	DQ10	138	DQ15	48	VTT,NC	168	RESET#	78	VDD	198	S3#,NC	108	DQ56	228	DQ61
19	DQ11	139	VSS	49	VTT,NC	169	CKE1,NC	79	S2#,NC	199	VSS	109	DQ57	229	VSS
20	VSS	140	DQ20	50	CKE0	170	VDD	80	VSS	200	DQ36	110	VSS	230	DM7, DQS16, TDQS16
21	DQ16	141	DQ21	51	VDD	171	A15,NC	81	DQ32	201	DQ37	111	DQS7#	231	NC, DQS16#, TDQS16#
22	DQ17	142	VSS	52	BA2	172	A14	82	DQ33	202	VSS	112	DQS7	232	VSS
23	VSS	143	DM2, DQS11, TDQS11	53	ERR_Out#, NC	173	VDD	83	VSS	203	DM4, DQS13, TDQS13	113	VSS	233	DQ62
24	DQS2#	144	NC, DQS11#, TDQS11#	54		174	A12/BC#	84	DQS4#	204	NC, DQS13#, TDQS13#	114	DQ58	234	DQ63
25	DQS2	145	VSS	55	A11	175	A9	85	DQS4	205	VSS	115	DQ59	235	VSS
26	VSS	146	DQ22	56	A7	176	VDD	86	VSS	206	DQ38	116	VSS	236	VDDSPD
27	DQ18	147	DQ23	57	VDD	177	A8	87	DQ34	207	DQ39	117	SA0	237	SA0
28	DQ19	148	VSS	58	A5	178	A6	88	DQ35	208	VSS	118	SCL	238	SA1
29	VSS	149	DQ28	59	A4	179	VDD	89	VSS	209	DQ44	119	SA2	239	VSS
30	DQ24	150	DQ29	60	VDD	180	A3	90	DQ40	210	DQ45	120	VTT	240	VTT

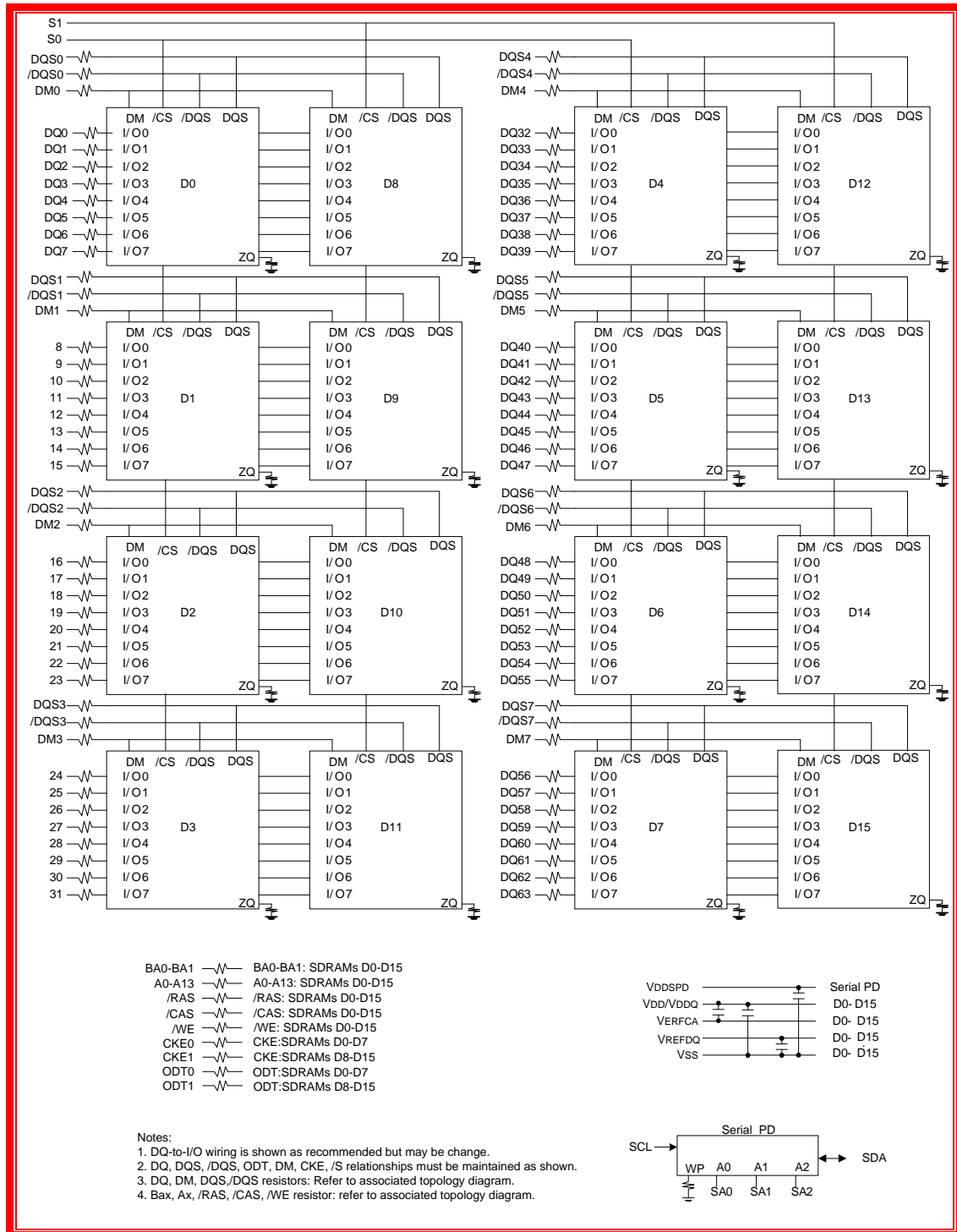
NC = No Connect, RFU = Reserved for Future Use

6. Architecture

Pin Definition

Pin Name	Description	Pin Name	Description
A0 - A13 (A14 or A15)	SDRAM address bus	SCL	Serial Presence Detect Clock Input
BA0 - BA1 (or BA2)	SDRAM Bank Address Inputs	SDA	Serial Presence Detect Data input/output
/RAS	SDRAM row address strobe	SA0 – SA2	Serial Presence Detect Address Inputs
/CAS	SDRAM column address strobe	VDD	Power Supply
/WE	SDRAM write enable	VDDID	VDD Identification Flag
/S0 - /S1	DIMM Rank Select Lines	VDDQ	SDRAM I/O Driver power supply
CK0 – CKE1	SDRAM clock enable lines	VREFDQ	SDRAM I/O Reference supply
DQ0 – DQ63	DIMM memory data bus	VREFCA	SDRAM Command/address reference supply.
CB0 – CB7	DIMM ECC check bit	VSS	Ground
DQS0 – DQS8 /DQS0-/DQS8	SDRAM data strobes	VDDSPD	Serial EEPROM positive power supply
DM0 – DM8	SDRAM data masks	NC	Spare Pin
ODT0-ODT1	Spare Pin	/Reset	Reset enable
CK0 – CK1 /CK0 - /CK1	Differential SDRAM Clocks	Event#	Reserved for optional temperature-sensing hardware
RSVD	Reserved for future use.	VTT	SDRAM I/O termination supply.

7. Function Block Diagram: - (4 GB, 2 Ranks, 256Mx8 DDR3 SDRAMs)



8. DRAM Absolute Maximum Ratings

Symbol	Parameter	Rating	Units	Note	
T_{OPER}	Operation Temperature	Normal Operating Temp.	0 to 85	°C	1,2
		Extended Temp.(optional)	85 to 95	°C	1,3
T_{STG}	Storage Temperature	-55 to 100	°C	4,5	
V_{IN}, V_{OUT}	Voltage on any pins relative to V _{ss}	-0.4 to +1.975	V	4	
V_{DD}	Voltage on VDD supply relative to V _{ss}	-0.4 to +1.975	V	4,6	
V_{DDQ}	Voltage on VDDQ supply relative to V _{ss}	-0.4 to +1.975	V	4,6	

Note:

1. Operating Temperature T_{OPER} is the case surface temperature on the center / top side of the DRAM.

For measurement conditions, please refer to the JEDEC document JESD51-2.

2. The Normal Temperature Range specifies the temperatures where all DRAM specifications will be supported. During operation, the DRAM case temperature must be maintained between 0 to 85 °C under all operating conditions.

3. Some applications require operation of the DRAM in the Extended Temperature Range between 85 °C and 95 °C case temperature. Full specifications are supported in this range, but the following additional conditions apply:

- a) Refresh commands must be doubled in frequency, therefore reducing the Refresh interval tREFI to 3.9 μs. It is also possible to specify a component with 1X refresh (tREFI to 7.8μs) in the Extended Temperature Range. Please refer to supplier data sheet and/or the DIMM SPD for option availability.
- b) If Self-Refresh operation is required in the Extended Temperature Range, then it is mandatory to either use the Manual Self-Refresh mode with Extended Temperature Range capability (MR2 A6 =0b and MR2 A7 = 1b) or enable the optional Auto Self-Refresh mode (MR2 A6 = 1b and MR2 A7 =0b). Please refer to the supplier data sheet and/or the DIMM SPD for Auto Self-Refresh option availability, Extended Temperature Range support and tREFI requirements in the Extended Temperature Range.

4. Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

5. Storage Temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JESD51-2 standard.

6. VDD and VDDQ must be within 300 mV of each other at all times;and VREF must be not greater than 0.6 x VDDQ, When VDD and VDDQ are less than 500 mV; VREF may be equal to or less than 300 mV

9. DRAM AC & DC Operating

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Recommended DC Operating Conditions						
V_{DD}	Supply Voltage	1.425	1.5	1.575	V	1,2
V_{DDQ}	Supply Voltage	1.425	1.5	1.575	V	1,2
Single Ended AC/DC Input Levels						
V_{IH} (DC)	DC Input High (Logic1) Voltage	$V_{REF} + 0.1$	-	V _{DD}	V	3
V_{IL} (DC)	DC Input Low (Logic 0) Voltage	V _{SS}	-	$V_{REF} - 0.1$	V	3
V_{IH} (AC)	AC Input High (Logic1) Voltage	$V_{REF} + 0.175$	-	-	V	3
V_{IL} (AC)	AC Input Low (Logic 0) Voltage	-	-	$V_{REF} - 0.175$	V	3
V_{REFDQ} (DC)	Reference Voltage for DQ, DM inputs	$0.49V_{DDQ}$	$0.5V_{DDQ}$	$0.51V_{DDQ}$	V	4,5
V_{REFCA} (DC)	Reference Voltage for ADD,CMD inputs	$0.49V_{DDQ}$	$0.5V_{DDQ}$	$0.51V_{DDQ}$	V	4,5
Single Ended AC/DC output Levels						
V_{OH} (DC)	DC output high measurement level (for IV curve linearity)	-	$0.8 \times V_{DDQ}$	-	V	
V_{OM} (DC)	DC output mid measurement level (for IV curve linearity)	-	$0.5 \times V_{DDQ}$	-	V	
V_{OL} (DC)	DC output low measurement level (for IV curve linearity)	-	$0.2 \times V_{DDQ}$	-	V	
V_{OH} (AC)	AC output high measurement level (for output SR)	-	$V_{TT} + 0.1 \times V_{DDQ}$	-	V	6
V_{OL} (AC)	AC output low measurement level (for output SR)	-	$V_{TT} - 0.1 \times V_{DDQ}$	-	V	6

Symbol	Parameter	Min	Typ.	Max	Units	Notes
Differential AC/DC Input Levels						
V_{IHdiff}	Differential Input high	+0.2	-	Note 9	V	7
V_{ILdiff}	Differential Input logic Low	Note 9	-	-0.2	V	7
V_{IHdiff(ac)}	Differential Input high ac	2* (V _{IH (AC)} - V _{REF})	-	Note 9	V	8
V_{ILdiff(ac)}	Differential Input logic Low ac	Note 9	-	2* (V _{REF} - V _{IL (AC)})	V	8
Differential AC and DC Output Levels						
V_{OHdiff(AC)}	AC differential output high measurement level (for output SR)	-	+ 0.2 x V _{DDQ}	-	V	10
V_{OLdiff(AC)}	AC differential output low measurement level (for output SR)	-	- 0.2 x V _{DDQ}	-	V	10
Note:						
<ol style="list-style-type: none"> Under all conditions V_{DDQ} must be less than or equal to V_{DD}. V_{DDQ} tracks with V_{DD}. AC parameters are measured with V_{DD} and V_{DDQ} tied together. For DQ and DM, V_{ref} = V_{refDQ}. For input only pins except RESET#, V_{ref} = V_{refCA}. The ac peak noise on V_{Ref} may not allow V_{Ref} to deviate from V_{Ref(DC)} by more than +/-1% V_{DD} (for reference: approx. +/- 15 mV). For reference: approx. V_{DD}/2 +/- 15 mV. The swing of ± 0.1 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 Used to define a differential signal slew-rate. For CK - CK# use V_{IH}/V_{IL(ac)} of ADD/CMD and V_{REFCA}; for DQS - DQS#, DQSL, DQSL#, DQSU, DQSU# use V_{IH}/V_{IL(ac)} of DQs and V_{REFDQ}; if a reduced ac-high or ac-low level is used for a signal group, then the reduced level applies also here. These values are not defined, however the single-ended signals CK, CK#, DQS, DQS#, DQSL, DQSL#, DQSU, DQSU# need to be within the respective limits (V_{IH(dc)} max, V_{IL(dc)} min) for single- ended signals as well as the limitations for overshoot and undershoot. The swing of ± 0.2 × V_{DDQ} is based on approximately 50% of the static single-ended output high or low swing with a driver impedance of 40 Ω and an effective test load of 25 Ω to V_{TT} = V_{DDQ}/2 at each of the differential outputs. 						

10. Operating, Standby, and Refresh Currents

- 4GB UDIMM (2 Ranks, 256Mx8 DDR3 SDRAMs $T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$)

Symbol	Parameter/Condition		PC3-10600	Unit
I DD0	One bank; Active - Precharge		1740	mA
I DD1	One bank; Active - Read - Precharge		1720	mA
I DD2N	Precharge Standby Current		1300	mA
IDD2NT	Precharge Standby ODT Current		1380	mA
I DD2P	Precharge Power Down Current	1060	560	mA
	Precharge Power Down Current	392	192	mA
I DD2Q	Precharge Quiet Standby Current		1300	mA
I DD3N	Active Standby Current		1360	mA
I DD3P	Active Power-Down Current		590	mA
I DD4R	Operating Current Burst Read		2040	mA
I DD4W	Operating Current Burst Write		2080	mA
I DD5B	Burst Refresh Current		2480	mA
I DD6	Self-Refresh Current: Normal Temperature Range		400	mA
I DD6ET	Self-Refresh Current: Extended Temperature Range		480	mA
I DD6TC	Auto Self-Refresh Current		480	mA
I DD7	Operating Bank Interleave Read Current		2740	mA

11. Timing Parameters

($T_{CASE} = 0\text{ }^{\circ}\text{C} \sim 70\text{ }^{\circ}\text{C}$; $V_{DDQ} = V_{DD}$, See AC Characteristics)

Symbol	Parameter	PC3-10600		Unit
		Min.	Max.	
Clock Timing				
tCK (DLL-Off)	Minimum Clock Cycle Time	8	-	ns
tCK (avg)	Average Clock Period	1.5	3.3	ns
tCH (avg)	Average high pulse width	0.47	0.53	tCK (avg)
tCL (avg)	Average low pulse width	0.47	0.53	tCK (avg)
tCK (abs)	Absolute Clock Period	tCK(avg) min + tJIT(per) min	tCK(avg) max + tJIT(per) max -	Ps
tCH (abs)	Absolute high pulse width	0.43	-	tCK (avg)
tCL (abs)	Absolute low pulse width	0.43	-	tCK (avg)
JIT (per)	Clock Period Jitter	-80	80	Ps
TJIT (per, lck)	Clock Period Jitter during DLL locking period.	-70	70	Ps
JIT (CC)	Cycle to Cycle Period Jitter	160		Ps
TJIT (CC, lck)	Cycle to Cycle Period Jitter during DLL locking period.	140		Ps
TJIT (duty)		-	-	Ps
TERR (2per)	Cumulative error across 2 cycle	-118	118	Ps
TERR (3per)	Cumulative error across 3 cycle	-140	140	Ps
TERR (4per)	Cumulative error across 4 cycle	-155	155	Ps
TERR (5per)	Cumulative error across 5 cycle	-168	168	Ps
TERR (6per)	Cumulative error across 6 cycle	-177	177	Ps
TERR (7per)	Cumulative error across 7 cycle	-186	186	Ps
TERR (8per)	Cumulative error across 3 cycle	-193	193	Ps
TERR (9per)	Cumulative error across 4 cycle	-200	200	Ps
TERR (10per)	Cumulative error across 5 cycle	-205	205	Ps

TERR (11per)	Cumulative error across 6 cycle	-210	210	Ps
TERR (12per)	Cumulative error across 7 cycle	-215	215	Ps
TERR (nper)	Cumulative error across 13~50 cycle	$tERR(nper)min = (1 + 0.68ln(n)) *$ $tJIT(per)min$ $tERR(nper)max = (1 + 0.68ln(n)) *$ $tJIT(per)max$		Ps
Data Timing				
Symbol	Parameter	Min.	Max.	Unit
tDSQ	DQS, DQS# to DQ skew, per group, per access	-	125	Ps
tQH	DQ output hold time from DQS, DQS#	0.38	-	tCK(avg)
tLZ (DQ)	DQ low-impedance time from CK, CK#	-500	250	Ps
tHZ(DQ)	DQ high impedance time from CK, CK#	-	250	Ps
tDS(base) AC150	Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	30	-	Ps
tDH(base) DC 100	Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	65	-	Ps
Data Strobe Timing				
Symbol	Parameter	Min.	Max.	Unit
tRPRE	DQS,DQS# differential READ Preamble	0.9		tCK(avg)
tRPST	DQS, DQS# differential READ Postamble	0.3		tCK(avg)
tQSH	DQS, DQS# differential output high time	0.4		tCK(avg)
tQSL	DQS, DQS# differential output low time	0.4		tCK(avg)
tWPRE	DQS, DQS# differential WRITE Preamble	0.9		tCK(avg)
tWPST	DQS, DQS# differential WRITE Postamble	0.3		tCK(avg)
tDQSK	DQS, DQS# rising edge output access time from rising CK, CK#	-225	225	Ps

tLZ(DQS)	DQS and DQS# low-impedance time (Referenced from RL - 1)	-450	225	Ps
tHZ(DQS)	DQS and DQS# high-impedance time (Referenced from RL + BL/2)	-	225	Ps
tDQSL	DQS, DQS# differential input low pulse width	0.4	0.6	tCK(avg)
tDQSH	DQS, DQS# differential input high pulse width	0.4	0.6	tCK(avg)
tDQSS	DQS, DQS# rising edge to CK, CK# rising edge	-0.25	0.25	tCK(avg)
tDSS	DQS, DQS# falling edge setup time to CK, CK# rising edge	0.2	-	tCK(avg)
tDSH	DQS, DQS# falling edge hold time from CK, CK# rising edge	0.2	-	tCK(avg)
Command and Address Timing				
Symbol	Parameter	Min.	Max.	Unit
tDLLK	DLL locking time	512	-	nCK
tRTP	Internal READ Command to PRECHARGE Command delay	max(4nCK, 7.5ns)	-	
tWTR	Delay from start of internal write transaction to Internal read command	max(4nCK, 7.5ns)	-	
tWR	WRITE recovery time	15	-	ns
tMRD	Mode Register Set command cycle time	4	-	nCK
tMOD	Mode Register Set command update delay	max(12nCK, 15ns)	-	
tRCD	Refer to Section 1 Feature			
tRP	Refer to Section 1 Feature			
tRC	Refer to Section 1 Feature			
tCCD		4	-	nCK

tDAL (min)	Auto precharge write recovery + precharge time	WR + roundup(tRP / tCK(avg))		nCK
tMPRR	Multi-Purpose Register Recovery Time	1	-	nCK
tRAS	ACTIVE to PRECHARGE command period	36	9 tREFI	ns
tRRD	ACTIVE to ACTIVE command period for 1KB page size	max(4nCK, 6ns)	-	
tRRD	ACTIVE to ACTIVE command period for 2KB page size	max(4nCK, 7.5ns)	-	
tFAW	Four activate window for 1KB page size	30	-	ns
tFAW	Four activate window for 2KB page size	45	-	ns
tIS (base)	Command and Address setup time to CK, CK#, referenced to Vih(ac) / Vil(ac) levels.	65		ns
tIH(base)	Command and Address hold time from CK, CK# referenced to Vih(dc) / Vil(dc) levels	140		ps
tIS(base) AC150	Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	65+125		ps
Calibration Timing				
Symbol	Parameter	Min.	Max.	Unit
tZQinit	Power-up and RESET calibration time	512	-	nCK
tZQoper	Normal operation Full calibration time	256	-	nCK
tZQCS	Normal operation Short calibration time	64	-	nCK
Reset Timing				
Symbol	Parameter	Min.	Max.	Unit
tXPR	Exit Reset from CKE HIGH to a valid command	max(5nCK, tRFC(min) + 10ns)	-	
Self Refresh Timings				

Symbol	Parameter	Min.	Max.	Unit
tXS	Exit Self Refresh to commands not requiring a locked DLL	Max(5nCK), tRFC(min) +10ns)		
tXSDLL	Exit Self Refresh to commands requiring a locked DLL.	tDLL(min)	-	nCK
tCKESR	Minimum CKE low width for Self Refresh entry to exit timing.	tCKE9min) +1nCK	-	
tCKSRE	Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	Max(5nCK, ,10ns)	-	
tCKSRX	Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	Max(5nCK, ,10ns)	-	
Power Down Timings				
Symbol	Parameter	Min.	Max.	Unit
tXP	Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	max(3nCK, 6ns)	-	
tXPDLL	Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	max(10nCK, 24ns)	-	
tCKE	CKE minimum pulse width	max(3nCK, 5.625ns)	-	
tCPDED	Command pass disable delay	1	-	nCK
tPD	Power Down Entry to Exit Timing	tCK(min)	9*tREFI	
tACTPDEN	Timing of ACT command to Power Down entry	1	-	nCK
tPRPDEN	Timing of PRE or PREA command to Power Down entry	1	-	nCK

tRDPDEN	Timing of RD/RDA command to Power Down entry	RL+4+1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	WL + 4 + WR + 1	-	nCK
tWRPDEN	Timing of WR command to Power Down entry (BC4MRS)	WL + 2 + (tWR / tCK(avg))	-	nCK
tWRAPDEN	Timing of WRA command to Power Down entry (BC4MRS)	WL + 2 + WR + 1	-	nCK
tREFPDEN	Timing of REF command to Power Down entry	1	-	nCK
tMRSPDEN	Timing of MRS command to Power Down entry	tMOD(mi n)	-	nCK
ODT Timings				
Symbol	Parameter	Min.	Max.	Unit
ODTH4	ODT high time without write command or with write command and BC4	4	-	nCK
ODTH8	ODT high time with Write command and BL8	6	-	nCK
tAONPD	Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	1	9	ns
tAOFPD	Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	1	9	ns
tAON	RTT-turn-on	-250	250	ps
tAOF	RTT_Nom and RTT_WR turn-off time from ODTLoff reference	0.3	0.7	tCK(avg)
tADC	RTT dynamic change skew	0.30.7		tCK(avg)

Write Leveling Timing				
Symbol	Parameter	Min.	Max.	Unit
tWLMRD	First DQS/DQS# rising edge after write leveling mode is programmed	40	-	nCK
tWLDQSEN	DQS/DQS# delay after write leveling mode is programmed	25	-	nCK
tWLS	Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	195	-	ps
tWLH	Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	195	-	ps
tWLO	Write leveling output delay	0	9	ns
tWLOE	Write leveling output error	0	2	ns

12. SPD Serial Presence Detect – (4GB)

2 RANK UNBUFFERED DDR SDRAM DIMM based on 256Mx8, 8Banks, 8K Refresh, DDR3 SDRAMs with SPD

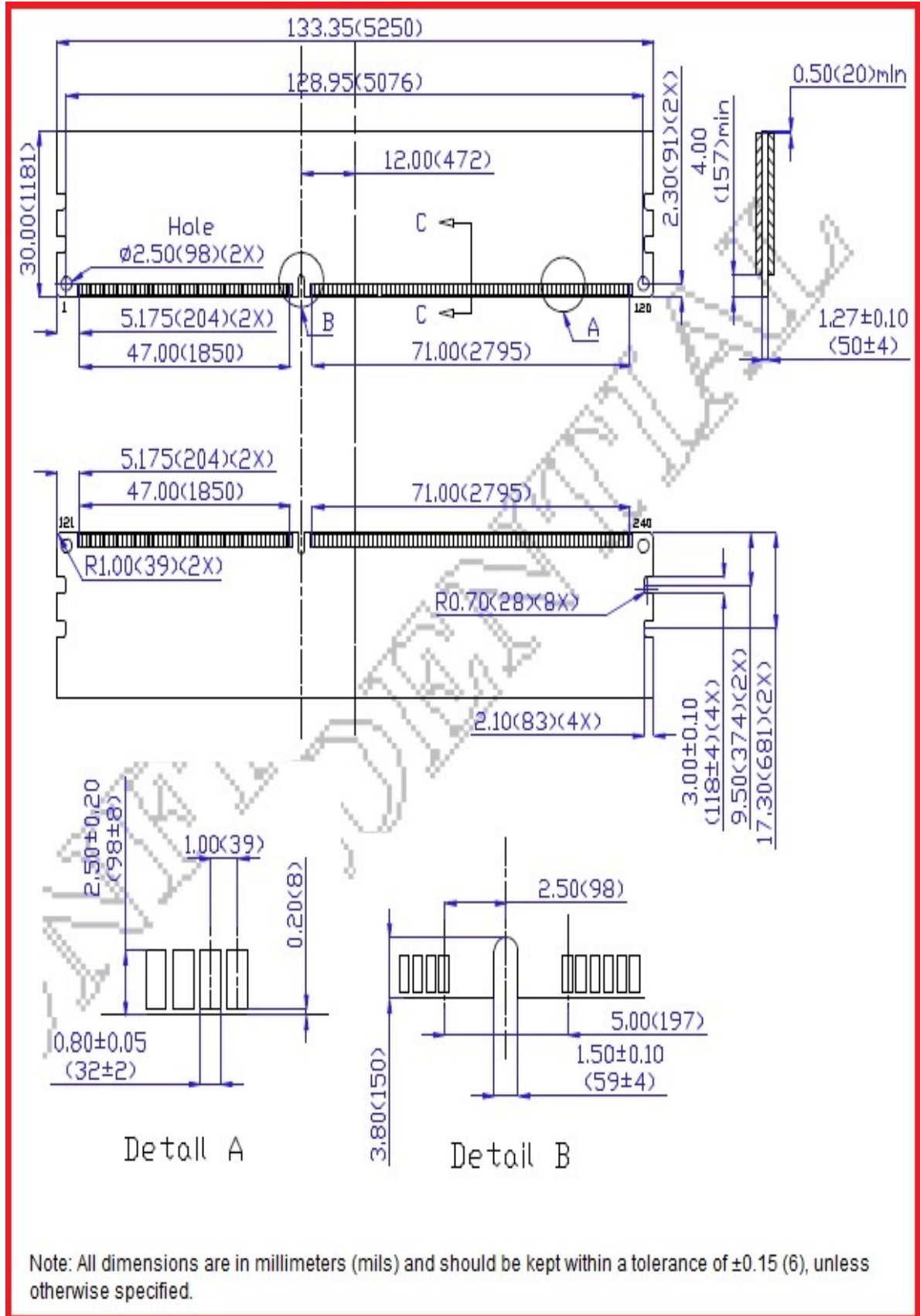
Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
0	Number of Serial PD Bytes Written during Production	92	
1	SPD Revision	10	
2	Key Byte/DRAM Device Type	0B	
3	Key Byte/Module type	02	
4	SDRAM Density and Banks	03	
5	SDRAM Address	19	
6	Reserve	00	
7	Module Organization	09	
8	Module Memory Bus Width	03	
9	Fine Timebase (FTB) Dividend/Divisor	52	
10	Medium Timebase (MTB) Dividend	01	
11	Medium Timebase (MTB) Divisor	08	
12	SDRAM Minimum Cycle Time (tCKmin)	0C	
13	Reserve	00	
14	CAS latency, least Significant Byte	3C	
15	CAS latency, most Significant Byte	00	
16	Minimum CAS Latency Time (tAAmin)	69	
17	Minimum Write Recovery Time (tWRmin)	78	

Byte	Description	Serial PD Data Entry (Hexadecimal)	Note
18	Minimum RAS# to CAS# Delay Time (tRCDmin)	69	
19	Minimum Row Active to Row Active Delay Time (tRRDmin)	30	
20	Minimum Row Precharge Delay Time (tRPmin)	69	
21	Upper Nibbles for tRAS and tRC	11	
22	Minimum Active to Precharge Delay Time (tRASmin), Least Significant Byte	20	
23	Minimum Active to Active/Refresh Delay Time (tRCmin), Least Significant Byte	89	
24	Minimum Refresh Recovery Delay Time (tRFCmin), Least Significant Byte	00	
25	Minimum Refresh Recovery Delay Time (tRFCmin), Most Significant Byte	05	
26	Minimum Internal Write to Read Command Delay Time (tWTRmin)	3C	
27	Minimum Internal Read to Precharge Command Delay Time (tRTPmin)	3C	
28	Upper Nibble for tFAW	00	
29	Minimum Four Activate Window Delay Time (tFAWmin)	F0	
30	SDRAM Optional Features	83	
31	SDRAM Thermal and Refresh Options	05	
32	Module Thermal Sensor	00	
33	SDRAM Device Type	00	

34-59	Reserve	00	
60-63	Module Type Specific Section,	0F 11 01 01	
64-117	Reserve	-	
117-118	Module ID: Module Manufacturer's JEDEC ID Code	86 F1	
119	Module ID: Module Manufacturing Location	02	
120-121	Module ID: Module Manufacturing Date	09 2E	
122-255	reserve	-	

13. PACKAGE DIMENSION

- (4GB, 2 Ranks, 256Mx8 DDR3 base UDIMM)



14. RoHS Declaration

innodisk

Declaration of Conformity

We, InnoDisk Co., Ltd, here declare the product M3U0-4GSJACN9-(X) complies with the requirement of RoHS directives 2002/95/EC and 2006/122/EC.

Innodisk ensures the above product meets RoHS requirements of six restricted substances. This declaration is based on vendor supplied analysis/MSDS, material certifications, and/ or 3rd party test reports of the component/ raw materials used in the manufacture of products.

✚ RoHS Exemptions Applied Of 7(C)-I for Resist.

Name of hazardous substance	Limited of RoHS ppm (mg/kg)
Cd	< 100 ppm
Pb	< 1000 ppm
Hg	< 1000 ppm
Chromium VI (Cr+6)	< 1000 ppm
Polybromodiphenyl ether (PBDE)	< 1000 ppm
Polybrominated Biphenyls (PBB)	< 1000 ppm
Perfluorooctane Sulfonate (PFOS)	Not Contained

Date issued : 2013/05/20

Manufacturer: : Innodisk Co., Ltd.

Address : 221 5F, No. 237, Sec.1 Datong Rd., Xizhi City, New Taipei City, Taiwan

Authorized Signature :

QA Dept. Director - *Ryan Tsai*

Revision Log

Rev	Date	Modification
0.1	18 th December 2013	Preliminary Edition
1.0	19 th December 2013	Official released.