Approval Sheet

Customer	
Product Number	**MM111-5CGS1A1ACA00**
Type	**CXL 2.0 E3.S 2T**
Capacity	**64GB**
Operating temperature	**Tc=0 to 70°C**
Date	**5th Mar 2025**

The Total Solution For Industrial Flash Storage

1. CXL FEATURES

- Compliant with PCI Express® Base Specification Rev. 5.0
- Compliant with CXL™ 1.1 & CXL™ 2.0
- PCIe / CXL io Base
  - Single link with x8 lanes
  - Up to 32GT/S data rate
- CXL DVSEC (Designated Vendor-Specific Extended Capability)
  - CXL device
  - Flex Port
  - Register Locator
  - No Data Response NDR (ECN)
- Type-3 Single Logical Device (SDL)
- Vendor Defined Message (VDM) for CXL power management
- CXL Memory Mapped IO (MMIO) register
  - Component registers
  - Device registers
- Mailbox
- Three Data Object Exchange (DOE) instances :
  - CDAT DOE
  - Compliance DOE
  - Security DOE
- Datapath protection for RAS
- Metadata storage
- CXL Performance Monitoring Unit (CPMU)
- Media Side I2C/I3C Master ; Host Side SMBUS Slave
- RoHS/Halogen-free
- *CXL Device Speed : Auto Detect = > 4400 MT/s (Controller Limitation)

*Note : The device speed is not the same as the speed transmitted through PCIe

2. RAS FEATURES

- CXL Link CRC and Retry
- CXL Link Retrain and Recovery
- Data Poison
- Viral
- Memory ECC SEC/DED
- Automatic data scrubbing of correctable errors
- DDR Read CRC / Write CRC and Retry
- DDR CA Parity and Retry
- Errors Logging and Injection
- Patrol and Demand Scrub
- hPPR & sPPR
- Memory data scrambling
- Memory sparing
- Memory mirroring

3. DEVICE PERFORMANCE[1] @ PCI Express® Gen.5 x8

- Data Transfer Rate (64Byte Cache line size)

- All Read	21.6 GB/S
- 1Read/ 1Write	26.5 GB/S
- 2Read/ 1Write	25.1 GB/S
- 3Read/ 1Write	25.0 GB/S
- All Write	25.0 GB/S

- Latency

- Idle Latency	< 260 ns
- Device Latency (Pin to Pin)	< 150 ns
- QoS of Latency (99.9%)	< 450 ns

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1) Based on PCI Express® Gen.5 x8, All performance (bandwidth/Latency) is measured by using Intel® MLC in Ubuntu 20.04.6 LTS with all threads operated by all activated cores. Data size of read / write is 64Byte with random address, aligned with cache line size. Actual performance may vary depending on use conditions and environment.

4. Environmental Specifications

- Temperature – Operating 0~70°C

5. Power Requirements

- Supply Voltage / Tolerance 12V±10%
- Power Consumption – Active Power 39.1W

6. Physical Dimension

- Width 76.00±0.25mm
- Length 112.75±0.4mm
- Height 16.8+0/-0.3mm
- Weight Up to 245 g

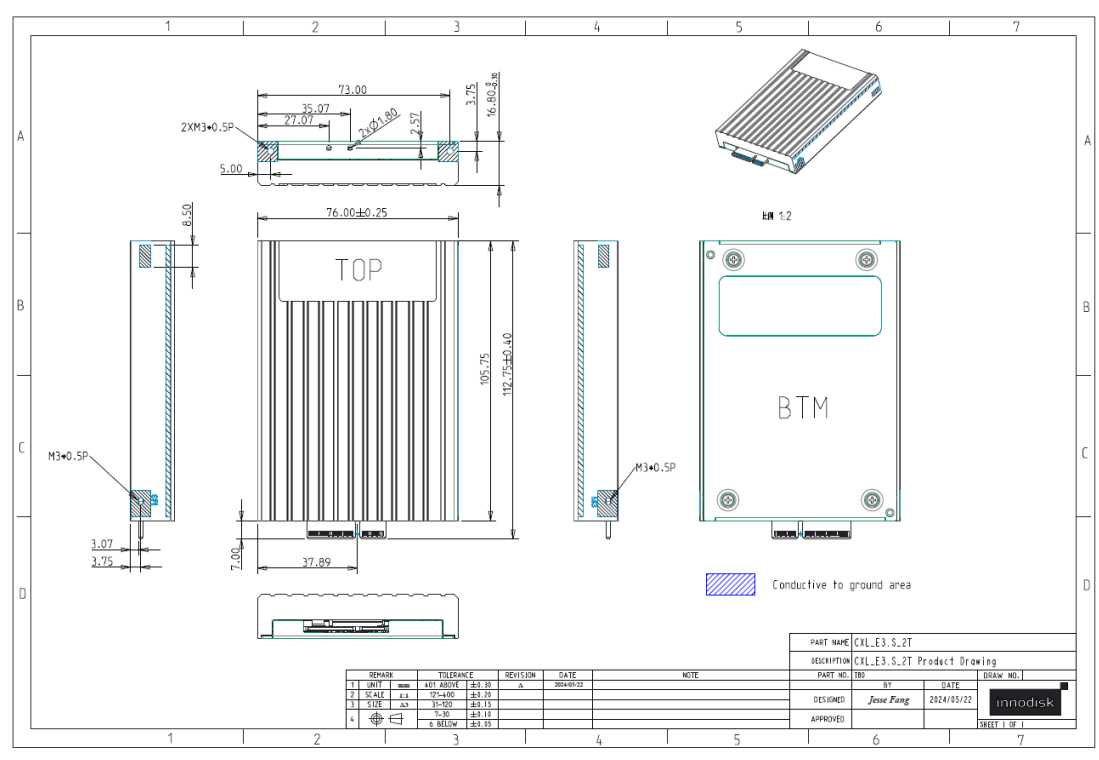
7. Led Information

- Green Color (Driven by the device)
- Amber / Blue Color (Driven by the host)

8. Mechanical Specifications

- EDSFF E3.S 2T Physical

Parameter	Unit	Description
Width	mm	76.00±0.25
Length	mm	112.75±0.40
Height	mm	Max 16.8(16.8+0/-0.3)
Weight	g	Up to 245

- 

9. LED Information

- The usage and details of the LEDs on EDSFF devices follows SNIA SFF-TA-1009 Rev3.1

LED description	Green	Amber	Blue
Driven by	Device	Host (LED signal)	Host (LED signal)
Function	Power, Activity	Host Defined	Host Defined

10. Pin Descriptions

- **The pin assignments and description follows SNIA SFF-TA-1009**

Pin	Signal	Signal	Pin
B1	12 V	GND	A1
B2	12 V	GND	A2
B3	12 V	GND	A3
B4	12 V	GND	A4
B5	12 V	GND	A5
B6	12 V	GND	A6
B7	MFG	SMBCLK	A7
B8	RFU	SMBDATA	A8
B9	DUALPORTEN#	SMRST#	A9
B10	PERST0#	LED	A10
B11	3.3 Vaux	PERST1#	A11
B12	PWRDIS	PRSNT0#	A12
B13	GND	GND	A13
B14	REFCLKn0	REFCLKn1	A14
B15	REFCLKp0	REFCLKp1	A15
B16	GND	GND	A16
B17	PETn0	PERn0	A17
B18	PETp0	PERp0	A18
B19	GND	GND	A19
B20	PETn1	PERn1	A20
B21	PETp1	PERp1	A21
B22	GND	GND	A22
B23	PETn2	PERn2	A23
B24	PETp2	PERp2	A24
B25	GND	GND	A25
B26	PETn3	PERn3	A26
B27	PETp3	PERp3	A27
B28	GND	GND	A28
	Key	Key	
B29	GND	GND	A29
B30	PETn4	PERn4	A30
B31	PETp4	PERp4	A31
B32	GND	GND	A32
B33	PETn5	PERn5	A33
B34	PETp5	PERp5	A34
B35	GND	GND	A35
B36	PETn6	PERn6	A36
B37	PETp6	PERp6	A37
B38	GND	GND	A38
B39	PETn7	PERn7	A39
B40	PETp7	PERp7	A40
B41	GND	GND	A41
B42	PRSNT1#	RFU	A42

11. References

- This document leverages and references the below standards specification.

Item	Website
• PCI Express® Base Specification Revision 5.0	• https://www.pcisig.com/specifications
• PCI Express® Card Electromechanical Specification	• https://www.pcisig.com/specifications
• CXL™ 1.1 & 2.0 Specification.	• https://www.computeexpresslink.org
• SFF-TA-1002 & SFF-TA-1008 & SFF-TA-1009	• https://www.snia.org/sff/specifications
• SNIA / SFF-TA-1023 - Specification for Thermal	• https://www.snia.org/sff/specifications
• JEDEC® CXL Memory Module Label - JESD405 - 1A , January 2024	• https://www.jedec.org/
• JEDEC® CXL Memory Module Reference Base Standard – JESD317A, January 2024	
• JEDEC® CXL Memory Controller Standard – JESD319, September 2024	
• JEDEC® CXL Memory Device Management Standard – JESD325, September 2024	

12. RoHS Declaration

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宜鼎國際股份有限公司
Innodisk Corporation

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Tel:(02)7703-3000 Internet: https://www.innodisk.com/

RoHS 自我宣告書(RoHS Declaration of Conformity)

Manufacturer Products: All Innodisk EM FLASH, DRAM and EP products

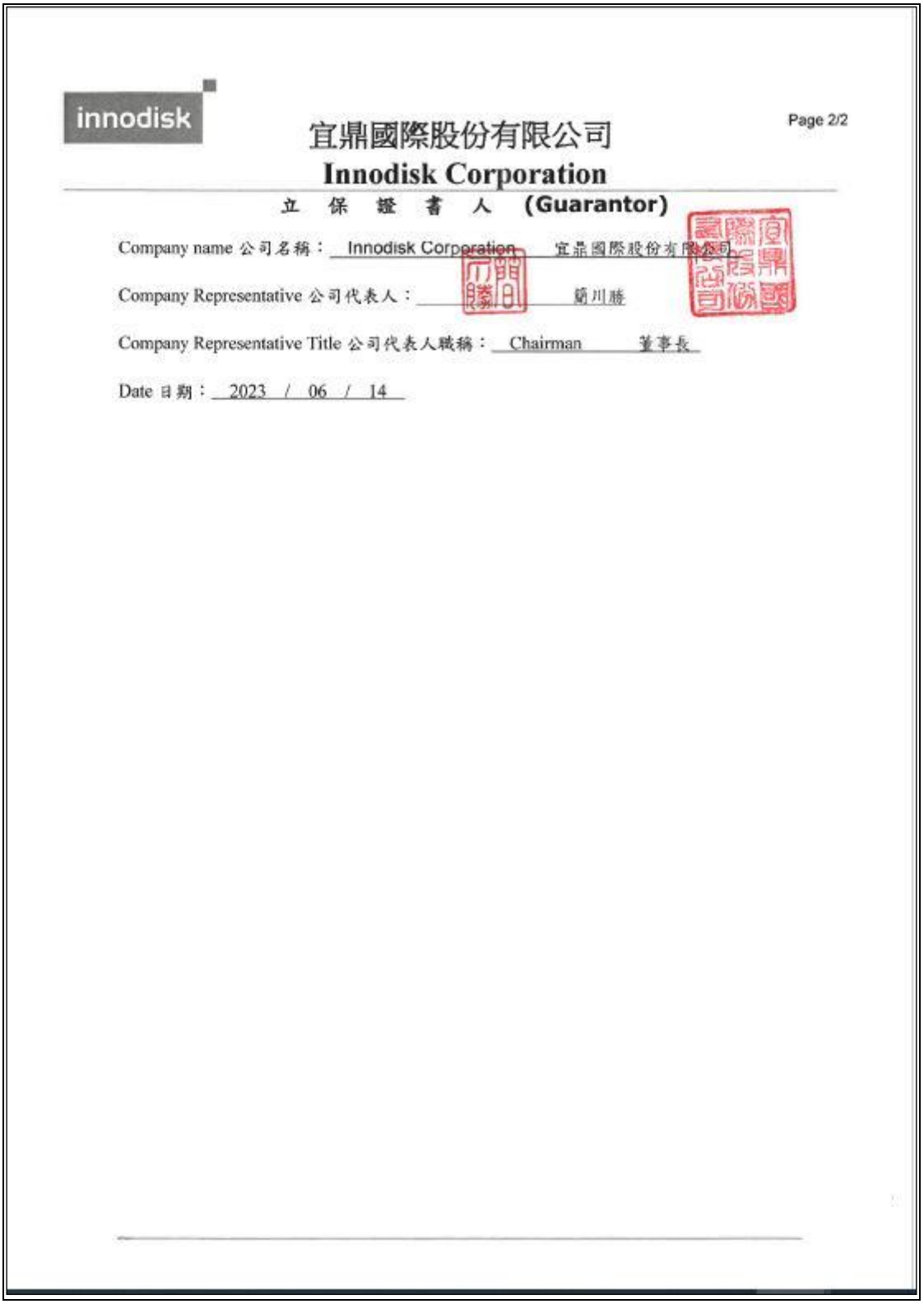
一、 宜鼎國際股份有限公司（以下稱本公司）特此保證售予貴公司之所有產品，皆符合歐盟 2011/65/EU 及(EU) 2015/863 關於 RoHS 之規範要求。
Innodisk Corporation declares that all products sold to the company, are complied with European Union RoHS Directive (2011/65/EU) and (EU) 2015/863 requirement.

二、 本公司同意因本保證書或與本保證書相關事宜有所爭議時，雙方宜友好協商，達成協議。
Innodisk Corporation agrees that both parties shall settle any dispute arising from or in connection with this Declaration of Conformity by friendly negotiations.

三、 本公司聲明我們的產品符合 RoHS 指令的附件中 7(a)、7(c)-I、6(c)允許豁免。
We declare, our products permitted by the following exemptions specified in the Annex of the RoHS directive.

※ 7(a) Lead in high melting temperature type solders(i.e. lead-based alloys containing 85% by weight or more lead).
※ 7(c)-I Electrical and electronic components containing lead in a glass or ceramic other than dielectric ceramic in capacitors, e.g. piezoelectric devices, or in a glass or ceramic matrix compound.
※ 6(c) Copper alloy containing up to 4% lead by weight. (This exemption applies to products that use antennas)

Name of hazardous substance	Limited of RoHS ppm（mg/kg）
鉛（Pb）	< 1000 ppm
汞（Hg）	< 1000 ppm
鎘（Cd）	< 100 ppm
六價鉻（Cr 6+）	< 1000 ppm
多溴聯苯（PBBs）	< 1000 ppm
多溴二苯醚（PBDEs）	< 1000 ppm
鄰苯二甲酸二(2-乙基己基)酯（DEHP）	< 1000 ppm
鄰苯二甲酸丁酯苯甲酯（BBP）	< 1000 ppm
鄰苯二甲酸二丁酯（DBP）	< 1000 ppm
鄰苯二甲酸二異丁酯（DIBP）	< 1000 ppm



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宜鼎國際股份有限公司

Innodisk Corporation

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立 保 證 書 人 (Guarantor)

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： 簡川勝

Company Representative Title 公司代表人職稱： Chairman 董事長

Date 日期： 2023 / 06 / 14

13. REACH Declaration

innodisk

宜鼎國際股份有限公司
Innodisk Corporation
REACH Declaration

Tel:(02)7703-3000 Fax:(02) 7703-3555 Internet: https://www.innodisk.com/

Innodisk Corporation pursues its social responsibility for global environmental preservation by committing to be compliant with REACH regulation (REGULATION (EC) No 1907/2006).
We hereby confirm that the product(s),

Scope: Flash Memory, DRAM Module and Embedded Peripherals Products.

■ The standard products of **not listed in** the ***Appendix2*** meet the requirements of REACH SVHC regulations(SVHCs < 0.1% in Article), as described in the candidate list table currently including 240 substances (release date: 23-JAN-2024) and shown on the ECHA website. https://echa.europa.eu/candidate-list-table

■ The standard products listed in the ***Appendix2*** contain(s) one or more hazardous substances or constituents exceeding 0.1 % by weight in article if not otherwise specified in candidate list table.
Where the threshold value is exceeded, the substances in question are to be declared in accompanying. (SVHCs > 0.1% in Article).

■ Comply with REACH Annex XVII.

Guarantor

Company name 公司名稱： Innodisk Corporation 宜鼎國際股份有限公司

Company Representative 公司代表人： Yichuan Chen 陳怡全

Company Representative Title 公司代表人職稱：Quality Assurance Div. SR. Manager 品保處經理

Date 日期：2024 / 02 / 19

1

14. SPD

Byte Number	Function Described	Function supported	Hex Value
0	Number of Bytes in SPD Device	1024 Bytes	30
1	SPD Revision for Base Configuration Parameters	Revision 1.0	10
2	Key Byte / Host Bus Command Protocol Type	DDR5 SDRAM	12
3	Key Byte / Module Type	RDIMM	01
4	First SDRAM Density and Package	Monolithic 16Gb	04
5	First SDRAM Addressing	10 columns/16 rows	00
6	First SDRAM I/O Width	x8	20
7	First SDRAM Bank Groups & Banks Per Bank Group	8BGs / 4Banks per BG	62
8	Second SDRAM Density and Package	N/A	00
9	Second SDRAM Addressing	N/A	00
10	Second SDRAM I/O Width	N/A	00
11	Second SDRAM Bank Groups & Banks Per Bank Group	N/A	00
12	SDRAM BL32 & Post Package Repair	BL32 supported / sPPR	B0
13	SDRAM Duty Cycle Adjuster & Partial Array Self Refresh	PASR not supported	02
14	SDRAM Fault Handling	Yes	01
15	Reserved	Reserved	00
16	SDRAM Nominal Voltage, VDD	1.1V	00
17	SDRAM Nominal Voltage, VDDQ	1.1V	00
18	SDRAM Nominal Voltage, VPP	1.8V	00
19	SDRAM Timing	Standard	00
20	SDRAM Minimum Cycle Time (t_{CKAVG}min), Least Significant Byte	357ps	65
21	SDRAM Minimum Cycle Time (t_{CKAVG}min), Most Significant Byte	357ps	01
22	SDRAM Maximum Cycle Time (t_{CKAVG}max), Least Significant Byte	1010ps	F2
23	SDRAM Maximum Cycle Time (t_{CKAVG}max), Most Significant Byte	1010ps	03
24	CAS Latencies Supported, First Byte	22,26,28,30,32,36,40,42,46,50	7A
25	CAS Latencies Supported, Second Byte	22,26,28,30,32,36,40,42,46,50	AD
26	CAS Latencies Supported, Third Byte	22,26,28,30,32,36,40,42,46,50	00
27	CAS Latencies Supported, Fourth Byte	22,26,28,30,32,36,40,42,46,50	00
28	CAS Latencies Supported, Fifth Byte	22,26,28,30,32,36,40,42,46,50	00
29	Reserved	Reserved	00
30	SDRAM Minimum CAS Latency Time (t_{AA}min), Least Significant Byte	16000ps	80
31	SDRAM Minimum CAS Latency Time (t_{AA}min), Most Significant Byte	16000ps	3E
32	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Least Significant Byte	16000ps	80

33	SDRAM Minimum RAS to CAS Delay Time (t_{RCD}min), Most Significant Byte	16000ps	3E
34	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Least Significant Byte	16000ps	80
35	SDRAM Minimum Row Precharge Delay Time (t_{RP}min), Most Significant Byte	16000ps	3E
36	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Least Significant Byte	32000ps	00
37	SDRAM Minimum Active to Precharge Delay Time (t_{RAS}min), Most Significant Byte	32000ps	7D
38	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Least Significant Byte	48000os	80
39	SDRAM Minimum Active to Active/Refresh Delay Time (t_{RC}min), Most Significant Byte	48000os	BB
40	SDRAM Minimum Write Recovery Time (t_{WR}min), Least Significant Byte	30000ps	30
41	SDRAM Minimum Write Recovery Time (t_{WR}min), Most Significant Byte	30000ps	75
42	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Least Significant Byte	295ns	27
43	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC1}min, t_{RFC1}_slr min), Most Significant Byte	295ns	01
44	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Least Significant Byte	160ns	A0
45	SDRAM Minimum Refresh Recovery Delay Time (t_{RFC2}min, t_{RFC2}_slr min), Most Significant Byte	160ns	00
46	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}min, t_{RFCsb}_slr min), Least Significant Byte	130ns	82
47	SDRAM Minimum Refresh Recovery Delay Time (t_{RFCsb}_dlr min), Most Significant Byte	130ns	00
48	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Least Significant Byte	N/A	00
49	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC1}_dlr min), Most Significant Byte	N/A	00
50	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Least Significant Byte	N/A	00
51	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFC2}_dlr min), Most Significant Byte	N/A	00
52	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Least Significant Byte	N/A	00
53	SDRAM Minimum Refresh Recovery Delay Time, 3DS Different Logical Rank (t_{RFCsb}_dlr min), Most Significant Byte	N/A	00

54	SDRAM Refresh Management, First Byte, First SDRAM	N/A	00
55	SDRAM Refresh Management, Second Byte, First SDRAM	N/A	00
56	SDRAM Refresh Management, First Byte, Second SDRAM	N/A	00
57	SDRAM Refresh Management, Second Byte, Second SDRAM	N/A	00
58	SDRAM Adaptive Refresh Management Level A, First Byte, First SDRAM	N/A	00
59	SDRAM Adaptive Refresh Management Level A, Second Byte, First SDRAM	N/A	00
60	SDRAM Adaptive Refresh Management Level A, First Byte, Second SDRAM	N/A	00
61	SDRAM Adaptive Refresh Management Level A, Second Byte, Second SDRAM	N/A	00
62	SDRAM Adaptive Refresh Management Level B, First Byte, First SDRAM	N/A	00
63	SDRAM Adaptive Refresh Management Level B, Second Byte, First SDRAM	N/A	00
64	SDRAM Adaptive Refresh Management Level B, First Byte, Second SDRAM	N/A	00
65	SDRAM Adaptive Refresh Management Level B, Second Byte, Second SDRAM	N/A	00
66	SDRAM Adaptive Refresh Management Level C, First Byte, First SDRAM	N/A	00
67	SDRAM Adaptive Refresh Management Level C, Second Byte, First SDRAM	N/A	00
68	SDRAM Adaptive Refresh Management Level C, First Byte, Second SDRAM	N/A	00
69	SDRAM Adaptive Refresh Management Level C, Second Byte, Second SDRAM	N/A	00
70	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Least Significant Byte	5000ps	88
71	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Most Significant Byte	5000ps	13
72	SDRAM Minimum Active to Active Command Delay Time, Same Bank Group (t_{RRD_L}min), Lower Clock Limit	8nCK	08
73	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Least Significant Byte	5000ps	88
74	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Most Significant Byte	5000ps	13
75	SDRAM Minimum CAS_n to CAS_n Command Delay Time, Same Bank Group (tCCD_Lmin), Lower Clock Limit	8nCK	08
76	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Least Significant Byte	20000ps	20
77	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Most Significant Byte	20000ps	4E
78	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Same Bank Group ($t_{CCD_L_WR}$min), Lower Clock Limit	32nCK	20
79	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Least Significant Byte	10000ps	10

80	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Most Significant Byte	10000ps	27
81	SDRAM Minimum Write CAS_n to Write CAS_n Command Delay Time, Second Write not RMW, Same Bank Group ($t_{CCD_L_WR2}$min), Lower Clock Limit	16nCK	10
82	SDRAM Minimum Four Activate Window (t_{FAW}min), Least Significant Byte	11428ps	A4
83	SDRAM Minimum Four Activate Window (t_{FAW}min), Most Significant Byte	11428ps	2C
84	SDRAM Minimum Four Activate Window (t_{FAW}min), Lower Clock Limit	32nCK	20
85	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Least Significant Byte	10000ps	10
86	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Most Significant Byte	10000ps	27
87	SDRAM Minimum Internal Write to Read Command Delay Time, Same Bank Group, (t_{WTR_L}min), Lower Clock Limit	16nCK	10
88	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Least Significant Byte	2500ps	C4
89	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Most Significant Byte	2500ps	09
90	SDRAM Minimum Internal Write to Read Command Delay Time, Different Bank Group, (t_{WTR_S}min), Lower Clock Limit	4nCK	04
91	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Least Significant Byte	7500ps	4C
92	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Most Significant Byte	7500ps	1D
93	SDRAM Minimum Internal Read to Precharge Command Delay Time, (t_{RTP}min), Lower Clock Limit	12nCK	0C
94~127	Reserved -- must be coded as 0x00	Reserved	00
128~191	Reserved for future use	Reserved	00
192	SPD Revision for SPD bytes 192~447	Revision 1.0	10
193	Hashing Sequence	No authentication	00
194	SPD Manufacturer ID Code, First Byte	Renesas	80
195	SPD Manufacturer ID Code, Second Byte	Renesas	B3
196	SPD Device Type	Renesas	80
197	SPD Device Revision Number	Renesas	21
198	PMIC 0 Manufacturer ID Code, First Byte	Montage	86
199	PMIC 0 Manufacturer ID Code, Second Byte	Montage	32
200	PMIC 0 Device Type	Montage	80
201	PMIC 0 Revision Number	Montage	14

202	PMIC 1 Manufacturer ID Code, First Byte	N/A	00
203	PMIC 1 Manufacturer ID Code, Second Byte	N/A	00
204	PMIC 1 Device Type	N/A	00
205	PMIC 1 Revision Number	N/A	00
206	PMIC 2 Manufacturer ID Code, First Byte	N/A	00
207	PMIC 2 Manufacturer ID Code, Second Byte	N/A	00
208	PMIC 2 Device Type	N/A	00
209	PMIC 2 Revision Number	N/A	00
210	Thermal Sensor Manufacturer ID Code, First Byte	IDT (Renesas)	80
211	Thermal Sensor Manufacturer ID Code, Second Byte	IDT (Renesas)	B3
212	Thermal Sensor Device Type	IDT (Renesas)	C0
213	Thermal Sensor Revision Number	IDT (Renesas)	12
214	DRAM Specification Level	Reserved	00
215	SPD Specification Level	N/A	00
216	PMIC0 Specification Level	N/A	00
217	PMIC1 Specification Level	N/A	00
218	PMIC2 Specification Level	N/A	00
219	TS Specification Level	N/A	00
220	DIMM Specification Level	N/A	00
221~229	Reserved	Reserved	00
230	Module Nominal Height	31 < height <= 32 mm	11
231	Module Maximum Thickness	Back 2 < thickness <= 3 mm, front 1 < thickness <= 2 mm	21
232	Reference Raw Card Used	R/C E rev 0	04
233	DIMM Attributes	Tc 0 to +95 °C, 1row	81
234	Module Organization	Symmetrical 2 Package Ranks	08
235	Memory Channel Bus Width	2 channels, 32 bits per channel, 8 bits ECC	32
236~239	Reserved	Reserved	00
240	Registering Clock Driver Manufacturer ID Code, First Byte	Rambus	86
241	Registering Clock Driver Manufacturer ID Code, Second Byte	Rambus	9D
242	Register Device Type	Rambus	80
243	Register Revision Number	Rambus	10
246	Data Buffer Device Type	N/A	00
247	Data Buffer Revision Number	N/A	00
248	RCD-RW08 Clock Driver Enable	Enabled	00
249	RCD-RW09 Output Address and Control Enable	Enabled	00

250	RCD-RW0A QCK Driver Characteristics	Normal	2A
251	RCD-RW0B	Normal	4A
252	RCD-RW0C QxCA and QxCS_n Driver Characteristics	Normal	55
253	RCD-RW0D Data Buffer Interface Driver Characteristics	Normal	00
254	RCD-RW0E QCK, QCA and QCS Output Slew Rate	Normal	01
255	RCD-RW0F BCK, BCOM, and BCS Output Slew Rate	Normal	00
256	DB-RW86 DQS RTT Park Termination	Normal	00
257~447	Reserved	Reserved	00
448~509	Reserved for future use	Reserved	00
510~511	CRC for SPD bytes 0~509	CRC	B9 38
512	Module Manufacturer ID Code, First Byte	Advantech	8A
513	Module Manufacturer ID Code, Second Byte	Advantech	C8
514	Module Manufacturing Location	Made in Taiwan	02
515~516	Module Manufacturing Date		-
517~520	Module Serial Number		-
521~550	Module Part Number	MM111-5CGS1A1ACA00	4D 4D 31 31 31 2D 35 43 47 53 31 41 31 41 43 41 30 30 20 20 20 20 20 20 20 20 20 20 20 20
551	Module Revision Code		00
552	DRAM Manufacturer ID Code, First Byte	Samsung	80
553	DRAM Manufacturer ID Code, Second Byte	Samsung	CE
554	DRAM Stepping		00
555~639	Manufacturer's Specific Data		-
640~703	End User Programmable	Reserved	00
704~767	End User Programmable	Reserved	00
768~831	End User Programmable	Reserved	00
832~895	End User Programmable	Reserved	00
896~959	End User Programmable	Reserved	00
960~1023	End User Programmable	Reserved	00

Revision Log

Rev	Date	Modification
0.1	23th May 2024	Preliminary Edition
0.2	16th Sep 2024	Revised by more Function
0.3	18th Nov 2024	Revised by Device Speed